AK4204

Stereo Cap-less LINE-Amp and Video-Amp

GENERAL DESCRIPTION

The AK4204 is an audio stereo cap-less line driver with 1-channel video driver. It eliminates the need for large DC-blocking capacitors with a built-in Charge-pump circuit. The AK4204 achieves 2Vrms outputs with excellent linearity by single 3.3V power supply. It is well suitable for Blu-ray player and set-top box systems. The AK4204 is available in small 16-pin TSSOP, saving the system space and cost.

FEATURE

1. Audio Line-Amp

- ☐ **Single-ended Input**
- ☐ **Stereo Cap-less Amplifier (No DC-blocking capacitors required)**
- ☐ **Line-Out level: 2.0Vrms**
- ☐ **THD+N: -98dB**
- ☐ **S/N: 102dB**
- ☐ **Output gain: 6dB**
- ☐ **Low-pass Filter: fc= 130kHz**
- ☐ **Pop Noise Free Ground-referenced Output**
- ☐ **Audio Mute Function**

2. Video Amp

- ☐ **1ch Stereo Cap-less Amplifier (No DC-blocking capacitors required)**
- ☐ **Integrated Video Amplifier (+6dB)**
- ☐ **Input Level: 1.5Vpp (max)**
- ☐ **SN: 81dB(typ), Bandwidth: 100kHz ~ 6MHz**
- ☐ **LPF: -0.5dB@ 6.75MHz (typ), -43dB@27MHz (typ)**
- ☐ **Video Mute Function**

- ☐ **Power Supply: 3.0V ~ 3.6V**
- ☐ **Ta: –20 ~ 85°C**
- ☐ **Package: 16pinTSSOP**

■ Block Diagram

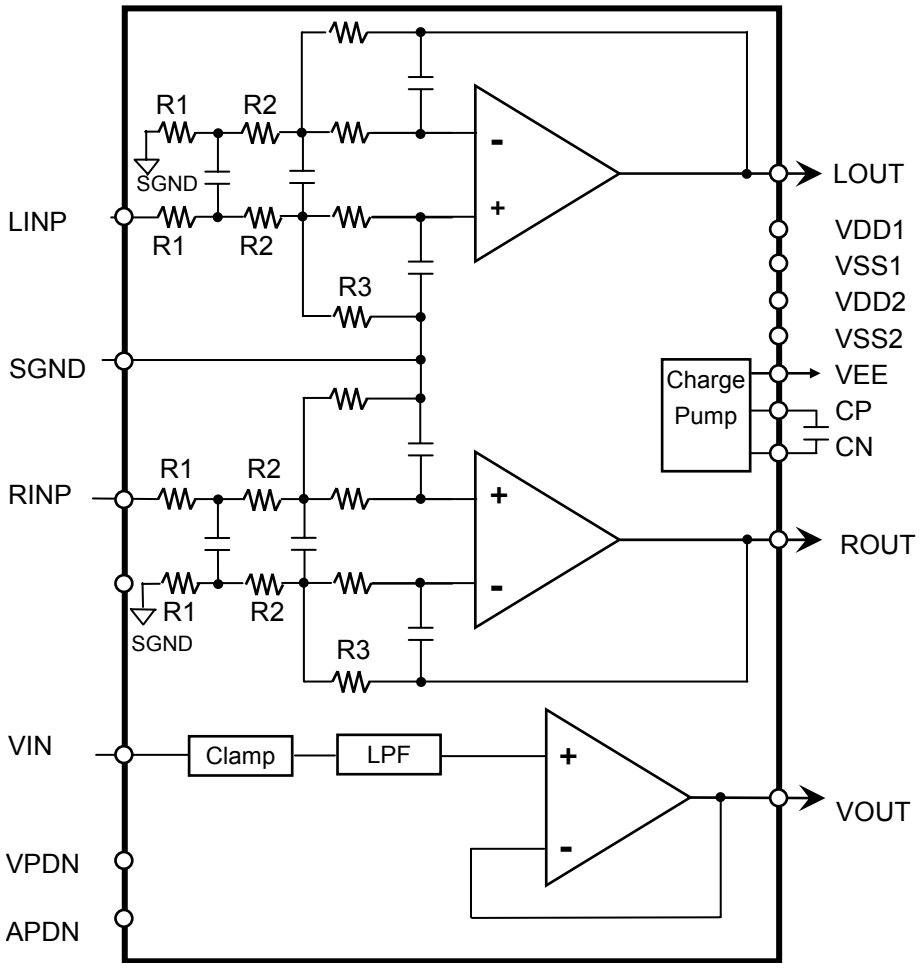
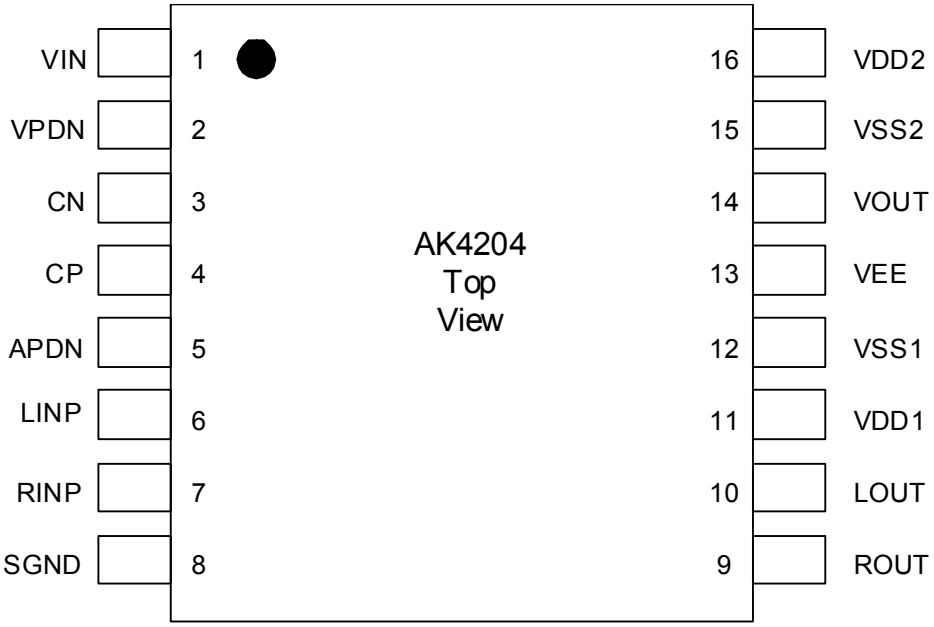


Figure 1. AK4204 Block Diagram

■ Ordering Guide

AK4204ET	–20 ~ +85°C	16 pin TSSOP (0.65mm pitch)
AKD4204	Evaluation board for AK4204	

■ Pin Layout



PIN/FUNCTION

No.	Pin Name	I/O	Function
1	VIN	I	Video Signal Input pin
2	VPDN	I	Video Block Power Down pin
3	CN	I	Negative Charge Pump Capacitor Terminal pin
4	CP	O	Positive Charge Pump Capacitor Terminal pin
5	APDN	I	Audio Block Power Down pin
6	LINP	I	Lch Audio Positive Input pin
7	RINP	I	Rch Audio Positive Input pin
8	SGND	I	Reference Voltage Input pin for Audio Signal (0V)
9	ROUT	O	Audio Output pin (R channel)
10	LOUT	O	Audio Output pin (L channel)
11	VDD1	-	Power Supply 1 pin; 3.0V~3.6V Connect a 0.1μF ceramic capacitor in parallel with a 10μF 3.3V electrolytic capacitor between this pin and VSS1.
12	VSS1	-	Ground 1 pin
13	VEE	O	Negative Voltage Output pin Connect to VSS1 via a 10μF 3.3V electrolytic capacitor.
14	VOUT	O	Video Signal Output pin
15	VSS2	-	Ground 2 pin
16	VDD2	-	Power Supply 2 pin; 3.0V~3.6V Connect a 0.1μF ceramic capacitor in parallel with a 10μF 3.3V electrolytic capacitor between this pin and VSS2.

ABSOLUTE MAXIMUM RATINGS

(VSS1=VSS2 = 0V; Note 1, Note 2)

Parameter	Symbol	min	max	Unit
Power Supply	VDD1 VDD2	-0.3	4.0	V
Input Current (any pins except for supplies)	IIN	-	±10	mA
Audio Input Voltage	VINA	VEE-0.3	VDD1 +0.3	V
Video Input Voltage	VINV	-0.3	VDD2+0.3	V
Ambient Operating Temperature	Ta	-20	85	°C
Storage Temperature	Tstg	-65	150	°C

Note 1. All voltages are respect to ground.
Note 2. VSS1 and VSS2 must be connected to the same analog plane.
Note 3. VDD1 and VDD2 must have the same voltage.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMEND OPERATING CONDITIONS

(VSS1 = VSS2 = 0V)

Parameter	Symbol	min	typ	max	Unit
Power Supply	VDD1	3.0	3.3	3.6	V
	VDD2	3.0	3.3	3.6	V

Note 3. VDD1 and VDD2 must have the same voltage.

Note: AKM assumes no responsibility for the usage beyond the conditions in this datasheet.

ELECTICAL CHARACTERISTICS

(Ta=25°C; VDD1= VDD2 = 3.3V; VSS1= VSS2 = 0V)

Power Supplies				
Parameter	**min**	**typ**	**max**	**Unit**
Power Supply (VDD1+VDD2) Normal Operation (Note 4)		18	30	mA

Note 4. No input and no load.

ANALOG CHARACTERISTICS (Audio)

(Ta=25°C; VDD1=VDD2= 3.3V; VSS1=VSS2=0V; Input Signal Frequency =1kHz; Measurement band width=10Hz ~ 20kHz; R_L =5kΩ, unless otherwise specified)

Parameter		min	typ	max	Unit
Output Level (Note 5)		-	2	-	Vrms
Gain		5.5	6	6.5	dB
THD+N (at 2Vrms output, VDD1≥3.135V)			-98	-	dB
Dynamic Range (-60dBFS with A-weighted)		98	102		dB
S/N (A-weighted)		98	102		dB
Inter channel Isolation		-	100		dB
Output Offset Voltage			±0	±5	mV
LPF Frequency Response	-3dB	-	130	-	kHz

Note 5. VDD1= ≥3.135V, THD+N=-98dB (typ.)

ANALOG CHARACTERISTICS (Video)

(Ta=25°C; VDD1=VDD2= 3.3V; VSS1=VSS2=0V; unless otherwise specified, Note 6, Note 7)

Parameter	Conditions	min	typ	max	Unit
Input Signal				1.5	Vpp
Output Gain	Input=0.2Vp-p, 100kHz	5.5	6	6.5	dB
Output Signal	f=100kHz, THD=-30dB.	2.52			Vpp
Frequency Response Input=0.2Vpp, Sin Wave (0dB at 100kHz)	Response at 6.75MHz	-	-0.5	-	dB
	Response at 27MHz	-	-43	-	dB
Group Delay Distortion	|GD3MHz–GD6MHz|	-	10	-	nsec
S/N (*)	BW= 100kHz to 6MHz.	72	81		dB
Load Resistance	R1+R2 (Note 8)	140	150	-	Ω
Load Capacitance	C1 (Note 8)			400	pF
	C2 (Note 8)			15	pF

Note 6. The analog characteristics are specified at the pin of each output.

Note 7. Input Sync Tip Level=-0.43V~-0.14V(the sync chip level based on the pedestal level)
Horizontal Line Sync Pulse=4.0µs ~5.4µs, Equalizing Pulse=2.0µs ~2.7µs, Serration Pulse=4.0µs ~5.4µs

Note 8. Refer to Figure 2.
*CCIR 567 weighting.

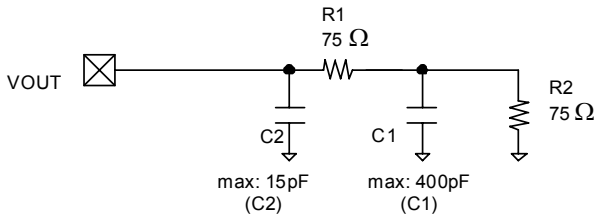


Figure 2. Load Resistance R1+R2 and Load Capacitance C1/C2.

OPERATION OVERVIEW

■ Charge Pump Circuit

Internal negative power supply circuit (Figure 3) supplies the negative voltage to the video amp, and the video amp 0V output is used for a pedestal level (Figure 4 and Figure 5). Therefore, the output coupling capacitor can be removed.

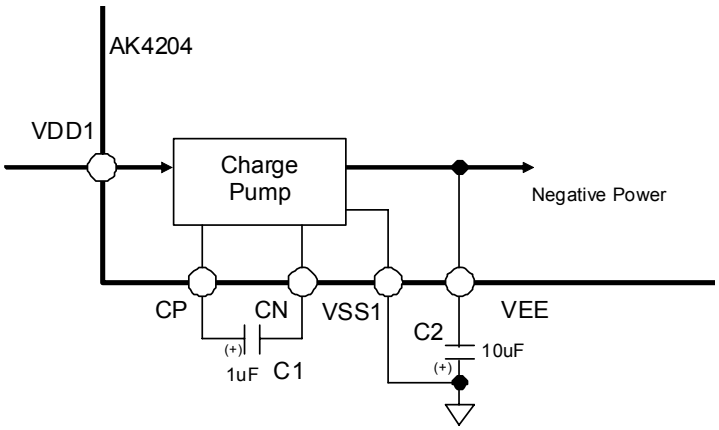


Figure 3. Charge Pump Circuit

Note 9. C1 and C2 should be low ESR (Equivalent Series Resistance) capacitors. When these capacitors are polarized, the positive polarity pins should be connected to the CP or VSS1 pin.

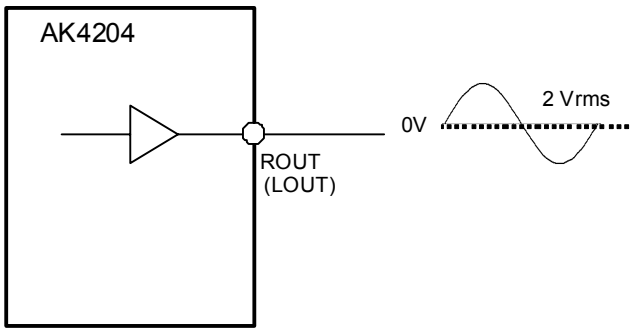


Figure 4. Audio Signal Output

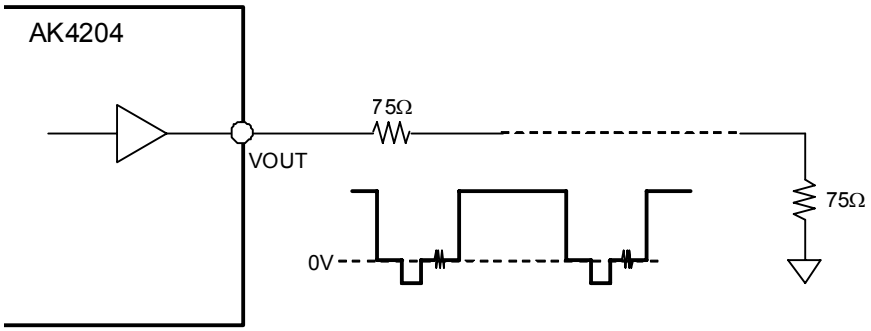


Figure 5. Video Signal Output

■ Audio Circuit Power-Up Sequence

The audio circuit of the AK4204 is powered-up when the APDN pin becomes "H". The charge pump starts operation when the APDN pin or VPDN pin is "H". The figure below shows an example of when the VPDN pin becoes "H" before the APDN pin.

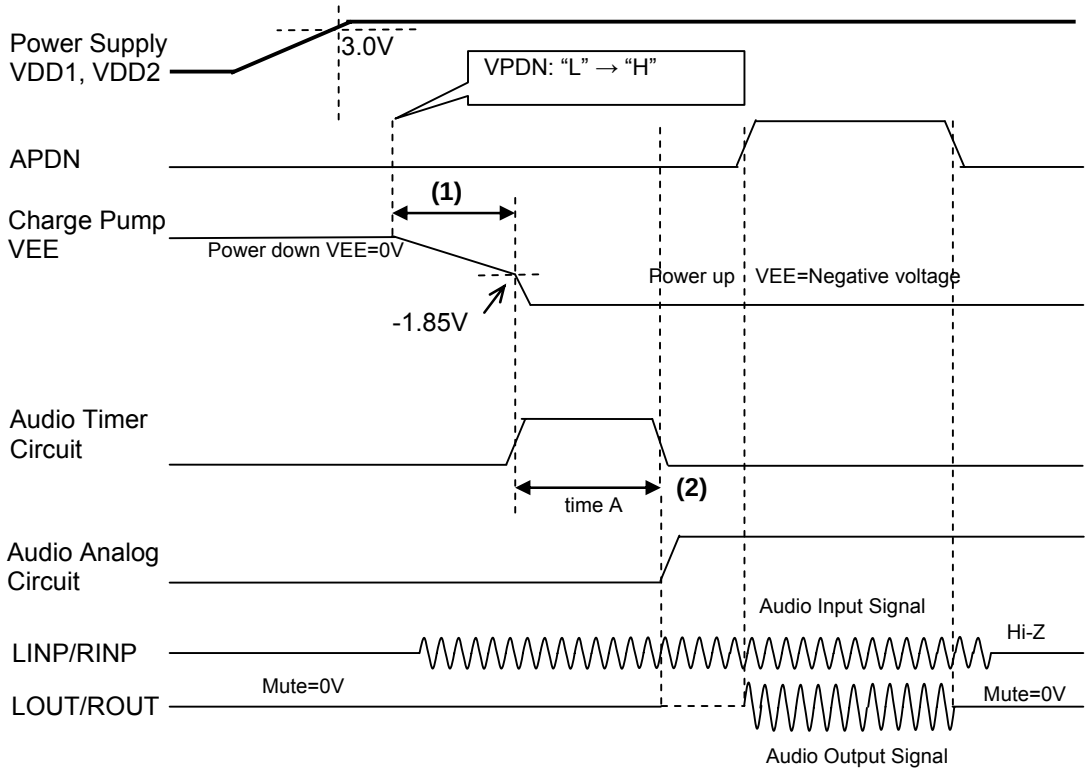


Figure 6. System Reset Diagram

(1) When VDD1 and VDD2 are powered-up, audio analog output is connected to VSS internally via a mute switch. The charge pump is powered-up in slow start mode, and the VEE voltage reachs -1.85V in 0.4ms (typ.).
(2) When the VEE reachs -1.85V, the audio timer circuit starts counting the "timeA" period (max. 15ms). The audio analog circuit is enabled after "time A". When the APDN pin becomes "H" while the audio analog circuit is enabled, the mute switch is released immediately and the audio signal is output.
(3) No audible click noise occurs under normal conditions.

■ Video Circuit Power-Up Sequence

The video circuit of the AK4204 is powered-up when the VPDN pin becomes "H". The charge pump starts operation when the VPDN pin or APDN pin is "H". The figure below shows an example of when the APDN pin becoes "H" before the VPDN pin.

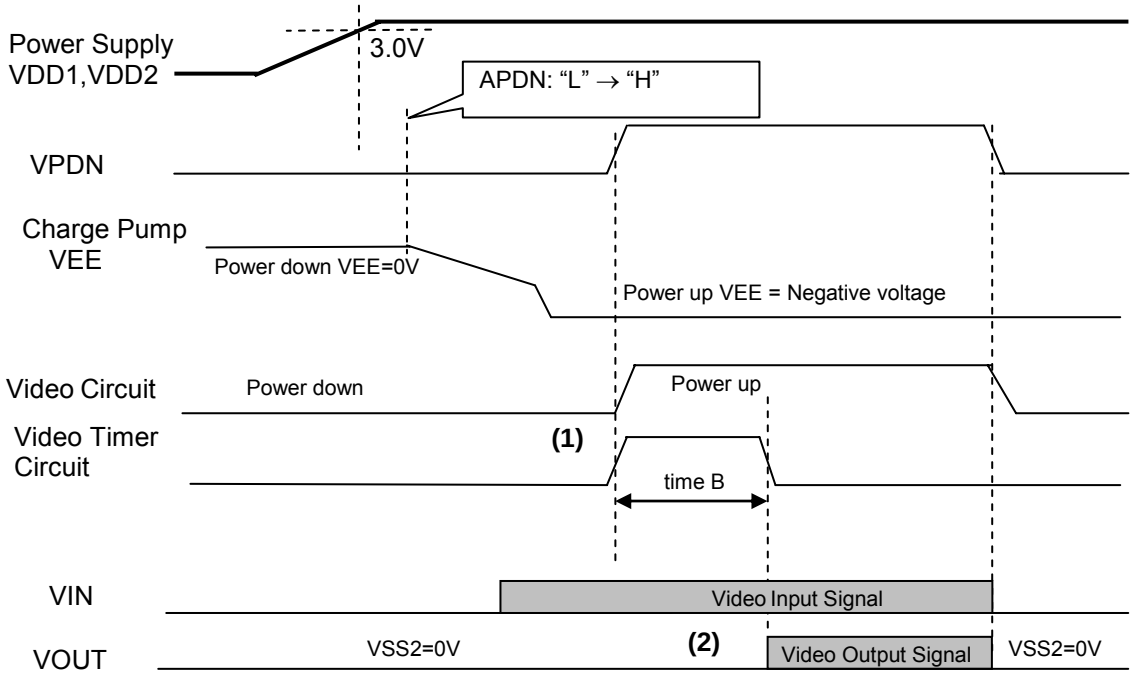


Figure 7. System Reset Diagram

(1) When the VPDN pin goes to "H", the video timer circuit starts counting "timeB" period (max. 100ms).
(2) After the "timeB" period, the video output becomes ebable exiting 0V state.

SYSTEM DESIGN

Figure 8 shows the system connection diagram for the AK4204. An evaluation board [AKD4204] demonstrates the optimum layout, power supply arrangements and measurement results.

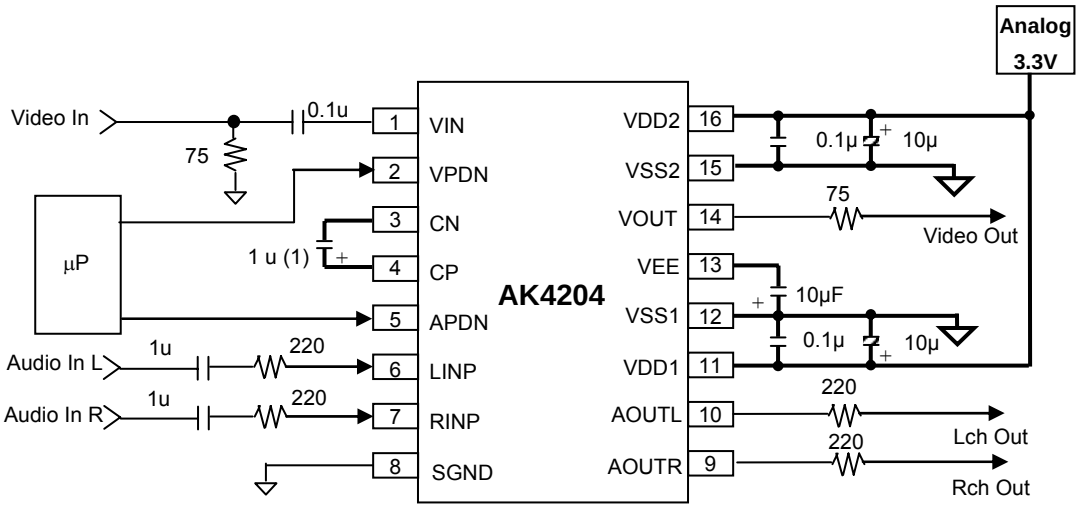


Figure 8. Typical Connection Diagram

1. Grounding and Power Supply Decoupling

The AK4204 requires careful attention to power supply and grounding arrangements. VDD1 and VDD2 are usually supplied from the analog supply in the system. If VDD1 and VDD2 are supplied separately, they must be powered-up at the same time. VSS1 and VSS2 pins must be connected to the analog ground plane. System analog ground and digital ground should be wired separately and connected together as close as possible to where the supplies are brought onto the printed circuit board. Decoupling capacitors for high frequency should be placed as near as possible to the supply pin.

2. Notes for Drawing a Board

Analog input and output pins should be as near as possible in order to avoid unwanted coupling into the AK4204. Unused pins should be open.

3. Analog Input

3-1. Audio Signal Input

The audio signal inputs are single-ended input. Connect a capacitor about 1uF to each input pin for AC coupling.

3-2. Video Signal Input

Tip Sync level is fixed by an internal clamp circuit. Connect a capacitor about 0.1uF to the VIN pin for AC coupling.

4. Analog Output

4-1. Audio Signal Output

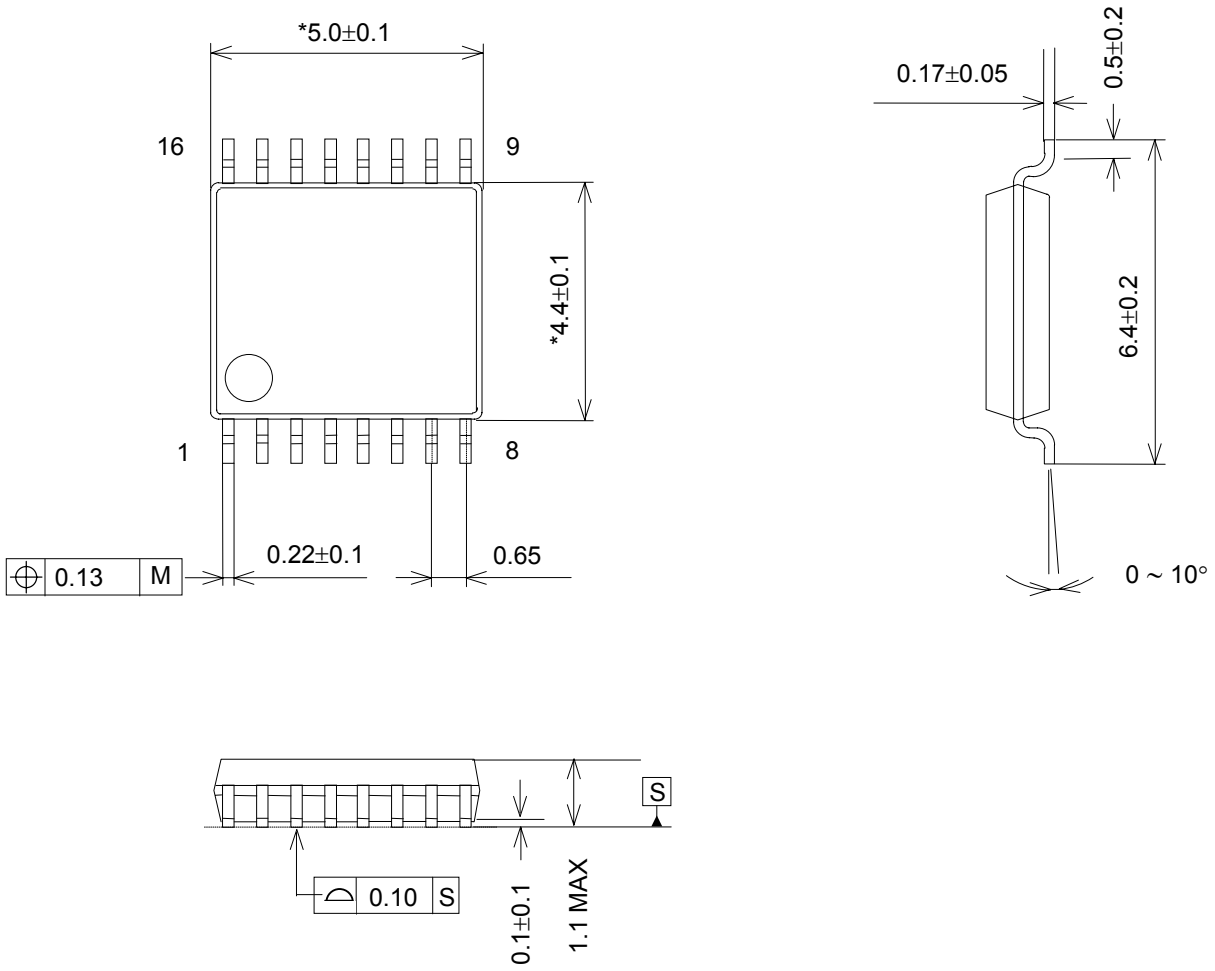
The audio signal outputs are single-ended output. The output rages to 2.0Vrms (typ) centered VSS (0V, typ) via LPF. The DC offset is less than ±5mV.

4-2. Video Signal Output

The integrated 1-channel video amplifier has drivability for a load resistance of 150Ω. The output gain is +6dB (typ) via LPF. DC offset is less than ±100mV.

PACKAGE

16pin TSSOP (Unit: mm)

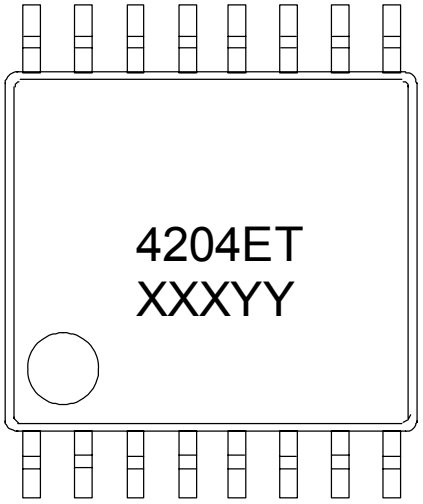


NOTE: Dimension "*" does not include mold flash.

■ Package & Lead Frame Material

Package molding compound: Epoxy Resign, Halogen (Br, Cl) Free
Lead frame material: Cu Alloy
Lead frame surface treatment: Solder (Pb free) Plate

MARKING



1) Pin #1 indication
2) Date Code: XXXYY (5 digits)
   XXX: Lot#
   YY: Date Code
3) Marketing Code: 4204ET

REVISION HISTORY

Date (Y/M/D)	Revision	Reason	Page	Contents
12/06/05	00	First Edition		
12/07/23	01	Specification Addition	6	ANALOG CHARACTERISTICS (Audio) Gain: The minimum and maximum values were added. Dynamic Range: The minimum value was added. S/N: The minimum value was added. ANALOG CHARACTERISTICS (Video) Output Gain: The minimum and maximum values were added. S/N: The minimum value was added.

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