

**Power Products Division**

*Advance Information*

**SELF-OSCILLATING  
HALF-BRIDGE DRIVER**

The MPIC2151 is a high voltage, high speed, self-oscillating power MOSFET and IGBT driver with both high side and low side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The front-end features a programmable oscillator which is similar to the 555 timer. The output drivers feature a high pulse current buffer stage and an internal deadtime designed for minimum driver cross-conduction. Propagation delays for the two channels are matched to simplify use in 50% duty cycle applications. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration that operates off a high voltage rail from 10 to 600 volts.

- Floating Channel Designed for Bootstrap Operation
- Fully Operational to +600 V
- Tolerant to Negative Transient Voltage
- dV/dt Immune
- Undervoltage Lockout
- Programmable Oscillator Frequency:

$$f = \frac{1}{1.4 (RT + 75\Omega) CT}$$

- Matched Propagation Delay for Both Channels
- Low Side Output In Phase with RT

**PRODUCT SUMMARY**

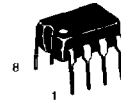
<b>V<sub>OFFSET</sub></b>	<b>600 V MAX</b>
<b>Duty Cycle</b>	<b>50%</b>
<b>V<sub>OUT</sub></b>	<b>10 – 20 V</b>
<b>t<sub>rrf</sub> (typical)</b>	<b>120 &amp; 60 ns</b>
<b>Deadtime (typical)</b>	<b>1.2 μs</b>

This document contains information on a new product. Specifications and information herein are subject to change without notice.

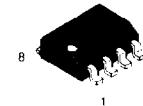
REV 1

**MPIC2151**

**SELF-OSCILLATING  
HALF-BRIDGE  
DRIVER**



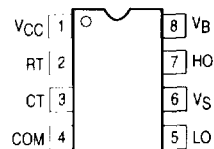
**P SUFFIX**  
PLASTIC PACKAGE  
CASE 626-05



**D SUFFIX**  
PLASTIC PACKAGE  
CASE 751-05  
(SO-8)

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**PIN CONNECTIONS**

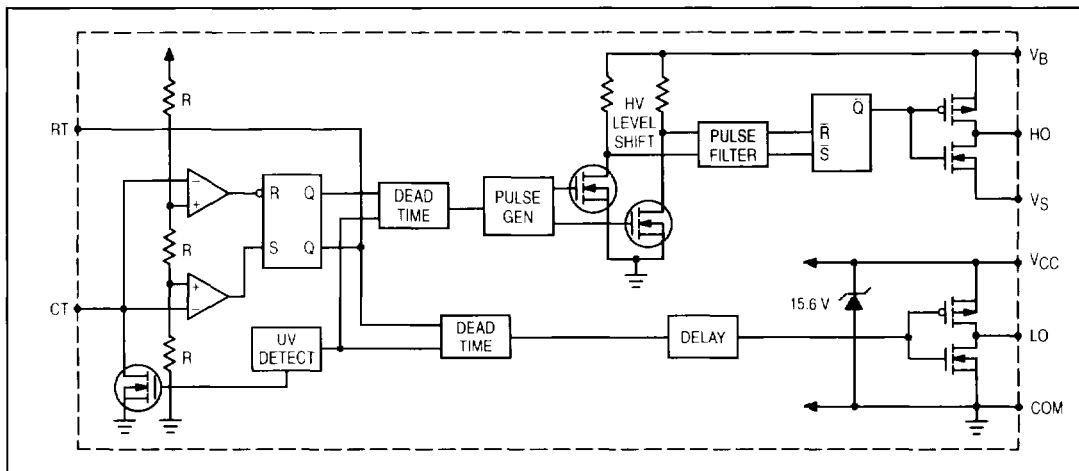


(TOP VIEW)

**ORDERING INFORMATION**

Device	Package
MPIC2151D	SOIC
MPIC2151P	PDIP

SIMPLIFIED BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM, all currents are defined positive into any lead. The Thermal Resistance and Power Dissipation ratings are measured under board mounted and still air conditions

Rating	Symbol	Min	Max	Unit
High Side Floating Supply Absolute Voltage	V <sub>B</sub>	-0.3	625	V <sub>DC</sub>
High Side Floating Supply Offset Voltage	V <sub>S</sub>	V <sub>B</sub> -25	V <sub>B</sub> +0.3	
High Side Floating Output Voltage	V <sub>HO</sub>	V <sub>S</sub> -0.3	V <sub>B</sub> +0.3	
Low Side Output Voltage	V <sub>LO</sub>	-0.3	V <sub>CC</sub> +0.3	
RT Voltage	V <sub>RT</sub>	-0.3	V <sub>CC</sub> +0.3	
CT Voltage	V <sub>CT</sub>	-0.3	V <sub>CC</sub> +0.3	
Supply Current (Note 1)	I <sub>CC</sub>		25	mA <sub>DC</sub>
High Side Output Current	I <sub>HO</sub>	-500	500	
Low Side Output Current	I <sub>LO</sub>	-500	500	
RT Output Current	I <sub>RT</sub>	-5.0	5.0	
Allowable Offset Supply Voltage Transient	dV <sub>S</sub> /dt	-	50	V/ns
*Package Power Dissipation @ T <sub>C</sub> : +25 C	P <sub>D</sub>	-	1.0	Watt
			0.625	
Operating and Storage Temperature	T <sub>j</sub> , T <sub>stg</sub>	-55	150	C
Thermal Resistance, Junction to Ambient	R <sub>thJA</sub>	-	125	C/W
			200	
Lead Temperature for Soldering Purposes, 10 seconds	T <sub>L</sub>	-	260	C

RECOMMENDED OPERATING CONDITIONS

The Input/Output logic timing Diagram is shown in Figure 1. For proper operation the device should be used within the recommended conditions.

Rating	Symbol	Min	Max	Unit
High Side Floating Supply Absolute Voltage	V <sub>B</sub>	V <sub>S</sub> +10	V <sub>S</sub> +V <sub>clamp</sub>	V
High Side Floating Supply Offset Voltage	V <sub>S</sub>	-	600	
High Side Floating Output Voltage	V <sub>HO</sub>	V <sub>S</sub>	V <sub>B</sub>	
Low Side Output Voltage	V <sub>LO</sub>	0	V <sub>CC</sub>	
Supply Current (Note 1)	I <sub>CC</sub>	-	5.0	mA
Ambient Temperature	T <sub>A</sub>	-40	125	C

Note 1: Because the MPIC2151 is designed specifically for off-line supply systems, this IC contains a zener clamp structure between the chip V<sub>CC</sub> and COM which has a nominal breakdown voltage of 15.6 V. Therefore, the IC supply voltage is normally derived by forcing current into the supply lead (typically by means of a high value resistor connected between the chip V<sub>CC</sub> and the rectified line voltage and a local decoupling capacitor from V<sub>CC</sub> to COM) and allowing the internal zener clamp circuit to determine the nominal supply voltage. Therefore, this circuit should not be driven by a DC, low impedance power source of greater than V<sub>CLAMP</sub>.

**ELECTRICAL CHARACTERISTICS** ( $T_C = 25\text{ }^\circ\text{C}$  unless otherwise specified)

Characteristic	Symbol	Min	Typ	Max	Unit
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**STATIC ELECTRICAL CHARACTERISTICS****Supply Characteristics**

$V_{BIAS}$  ( $V_{CC}$ ,  $V_{BS}$ ) = 12 V,  $V_{SS}$  = COM and  $C_L = 1000\text{ pF}$  unless otherwise specified.

$V_{CC}$ Supply Undervoltage Positive Going Threshold	$V_{CCUV+}$	-	8.4	-	$V_{DC}$
$V_{CC}$ Supply Undervoltage Negative Going Threshold	$V_{CCUV-}$	-	8.0	-	
Quiescent $V_{CC}$ Supply Current	$I_{QCC}$	-	400	-	$\mu\text{A}$
$V_{CC}$ Zener Shunt Clamp Voltage @ $I_{OC} = 5\text{ mA}$	$V_{CLAMP}$	-	15.6	-	$V_{DC}$

**Floating Supply Characteristics**

Offset Supply Leakage Current @ $V_B = V_S = 600\text{ V}$	$I_{LK}$	-	-	50	$\mu\text{ADC}$
Quiescent $V_{BS}$ Supply Current	$I_{QBS}$	-	10	-	

**Oscillator I/O Characteristics**

Oscillator Frequency @ $RT = 35.7\text{ K}\Omega$ , $CT = 1\text{ nF}$	$f_{OSC}$	-	20	-	$\text{kHz}$
Oscillator Frequency @ $RT = 7.04\text{ K}\Omega$ , $CT = 1\text{ nF}$	$f_{OSC}$	-	100	-	
CT Input Current	$I_{CT}$	-	0.001	1.0	$\mu\text{A}$
CT Undervoltage Lockout @ $2.5\text{ V} < V_{CC} < V_{CCUV+}$	$V_{CTUV}$	-	0	-	$\text{mV}$
RT High Level Output Voltage, $V_{CC} - RT$ @ $I_{RT} = -100\text{ }\mu\text{A}$ @ $I_{RT} = -1\text{ mA}$	$V_{RT+}$	-	20	-	
	$V_{RT+}$	-	200	-	
RT Low Level Output Voltage, $V_{CC} + RT$ @ $I_{RT} = 100\text{ }\mu\text{A}$ @ $I_{RT} = 1\text{ mA}$	$V_{RT-}$	-	20	-	
	$V_{RT-}$	-	200	-	
RT Undervoltage Lockout, $V_{CC} - RT$ @ $2.5\text{ V} < V_{CC} < V_{CCUV+}$	$V_{RTUV}$	-	0	-	
2/3 $V_{CC}$ Threshold	$V_{CT+}$	-	8.0	-	$V_{DC}$
1/3 $V_{CC}$ Threshold	$V_{CT-}$	-	4.0	-	

**Output Characteristics**

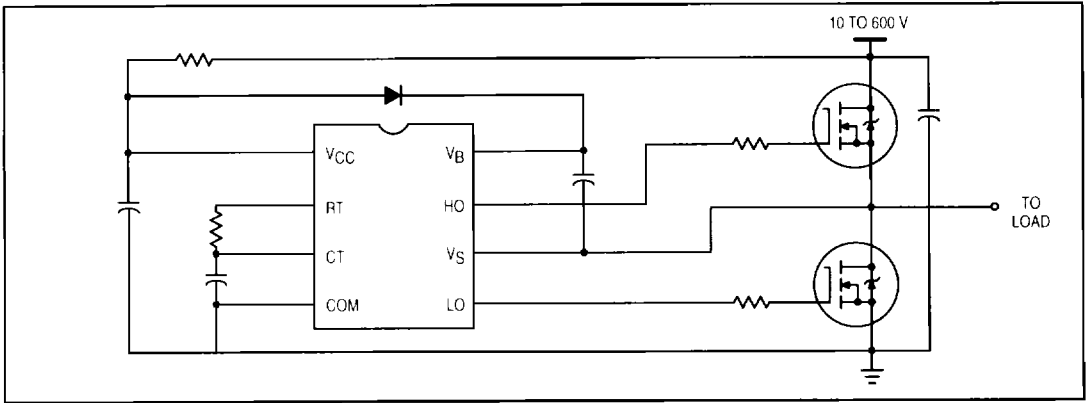
High Level Output Voltage, $V_{BIAS}-V_O$ @ $I_O = 0\text{ A}$	$V_{OH}$	-	-	100	$\text{mV}$
Low Level Output Voltage, $V_O$ @ $I_O = 0\text{ A}$	$V_{OL}$	-	-	100	

**Dynamic Electrical Characteristics**

$V_{BIAS}$  ( $V_{CC}$ ,  $V_{BS}$ ) = 12 V and  $C_L = 1000\text{ pF}$  unless otherwise specified.  $T_A = 25\text{ }^\circ\text{C}$ .

Turn-On Rise Time	$t_r$	-	120	-	$\text{ns}$
Turn-Off Fall Time	$t_f$	-	60	-	
Deadtime, LS Turn-Off to HS Turn-On & HS Turn-Off to LS Turn-On	$DT$	-	1.2	-	$\mu\text{A}$
RT Duty Cycle, $f_{OSC} = 20\text{ kHz}$	$DC$	-	50	-	%

TYPICAL CONNECTION



LEAD DEFINITIONS

Symbol	Lead Description
RT	Oscillator timing resistor input; a resistor is connected from RT to CT. RT is in phase with LO for normal IC operation.
CT	Oscillator timing capacitor input; a capacitor is connected from CT to COM in order to program the oscillator frequency according to the following equation: $f = \frac{1}{1.4 (RT + 75\Omega) CT}$ where 75Ω is the effective impedance of the RT output stage.
VB	High Side Floating Supply
HO	High Side Gate Drive Output
VS	High Side Floating Supply Return
VCC	Logic and Low Side Fixed Supply
LO	Low Side Gate Drive Output
COM	Logic and Low Side Return

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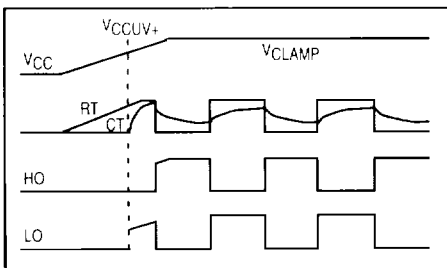


Figure 1. Input / Output Timing Diagram

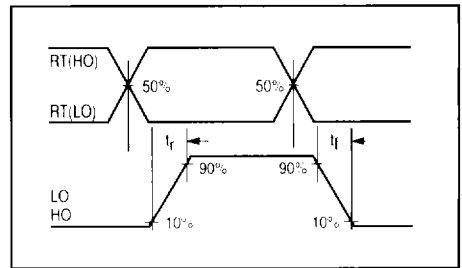


Figure 2. Switching Time Waveform Definitions

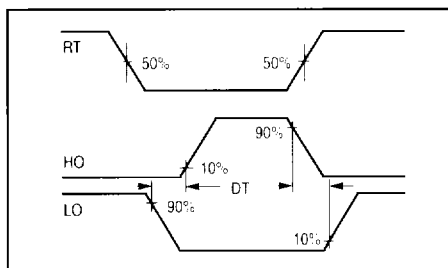


Figure 3. Deadtime Waveform Definitions