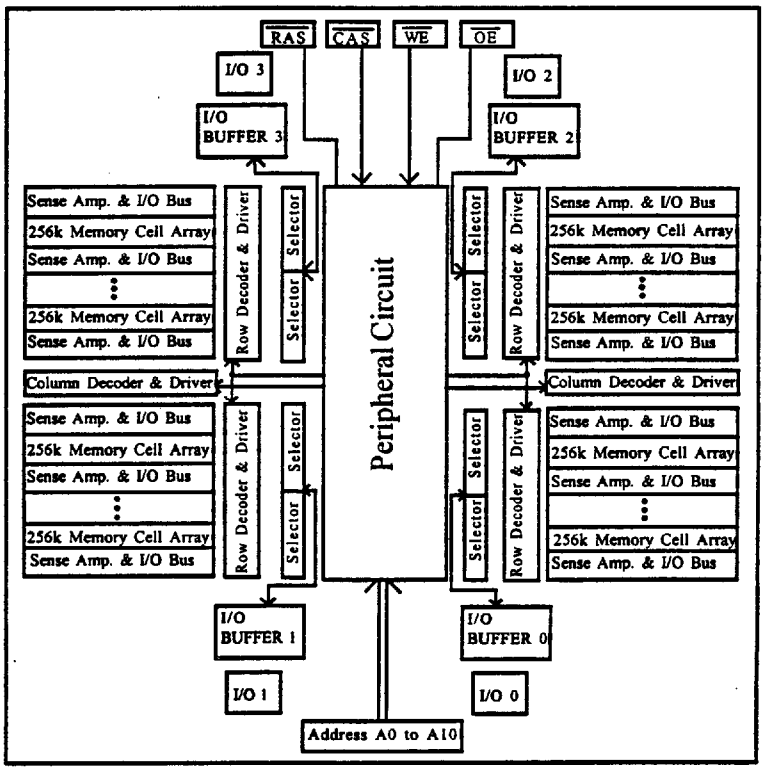
16Meg DRAM - Radiation Hardened

14C0164RP

CMOS 4M x 4 bit Dynamic RAM

For Space Applications



SEI's 14C0164RP (RP for RAD-PAK®) high density 16 Megabit (4 Mword x 4-bit) DRAM microcircuit features a minimum 100 kilorad (Si) total dose tolerance. The 14C0164RP employs the most advanced CMOS technology for high performance and low power. The 14C0164RP offers Fast Page Mode as a high speed access mode. These advanced CMOS features combined with SEi's radiation hardened RAD-PAK® packaging technology makes the 14C0164RP a complete solution for high-speed memory needs. Capable of surviving space environments, the 14C0164RP is ideal for satellite, spacecraft, and space probe missions. SEi's RAD-PAK® advanced technology incorporates radiation shielding in the microcircuit package. It eliminates box shielding while providing lifetime in orbit. The 14C0164RP provides a total dose survivability of greater than 100krad(Si). It is available in Class S packaging and screening.

SEi SPACE ELECTRONICS INCORPORATED
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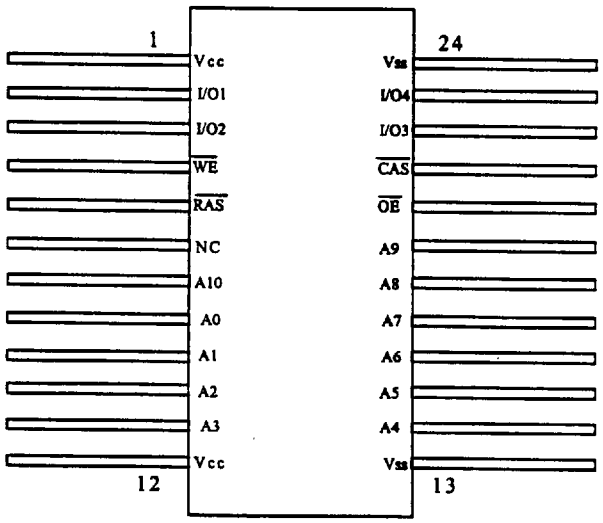
Radiation Hardened

14C0164RP

CMOS 24 Pin
4 Megaword x 4 bit Dynamic RAM



PIN CONFIGURATION

TOP VIEW

Features:

- 4 Megaword x 4 bit Organization
- RAD-PAK® Radiation Hardened Against Natural Space Radiation
- Total Dose Hardness >100 krad (Si)
- Package:
  - 24 Pin RAD-PAK® flat pack (420 mils x 740 mils)
  - Weight – 6.0 grams
  - 24 Pin RAD-PAK® DIP (1.490 mils x 610 mils)
  - Weight - 6.0 grams
- Single 5V (±10%)
- High Speed Access Time
  - 70 ns
- Long Refresh Period
  -2048 Refresh Cycles: 32ms
- Low Power Dissipation
  - Active Mode: 550mW(max)
  - Standby Mode: 11mW(max),
- Fast Page Mode Capability
- 3 Variations of Refresh
  - RAS-only refresh
  - CAS-before-RAS refresh
  - Hidden refresh
- Test Function
  - 16 Bit Parallel Test Mode
- Screening per TM 5004
- QCI per TM5005

TQM
Total Quality Management

Aug 1996

For Further Information Contact:
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14C0164RP ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	MIN	MAX	UNIT
Voltage on Any Pin Relative to Vss	V_T	-1.0	+7.0	V
Supply Voltage Relative to Vss	Vcc	-1.0	+7.0	V
Short Circuit Output Current	Iout		50	mA
Power Dissipation	P_T		1.0	W
Operating Temperature	Topr	0	+70	°C
Storage Temperature	Tstg	-55	+125	°C

14C0164RP RECOMMENDED DC OPERATING CONDITIONS

(Ta = 0 to +70°C)

PARAMETER 1/	SYMBOL	MIN	MAX	UNIT
Supply Voltage	Vcc	4.5	5.5	V
Input High Voltage	V_{IH}	2.4	6.5	V
Input Low Voltage	V_{IL}	-1.0	0.8	W

Note:

1/ All voltage referred to Vss.

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14C0164RP DC ELECTRICAL CHARACTERISTICS

(Ta = 0 to +70 °C, Vcc = 5V ± 10%, Vss = 0V, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITION	MIN	MAX	UNIT
Operating Current 2/ 3/	I_{CC1}	t_{RC} = min		100	µA
Standby Current	I_{CC2}	TTL interface RAS, CAS = V_{IH} Dout = High-Z		2	mA
		CMOS interface RAS, CAS > V_{CC} - 0.2V Dout = High-Z		1	
$\overline{\text{RAS}}$-only Refresh Current 3/	I_{CC3}	t_{RC} = min		100	mA
Standby Current 2/	I_{CC5}	RAS = V_{IH} CAS = V_{IL} Dont = enable		5	mA
$\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ Refresh Current	I_{CC6}	t_{RC} = min		100	mA
Fast Page Mode Current 2/ 4/	I_{CC7}	t_{PC} = min		70	mA
Input Leakage Current	I_{LI}	0V ≤ V_{IN} ≤ 7V	-10	10	µA
Output Leakage Current	I_{LO}	0V ≤ Vout ≤ 7V Dout = disable	-10	10	µA
Output High Voltage	V_{OH}	High Iout = -5mA	2.4	Vcc	V
Output Low Voltage	V_{OL}	Low Iout = 4.2mA	0	0.4	V

Note:

2/ Icc depends on output load condition when the device is selected. Icc max is specified at the output open condition.

3/ Address can be changed once or less while $\overline{\text{RAS}}$ = V_{IL}.

4/ Address can be changed once or less while $\overline{\text{CAS}}$ = V_{IH}.

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14C0164RP CAPACITANCE

(Ta = 25°C, Vcc = 5V ±10%, unless otherwise specified)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Input Capacitance (Address) 5/	C_{I1}		---	5	pF
Input Capacitance (Clocks) 5/	C_{I2}		---	7	pF
Output Capacitance (Data-in, Data-out) 5/ 6/	$C_{I/O}$		---	7	pF

Note:

5/ Capacitance measured with Boonton Meter or effective capacitance measuring method.
6/ $\overline{CAS}$ = V_{IH} to disable Dout.

14C0164RP AC ELECTRICAL CHARACTERISTICS 7/ 8/ 9/ 25/ 26/

(Ta = 0 to +70°C, Vcc = 5V ±10%, unless otherwise noted)

Read, Write, Read-Modify-Write and Refresh Cycles

PARAMETER	SYMBOL	MIN	MAX	UNIT
Random Read or Write Cycle Time	t_{RC}	130	—	ns
$\overline{RAS}$ Precharge Time	t_{RP}	50	—	ns
$\overline{CAS}$ Precharge Time	t_{CP}	10	—	ns
$\overline{RAS}$ Pulse Width	t_{RAS}	70	10000	ns
$\overline{CAS}$ Pulse Width	t_{CAS}	18	10000	ns
Row Address Setup Time	t_{ASR}	0	—	ns
Row Address Hold Time	t_{RAH}	10	—	ns
Column Address Setup Time	t_{ASC}	0	—	ns
Column Address Hold Time	t_{CAH}	15	—	ns
$\overline{RAS}$ to $\overline{CAS}$ Delay Time 10/	t_{RCD}	20	52	ns
$\overline{RAS}$ to Column Address Delay Time 11/	t_{RAD}	15	35	ns
$\overline{RAS}$ Hold Time	t_{RSH}	18	—	ns
$\overline{CAS}$ Hold Time	t_{CSH}	70	—	ns
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	5	—	ns

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Read, Write, Read-Modify-Write and Refresh Cycles (continued)

PARAMETER		SYMBOL	MIN	MAX	UNIT
$\overline{OE}$ to Din Delay Time	12/	t_{OED}	18	—	ns
$\overline{OE}$ Delay Time from Din	13/	t_{DZO}	0	—	ns
$\overline{CAS}$ Delay Time from Din	13/	t_{DZC}	0	—	ns
Transition Time (Rise and Fall)	14/	t_T	3	50	ns

Read Cycle

PARAMETER		SYMBOL	MIN	MAX	UNIT
Access Time from $\overline{RAS}$	15/ 16/ 27/	t_{RAC}	---	70	ns
Access Time from $\overline{CAS}$	16/ 17/ 24/ 27/	t_{CAC}	---	18	ns
Access Time from Address	16/ 18/ 24/ 27/	t_{AA}	---	35	ns
Access Time from $\overline{OE}$	16/ 27/	t_{OEA}	---	18	ns
Read Command Setup Time		t_{RCS}	0	---	ns
Read Command Hold Time to $\overline{CAS}$	19/	t_{RCH}	0	---	ns
Read Command Hold Time to $\overline{RAS}$	19/	t_{RRH}	0	---	ns
Column Address to $\overline{RAS}$ Lead Time		t_{RAL}	35	---	ns
Column Address to $\overline{CAS}$ Lead Time		t_{CAL}	35	---	ns
$\overline{CAS}$ to Output in Low-Z		t_{CLZ}	0	---	ns
Output Data Hold Time		t_{OH}	3	---	ns
Output Data Hold Time from $\overline{OE}$		t_{OHO}	3	---	ns
Output Buffer Turn-Off Time	20/	t_{OFF}	---	15	ns
Output Buffer Turn-Off to $\overline{OE}$	20/	t_{OEZ}	---	15	ns
$\overline{CAS}$ to Din Delay Time	12/	t_{CDD}	18	---	ns

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Write Cycle

PARAMETER		SYMBOL	MIN	MAX	UNIT
Write Command Setup Time	21/	t_{WCS}	0	---	ns
Write Command Hold TIme		t_{WCH}	15	---	ns
Write CommandPulse Width		t_{WP}	10	---	ns
Write Command to $\overline{RAS}$ Lead Time		t_{RWL}	18	---	ns
Write Command to $\overline{CAS}$ Lead Time		t_{CWL}	18	---	ns
Data-in Setup Time	22/	t_{DS}	0	---	ns
Data-in Hold Time	22/	t_{DH}	15	---	ns

Read-Modify-Write Cycle

PARAMETER		SYMBOL	MIN	MAX	UNIT
Read-Modify-Write Cycle Time		t_{RWC}	181	---	ns
$\overline{RAS}$ to $\overline{WE}$ Delay Time	21/	t_{RWD}	98	---	ns
$\overline{CAS}$ to $\overline{WE}$ Delay Time	21/	t_{CWD}	46	---	ns
Column Address to $\overline{WE}$ Delay Time	21/	t_{AWD}	63	---	ns
$\overline{OE}$ Hold Time from $\overline{WE}$		t_{OEH}	18	---	ns

Refresh Cycle

PARAMETER	SYMBOL	MIN	MAX	UNIT
$\overline{CAS}$ Setup Time (CBR Refresh Cycle)	t_{CSR}	5	---	ns
$\overline{CAS}$ Hold Time (CBR Refresh Cycle)	t_{CHR}	10	---	ns
$\overline{WE}$ Setup Time (CBR Refresh Cycle)	t_{WRP}	0	---	ns
$\overline{WE}$ Hold Time (CBR Refresh Cycle)	t_{WRH}	10	---	ns
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	0	---	ns

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Fast Page Mode Cycle

PARAMETER	SYMBOL	MIN	MAX	UNIT
Fast Page Mode Cycle Time	t_{PC}	45	---	ns
Fast Page Mode $\overline{RAS}$ Pulse Width 23/	t_{RASP}	---	100000	ns
Access Time from $\overline{CAS}$ Precharge 16/ 24/ 27/	t_{CPA}	---	40	ns
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RASP}	40	---	ns

Fast Page Mode Read-Modify-Write Cycle

PARAMETER	SYMBOL	MIN	MAX	UNIT
Fast Page Mode Read-Modify-Write Cycle Time	t_{PRWC}	96	---	ns
$\overline{WE}$ Delay Time from $\overline{CAS}$ Precharge 21/	t_{CPW}	68	---	ns

Test Mode Cycle 27/

PARAMETER	SYMBOL	MIN	MAX	UNIT
Test Mode $\overline{WE}$ Setup Time	t_{WTS}	0	---	ns
Test Mode $\overline{WE}$ Hold Time	t_{WTH}	10	---	ns

Refresh Cycle

PARAMETER	SYMBOL	MIN	MAX	UNIT
Refresh Period 28/	t_{REF}		32	ms

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Notes:

8/ AC measurements assume $t_T = 5$ ns.

9/ An initial pause of 200 µs is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing RAS-only refresh or CAS-before-RAS refresh). If the internal refresh counter is used, a minimum of eight CAS-before-RAS refresh cycles are required.

10/ Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.

11/ Operation with the t_{RAD} (max) limit insures that T_{RAC} (max) can be met, T_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by tAA.

12/ Either t_{OED} or t_{CDD} must be satisfied.

13/ Either t_{DZO} or t_{DZC} must be satisfied.

14/ V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} (min) and V_{IL} (max).

15/ Assumes that $I_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in thistable, t_{RAC} exceeds the value shown.

16/ Measured with a load circuit equivalent to 2 TTL loads and 100 pF.

17/ Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max).

18/ Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \geq t_{RAD}$(max).

19/ Either t_{RCH} or t_{RRH} must be satisfied for a read cycles.

20/ t_{OFF} (max) and t_{OEZ} (max) define the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.

21/ t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPW} are not restrictive operations parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geq t_{RWD}$ (min), $t_{CWD} \geq t_{CWD}$ (min), and $t_{AWD} \geq t_{AWD}$(min), or $t_{CWD} \geq t_{CWD}$(min), $t_{AWD} \geq t_{AWD}$(min) and $t_{CPW} \geq t_{CPW}$(min), the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

22/ These parameters are referred to CAS leading edge in early write cycles and to $\overline{WE}$ leading edge in delayed write or read-modify-write cycles.

23/ t_{RASP} defines RAS pulse width in fast page mode cycles.

24/ Access time is determined by the longer of t_{AA} or t_{CAC} or t_{CPA}.

25/ In delayed write or read-modify-write cycles, OE must disable output buffer prior to applying data to the device. After RAS is reset, if $t_{OEH} \geq t_{CWL}$, the I/O pin will remain open circuit (high impedance); if $t_{OEH} \geq t_{CWL}$, invalid data will be out at each I/O.

26/ The 16M DRAM offers a 16-bits time saving parallel test mode. Address CA0 and CA1 for the 4M x 4 are don't care during test mode. Test mode is set by performing $\overline{WE}$-and-$\overline{CAS}$-before $\overline{RAS}$ (WCBR) cycle. In 16-bits parallel test mode, data is written into 4 bits in parallel at each I/O (I/O1 to I/O4) and read out from each I/O.

If 4 bits of each I/O are equal (all 1s or 0s), data output pin is a high state during test mode read cycle, then the device has passed. If they are not equal, data output pin is a low state, then the device has failed. Refresh during test mode operation can be performed by normal read cycles or by WCBR refresh cycles. To get out of test mode and enter a normal operation mode, perform either a regular $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle or $\overline{RAS}$-only refresh cycle.

27/ In a test mode read cycle, the value of t_{RAC}, t_{AA}, t_{CAC} and t_{CPA} is delayed by 2 ns to 5 ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.

28/ 2048 cycles.

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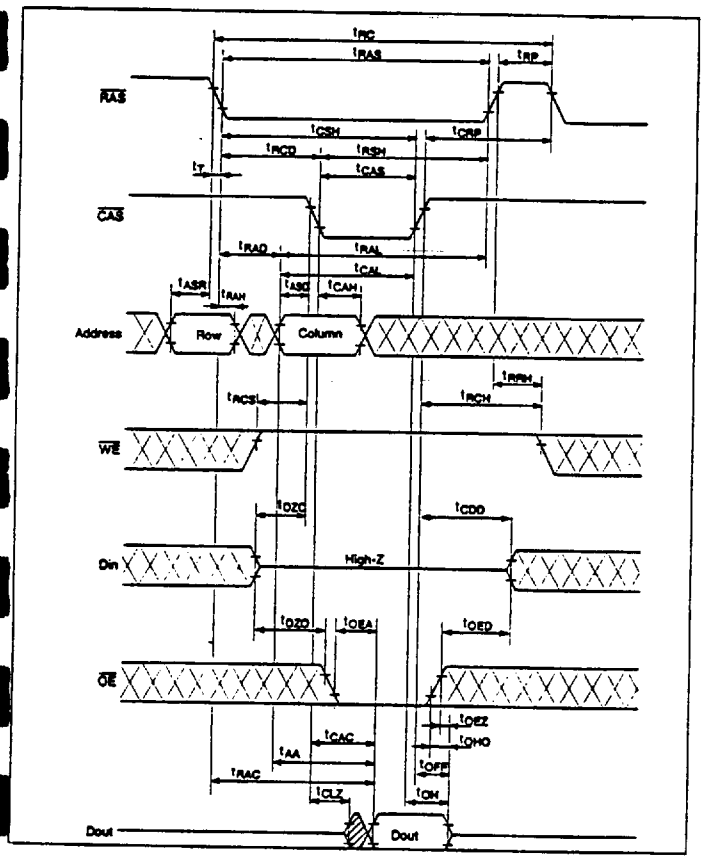
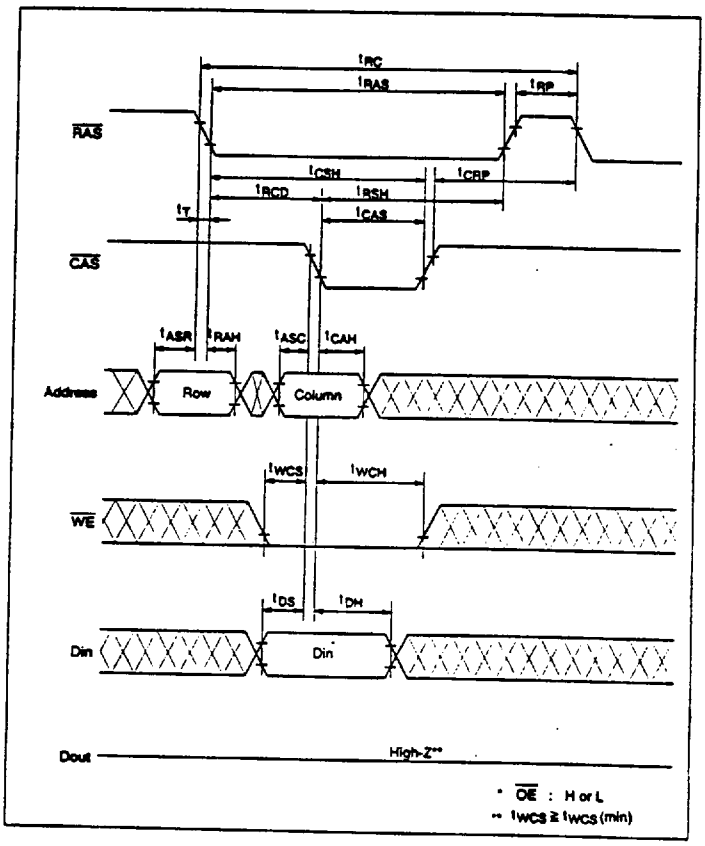
14C0164RP TIMING WAVEFORMS 29/

Read Cycle



Early Write Cycle



Note:

29/ ☒ H or L (H: $V_{IH(min)} \leq V_{IN} \leq V_{IN(max)}$, L: $V_{IL(min)} \leq V_{IN} \leq V_{IL(max)}$)

▨ Invalid Dout

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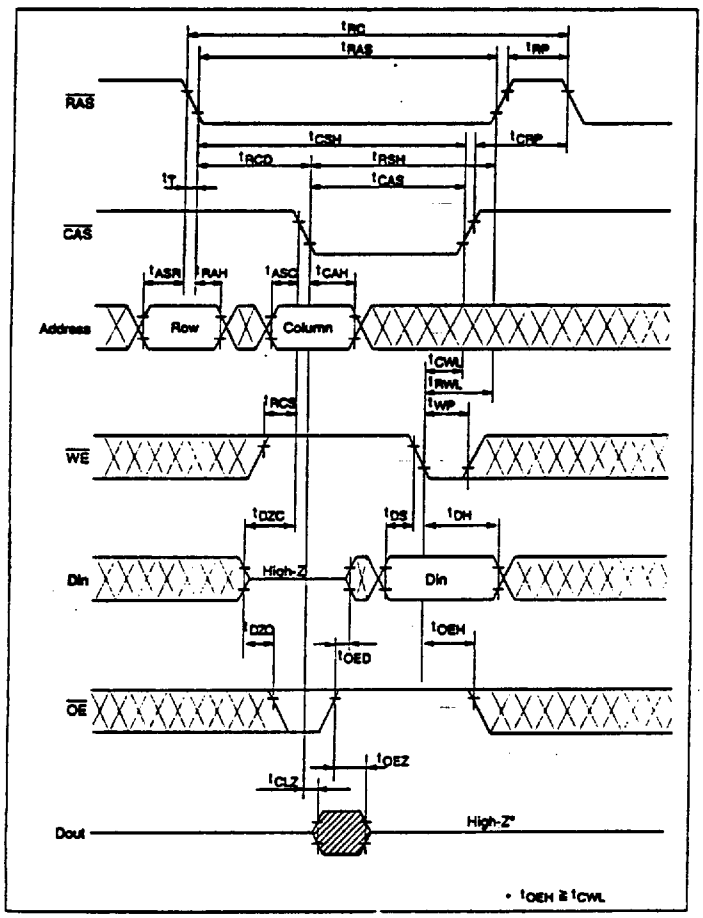
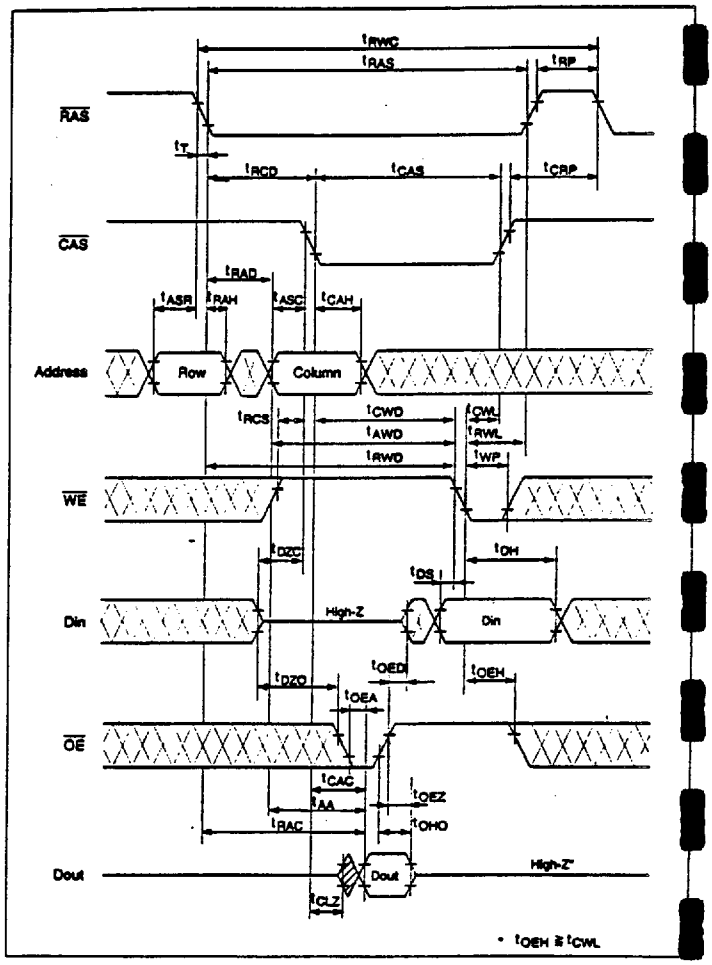
Delay Write Cycle 25/



Read-Modify-Write Cycle 25/



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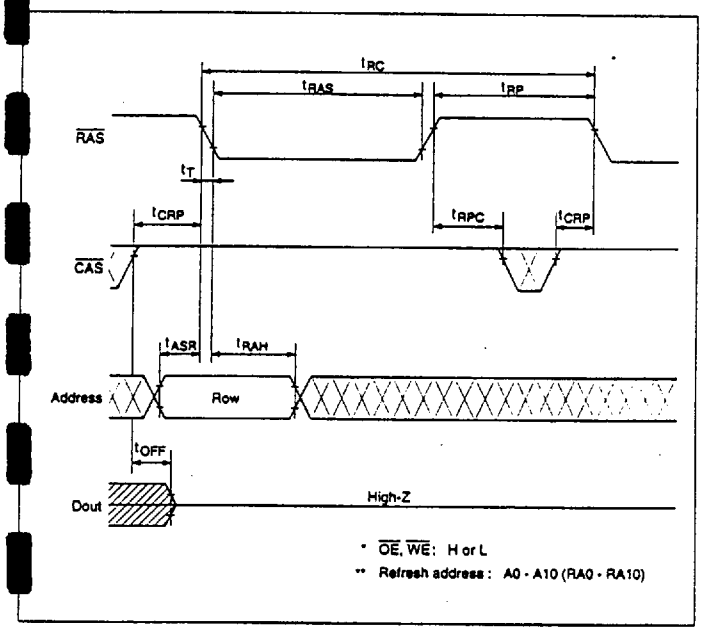
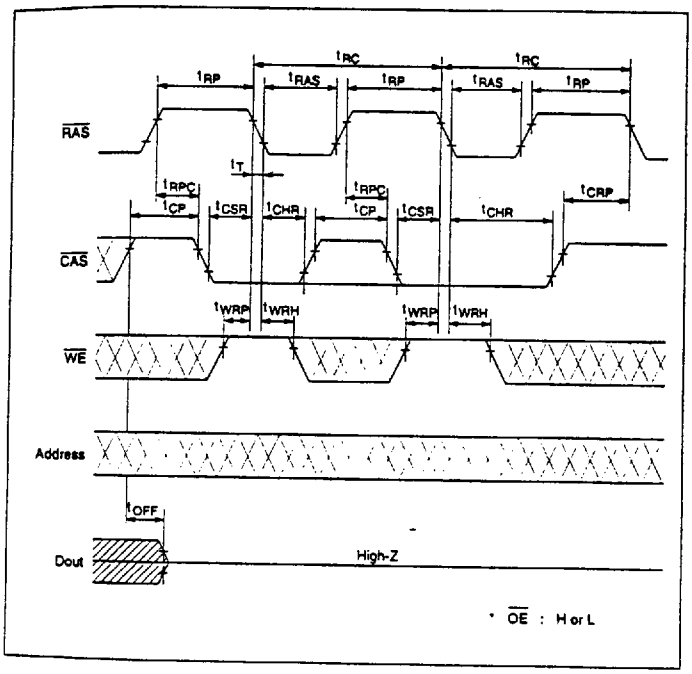
$\overline{\text{RAS}}$-Only Refresh Cycle



$\overline{\text{CAS}}$-Before-$\overline{\text{RAS}}$ Refresh Cycle



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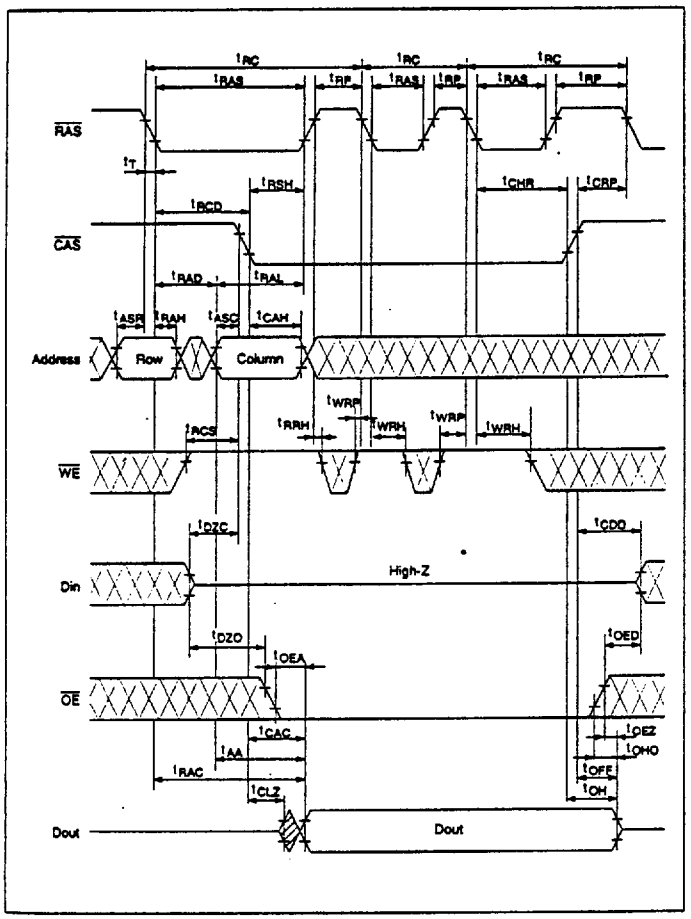
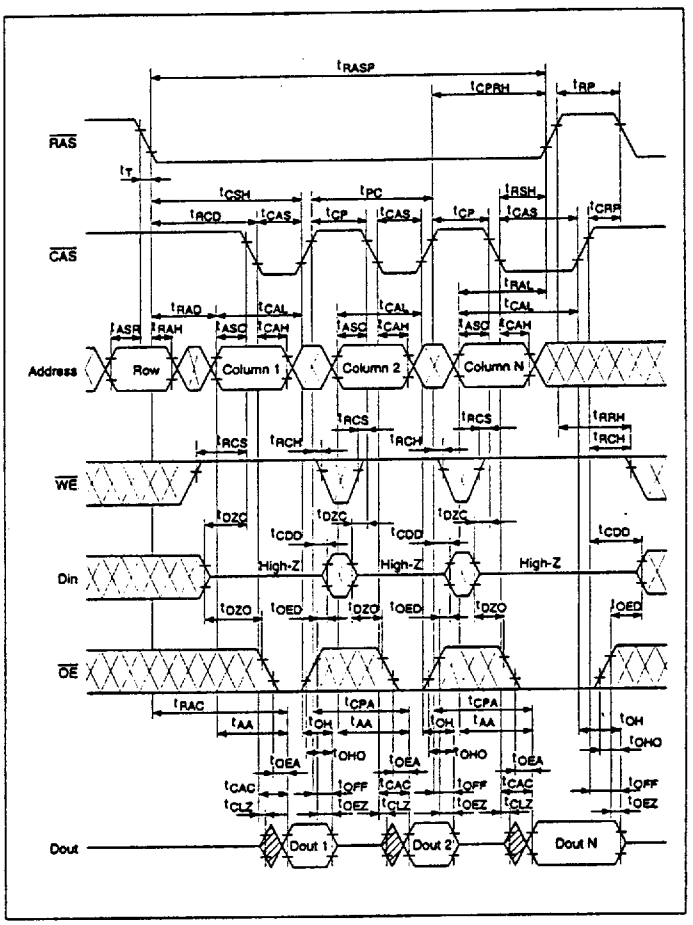
Hidden Refresh Cycle



Fast Page Mode Read Cycle



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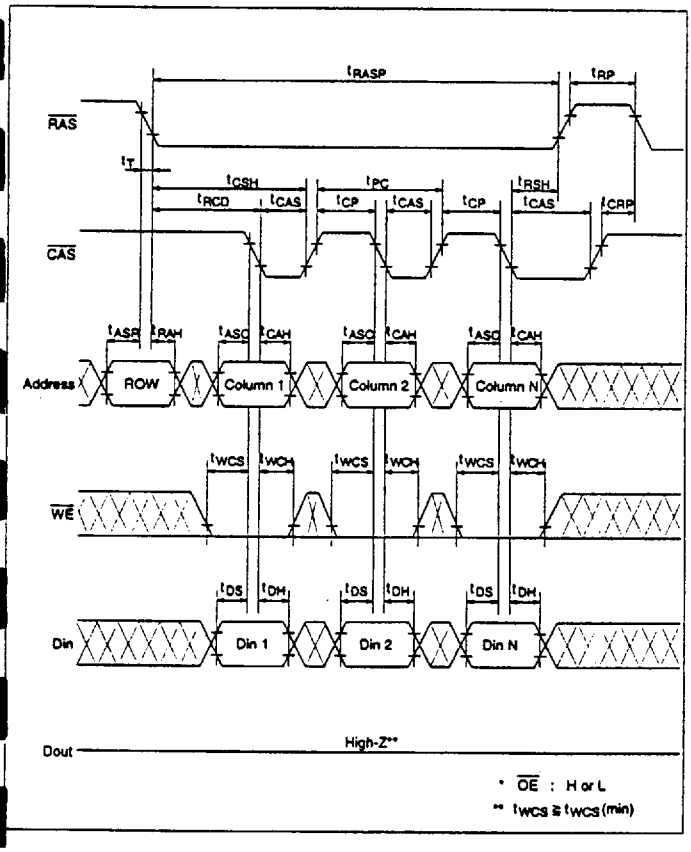
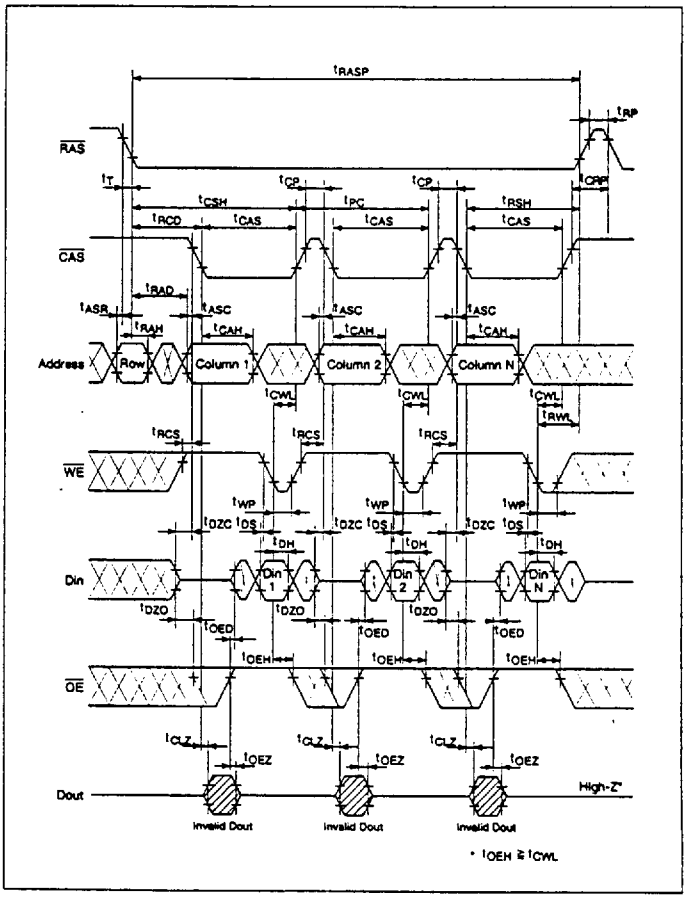
Fast Page Mode Early Write Cycle



Fast Page Mode Delayed Write Cycle 25/



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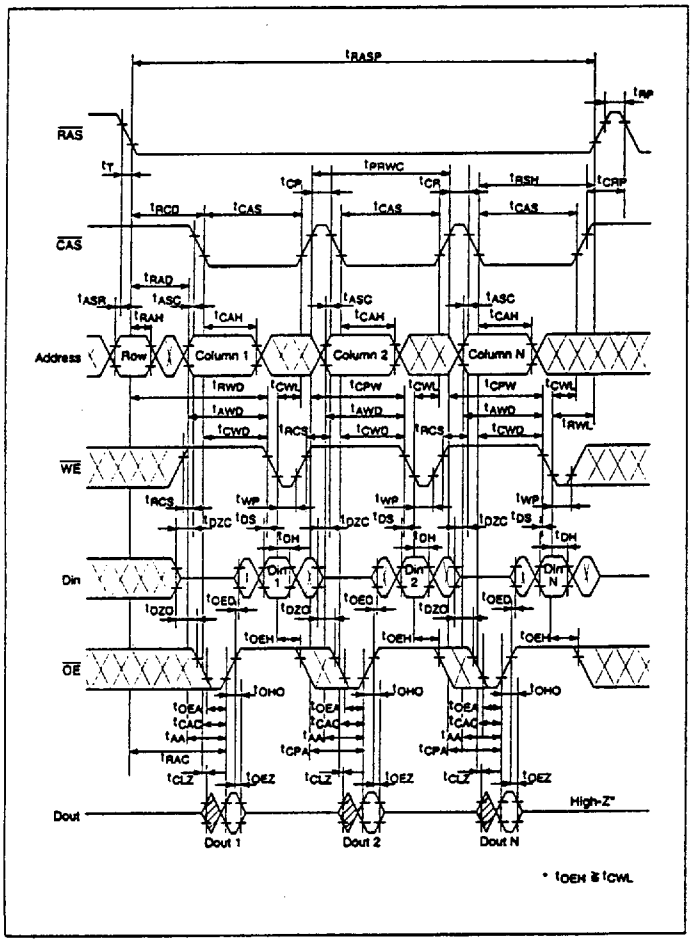
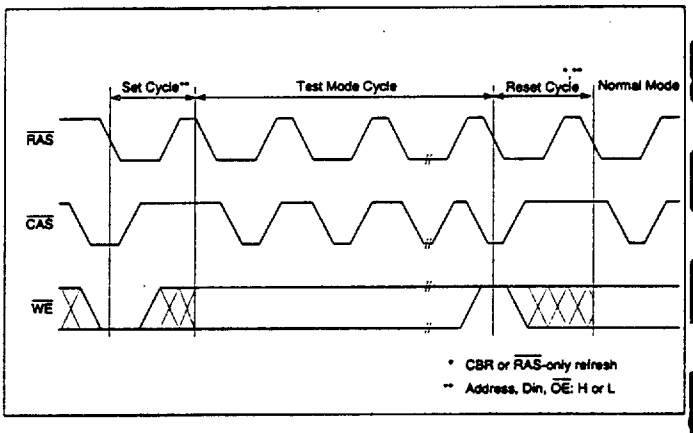
Fast Page Mode Read-Modify-Write Cycle 25/



Test Mode Cycle 26/



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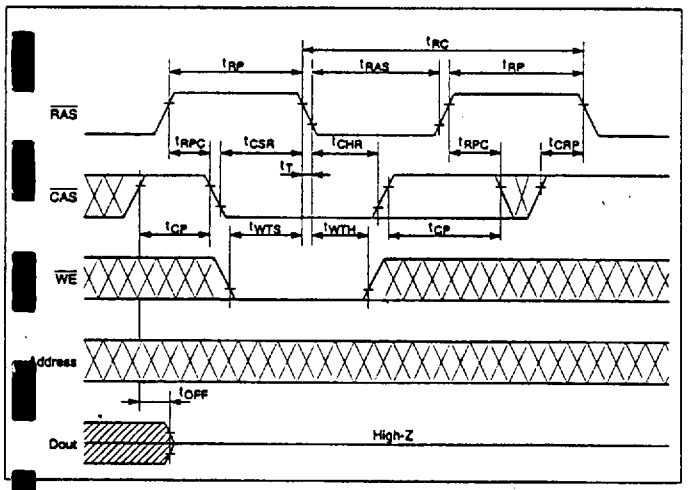
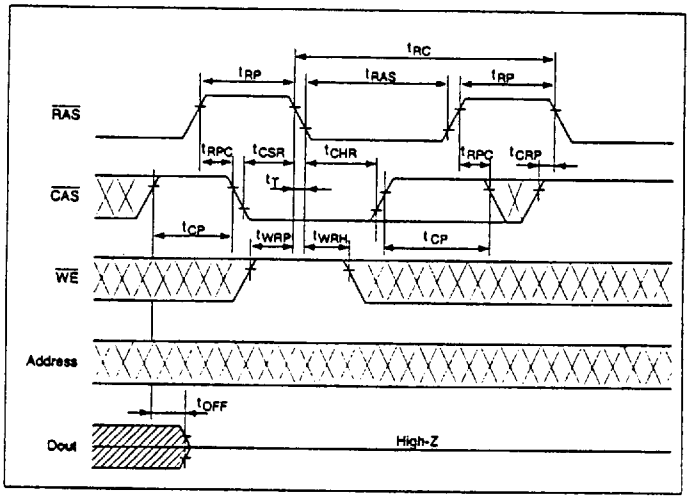
Test Mode Set Cycle



Test Mode Reset Cycle

CAS-Before-RAS Refresh Cycle



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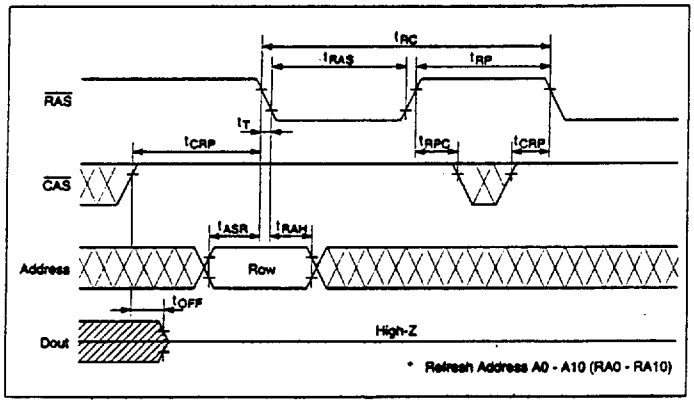
Test Mode Reset Cycle

$\overline{\text{RAS}}$-Only Refresh Cycle



14C0164RP Package Ordering Guide

Package Style	Case Outline 1/	Description
D	D-24	24 Pin Dual In Line Package
F	F-24	24 Pin Flat Package

Note:

1/ For outline information, see Appendix A (Package Information - Outline Dimension)

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