

Features :

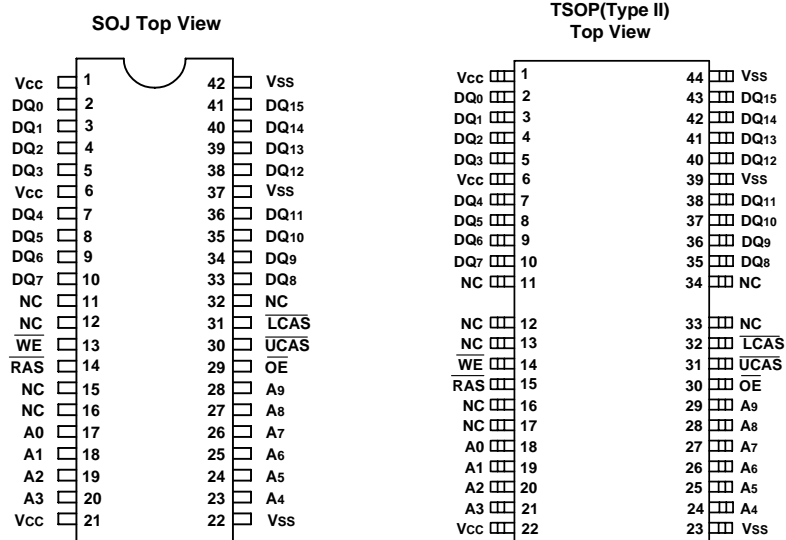
- * 1,048,576 words by 16 bits organization.
- * Fast access time and cycle time.
- * Dual $\overline{\text{CAS}}$ Input.
- * Low power dissipation.
- * Read-Modify-Write, $\overline{\text{RAS}}$ -Only Refresh, $\overline{\text{CAS}}$ -Before- $\overline{\text{RAS}}$ Refresh, Hidden Refresh.
- * 1024 refresh cycles per 16ms.
- * Available in 400 mil SOJ / TSOPII Packages.
- * Single 3.3V \pm 0.3V Power Supply.
- * Inputs and Outputs are TTL compatible.
- * Fast Page Mode operation.
- * Self refresh capability (S-Version)

Description :

The GLT4161L16 is a 1,048,576 x 16 bit high-performance CMOS dynamic random access memory. The GLT4161L16 offers Fast Page mode and has both BYTE WRITE and WORD WRITE access cycles via two $\overline{\text{CAS}}$ pins. The GLT4161L16 has symmetric address and accepts 1024-cycle refresh in 16ms interval.

All inputs are TTL compatible. Fast Page Mode operation allows random access up to 1024 x 16 bits within a page, with cycle times as short as 23ns.

HIGH PERFORMANCE	40	45	50	70
Max. $\overline{\text{RAS}}$ Access Time, (t_{RAC})	40 ns	45 ns	50 ns	70 ns
Max. Column Address Access Time, (t_{CAA})	20 ns	22 ns	25 ns	35 ns
Min. Extended Data Out Page Mode Cycle Time, (t_{PC})	23 ns	25 ns	28 ns	30 ns
Min. Read/Write Cycle Time, (t_{RC})	75 ns	80 ns	90 ns	124 ns
Max. $\overline{\text{CAS}}$ Access Time (t_{CAC})	12 ns	12 ns	15 ns	20 ns

Pin Configuration :

Pin Descriptions:

Name	Function
A ₀ - A ₉	Address Inputs
RAS	Row Address Strobe
UCAS	Column Address Strobe/Upper Byte Control
LCAS	Column Address Strobe/Lower Byte Control
WE	Write Enable
OE	Output Enable
DQ ₀ - DQ ₁₅	Data Inputs / Outputs
V _{CC}	+3.3V Power Supply
V _{SS}	Ground
NC	No Connection

Absolute Maximum Ratings*

Operating Temperature, T_A (ambient)
0°C to +70°C
 Storage Temperature(plastic)....-55°C to +150°C
 Voltage Relative to V_{SS}.....-1.0V to + 4.6V
 Short Circuit Output Current.....50mA
 Power Dissipation.....1.0W

*Note: Operation above Absolute Maximum Ratings can adversely affect device reliability.

Capacitance*

T_A=25°C, V_{CC}=3.3V±0.3V, V_{SS}=0V

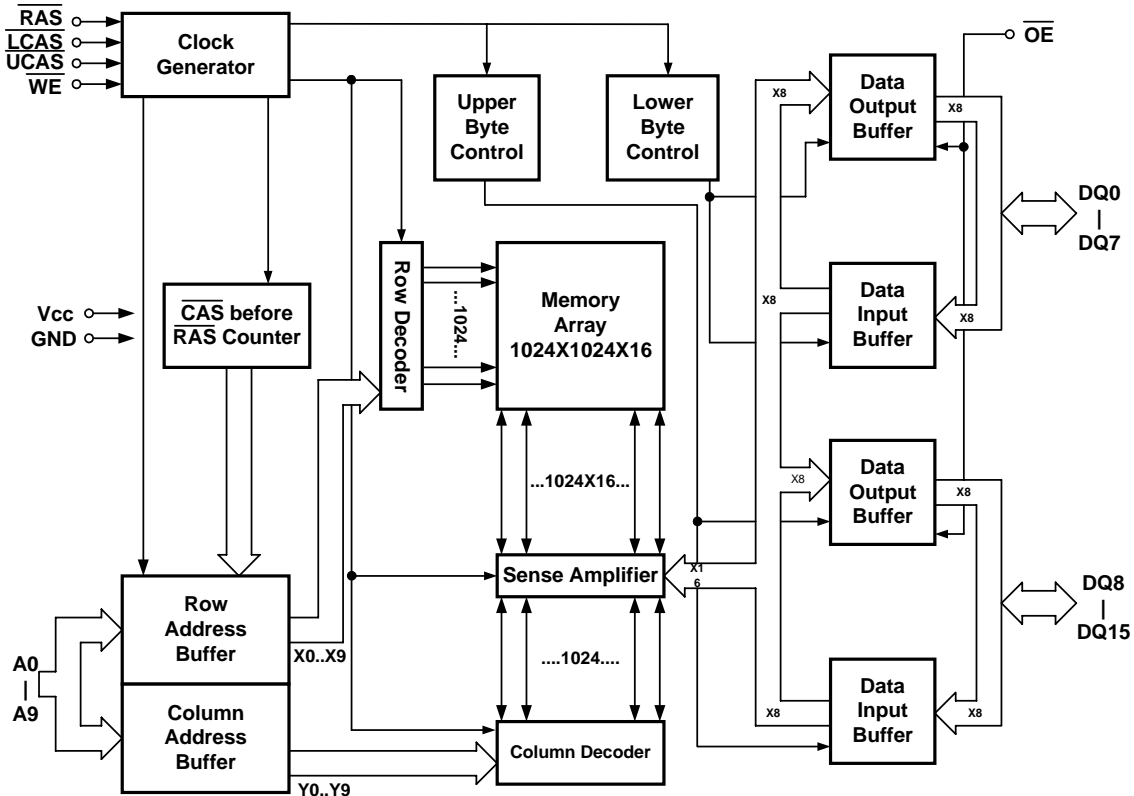
Symbol	Parameter	Max.	Unit
C _{IN1}	Address Input	5	pF
C _{IN2}	RAS, LCAS, UCAS, WE, OE	7	pF
C _{OUT}	Data Input/Output	7	pF

*Note: Capacitance is sampled and not 100% tested

Electrical Specifications

- CAS means UCAS and LCAS.
- All voltages are referenced to GND.
- After power up, wait more than 100µs and then, execute eight CAS-before-RAS or RAS-only refresh cycles as dummy cycles to initialize internal circuit.

Block Diagram :



Truth Table: GLT4161L16

Function		$\overline{\text{RAS}}$	$\overline{\text{LCAS}}$	$\overline{\text{UCAS}}$	$\overline{\text{WE}}$	$\overline{\text{OE}}$	ADDRESS	DQs	Notes
Standby		H	H→X	H→X	X	X		High-Z	
Read: Word		L	L	L	H	L	ROW/COL	Data Out	
Read: Lower Byte		L	L	H	H	L	ROW/COL	Lower Byte,Data-Out Upper Byte,High-Z	
Read: Upper Byte		L	H	L	H	L	ROW/COL	Lower Byte,High-Z Upper Byte,Data-Out	
Write: Word(Early Write)		L	L	L	L	X	ROW/COL	Data-In	
Write: Lower Byte (Early)		L	L	H	L	X	ROW/COL	Lower Byte,Data-In Upper Byte,High-Z	
Write: Upper Byte (Early)		L	H	L	L	X	ROW/COL	Lower Byte,High-Z Upper Byte,Data-In	
Read Write		L	L	L	H→L	L→H	ROW/COL	Data-Out,Data-In	1,2
Fast-Page- Mode Read	1st Cycle	L	H→L	H→L	H	L	ROW/COL	Data-Out	1
	2nd Cycle	L	H→L	H→L	H	L	COL	Data-Out	1
Fast-Page- Mode Write	1st Cycle	L	H→L	H→L	L	X	ROW/COL	Data-In	2
	2nd Cycle	L	H→L	H→L	L	X	COL	Data-In	2
Fast-Page- Mode Read- Write	1st Cycle	L	H→L	H→L	H→L	L→H	ROW/COL	Data-Out,Data-In	1,2
	2nd Cycle	L	H→L	H→L	H→L	L→H	COL	Data-Out,Data-In	1,2
Hidden Refresh	Read	L→H→L	L	L	H	L	ROW/COL	Data-Out	1
	Write	L→H→L	L	L	L	X	ROW/COL	Data-In	2,3
$\overline{\text{RAS}}$ -Only Refresh		L	H	H	X	X	ROW	High-Z	
CBR Refresh		H→L	L	L	X	X		High-Z	4

Notes:

1. These READ cycles may also be BYTE READ cycles (either $\overline{\text{UCAS}}$ or $\overline{\text{LCAS}}$ active).
2. These WRITE cycles may also be BYTE WRITE cycles (either $\overline{\text{UCAS}}$ or $\overline{\text{LCAS}}$ active).
3. EARLY WRITE only.
4. At least one of the two $\overline{\text{CAS}}$ signals must be active ($\overline{\text{UCAS}}$ or $\overline{\text{LCAS}}$).

DC and Operating Characteristics (1-2)
 $T_A = 0^\circ\text{C to } 70^\circ\text{C}$, $V_{CC} = 3.3\text{V} \pm 0.3\text{V}$, $V_{SS} = 0\text{V}$, unless otherwise specified.

Sym.	Parameter	Test Conditions	Access Time	Min.	Typ	Max.	Unit	Notes
I_{LI}	Input Leakage Current (any input pin)	$0\text{V} \leq V_{IN} \leq V_{CC} + 0.3\text{V}$ (All other pins not under test = 0V)		-5		+5	μA	
I_{LO}	Output Leakage Current (for High-Z State)	$0\text{V} \leq V_{out} \leq V_{CC}$ Output is disabled (Hiz)		-5		+5	μA	
I_{CC1}	Operating Current, Random READ/WRITE	$t_{RC} = t_{RC}(\text{min.})$	$t_{RAC} = 40\text{ns}$ $t_{RAC} = 45\text{ns}$ $t_{RAC} = 50\text{ns}$ $t_{RAC} = 70\text{ns}$			160 150 140 130	mA	1,2
I_{CC2}	Standby Current,(TTL)	$\overline{\text{RAS}}, \overline{\text{UCAS}}, \overline{\text{LCAS}}$ at V_{IH} other inputs $\geq V_{SS}$				1	mA	
I_{CC3}	Refresh Current, RAS-Only	$\overline{\text{RAS}}$ cycling, $\overline{\text{UCAS}}, \overline{\text{LCAS}}$ at V_{IH} $t_{RC} = t_{RC}(\text{min.})$	$t_{RAC} = 40\text{ns}$ $t_{RAC} = 45\text{ns}$ $t_{RAC} = 50\text{ns}$ $t_{RAC} = 70\text{ns}$			160 150 140 130	mA	2
I_{CC4}	Operating Current, FAST Page Mode	$\overline{\text{RAS}}$ at V_{IL} , $\overline{\text{UCAS}}, \overline{\text{LCAS}}$ address cycling: $t_{PC} = t_{PC}(\text{min.})$	$t_{RAC} = 40\text{ns}$ $t_{RAC} = 45\text{ns}$ $t_{RAC} = 50\text{ns}$ $t_{RAC} = 70\text{ns}$			160 150 140 130	mA	1,2
I_{CC5}	Refresh Current, CAS Before RAS	$\overline{\text{RAS}}, \overline{\text{UCAS}}, \overline{\text{LCAS}}$ address cycling: $t_{RC} = t_{RC}(\text{min.})$	$t_{RAC} = 40\text{ns}$ $t_{RAC} = 45\text{ns}$ $t_{RAC} = 50\text{ns}$ $t_{RAC} = 70\text{ns}$			160 150 140 130	mA	1
I_{CC6}	Standby Current, (CMOS)	$\overline{\text{RAS}} \geq V_{CC} - 0.2\text{V}$, $\overline{\text{UCAS}} \geq V_{CC} - 0.2\text{V}$, $\overline{\text{LCAS}} \geq V_{CC} - 0.2\text{V}$, All other inputs V_{SS}				300	μA	1,5
I_{CC7}	Self Refresh Current	$\overline{\text{RAS}} = \overline{\text{UCAS}} = \overline{\text{LCAS}} = V_{IL}$ $\overline{\text{WE}} = \overline{\text{OE}} = A_0 \sim A_9 = V_{CC} - 0.2\text{V}$ or 0.2V $DQ_0 \sim DQ_{15} = V_{CC} - 0.2\text{V}, 0.2\text{V}$ or Open				300	μA	
V_{IL}	Input Low Voltage			-0.3		+0.8	V	3
V_{IH}	Input High Voltage			2.0		$V_{CC} + 0.3$	V	4
V_{OL}	Output Low Voltage	$I_{OL} = 2\text{mA}$				0.4	V	
V_{OH}	Output High Voltage	$I_{OH} = -2\text{mA}$		2.4			V	

Notes:

- I_{CC} is dependent on output loading when the device output is selected. Specified $I_{CC}(\text{max.})$ is measured with the output open.
- I_{CC} is dependent upon the number of address transitions specified $I_{CC}(\text{max.})$ is measured with a maximum of one transition per address cycle in random Read/Write and Fast Page Mode.
- Specified $V_{IL}(\text{min.})$ is steady state operation. During transitions $V_{IL}(\text{min.})$ may undershoot to -1.0V for a period not to exceed 15ns. All AC parameters are measured with $V_{IL}(\text{min.}) \geq V_{SS}$ and $V_{IH}(\text{max.}) \leq V_{CC}$.
- Specified $V_{IH}(\text{max.})$ is steady state operation. During transitions $V_{IH}(\text{max.})$ may undershoot to $+1.0\text{V}$ for a period not to exceed 15ns. All AC parameters are measured with $V_{IL}(\text{min.}) \geq V_{SS}$ and $V_{IH}(\text{max.}) \leq V_{CC}$.
- S-Veraion

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AC Characteristics
 $T_A = 0^\circ\text{C to } 70^\circ\text{C}$, $V_{CC} = 3.3\text{V} \pm 0.3\text{V}$, $V_{IH} / V_{IL} = 3.0/0\text{ V}$, $V_{OH}/V_{OL} = 2.0/0.8\text{V}$

 An initial pause of 100 μs and 8 CAS-before-RAS or RAS-only refresh cycles are required after power-up.

Parameter	Symbol	40		45		50		70		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
Read or Write Cycle Time	t_{RC}	75		80		90		124		ns	
Read Modify Write Cycle Time	t_{RWC}	110		110		130		170		ns	
RAS Precharge Time	t_{RP}	25		25		30		50		ns	
RAS Pulse Width	t_{RAS}	40	100K	45	100k	50	100K	70	10k	ns	
Access Time from RAS	t_{RAC}		40		45		50		70	ns	3, 4
Access Time from CAS	t_{CAC}		12		12		15		20	ns	3, 4
Access Time from Column Address	t_{AA}		20		22		25		35	ns	3, 4
CAS to Output Low-Z	t_{CLZ}	0		0		0		3		ns	3
RAS Hold Time	t_{RSH}	12		13		15		20		ns	
CAS Hold Time	t_{CSH}	40		46		50		50		ns	
CAS Pulse Width	t_{CAS}	12	10k	13	10k	15	10k	15	10k	ns	
RAS to CAS Delay Time	t_{RCD}	17	28	18	33	19	36	20	50	ns	
RAS to Column Address Delay Time	t_{RAD}	12	20	13	23	15	26	15	35	ns	7
CAS to RAS Precharge Time	t_{CRP}	5		5		5		5		ns	
Row Address Set-Up Time	t_{ASR}	0		0		0		0		ns	
Row Address Hold Time	t_{RAH}	7		8		9		10		ns	
Column Address Set-Up Time	t_{ASC}	0		0		0		0		ns	
Column Address Hold Time	t_{CAH}	5		6		7		15		ns	
Column Address to RAS Lead Time	t_{RAL}	20		23		25		35		ns	
Column Address Hold Time Referenced to RAS	t_{AR}	30		39		40		50		ns	
Read Command Set-Up Time	t_{RCS}	0		0		0		0		ns	
Read Command Hold Time Referenced to CAS	t_{RCH}	0		0		0		0		ns	4
Read Command Hold Time Referenced to RAS	t_{RRH}	0		0		0		0		ns	4
Write Command Set-Up Time	t_{WCS}	0		0		0		0		ns	8,9
Write Command Hold Time	t_{WCH}	5		6		7		15		ns	
Write Command Pulse Width	t_{WP}	5		6		7		15		ns	
Write Command to RAS Lead Time	t_{RWL}	12		12		15		30		ns	
Write Command to CAS Lead Time	t_{CWL}	12		12		15		15		ns	

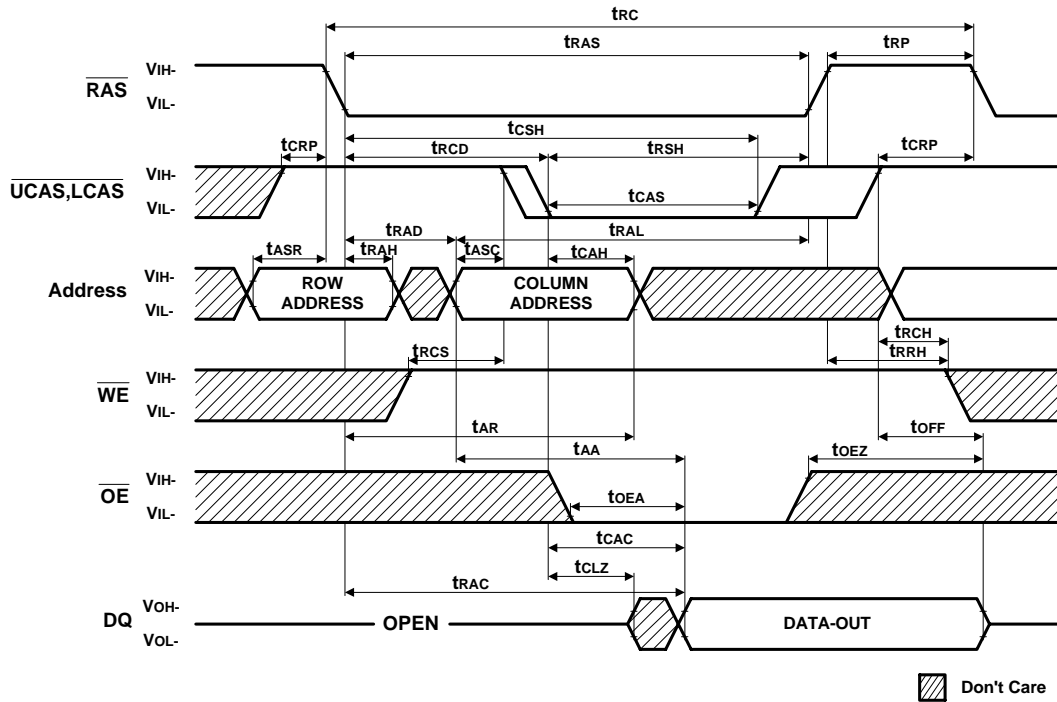
AC Characteristics

Parameter	Symbol	40		45		50		70		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
Data Set-Up Time	t_{DS}	0		0		0		0		ns	
Data Hold Time	t_{DH}	5		7		8		15		ns	
\overline{RAS} to \overline{WE} Delay Time	t_{RWD}	58		68		73		94		ns	
CAS to \overline{WE} Delay Time	t_{CWD}	30		30		31		44		ns	
Column Address to \overline{WE} Delay Time	t_{AWD}	38		40		43		59		ns	
\overline{RAS} to CAS Precharge Time	t_{RPC}	5		5		5		0		ns	
Access Time from CAS Precharge	t_{CPA}		22		25		27		40	ns	
EDO Page Mode Cycle Time	t_{PC}	23		25		28		30		ns	
EDO Page Mode Read-Modify-Write Cycle Time	t_{PRWC}	60		65		70		75		ns	
CAS Precharge Time (EDO Page Mode)	t_{CP}	5		7		7		10		ns	
RAS Pulse Width (EDO Page Mode Only)	t_{RASP}	40	100k	45	100k	50	100k	70	100k	ns	
Access Time from OE	t_{OEA}		12		12		15		20	ns	
OE to Data Delay Time	t_{OED}	6		8		8		20		ns	
OE to Output High-Z	t_{OEZ}	3	6	3	8	3	8	3	20	ns	
OE Command Hold Time	t_{OEH}	8		8		8		20		ns	
CAS Set-Up Time for CAS-before-RAS Cycle	t_{CSR}	5		5		5		5		ns	
CAS Hold Time for CAS-before-RAS Cycle	t_{CHR}	10		10		10		15		ns	
Transition Time	t_T	3	50	3	50	3	50	2	50	ns	
Refresh Period	t_{REF}		16		16		16		16	ms	
\overline{RAS} pulse width (\overline{CAS} -before- \overline{RAS} Self refresh)	t_{RASS}	100		100		100		100		μ s	
\overline{RAS} precharge time (\overline{CAS} -before- \overline{RAS} Self refresh)	t_{RPS}	90		95		100		130		ns	
\overline{CAS} precharge time (\overline{CAS} -before- \overline{RAS} Self refresh)	t_{CHS}	-50		-50		-50		-50		ns	

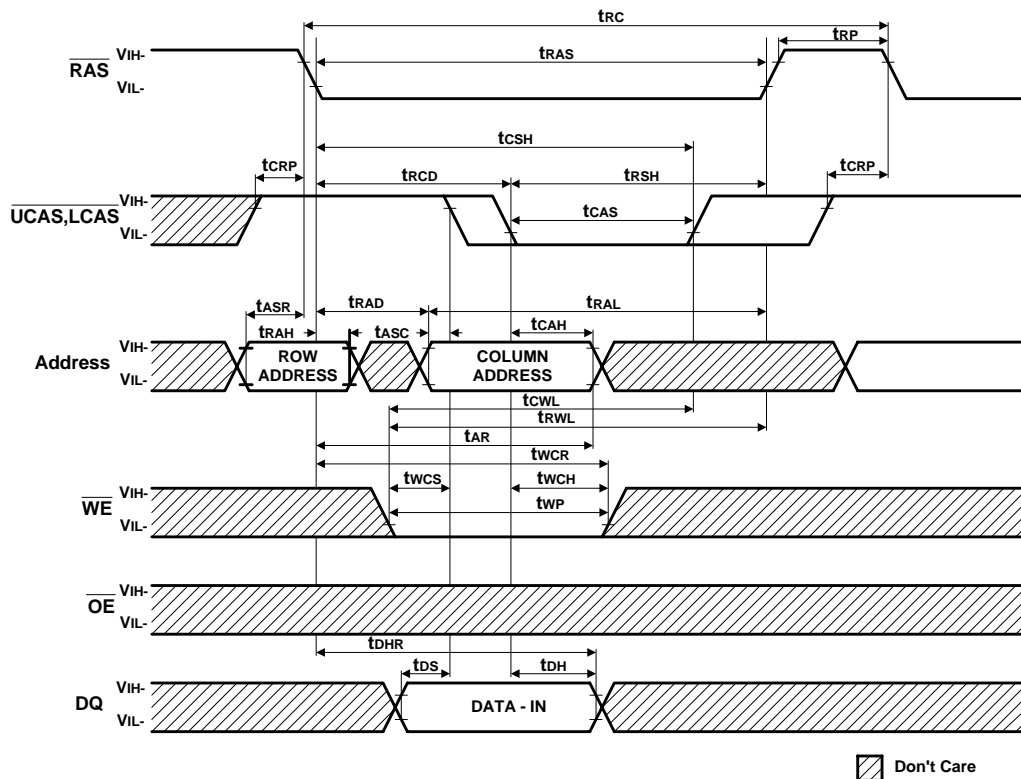
Notes:

1. Measure with a load equivalent to one TTL inputs and 50 pF.
2. Assumes that $t_{RCD} \leq t_{RCD}(\text{max.})$. If t_{RCD} is greater than $t_{RCD}(\text{max.})$, access time will be t_{AA} dominant.
3. Assumes that $t_{RAD} \leq t_{RAD}(\text{max.})$. If t_{RAD} is greater than $t_{RCD}(\text{max.})$, access time will be controlled by t_{CAC} .
4. Either t_{RRH} or t_{RCH} must be satisfied for a Read Cycle.
5. Access time is determined by the longest of t_{CAA} , t_{CAC} and t_{CPA} .
6. Assumes that $t_{RAD} \geq t_{RAD}(\text{max.})$.
7. Operation within the $t_{RAD}(\text{max.})$ limit ensures that $t_{RAC}(\text{max.})$ can be met. $t_{RAD}(\text{max.})$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD}(\text{max.})$ limit, the access time is controlled by t_{CAA} and t_{CAC} .
8. t_{WCS} , t_{RWD} , t_{AWD} and t_{CWD} are not restrictive operating parameters.
9. $t_{WCS}(\text{min.})$ must be satisfied in an Early Write Cycle.
10. t_{DS} and t_{DH} are referenced to the latter occurrence of $\overline{\text{CAS}}$ of $\overline{\text{WE}}$.
11. t_T is measured between $V_{IH}(\text{min.})$ and $V_{IL}(\text{max.})$. AC-measurements assume $t_T = 1.5 \text{ ns}$.

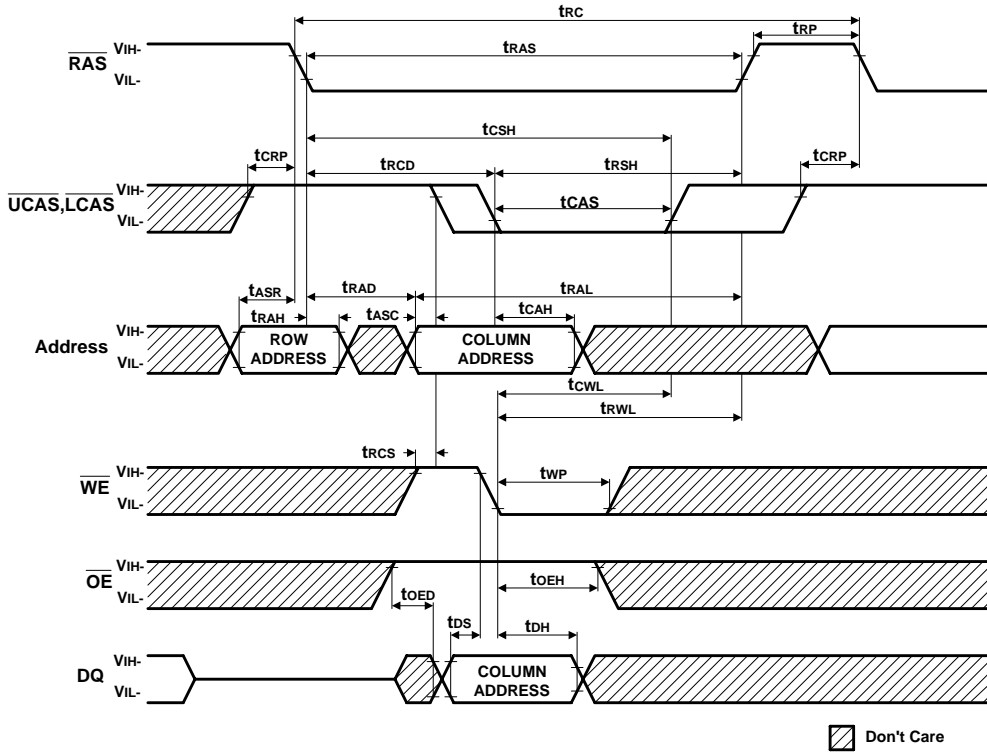
Read CYCLE



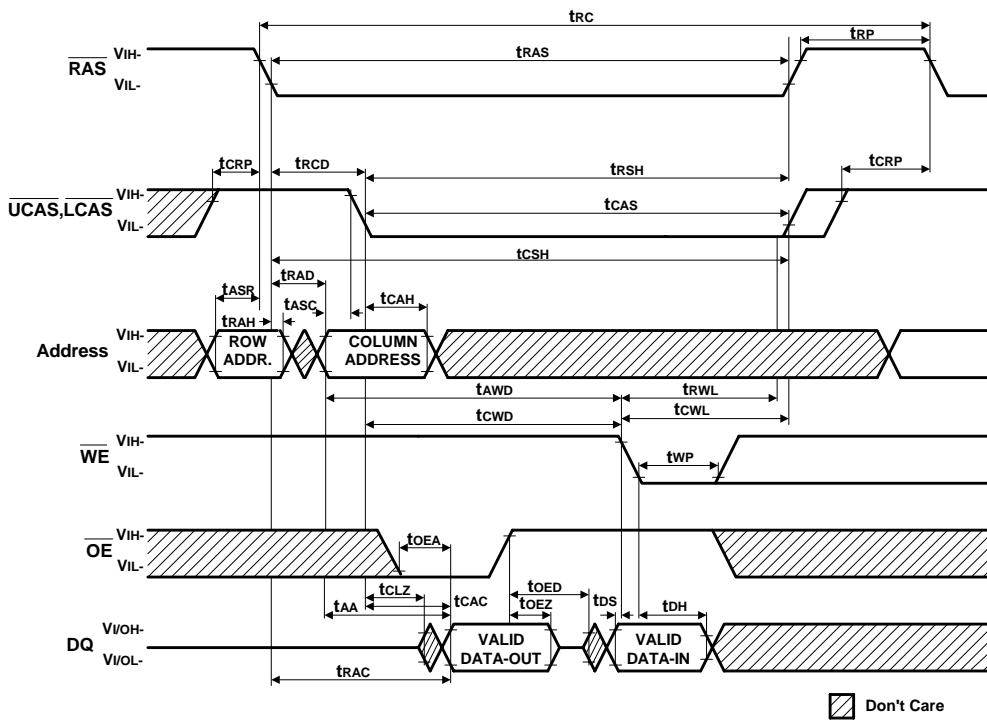
Early Write Cycle NOTE : D_{OUT} = OPEN



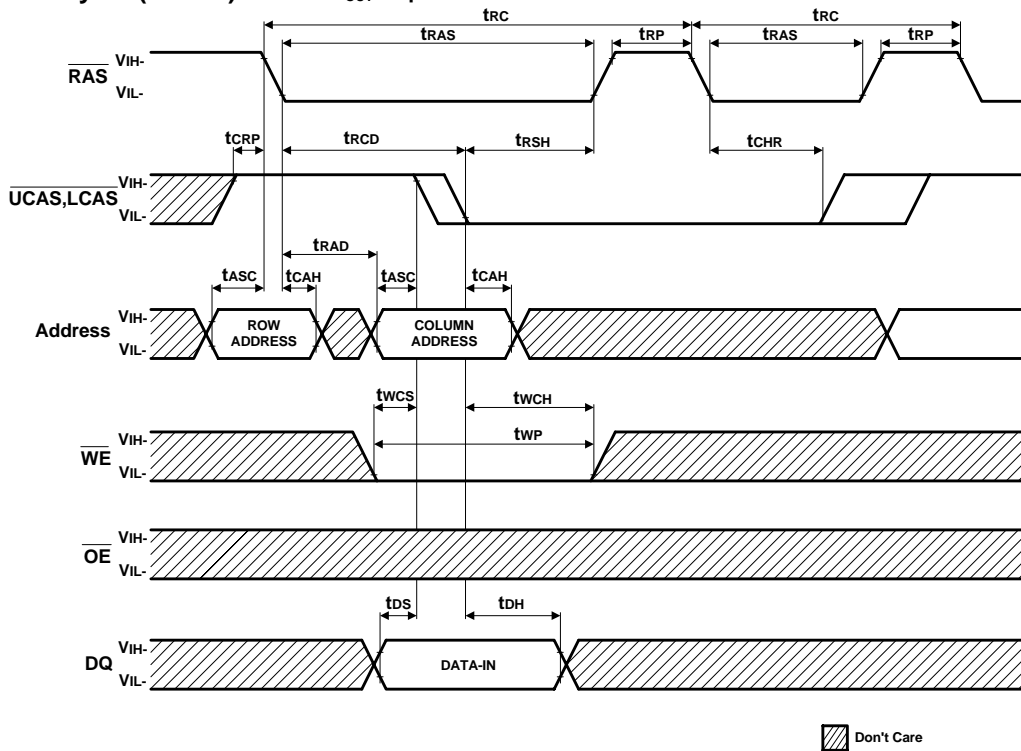
OE Controlled Write Cycle NOTE : D_{OUT} = OPEN



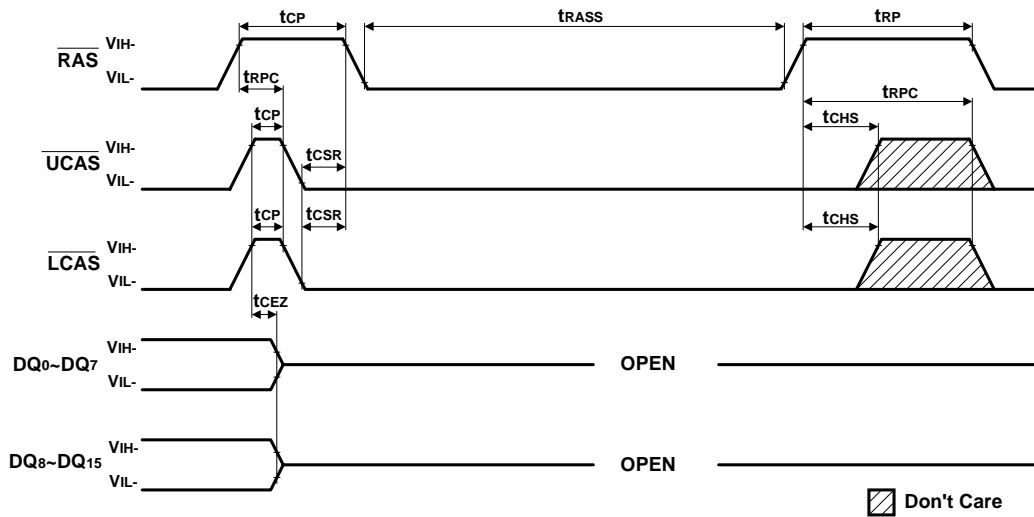
Read - Modify - Write Cycle



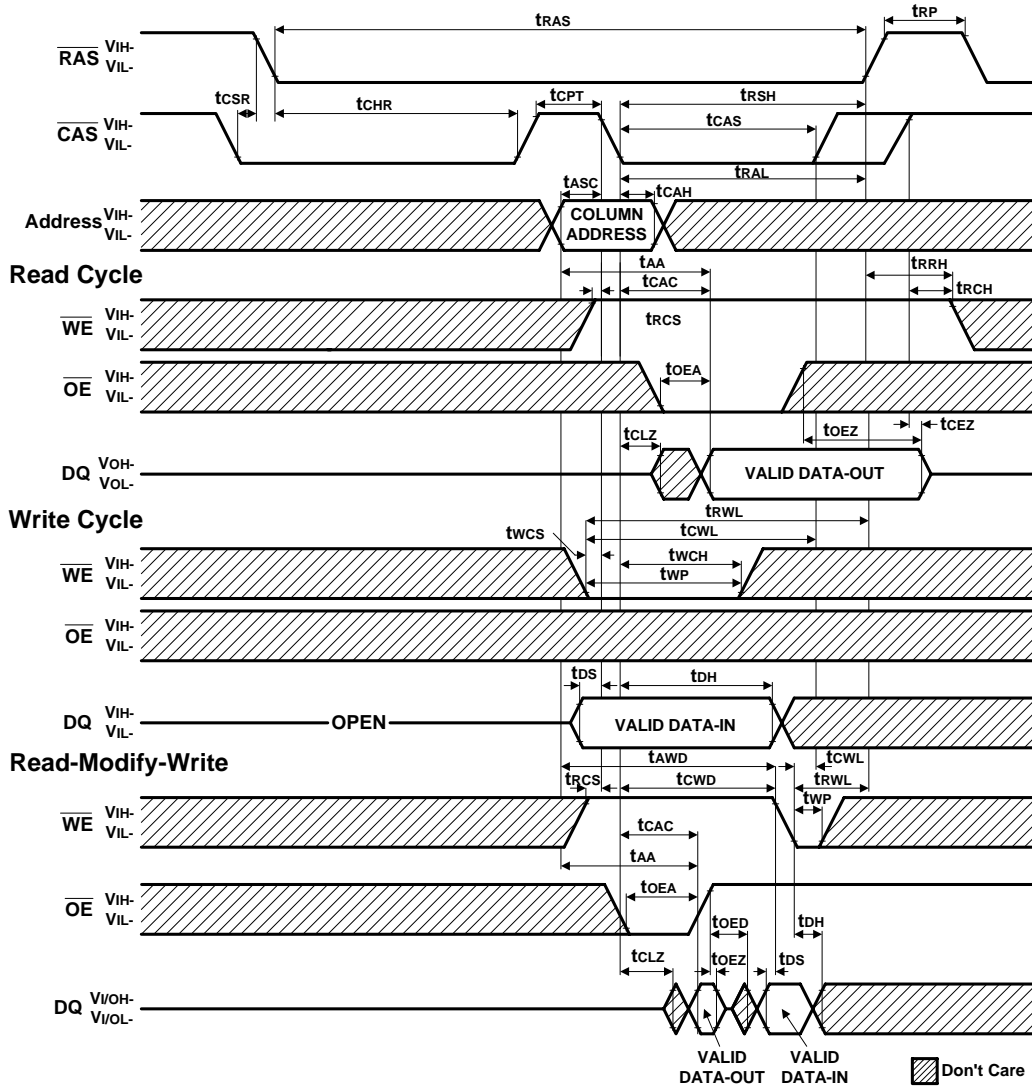
Hidden Refresh Cycle (Write) NOTE : D_{OUT} =Open



CAS - Before - RAS Self Refresh Cycle

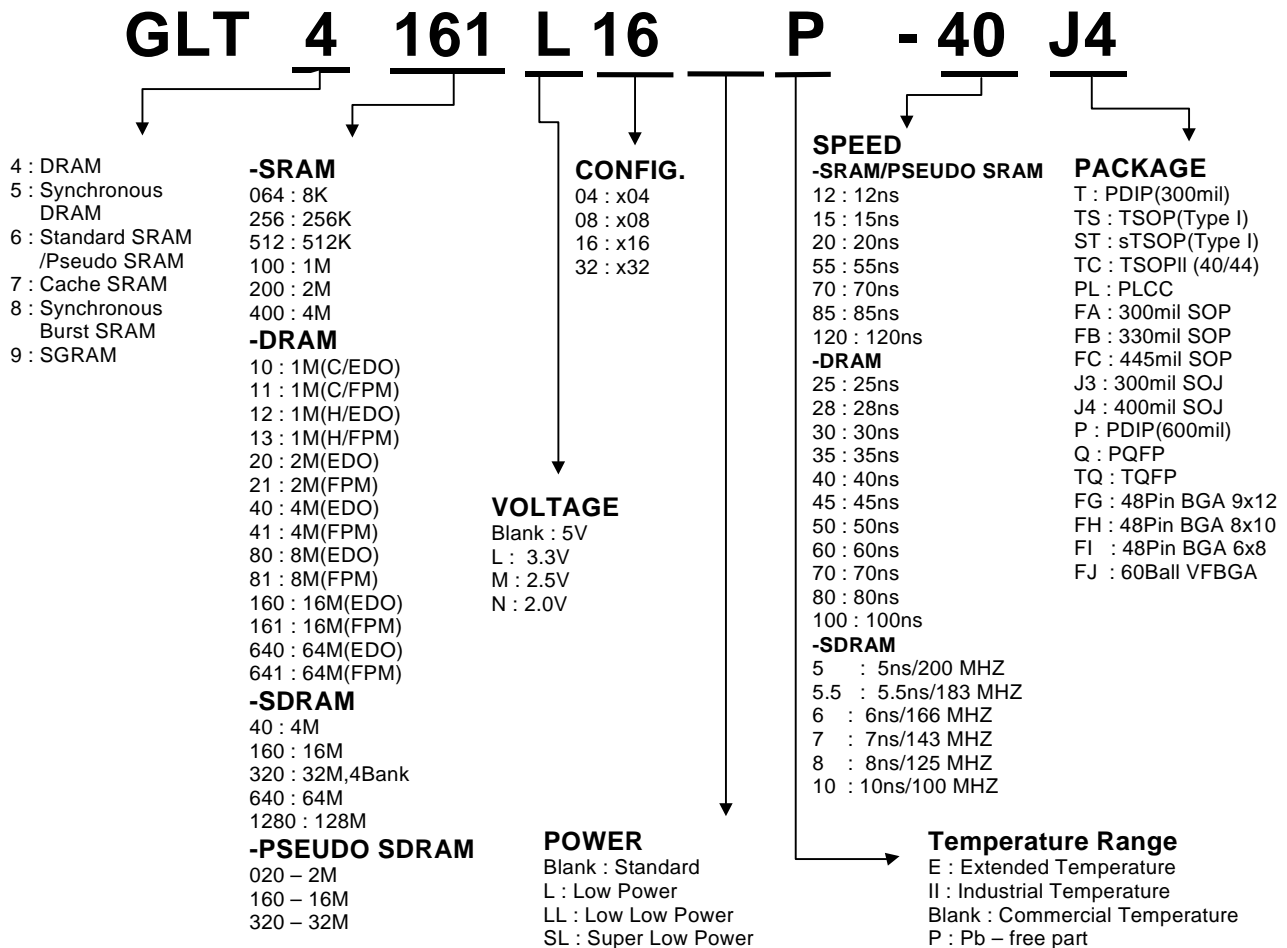


CAS - Before RAS Refresh Counter Test Cycle

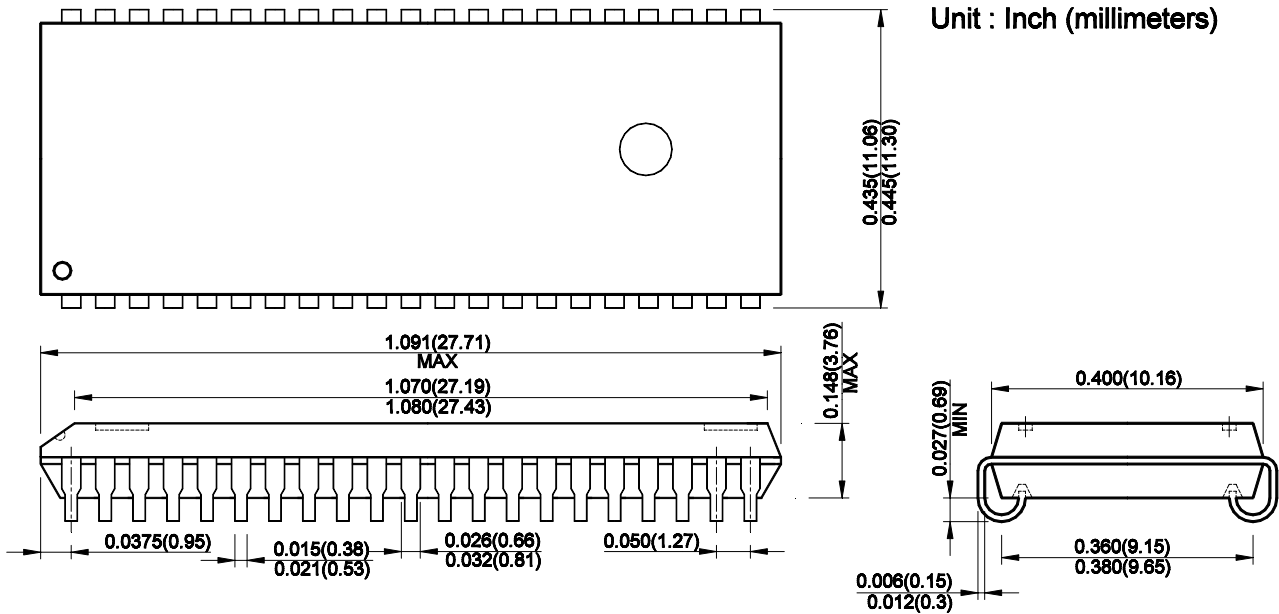


Ordering Information

Part Number	SPEED	POWER	FEATURE	PACKAGE
GLT4161L16-40J4	40ns	Normal	FPM	42L 400mil SOJ
GLT4161L16-45J4	45ns	Normal	FPM	42L 400mil SOJ
GLT4161L16-50J4	50ns	Normal	FPM	42L 400mil SOJ
GLT4161L16-70J4	70ns	Normal	FPM	42L 400mil SOJ
GLT4161L16-40TC	40ns	Normal	FPM	44/50L 400mil TSOPII
GLT4161L16-45TC	45ns	Normal	FPM	44/50L 400mil TSOPII
GLT4161L16-50TC	50ns	Normal	FPM	44/50L 400mil TSOPII
GLT4161L16-70TC	70ns	Normal	FPM	44/50L 400mil TSOPII

Parts Numbers (Top Mark) Definition :


Package Information
40/42L 400MIL SOJ



44/50L TSOPII 400MIL

