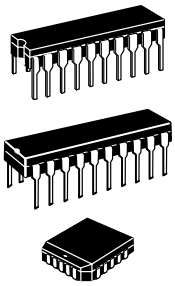
Quad TTL/NMOS to PECL* Translator

MC10H351



L SUFFIX
CERAMIC PACKAGE
CASE 732–03

P SUFFIX
PLASTIC PACKAGE
CASE 738–03

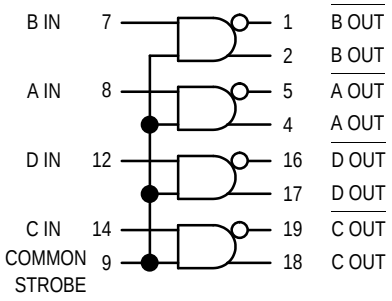
FN SUFFIX
PLCC
CASE 775–02

The MC10H351 is a quad translator for interfacing data between a saturated logic section and the PECL section of digital systems when only a +5.0 Vdc power supply is available. The MC10H351 has TTL/NMOS compatible inputs and PECL complementary open–emitter outputs that allow use as an inverting/non–inverting translator or as a differential line driver. When the common strobe input is at a low logic level, it forces all true outputs to the PECL low logic state (≈ +3.2 V) and all inverting outputs to the PECL high logic state (≈ +4.1 V).

The MC10H351 can also be used with the MC10H350 to transmit and receive TTL/NMOS information differentially via balanced twisted pair lines.

- Single +5.0 Power Supply
- All V_{CC} Pins Isolated On Chip
- Differentially Drive Balanced Lines
- t_{pd} = 1.3 nsec Typical

LOGIC DIAGRAM



V_{CC} (+5.0 VDC) = PINS 6, 11, 15, 20
GND = PIN 10

MAXIMUM RATINGS

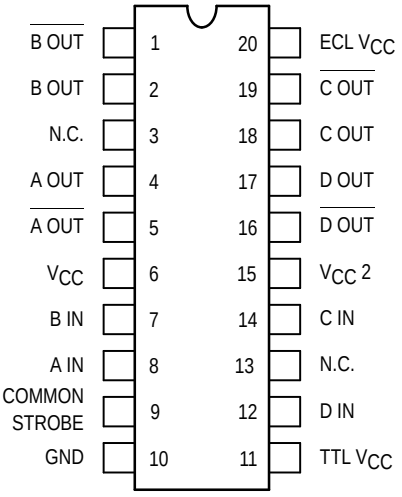
Characteristic	Symbol	Rating	Unit
Power Supply	V_{CC}	0 to +7.0	Vdc
Input Voltage (V_{CC} = 5.0 V)	V_I	0 to V_{CC}	Vdc
Output Current — Continuous — Surge	I_{out}	50 100	mA
Operating Temperature Range	T_A	0 to +75	°C
Storage Temperature Range — Plastic — Ceramic	T_{stg}	–55 to +150 –55 to +165	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = V_{CC1} = V_{CC2} = 5.0 V ± 5.0%)

Characteristic	Symbol	0° Min	0° Max	25° Min	25° Max	75° Min	75° Max	Unit
Power Supply Current	ECL	—	50	—	45	—	50	mA
	TTL	—	20	—	15	—	20	mA
Reverse Current Pins 7, 8, 12, 14 Pin 9	 I_R I_{INH}	 — —	 25 100	 — —	 20 80	 — —	 25 100	µA
Forward Current Pins 7, 8, 12, 14 Pin 9	 I_F I_{INL}	 — —	 –0.8 –3.2	 — —	 –0.6 –2.4	 — —	 –0.8 –3.2	mA
Input Breakdown Voltage	$V_{(BR)in}$	5.5	—	5.5	—	5.5	—	Vdc
Input Clamp Voltage (I_{in} = –18 mA)	V_I	—	–1.5	—	–1.5	—	–1.5	Vdc
High Output Voltage (1)	V_{OH}	3.98	4.16	4.02	4.19	4.08	4.27	Vdc
Low Output Voltage (1)	V_{OL}	3.05	3.37	3.05	3.37	3.05	3.37	Vdc
High Input Voltage	V_{IH}	2.0	—	2.0	—	2.0	—	Vdc
Low Input Voltage	V_{IL}	—	0.8	—	0.8	—	0.8	Vdc

(1) With V_{CC} at 5.0 V. V_{OH}/V_{OL} change 1:1 with V_{CC}.
*Positive Emitter Coupled Logic

DIP PIN ASSIGNMENT



Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 6–36 of the Motorola MECL Data Book (DL122/D).

AC PARAMETERS

Characteristic	Symbol	0°		25°		75°		Unit
		Min	Max	Min	Max	Min	Max	
Propagation Delay (1)	t_{pd}	0.4	2.2	0.4	2.2	0.4	2.1	ns
Rise Time (20% to 80%)	t_r	0.4	1.9	0.4	2.0	0.4	2.1	ns
Fall Time (80% to 20%)	t_f	0.4	1.9	0.4	2.0	0.4	2.1	ns
Maximum Operating Frequency	f_{max}	150	—	150	—	150	—	MHz

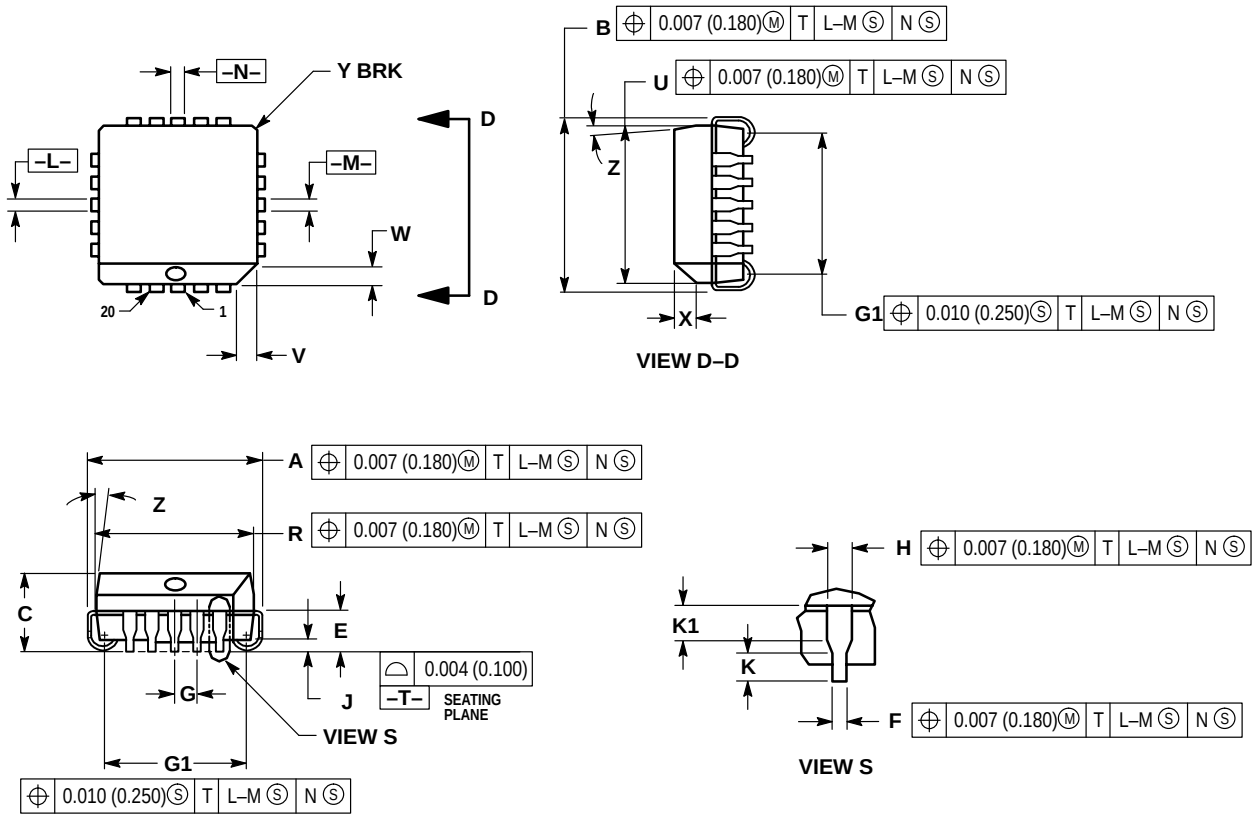
(1) Propagation delay is measured on this circuit from +1.5 volts on the input waveform to the 50% point on the output waveform.

NOTE:

Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Outputs are terminated through a 50–ohm resistor to V_{CC} –2.0 Vdc.

OUTLINE DIMENSIONS

FN SUFFIX
PLASTIC PLCC PACKAGE
CASE 775–02
ISSUE C

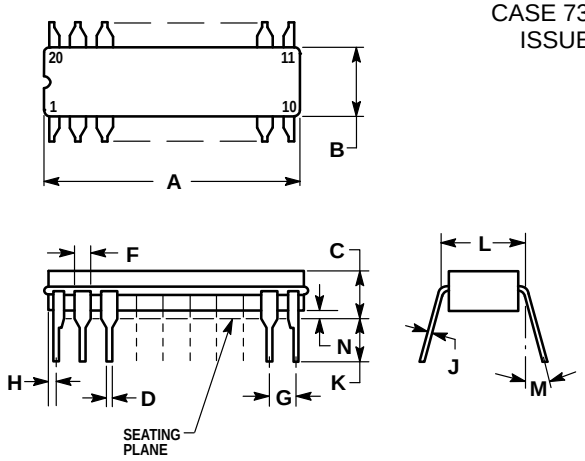


NOTES:
1. DATUMS –L–, –M–, AND –N– DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
2. DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM –T–, SEATING PLANE.
3. DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.
6. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
7. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.385	0.395	9.78	10.03
B	0.385	0.395	9.78	10.03
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	—	0.51	—
K	0.025	—	0.64	—
R	0.350	0.356	8.89	9.04
U	0.350	0.356	8.89	9.04
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	—	0.020	—	0.50
Z	2 °	10 °	2 °	10 °
G1	0.310	0.330	7.88	8.38
K1	0.040	—	1.02	—

OUTLINE DIMENSIONS

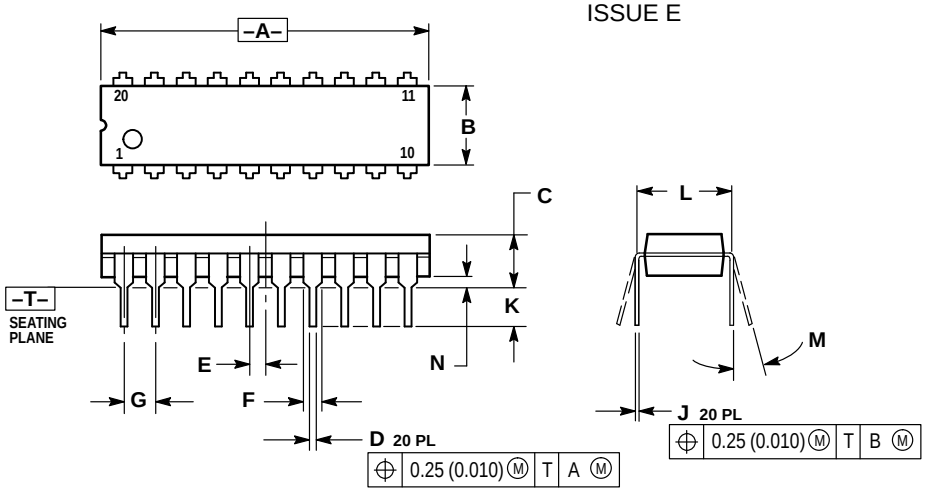
L SUFFIX
CERAMIC DIP PACKAGE
CASE 732–03
ISSUE E



NOTES:
1. LEADS WITHIN 0.010 DIAMETER, TRUE POSITION AT SEATING PLANE, AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSIONS A AND B INCLUDE MENISCUS.

	INCHES	
DIM	MIN	MAX
A	0.940	0.990
B	0.260	0.295
C	0.150	0.200
D	0.015	0.022
F	0.055	0.065
G	0.100 BSC	
H	0.020	0.050
J	0.008	0.012
K	0.125	0.160
L	0.300 BSC	
M	0°	15°
N	0.010	0.040

P SUFFIX
PLASTIC DIP PACKAGE
CASE 738–03
ISSUE E



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.010	1.070	25.66	27.17
B	0.240	0.260	6.10	6.60
C	0.150	0.180	3.81	4.57
D	0.015	0.022	0.39	0.55
E	0.050 BSC		1.27 BSC	
F	0.050	0.070	1.27	1.77
G	0.100 BSC		2.54 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.140	2.80	3.55
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

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Associated Documents

Item	Short Desc
Application Notes	H124, 125, 350-352 Translator I/O SPICE Modelling Kit
Application Notes	The ECL Translator Guide
Data Sheet	Quad TTL/NMOS to PECL* Translator

Device MC10H351

TTL, NMOS To ECL Translator

The MC10H351 is a quad translator for interfacing data be logic section and the PECL section of digital systems wher power supply is available. The MC10H351 has TTL/NMOS PECL complementary open-emitter outputs that allow use inverting/non-inverting translator or as a differential line dri common strobe input is at a low logic level, it forces all true low logic state (+3.2 V) and all inverting outputs to the PE +4.1 V).

The MC10H351 can also be used with the MC10H350 to tr TTL/NMOS information differentially via balanced twisted p

Features:

- Single +5.0 Power Supply
- All V_{CC} Pins Isolated On Chip
- Differentially Drive Balanced Lines
- t_{pd} = 1.3 nsec Typical

Orderable Parts

Action	Orderable Part	Short Desc.	Package Desc.	Pin Count	Case Outline	S
N/A	MC10H351FN	TTL, NMOS TO ECL Translator	PLCC	20	775-02	A
N/A	MC10H351FNR2	Tape and Reel	PLCC	20	775-02	A
N/A	MC10H351L	TTL, NMOS TO ECL Translator	CDIP		732-03	A
N/A	MC10H351M	TTL, NMOS TO ECL Translator	N/A	N/A	N/A	A
N/A	MC10H351MEL	Tape and Reel	N/A	N/A	N/A	A
N/A	MC10H351ML1	Tape and Reel	N/A	N/A	N/A	L
N/A	MC10H351MR1	Tape and Reel	N/A	N/A	N/A	L
N/A	MC10H351P	TTL, NMOS TO ECL Translator	PDIP	20	738-03	A