HEWLETT PACKARD

SC Duplex Single Mode Transceiver

Technical Data

HFCT-5103

Features

- **SC Duplex Single Mode Transceiver**
- **Singe + 5 V Power Supply**
- **Multisourced 1 x 9 Pin Configuration**
- **Aqueous Washable Plastic Package**
- **Interchangeable with HFBR-5103 and Other LED Multisourced 1 x 9 Transceivers**
- **Unconditionally Eyesafe Laser IEC 825/CDRH Class 1 Compliant**
- **Conforms to ANSI X3.184-1993 Standard for FDDI SMF-PMD Category 1 Optoelectronic Performance**
- **Compatible with the HFCT-5205**

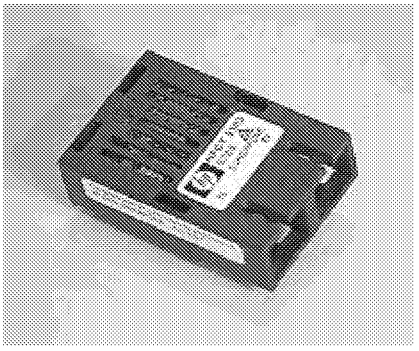
Applications

- **FDDI SMF-PMD1**
- **Fast Ethernet**
- **ATM Compatible**

Description

The HFCT-5103 transceiver is a high performance, cost effective module for serial optical data communications applications specified for a signal rate of 125 Mbd. It is designed to provide an FDDI SMF-PMD1 link. for FDDI or Fast Ethernet applications and is also compatible with ATM/ SONET/SDH transceivers.

This module is designed for single mode fiber and operates at a nominal wavelength of 1300 nm. It incorporates Hewlett-Packard's high performance, reliable, long wavelength optical devices and proven circuit technology to give long life and consistent service.

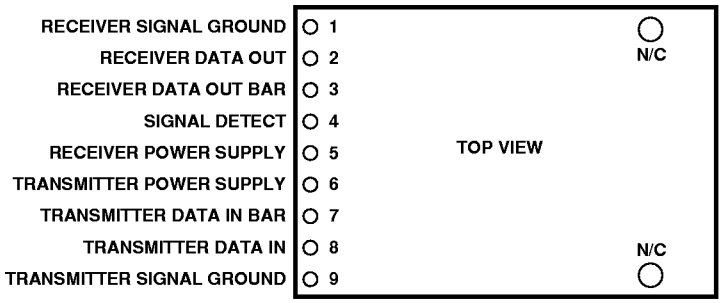


The transmitter section uses an advanced Fabry - Perot laser with full IEC 825 and CDRH Class I eye safety.

The receiver section uses an MOVPE grown planar PIN photodetector for low dark current and excellent responsivity.

A pseudo-ECL logic interface simplifies interface to external circuitry.

Connection Diagram



Pin Descriptions

Pin 1 Receiver Signal Ground V_{EE}:
Directly connect this pin to the receiver ground plane.

Pin 2 Receiver Data Out RD+ :
Terminate this high-speed, differential, PECL output with standard PECL techniques.

Pin 3 Receiver Data Out Bar RD–:
Terminate this high-speed, differential, PECL output with standard PECL techniques.

Pin 4 Signal Detect SD:
Normal optical input levels to the receiver result in a logic "1" output.

Low optical input levels to the receiver result in a fault condition indicated by a logic "0" output.

This Signal Detect output can be used to drive a PECL input on an upstream circuit, such as Signal Detect input or Loss of Signal-bar.

Pin 5 Receiver Power Supply V_{CC}:
Provide +5 V dc via the recommended transmitter power supply filter circuit. Locate the power supply filter circuit as close as possible to the V_{CC} pin.

Pin 6 Transmitter Power Supply V_{CC}:
Provide +5 V dc via the recommended transmitter power supply filter circuit. Locate the power supply filter circuit as close as possible to the V_{CC} pin.

Pin 7 Transmitter Data In Bar TD–:
Terminate this high-speed, differential Transmitter Data Input with standard PECL techniques.

Pin 8 Transmitter Data In TD+ :
Terminate this high-speed, differential Transmitter Data Input with standard PECL techniques.

Pin 9 Transmitter Signal Ground V_{EE}:
Directly connect this pin to the transmitter ground plane.

Mounting Studs
The mounting studs are provided for mechanical attachment to the circuit board. They are embedded in the nonconductive plastic housing and are not tied to the transceiver internal circuit and should be soldered into plated-through holes on the printed circuit board.

Functional Description Receiver Section

Design

The receiver section contains an InGaAs/InP photodetector and a preamplifier within the receptacle, coupled to a postamp/decision circuit on a separate circuit board.

The postamplifier is ac coupled to the preamplifier as illustrated in Figure 1. The coupling capacitor is large enough to pass the FDDI test pattern at 125 Mbd and the SONET/SDH test pattern at 155 Mbd without significant distortion or performance penalty. If a lower signal rate, or a code which has significantly more low frequency content is used, sensitivity, jitter and pulse distortion could be degraded.

Figure 1 also shows a filter network which limits the bandwidth of the preamp output signal. The filter is designed to bandlimit the preamp output noise and thus improve the receiver sensitivity. These components will also reduce the sensitivity of the receiver as the signal bit rate is increased above 155 Mbd.

Noise Immunity

The receiver includes internal circuit components to filter power supply noise. Under some conditions of EMI and power supply noise, external power supply filtering may be necessary. If receiver sensitivity is found to be degraded by power supply noise, the filter network illustrated in Figure 2 may be used to improve performance. The values of the filter components are general recommendations and may be changed to suit a particular system environment. Shielded inductors are recommended.

Terminating the Outputs

The PECL Data outputs of the receiver may be terminated with the standard Thevenin-equivalent 50 ohm to V_{CC} –2 V termination. Other standard PECL terminating techniques may be used.

The two outputs of the receiver should be terminated with identical load circuits to avoid unnecessarily large ac current in V_{CC}. If the outputs are loaded identically, the ac current is largely nulled. The SD output of the receiver is PECL logic and must be loaded if it is to be used. The signal detect circuit is much slower than the data path, so the ac noise generated by an asymmetrical load is negligible. Power consumption may be reduced by using a higher than normal load impedance for the SD output. Transmission line effects are not generally a problem as the switching rate is slow.

The Signal Detect Circuit

The signal detect circuit works by sensing the peak level of the received signal and comparing this level to a reference.

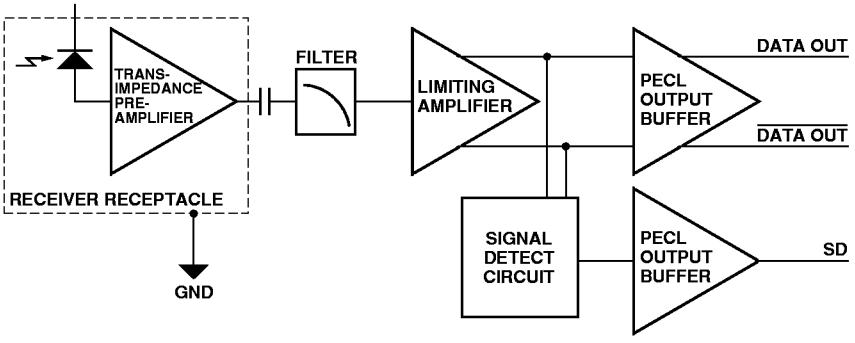


Figure 1. Receiver Block Diagram.

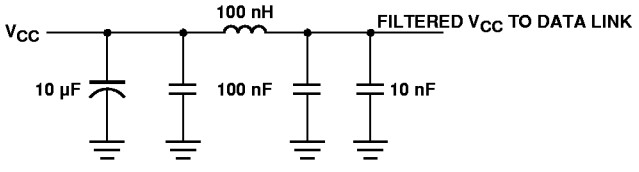


Figure 2. π Filter Network for Noise Filtering.

Functional Description Transmitter Section

Design

This transmitter section uses a buried heterostructure Fabry-Perot laser as its optical source. The package of this laser is designed to allow repeatable coupling into single mode fiber. In addition, this package has been designed to be compliant with IEC 825 Class 1 and CDRH Class I eye safety requirements. The optical output is controlled by a custom IC which detects the laser output via the monitor photodiode. This IC provides both dc and ac current drive to the laser to ensure correct modulation, eye diagram and extinction ratio over temperature, supply voltage and life.

PCB Mounting

The HFCT-5103 has two solderable mounting studs. These studs are not electrically connected. The transceiver is designed for common production processes. It may be wave soldered and aqueous washed providing the process plug is in place.

Each process plug can only be used once during processing, although with subsequent use, it can be used as a dust cover.

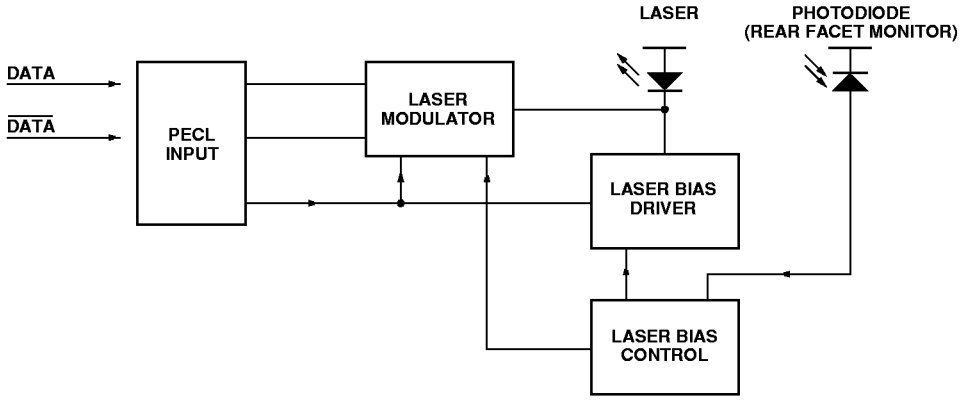


Figure 3. Simplified Transmitter Schematic.

Performance Specifications

Absolute Maximum Ratings

Parameter	Symbol	Minimum	Maximum	Units
Storage Temperature	T_s	–40	+85	°C
Operating Temperature	–	0	+70	°C
Lead Soldering Temperature/Time	–	–	+240/10	°C/s
Output Current (Other Outputs)	I_{out}	0	30	mA
Input Voltage	–	GND	V_{CC}	V
Power Supply Voltage	–	0	+6	V

Operating Environment

Parameter	Symbol	Minimum	Maximum	Units
Power Supply Voltage	V_{CC}	+4.75	+5.25	V
Ambient Operating Temperature	T_{op}	0	+70	°C

Transmitter Section

(Ambient Operating Temperature T_A = 0°C to 70°C, V_{CC} = 4.75 V to 5.25 V)

Parameter	Symbol	Minimum	Maximum	Units	Notes
Output Center Wavelength	λce	1261	1360	nm	–
Output Spectral Width (RMS)	Δλ	–	7.7	nm	–
Average Optical Output Power	P_o	–20	–14	dBm	1
Extinction Ratio	E_r	8.2	–	dB	–
Power Supply Current	I_{cc}	–	140	mA	2
Output Pulse Mask	Compliant with FDDI SMF-PMD1				
Output Eye	Compliant with Bellcore TR-NWT-000253 and ITU Recommendation G957				

Receiver Section

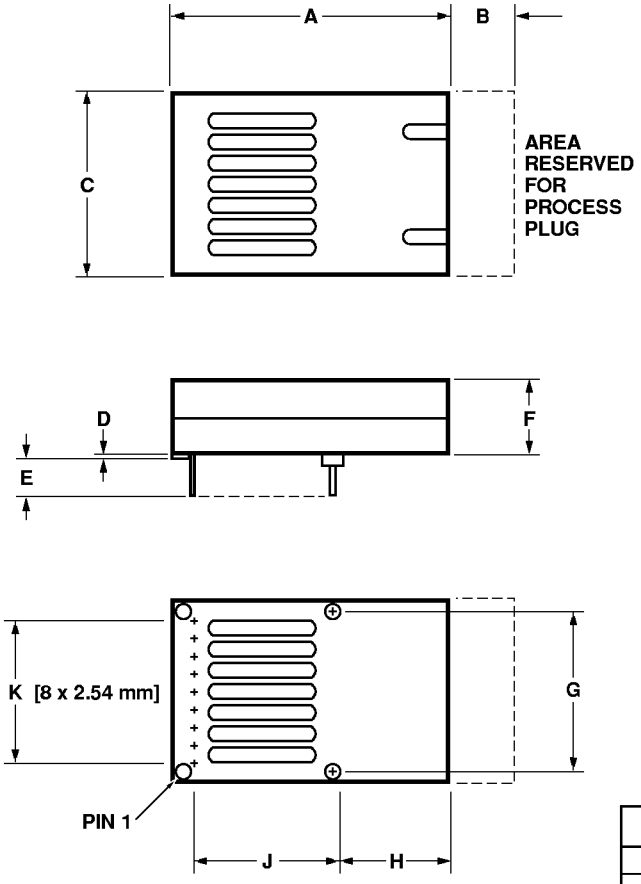
(Ambient Operating Temperature T_A = 0°C to 70°C, V_{CC} = 4.75 V to 5.25 V)

Parameter	Symbol	Minimum	Typical	Maximum	Units	Notes
Receiver Sensitivity	–	–	–	–31	dBm	3
Maximum Input Power	–	–8.0	–	–	dBm	–
Alarm ON	–	–43	–	–31	dBm	–
Hysteresis	–	0.5	–	4.0	dB	–
Power Supply Current	I_{cc}	–	80	100	mA	4
Data Outputs PECL Alarm Output PECL						

Notes:

1. Output power is power coupled into a single mode fiber.
2. The power supply current varies with temperature. Maximum current is specified at V_{CC} = Maximum @ maximum temperature (not including terminations) and end of life.
3. Minimum sensitivity and saturation levels for an FDDI test pattern as defined in FDDI SMF-PMD1 with 4B/5B NRZI encoded data that contains a duty cycle base-line wander effect of 50 kHz and a 2^{23}-1 PRBS with 72 ones and 72 zeros inserted (ITU-T recommendation G958).
4. The current excludes the output load current.

Drawing Dimensions



ELECTRICAL PINS ARE NOMINALLY 0.46/0.018 DIAMETER

MOUNTING POSTS ARE NOMINALLY 1.27/0.050 DIAMETER

DIM.	MIN.	MAX.
A	–	39.16
B	–	12.70
C	–	25.40
D	0.65	0.85
E	2.92	3.68
F	–	10.35
G	–	20.32
H	–	15.93
J	–	20.32
K	AS SHOWN IN DIAGRAM	

ALL DIMENSIONS IN MILLIMETERS

Ordering Information

HFCT-5103 X

- X: Temperature Range/Package color
  - B = 0 to +70°C/Black
  - D = 0 to +70°C/Blue
- HFCT-5103: Model Name: HFCT-5103

Recommended Part Number:
HFCT-5103D

Class I Laser Product: This product conforms to the applicable requirements of 21 CFR 1040 at the date of manufacture.

Date of Manufacture: _____
Hewlett-Packard Ltd., Whitehouse Rd., Ipswich, England

Handling Precautions

1. The HFCT-5103 can be damaged by current surges or overvoltage. Power supply transient precautions should be taken.

2. Normal handling precautions for electrostatic sensitive devices should be taken.

www.hp.com/go/fiber

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