M5M4V16169DTP/RT-7,-8,-10,-15

16MCDRAM:16M(1M-WORD BY 16-BIT) CACHED DRAM WITH 16K (1024-WORD BY 16-BIT) SRAM

Preliminary
This document is a preliminary Target Spec. and some of the contents are subject to change without notice.

DESCRIPTION

1. The M5M4V16169DTP/RT is a 16M-bit Cached DRAM which integrates input registers, a 1,048,576-word by 16-bit dynamic memory array and a 1024- word by 16-bit static RAM array as a Cache memory (block size 8x16) onto a single monolithic circuit. The block data transfer between the DRAM and the data transfer buffers (RB1/RB2/WB1/WB2) is performed in one instruction cycle, a fundamental advantage over a conventional DRAM/SRAM cache.
2. The RAM is fabricated with a high performance CMOS process, and is ideal for large-capacity memory systems where high speed, low power dissipation, and low cost are essential. The use of quadruple-layer polysilicon process combined with silicide and double layer aluminum wiring technology, a single-transistor dynamic storage stacked capacitor cell, and a six-transistor static storage cache cell provide high circuit density at reduced costs.

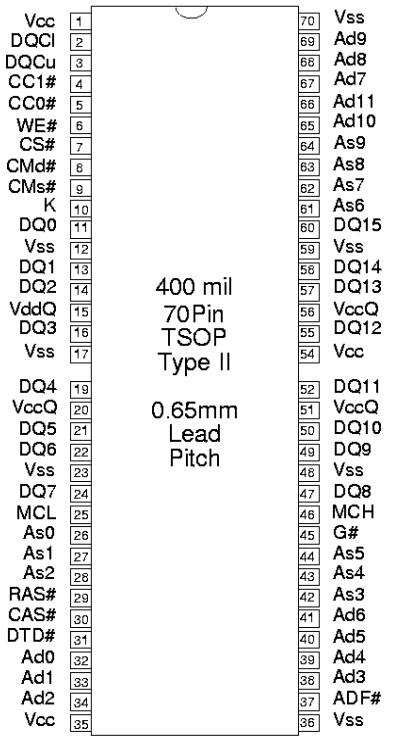
FEATURES

Type name	SRAM Access/cycle	DRAM Access/cycle	Power Dissipation (Typ)
M5M4V16169TP/RT-7	5.6ns/7ns	49ns/70ns	DRAM: 530 SRAM: 860
M5M4V16169TP/RT-8	6.4ns/8ns	56ns/80ns	DRAM: 500 SRAM: 800
M5M4V16169TP/RT-10	8.0ns/10ns	60ns/90ns	DRAM: 430 SRAM: 660
M5M4V16169TP/RT-15	8.0ns/15ns	75ns/120ns	DRAM: 330 SRAM: 420

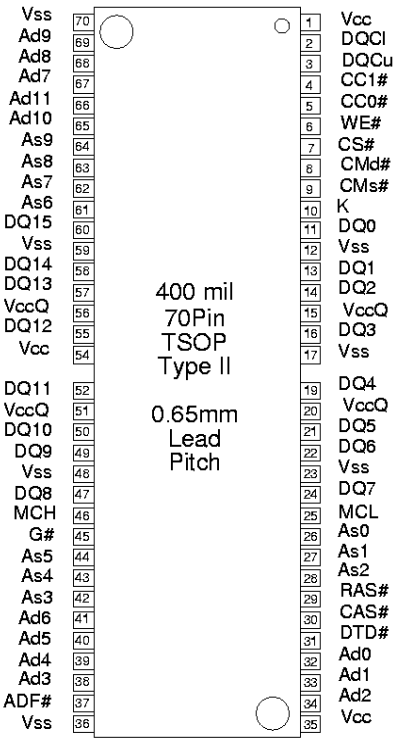
70-pin,400-mil TSOP (type II) with 0.65mm lead pitch and 23.49mm package length.
Multiplexed DRAM address inputs for reduced pin count and higher system densities.
Selectable output operation (transparent / ~~latched~~ / registered) using set command register cycle.
Single 3.3V +/- 0.3V Power Supply. (3.3V +/- 0.15V for -7 part)
2048 refresh cycles every 64ms (Ad0->Ad10).
Programmable burst length (1,2,4,8) and burst sequence (sequential,interleave) with no latency.
Synchronous design for precise control with an external clock (K).
Output retention by advanced mask clock (CMs#).
All inputs/outputs low capacitance and LVTTL compatible.
Separate DRAM and SRAM address inputs for fast SRAM access.
Page Mode capability.
Auto Refresh capability.
Self Refresh capability.

K	: Master Clock
CS#	: Chip Select
CMd#	: DRAM Clock Mask
RAS#	: Row Addr. Strobe
CAS#	: Column Addr. Strobe
DTD#	: Data Transfer Direction
Ad	: DRAM Address
CMs#	: SRAM Clock Mask
CC0#,CC1#	: Control Clocks
WE#	: Write Enable
DQC(u/l)	: I/O Byte Control
As	: SRAM Address
G#	: Output Enable
DQ	: Data I/O
Vcc	: Power Supply
VccQ	: DQ Power Supply
Vss	: Ground
ADF#	:Address Fetch clock This pin can be None-Connect.
MCL	:Must Connect Low
MCH	:Must Connect High

PINCONFIGURATION (TOP VIEW)

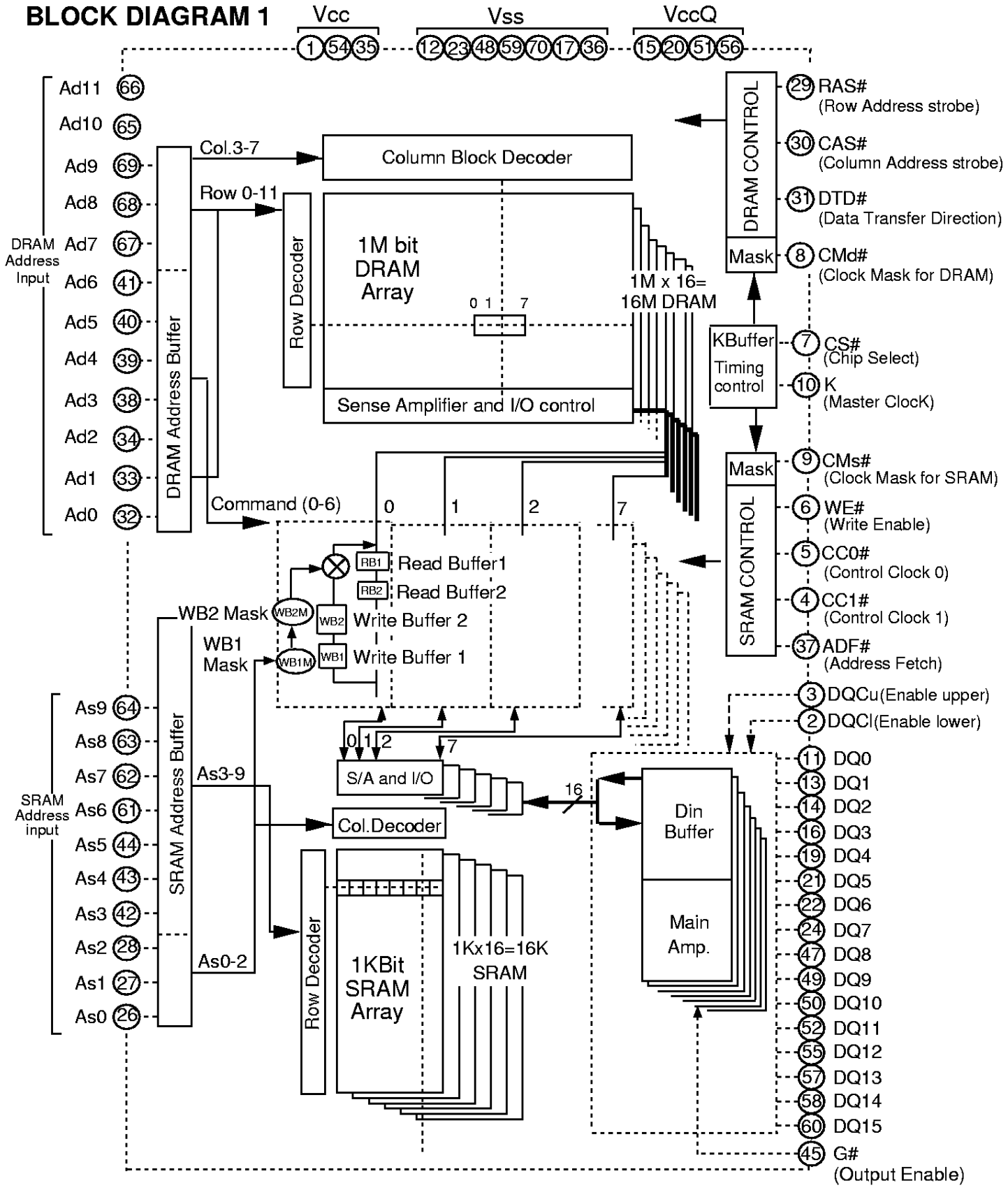


Package code:70P3S-L

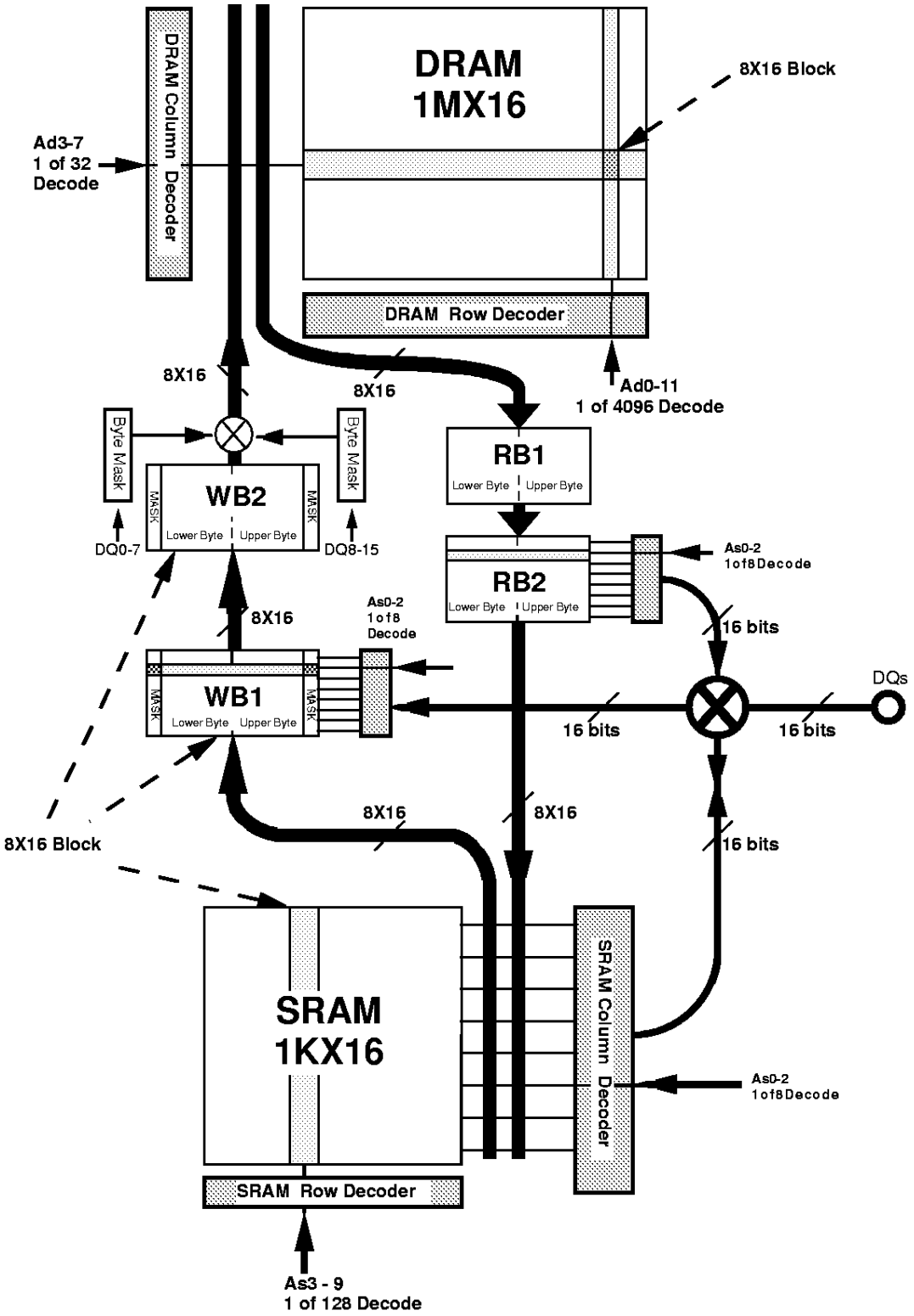


Package code:70P3S-M

BLOCK DIAGRAM 1



BLOCK DIAGRAM 2



FUNCTION TRUTH TABLE

Mnemonic CODE	CS#	SRAM					As (SRAM address)	DRAM				Ad (DRAM address)			
		Previous CMs#	CC0#	CC1#	DQC (u/l)	WE#	As0-9	Previous CMd#	RAS#	CAS#	DTD#	Ad0-11	Ad2	Ad1	Ad0
NOP	H	H	X	X	X	X	X	H	X	X	X	X			
SPD	X	L	X	X	X	X	X	X	X	X	X	X			
LBM	L	H	H	H	H	L	X	X	X	X	X	X			
DES	L	H	H	H	X	X	X	X	X	X	X	X			
SR	L	H	H	L	H	H	As0-9	X	X	X	X	X			
SW	L	H	H	L	H	L	As0-9	X	X	X	X	X			
BRT	L	H	L	H	L	H	As3-9 (2)	X	X	X	X	X			
BWT	L	H	L	H	L	L	As3-9 (2)	X	X	X	X	X			
BRTR	L	H	L	H	H	H	As0-9	X	X	X	X	X			
BWTW	L	H	L	H	H	L	As0-9	X	X	X	X	X			
BR	L	H	L	L	H	H	As0-2 (2)	X	X	X	X	X			
BW	L	H	L	L	H	L	As0-2 (2)	X	X	X	X	X			
DPD	X	X	X	X	X	X	X	L	X (1)	X (1)	X (1)	X			
DNOP	L	X	X	X	X	X	X	H	H	H	X	X			
DRT	L	X	X	X	X	X	X	H	H	L	H	Ad3-7 (2) (Col.Block)	0	0	0
DWT1	L	X	X	X	X	X	X	H	H	L	L	Ad3-7 (2) (Col.Block)	0	0	0
DWT1R	L	X	X	X	X	X	X	H	H	L	L	Ad3-7 (2) (Col.Block)	0	0	1
DWT2	L	X	X	X	X	X	X	H	H	L	L	Ad3-7 (2) (Col.Block)	0	1	0
DWT2R	L	X	X	X	X	X	X	H	H	L	L	Ad3-7 (2) (Col.Block)	0	1	1
DWT3	L	X	X	X	X	X	X	H	H	L	L	Ad3-7 (2) (Col.Block)	1	0	0
DWT3R	L	X	X	X	X	X	X	H	H	L	L	Ad3-7 (2) (Col.Block)	1	0	1
DWT4	L	X	X	X	X	X	X	H	H	L	L	Ad3-7 (2) (Col.Block)	1	1	0
DWT4R	L	X	X	X	X	X	X	H	H	L	L	Ad3-7 (2) (Col.Block)	1	1	1
ACT	L	X	X	X	X	X	X	H	L	H	H	Ad0-11 (Row Add.)			
PCG	L	X	X	X	X	X	X	H	L	H	L	X			
ARF	L	X	X	X	X	X	X	H (7)	L	L	H	X			
SRF	L	X	X	X	X	X	X	H (8)	L	L	H	X			
SCR	L	X	X	X	X	X	X	H	L	L	L	Command			

NOTES

1) For the DPD function, the RAS#, CAS# and DTD# inputs are DON'T CARE except for the L,L,H combination. (Respectively).
2) The unused addresses must be set to Low.
3) Use New: If BW or BWT or BWTW is initiated the same cycle as DWT1 or DWT1R, new data is loaded into the buffer and transferred to DRAM.
4) Clear 1 or 2 Transfer Mask Bits (as addressed by As0-2 and DQCU/L).
5) Actual number of bits transfer depends on the state of the DTBW Mask and the DQCU/DQCL inputs. Note: If DQC(U/L) is Low, the corresponding DQ(s) is(are) disabled (Input and Output Buffer). SR,SW,BR and BW cycles with DQCU and DQCL Low result in a Deselect SRAM operation.
6) Following a DWT1 or DWT1R cycle, the entire WB1 Transfer Mask is Set . (i.e. , data can no longer be transferred from WB1 to DRAM.) Succeeding Buffer-Writes or Buffer Write Transfers will Clear Mask bits.
7) CMd# during current cycle must be High (see timing diagram for Auto-Refresh).
8) CMd# during current cycle must be Low (see timing diagram for Self-Refresh).

FUNCTION TRUTH TABLE

Data Transfer Buffers					DQ pin		Function	
Write Buffers		Xfer Masks		Read Buffer RB1,2				
WB1	WB2	WB1 Mask	WB2 Mask		Din	Dout		
-	-	-	-	-	-	Hi-Z	No Operation	
-	-	-	-	-		Suspend	SRAM Power Down& Data retention	No operation
-	-	-	-	-	Byte mask	Hi-Z	DRAM Power Down	No operation
-	-	-	-	-	-	Hi-Z	Deselect SRAM	No operation
-	-	-	-	-	-	Valid	SRAM Read	SRAM->DO
-	-	-	-	-	Valid	Hi-Z	SRAM Write	DIN->SRAM
-	-	-	-	Use	-	Hi-Z	Buffer Read Xfer	RB2->SRAM
Load	-	Clear Mask	-	-	-	Hi-Z	Buffer Write Xfer	SRAM->WB1
-	-	-	-	Use	-	Valid	Buffer Read Xfer & Read	RB2->SRAM->DO
Load	-	Clear Mask	-	-	Valid	Hi-Z	Buffer Read Xfer & Read	DIN->SRAM->WB1
-	-	-	-	Use	-	Valid	Buffer Read	RB2->DO
Load	-	Clear 1 (4) or 2 bits	-	-	Valid	Hi-Z	Buffer Write	DIN->WB1
-	-	-	-	-	-	-	DRAM Power Down	No operation
-	-	-	-	-	-	-	DRAM No OPeration	No operation
-	-	-	-	Load	-	-	DRAM Read Xfer	DRAM->RB1->RB2
Use	Load/ Use	(6) Use	Load/ Use	-	-	-	DRAM Write Xfer1	(3) WB1->WB2->DRAM
Use	Load/ Use	(6) Use	Load/ Use	Load	-	-	DRAM Write Xfer1& Read	WB1->WB2 (3) ->DRAM->RB1->RB2
-	Use	-	Use	-	-	-	DRAM Write Xfer2	WB2->DRAM
-	Use	-	Use	Load	-	-	DRAM Write Xfer2& Read	WB2->DRAM ->RB1->RB2
Use	Load/ Use	-	Load	-	-	-	DRAM Write Xfer3	WB1->WB2->DRAM
Use	Load/ Use	-	Load	Load	-	-	DRAM Write Xfer3& Read	WB1->WB2 (3) ->DRAM->RB1->RB2
-	Use	-	-	-	-	-	DRAM Write Xfer4	WB2->DRAM
-	Use	-	-	Load	-	-	DRAM Write Xfer4& Read	WB2->DRAM->RB
-	-	-	-	-	-	-	DRAM Activate	Page Call
-	-	-	-	-	-	-	DRAM Precharge	
-	-	-	-	-	-	-	Auto Refresh	
-	-	-	-	-	-	-	Self Refresh Entry	
-	-	-	-	-	-	-	Set Command Register	

Function	Data Transferred (max)
Din --> SRAM	8/16 bits (5)
Din --> WB1	8/16bits (5)
SRAM --> WB1	128 bits (8X16bit-block)
WB1 --> WB2	128 bits (8X16bit-block)
WB2 --> DRAM	128 bits (8X16bit-block)

Function	Data Transferred (max)
WB2 --> RB	128 bits (8X16bit-block)
DRAM --> RB	128 bits (8X16bit-block)
RB --> Dout	8/16 bits (5)
RB --> SRAM	128 bits (8X16bit-block)

DO: Data Out
DIN: Data In
WB1: Write Buffer 1
WB2: Write Buffer 2
RB: Read Buffer

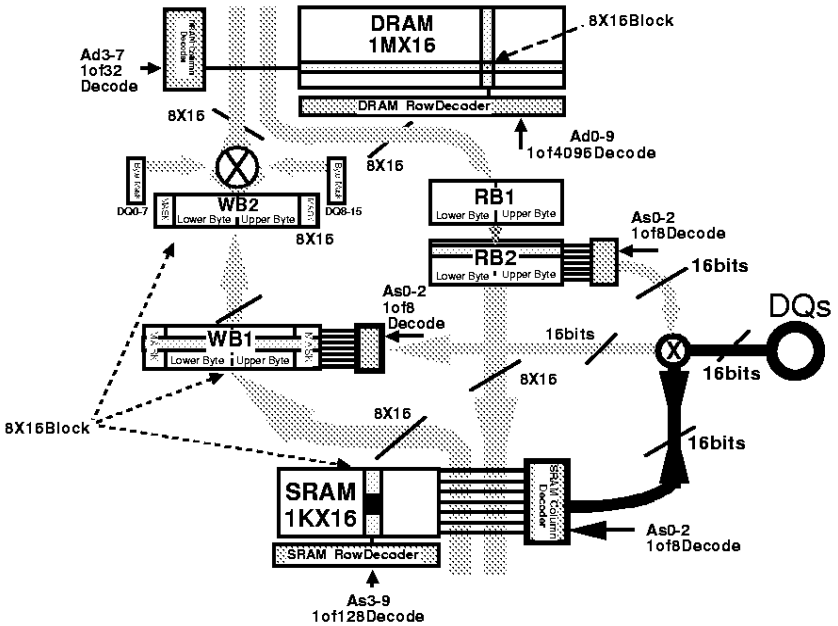
PIN DESCRIPTIONS(1)

K	Input	Master Clock Provides the fundamental timing and the internal clock frequency for the CDRAM. All external timing parameters (with the exception of G# in read cycle and CMd# in Self refresh cycle) are specified with respect to the rising edge of K.
CMd#	Input	DRAM Clock Mask controls the operation of the internal DRAM master clock (K). When CMd# is Low at the rising edge of K, the internal DRAM master clock (K) for the following cycle is ceased and input stages are powered-off, resulting in a DRAM Power Down.
RAS#	Input	Row Address Strobe is used in conjunction with Master clock K (depending on the states of CMd#, CAS#, and DTD#) to activate the DRAM (latching the Row Address lines and accessing 1 of 4096 rows), initiate a DRAM precharge cycle, perform a DRAM Read or Write Transfer, DRAM Write Transfer & Read, set the command registers, start an Auto-Refresh cycle, enter a Self-Refresh cycle,create a DRAM NOP cycle, or power down the DRAM.
CAS#	Input	Column Address Strobe is used in conjunction with the Master Clock K to latch the Column addresses. When preceded by RAS# in a DRAM access cycle, CAS# initiates a DRAM Write Transfer (WB1/2 -> DRAM, if DTD#=L), DRAM Write Transfer & Read (WB1/2 -> DRAM -> RB, if DTD#=L) or DRAM Read Transfer (DRAM -> RB, if DTD#=H), depending on the state of DTD# (see DTD# pin description).
DTD#	Input	Data Transfer Direction controls DRAM-to-RB(read) / WB-to-DRAM (write) direction. If preceded by a RAS# low cycle, both CAS# and DTD# low (on the rising edge of K) initiate a DRAM Write Transfer cycle. If DTD# stays High with the above conditions, a DRAM Read Transfer cycle results. DTD# can also initiate DRAM Activate, DRAM Precharge, Auto-Refresh, Set-Command Register, and Self Refresh cycles.
Ad0-Ad11	Input	DRAM Address Lines are Multiplexed to reduce pin count. Ad0-Ad11 (@ RAS=low,CAS=high,DTD=high, K=Rising edge) specify the Row Address of the DRAM to activate and refresh the selected page and Ad3-Ad7 (@ RAS=high,CAS=low,K=Rising edge) specify the Block Address of the DRAM. In addition, Ad0-Ad2 (@ RAS=high,CAS=low, K=Rising edge) specify the transfer operation of the DRAM . Also Ad0-Ad9 (@RAS=low,CAS=low, DTD=low, K=Rising Edge) are used as the command in set command register cycle.
CS#	Input	The Chip Select controls the operation of the CDRAM. When CS#=H at the rising edge of K and the previous CMd# or CMs# is high, the chip is in No Operation mode.
CMs#	Input	SRAM Clock Mask controls the operation of the internal SRAM master clock (Ks). When CMs# is asserted at a rising edge of K, the internal SRAM master clock for the following cycle is suspended, resulting in the power down of the SRAM portion of the circuit, including the Sense Amps. CMs# can also be used to retain output data during SRAM power-down.

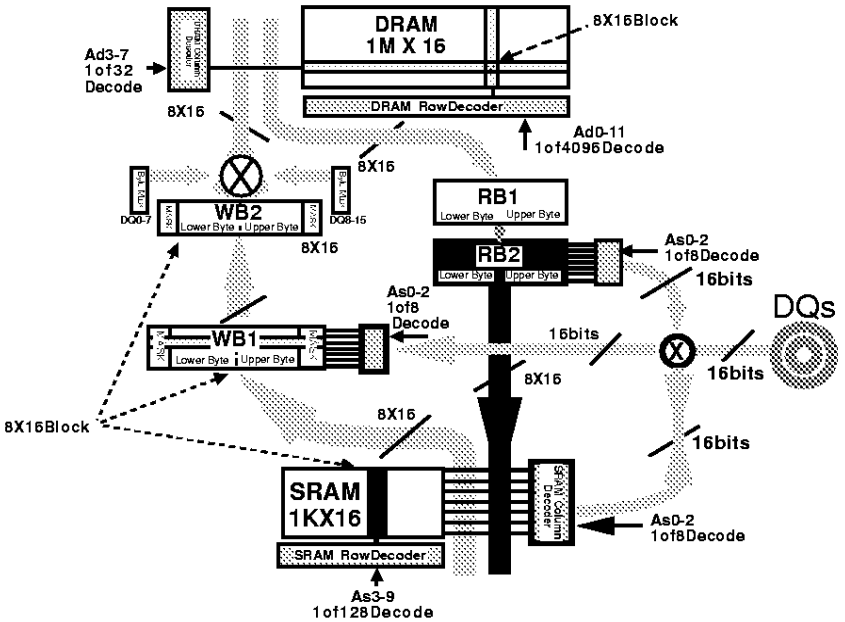
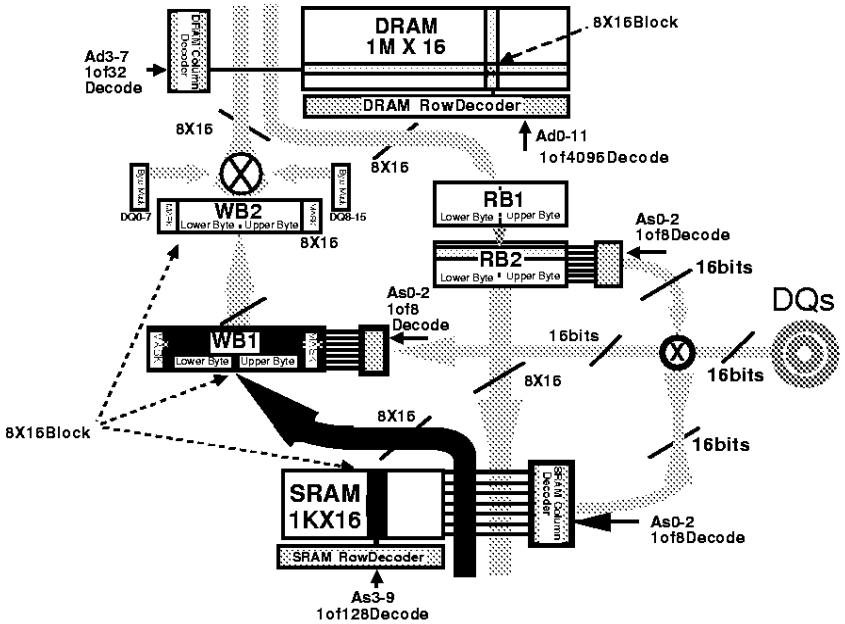
PIN DESCRIPTIONS(2)

DQCl,DQCu	Input	DQCu/l are I/OByte control signals. If G#=Low, DQCu/l have a control of output impedence: DQCu controls upper DQs (DQ8-15) & DQCl controls lower DQs (DQ0-7). DQCu/l also control both input data during SRAM Writes or Buffer Writes and transfer mask during Buffer Writes. (WB1 transfer Masks for each byte are written (bits are cleared) during Buffer Writes depending on DQCu/l inputs.)
WE#	Input	Write Enable controls SRAM and Buffer read and write operations. A high on the WE# pin causes either a Buffer Read, SRAM Read, Buffer Read Transfer and/or a Buffer Read Transfer & Read to occur (depending on the state of the CC0# and CC1# bits). A low on the WE# pin causes either a Buffer Write, SRAM Write, Buffer Write Transfer and/or a Buffer Write Transfer & Write to occur (depending on the state of the CC0# and CC1# inputs)
CC0#,CC1#	Inputs	The Control Clock Inputs control SRAM and Buffer operations. CC0# is Low for all Buffer Writes, Reads, and Transfers, and High for all other SRAM operations. CC1# is high for all Buffer Read Transfers and Buffer Write Transfers , and Deselect SRAM.
As0-As9	Inputs	SRAM Addresses are non-multiplexed, and access 1024 - 16-bit words (configured as 128 Rows X 8 Columns X 16 Bits, where the Block Size is 8 X 16) in the SRAM array. As0-As3 select word address within a block, and As3-As9 select the SRAM row(block).
G#	Input	The Output Enable is an asynchronous input. G#=high forces the outputs to high impedence.
DQ0-DQ15	Inputs / Outputs	Output operation is either transparent, ~~latched~~, or registered depending on the state of the command register. The Data Lines for the CDRAM are asynchronously controlled by G#.
VccQ	Supply	VccQ is the DQ power supply and allows the device to operate in a mixed voltage system (e.g., 5V data bus). As specified in the Table: Recommended Operating Conditions, VccQ must be greater-than or equal-to the highest voltage experienced by the data bus. For 3.3V system operation, VccQ may be tied to Vcc.

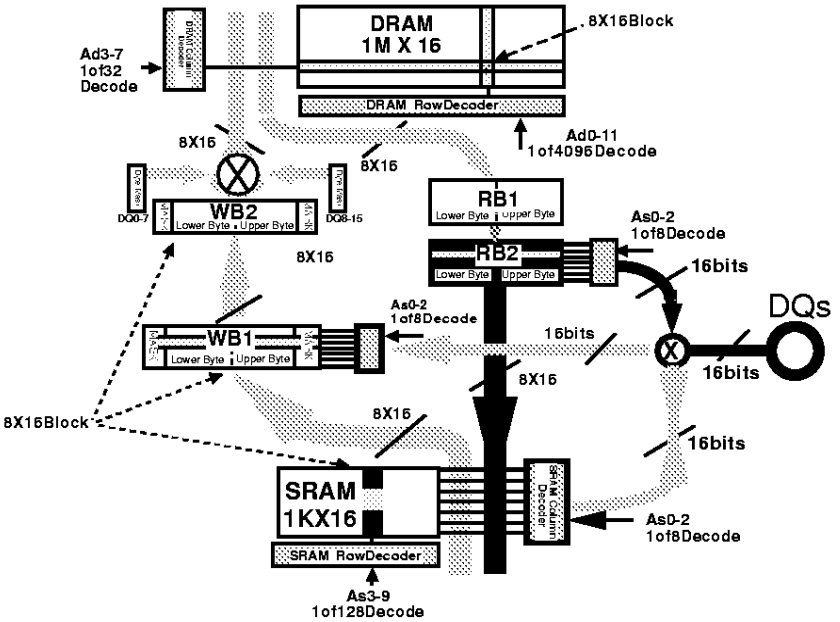
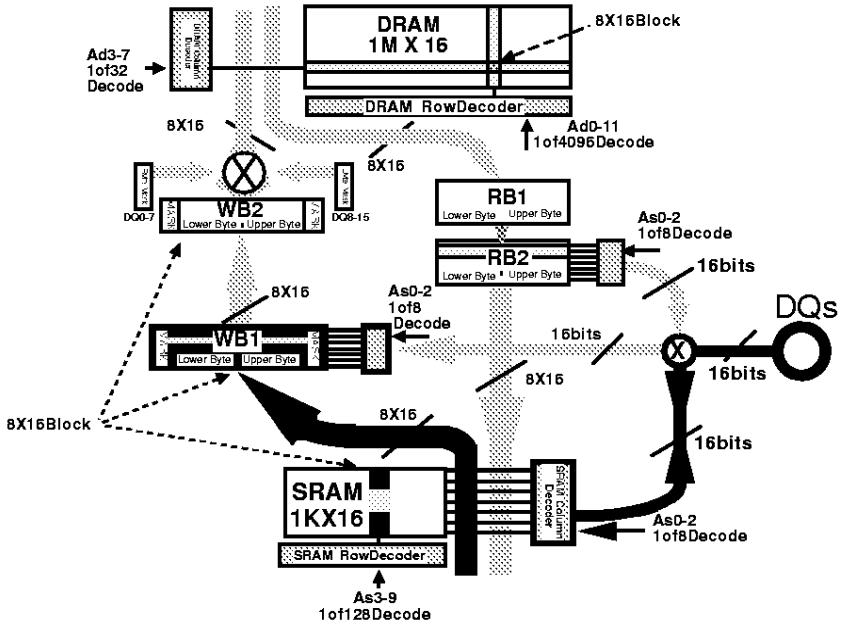
MODE DESCRIPTIONS (1)

NOP	No Operation. Outputs are high-impedance. All input buffers remain active.
SRAM Power-Down	If CMs#=Low at the rising edge of K, the SRAM enters SRAM Power Down at the next rising edge of K. During this mode, the internal SRAM K clock becomes inactive. The Output Buffers remain enabled and are controlled by G#. All input buffers of SRAM clocks and SRAM addresses are inactive.
Deselect SRAM	All transfer functions and input/output operations to and from the SRAM and Buffer are disabled. This cycle is useful for output impedance control (Hi-Z,Low-Z) without G#. Output buffers are active during this cycle for registered output mode control.
SRAM Read	Data is read from the SRAM to the I/O pins. Addresses As0-As9 are used to select the data to be read. As3-As9 decode the SRAM Row (=Block), and As0-As2 decode (1 of 8) the 16-bit word. DQCu and DQCl control the impedence (High-Z/Low-Z) of the upper and lower bytes, respectively.
SRAM Write	Data is written from the I/O pins to the SRAM. Addresses As0-As9 are used to select the location to be written. As3-As9 decode the SRAM Row (=Block), and As0-As2 decode (1of8) the 16-bit word to be written. DQCUu and DQCl control Upper and Lower byte writes, respectively. 

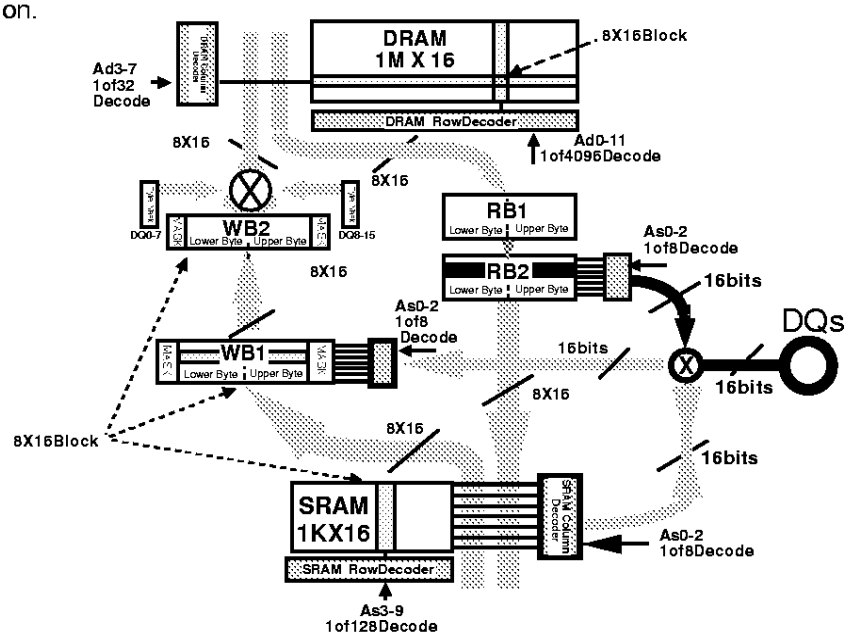
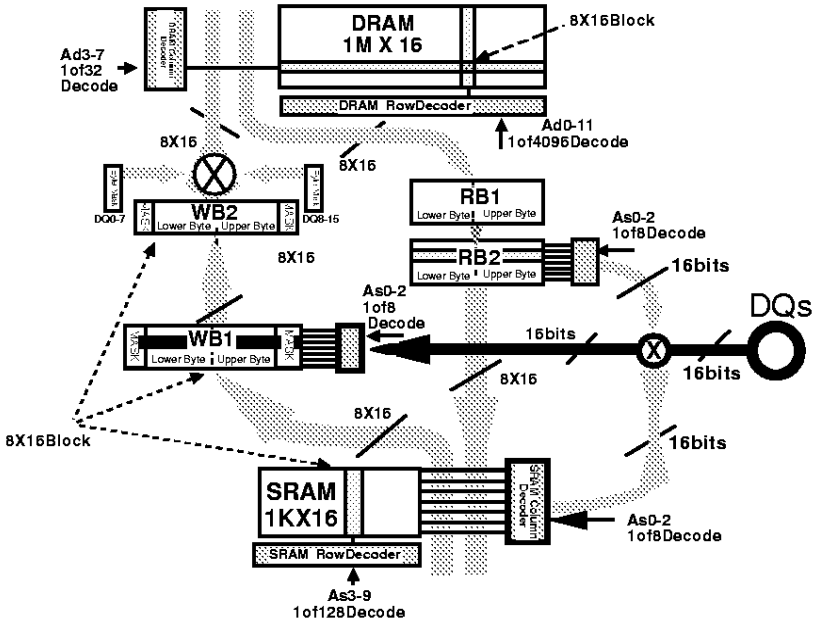
MODE DESCRIPTIONS (2)

Buffer Read Transfer	Data is transferred from the Read Buffer (RB2) to the SRAM. Addresses As3-9 select the SRAM row to which the 8X16 bit block is to be written. Addresses As0-As2 must be set low. 
Buffer Write Transfer	Data is transferred from the SRAM to the Write-Buffer1 (WB1). Addresses As3-As9 decode the SRAM Row (=8X16 bit block) to be transferred. Addresses As0-As2 must be set low. The Buffer Write Transfer cycle "clears" all transfer mask bits in the WB1 Mask (allowing all data to be transferred in a successive DRAM Write Transfer cycle). 

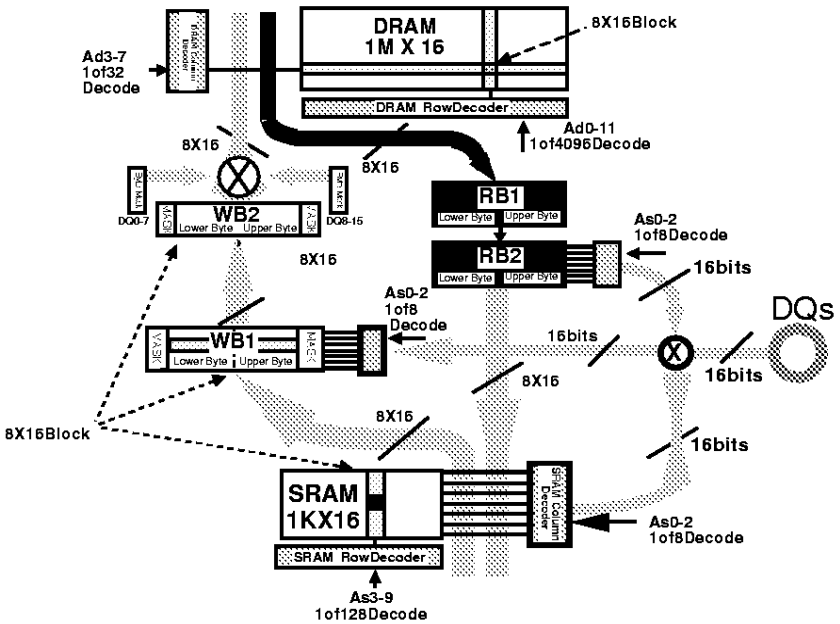
MODE DESCRIPTIONS (3)

Buffer Read Transfer & SRAM Read	Data is transferred from the Read Buffer (RB2) to the SRAM, and simultaneously, data (16 bit word) is read from the RB2 to the I/O pins. Addresses As3-9 select the SRAM Row to which the 8X16 bit block is to be written. Addresses As0-As2 decode the 16-bit word to be read. 
Buffer Write Transfer & SRAM Write	Data is first written from the I/O pins to SRAM as decoded by As0-As9. Then, the SRAM Row (=Block) decoded by As3-As9 is transferred to the Write-Buffer1 (WB1). The Buffer Write Transfer cycle "clears" all transfer mask bits in the WB1 Mask (allowing all data to be transferred in a successive DRAM Write Transfer cycle). DQCu and DQCl control Upper and Lower byte writes respectively, however all transfer mask bits in the WB1 are cleared. 

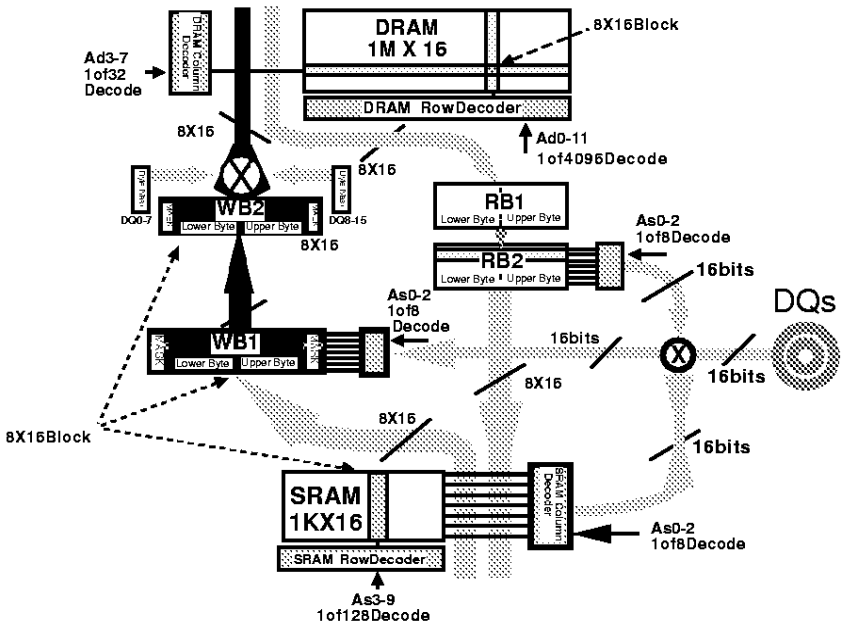
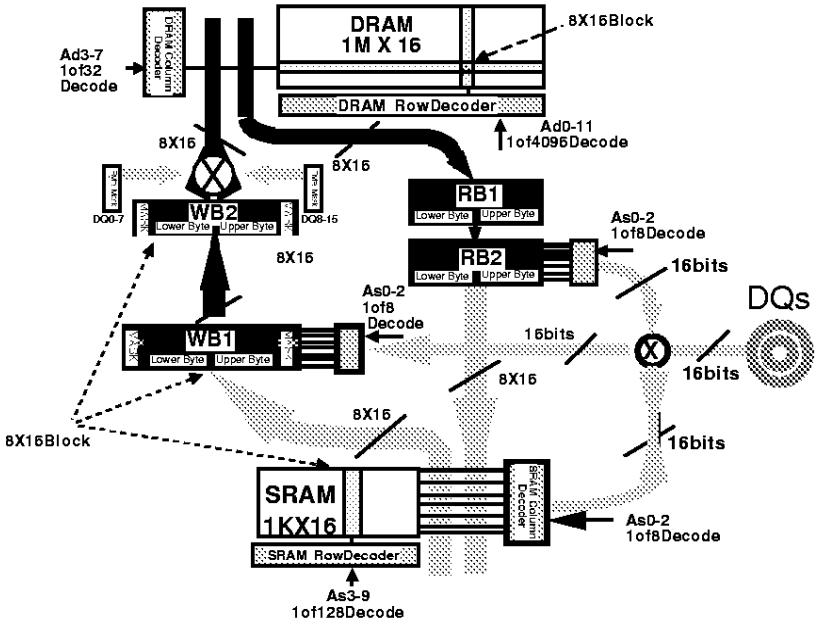
MODE DESCRIPTIONS (4)

Buffer Read	Data is read from the Read Buffer (RB2) to the I/O pins. Addresses As0-As2 are used to select (1 of 8) the 16-bit word to be read. Addresses As3-As9 must be set low for this operation. 
Buffer Write	Data is written from the I/O pins to the Write-Buffer1. Addresses As0-A2 are used to select (1of8) the 16-bit word to be written. Addresses As3-As9 must be set low for this operation. The transfer mask bits associated with the Upper and Lower bytes are cleared in the WB1 Mask. DQCu and DQCl control Upper and Lower byte writes (and associated tranfer mask bits), respectively. 

MODE DESCRIPTIONS (5)

DRAM Power-Down	If CMd#=Low at the rising edge of K, the DRAM enters DRAM Power Down at the next rising edge of K. During this mode, the internal DRAM K clock becomes inactive. Also all input buffers of DRAM clocks and DRAM addresses are inactive. Note that the latency of DRAM Read Transfer cycle is not counted up in this cycle.
DRAM NOP	The DNOP cycle is used when no other DRAM operations are desired, holding the DRAM in its present (precharge/activate) state.
DRAM Read Transfer	A Block (8x16) is transferred from the DRAM to the Read Buffer1 and 2 (RB1,RB2) as specified by Addresses Ad3-Ad7. Addresses Ad8-Ad11 and Ad0-Ad2 must be set to Low. After the Latency Period (specified in the Access Latency Table) new data will be present in the Read Buffer2. Prior to the Latency timeout, old data will be present in the RB2. (Notes 1,2,4) 

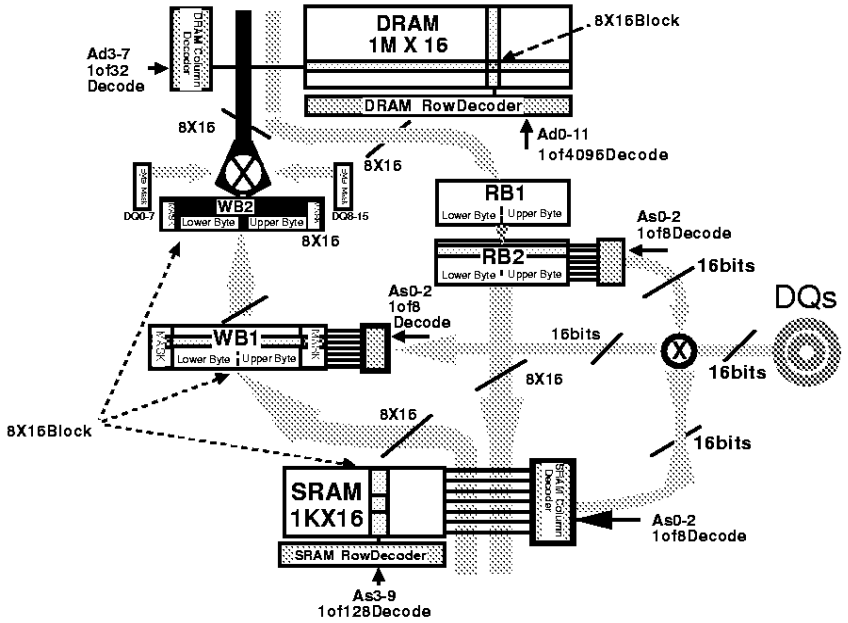
MODE DESCRIPTIONS (6)

DRAM Write Transfer1	Data (8X16 Block) is transferred from WB1 through WB2 to the DRAM block specified by Addresses Ad3-Ad7. Addresses Ad8-Ad11 must be set to Low. The Mask present in WB1 is also transferred to WB2 and controls the data written to the DRAM. After data has been transferred from WB1 to WB2 in the present cycle, the entire WB1 Mask is Set. (Notes 3,4) 
DRAM Write Transfer1 & Read	Data (8X16 Block) is transferred from WB1 through WB2 to the DRAM block specified by Addresses Ad3-Ad7. Addresses Ad8-A11 must be set to Low. The transfer mask present in WB1 is also transferred to WB2 and controls the data written to the DRAM. The block to which the data is written in DRAM is simultaneously transferred to the Read Buffer.(Notes 2,3,4) 

MODE DESCRIPTIONS (7)

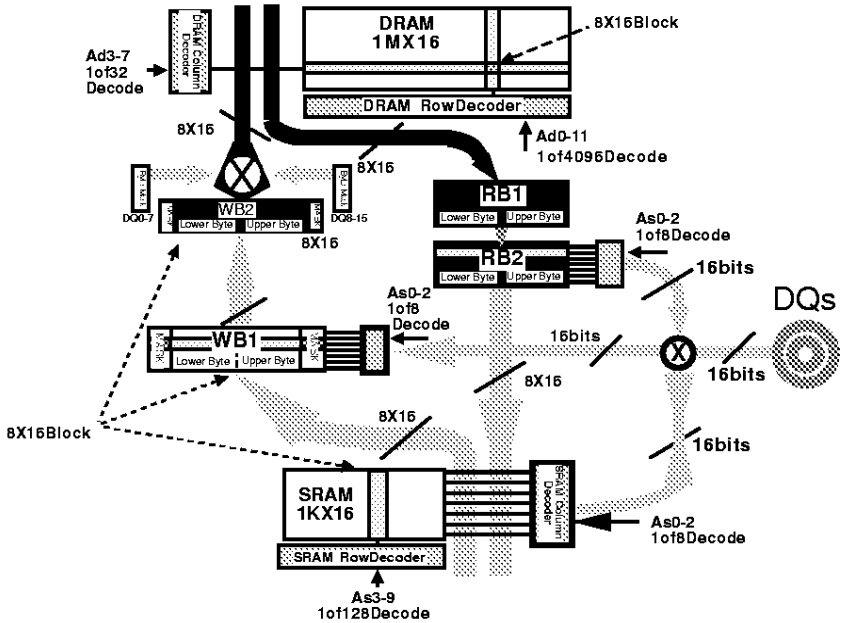
DRAM Write Transfer2

Data (8X16 Block) is transferred from WB2 to the DRAM block specified by Addresses Ad3-Ad7. Addresses Ad8-Ad11 must be set to Low. The WB2 Mask controls the data written to the DRAM. With the DWT2 function, the WB2 data and WB2 transfer mask remain unchanged. (Note 4)

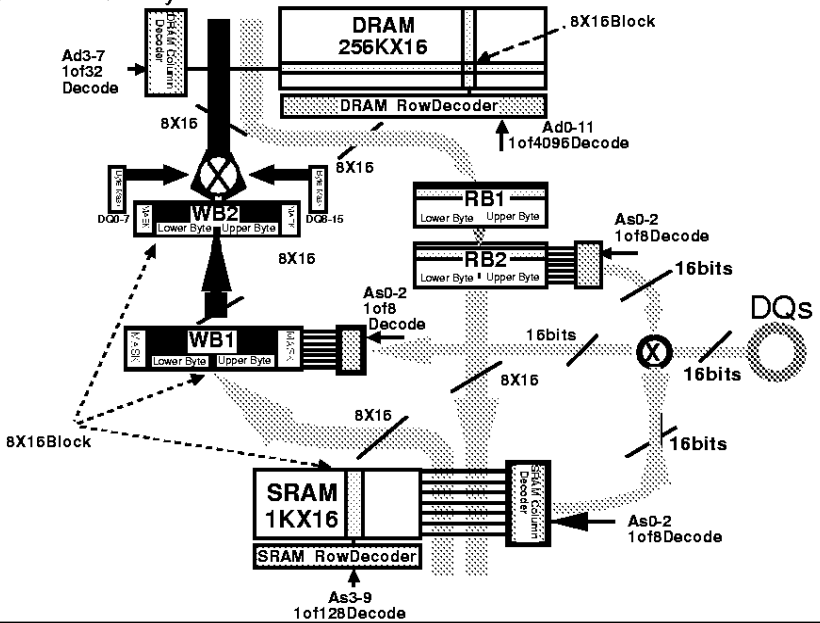
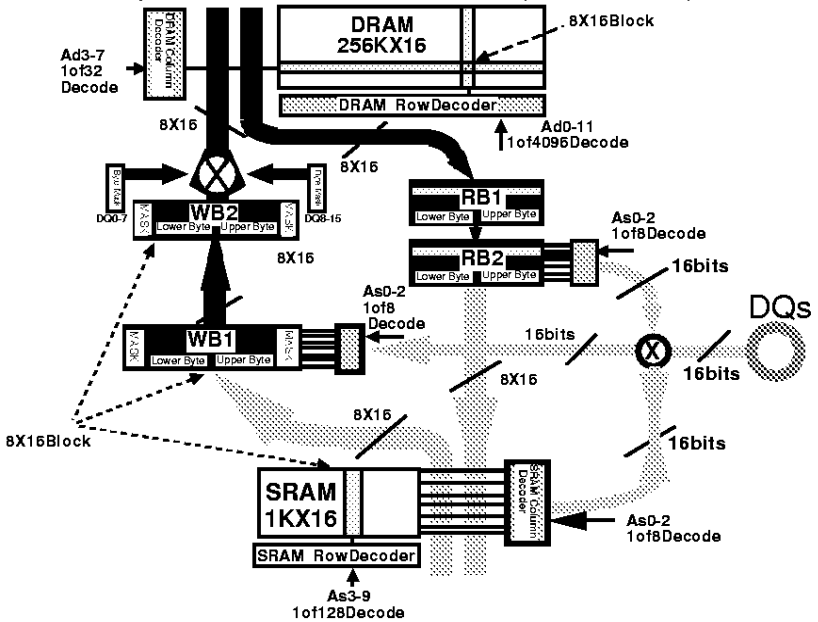


DRAM Write Transfer2 & Read

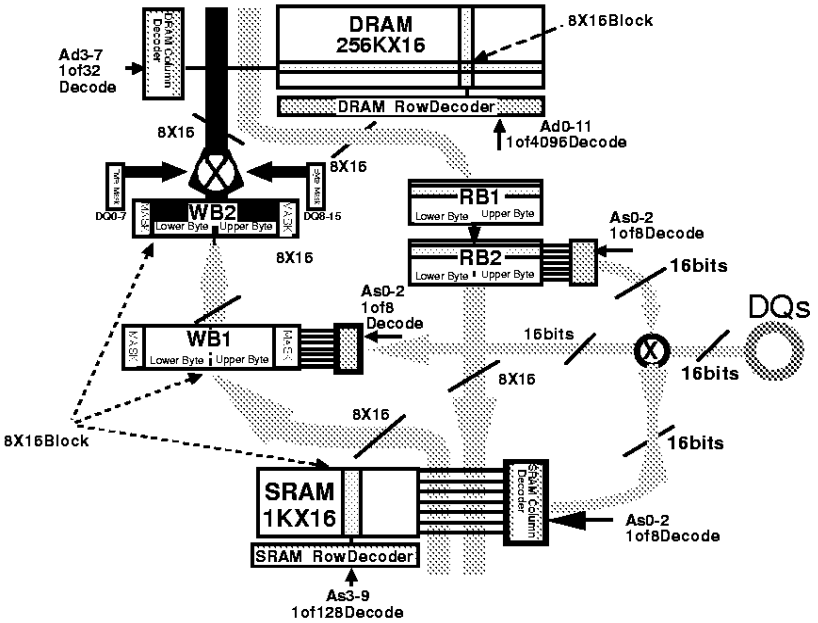
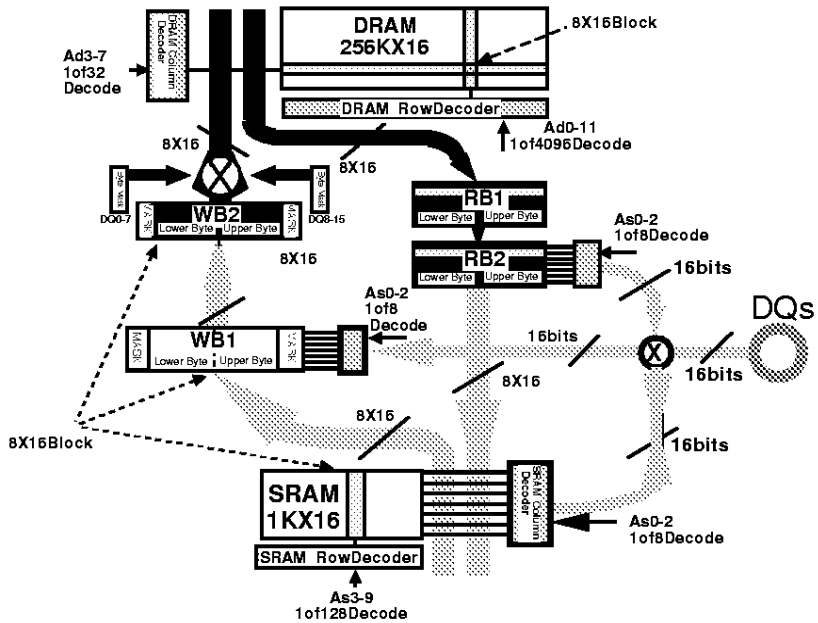
Data (8X16 Block) is transferred from WB2 to the DRAM block specified by Addresses Ad3-Ad7. Addresses Ad8-Ad11 must be set to Low. The WB2 transfer mask controls the data written to the DRAM. With the DWT2 function, the WB2 data and WB2 transfer mask remain unchanged. The block to which the data is written in DRAM is simultaneously transferred to the Read Buffer1 and 2. (Notes 1,2,4)



MODE DESCRIPTIONS (8)

DRAM Write Transfer3	Data (8X16 Block) is transferred from WB1 through WB2 to the DRAM block specified by Addresses Ad3-Ad7. Addresses Ad8-Ad9 must be set to Low. The Mask present in Byte MaskRegister controls the data written to the DRAM. The Byte Mask Register is set at Load Byte Mask cycle,where corresponding byte masks are set depending on DQ data in the cycle. (Note 4,5) The data of WB1 and the mask data of WBM1 are tranferred to WB2 and WBM2, however WBM1/2 is not used in this cycle. 
DRAM Write Transfer3 & Read	Data (8X16 Block) is transferred from WB1 through WB2 to the DRAM block specified by Addresses Ad3-Ad7. Addresses Ad8-Ad9 must be set to Low. The Mask present in Byte MaskRegister controls the data written to the DRAM. The block to which the data is written in DRAM is simultaneously transferred to the Read Buffer.(Notes 1,2,4,5) 

MODE DESCRIPTIONS (9)

DRAM Write Transfer4	Data (8X16 Block) is transferred from WB2 to the DRAM block specified by Addresses Ad3-Ad7. Addresses Ad8-Ad9 must be set to Low. The Mask present in Byte MaskRegister controls the data written to the DRAM. With the DWT4 function, the WB2 data and WB2 Mask remain unchanged. (Note 4,5) 
DRAM Write Transfer4 & Read	Data (8X16 Block) is transferred from WB2 to the DRAM block specified by Addresses Ad3-Ad7. Addresses Ad8-Ad9 must be set to Low. The Mask present in Byte MaskRegister controls the data written to the DRAM. With the DWT4R function, the WB2 data and WB2 transfer mask remain unchanged. The block to which the data is written in DRAM is simultaneously transferred to the Read Buffer. (Notes 1,2,4,5) 

MODE DESCRIPTIONS (10)

DRAM Activate	Addresses are latched from the Ad0-Ad11 inputs by the rising edge of K. Internally, a DRAM row is selected (Page Call) in preparation for a DRAM Read or Write Transfer cycle. A DRAM Precharge cycle must separate all DRAM Activate cycles.
DRAM Precharge	Internally, the active DRAM Row is deselected (completing the refresh process) and page-mode is disabled. The DRAM is precharged prior to another DRAM Activate cycle.
DRAM Auto-Refresh	Internally, a DRAM row is selected and refreshed (as addressed by an internal, self-incrementing counter), followed by an internally generated Precharge cycle. The Auto refresh cycle can be implemented only if the DRAM is in Precharge state (i.e., a Precharge or Auto-Refresh cycle occurred more recently than an Acitvate cycle). DRAM Auto-Refresh is similar to a CAS-Before-RAS (CBR) mode in standard DRAMs.
DRAM Self Refresh	All clock buffers are suspended, and CMd# asynchronously controls Self Refresh (CMd# rising edge initiates exit from Self Refresh). During Self Refresh, device enters a low power mode, with 2048 automatic refresh cycles.
Set Command Register	When SCR is initiated,the addresses present on the Ad0-Ad11 DRAM Address pins determine the DRAM Read Transfer Latency, the Output Mode (transparent / ~~latched~~ / registered), and WB1 transfer mask mode (set-all/ no change). No DRAM operation is executed in this cycle. Refer to the SCR Truth Table for legal Address values. During SCR cycle and the following 3 clock cycles(totally 4 clock cycles), only NOP,DNOP orDPD are allowed in DRAM portion and only NOP,DES or SPD are done in SRAM portion. The set commands are valid at least after the above 4 clocks later and the previous function is not guaranteed to work if it has not been completed.(i.e. DRT ,DWT1&R,DWT2&R and SR,BR and BRTR with registered output mode.)

Notes:
1) This function is performed in a Latency period specified in the Access Latency Table.
2) After the Latency Period (specified in the Access Latency Table) new data will be present in the Read Buffer2. Prior to the Latency timeout, old data will be present in the RB2.
3) After data has been transferred from WB1, the entire WB1 Mask is Set.
4) Valid Ad0-Ad2 addresses are shown in the FUNCTION TRUTH TABLE.

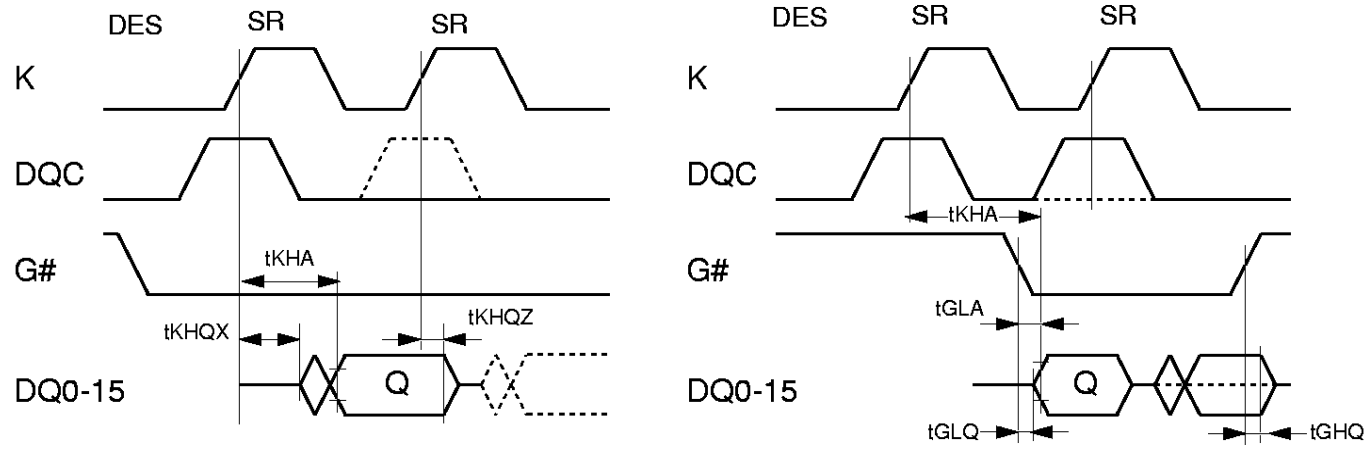
Power-On sequence

Before starting normal operation, the following power on sequence is necessary.
1) Apply power and maintain stable power (pause) for 500us.
2) Perform a precharge (PCG) operation.
3) After tRP, perform 8 auto refresh commands (ARF) with adequate interval (tRC).
4) Issue set command register (SCR) to initilize the mode register.

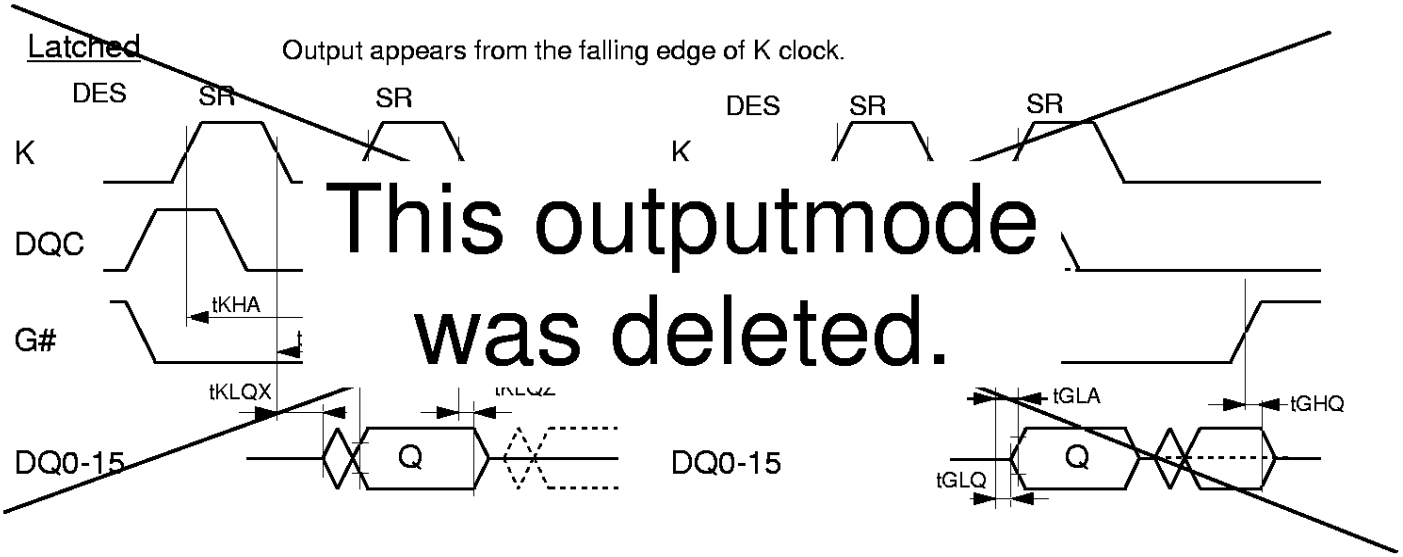
After this sequence, the RAM is in idle state and ready for normal operation.
Note that DNOP / DPD and DES / SPD or NOP command will be the stand-by command for the above power sequence.
Vcc must be powered-on at the same time or before VccQ is on.
And Vcc must be powered-off at the same time or after VccQ is off.

Output Operations

Transparent — Output appears from the rising edge of K clock.

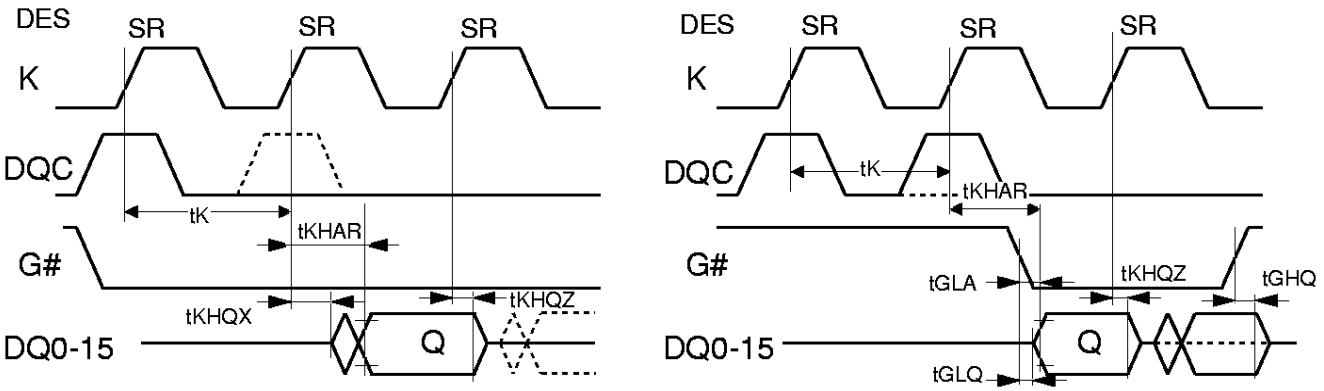


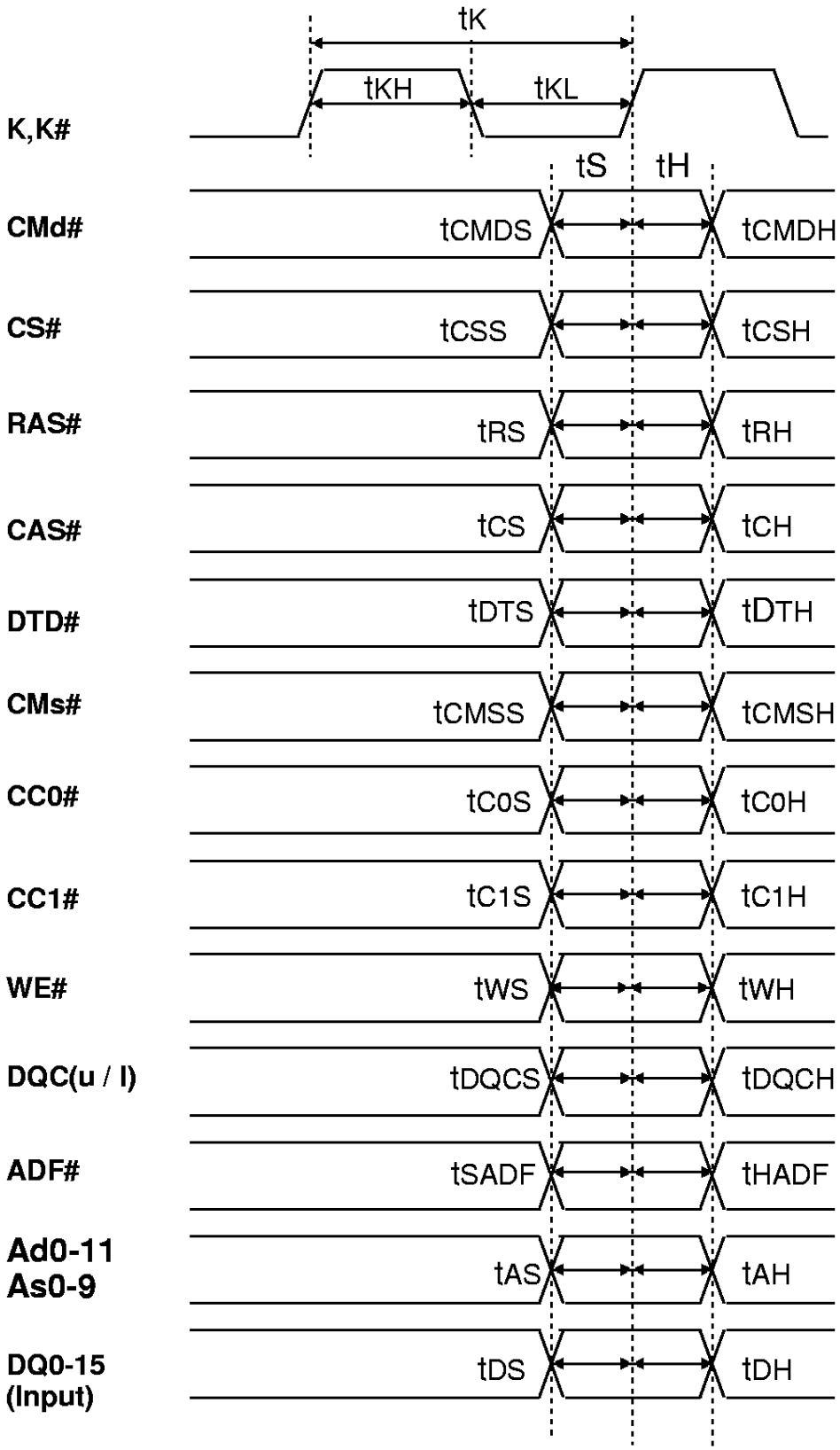
Latched — Output appears from the falling edge of K clock.



This outputmode was deleted.

Registered — Output appears from the rising edge of K clock.

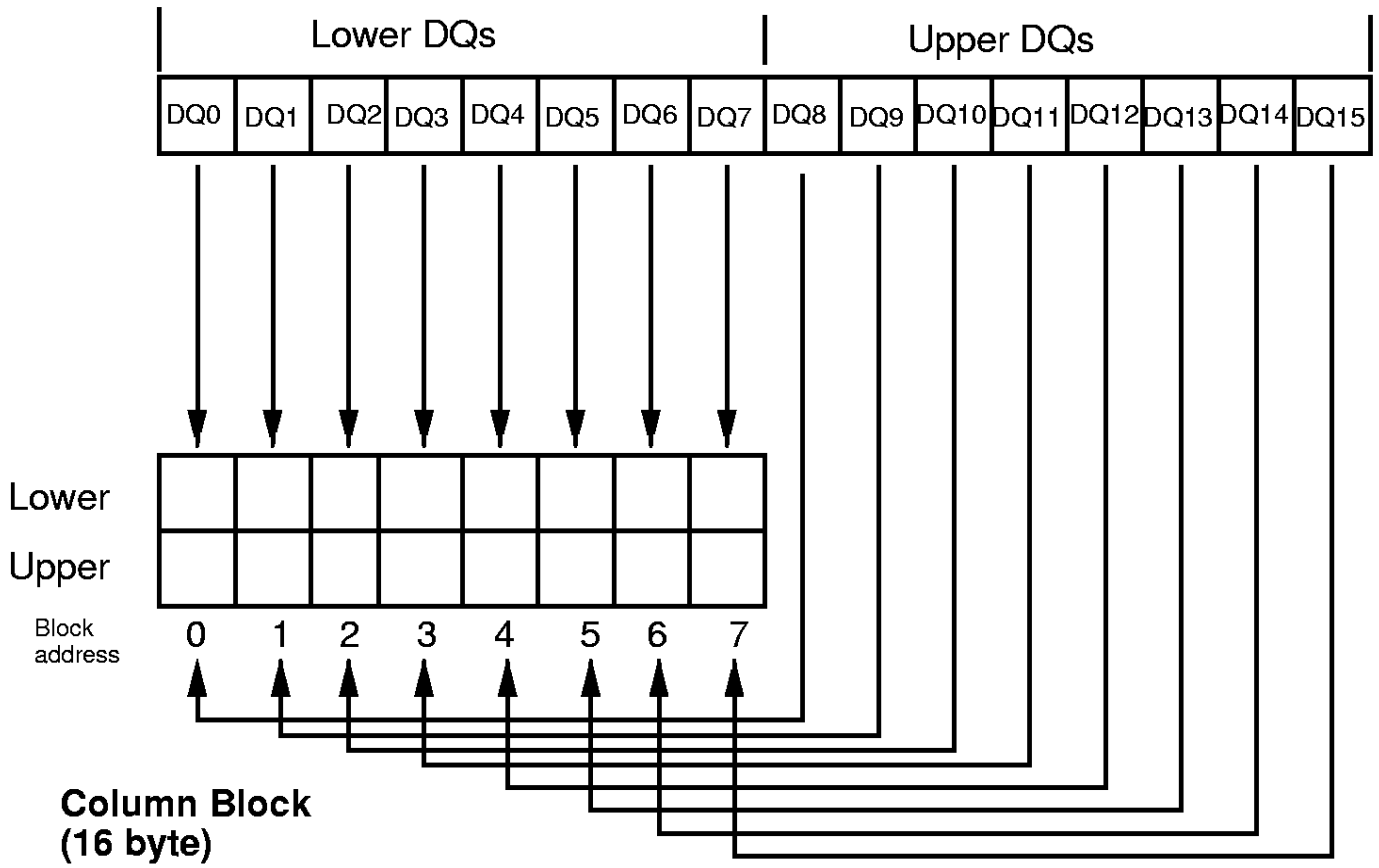



tK
tKH
tKL
K,K#
tS
tH
CMd#
tCMDS
tCMDH
CS#
tCSS
tCSH
RAS#
tRS
tRH
CAS#
tCS
tCH
DTD#
tDTS
tDTH
CMs#
tCMSS
tCMSH
CC0#
tC0S
tC0H
CC1#
tC1S
tC1H
WE#
tWS
tWH
DQC(u / l)
tDQCS
tDQCH
ADF#
tSADF
tHADF
Ad0-11
As0-9
tAS
tAH
DQ0-15
(Input)
tDS
tDH

Load Byte Mask

Byte mask allocation during DWT3 and DWT4

Byte Mask Register

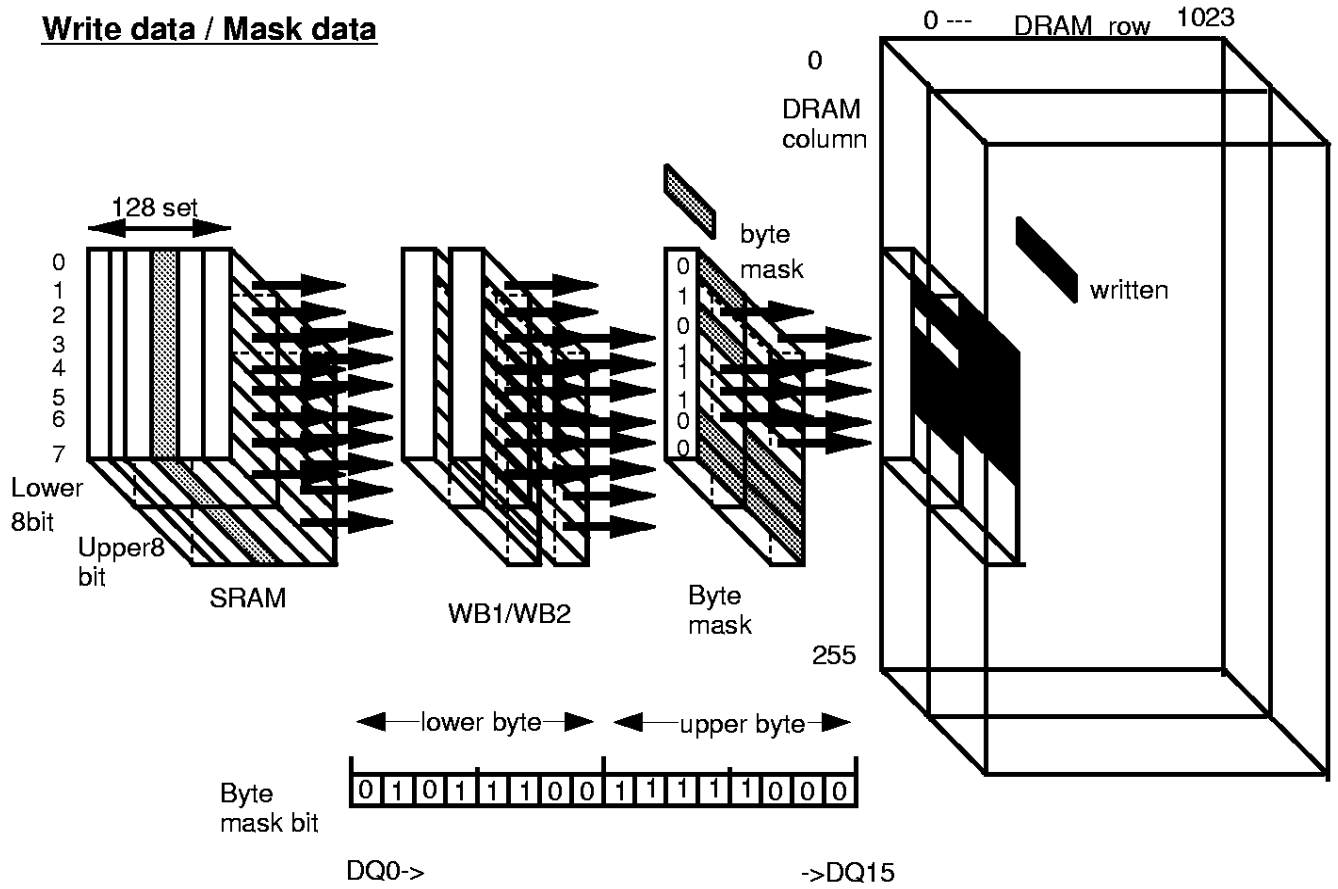


0 : mask, no write

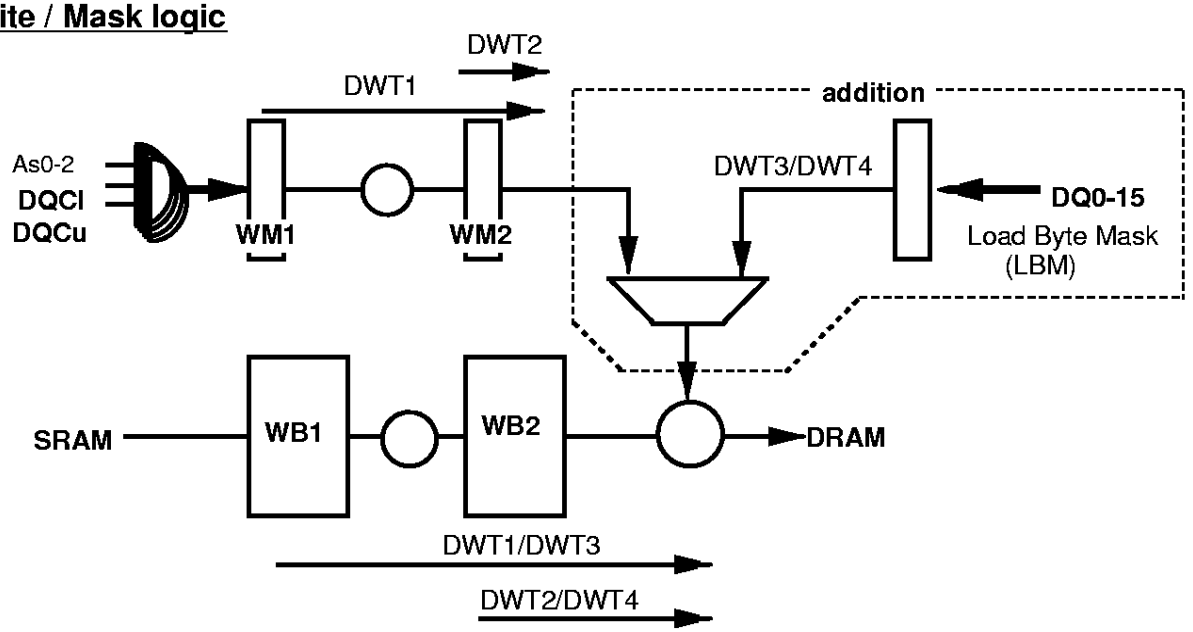
1 : unmask, write enable

DWT3 / DWT4

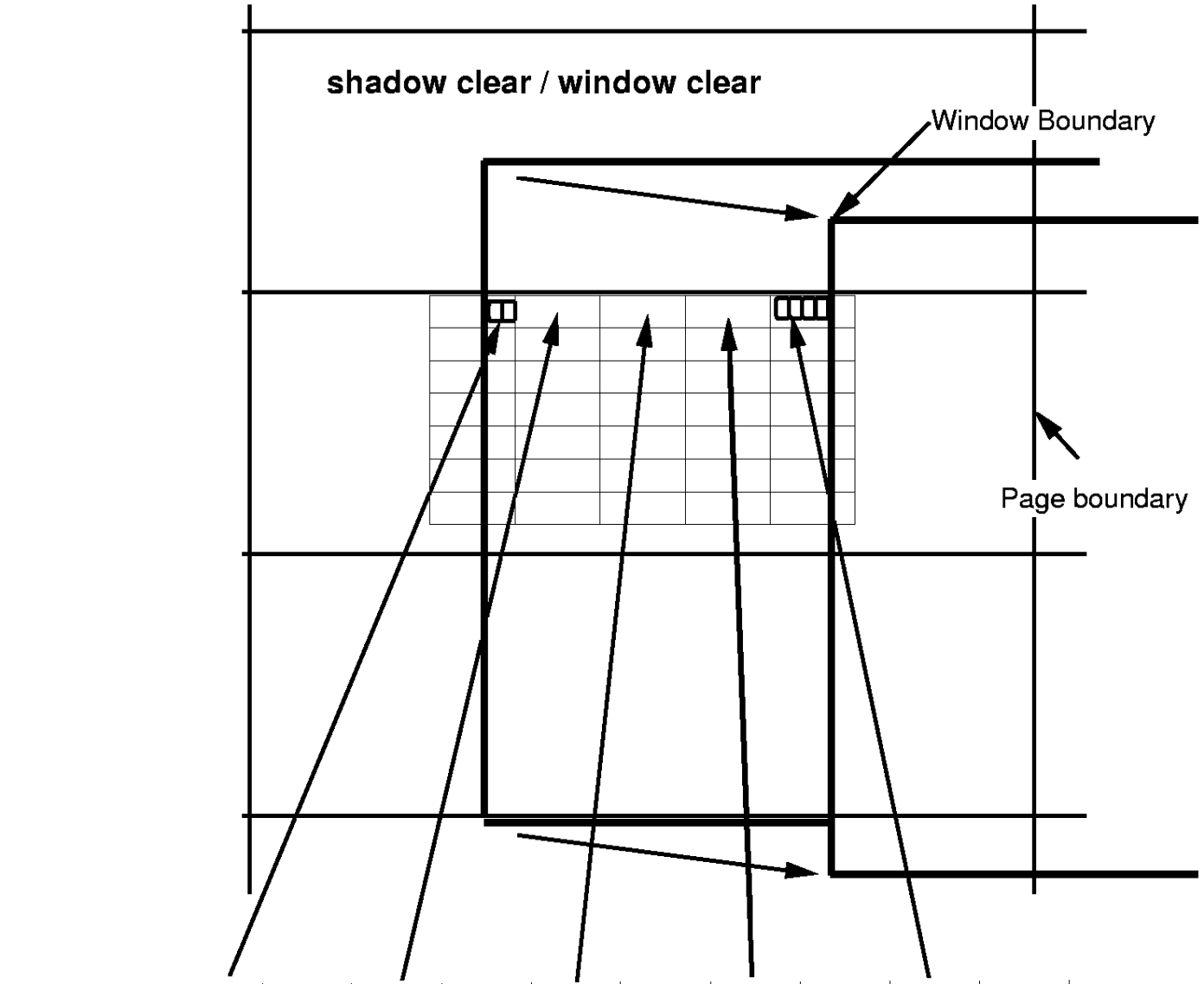
Write data / Mask data



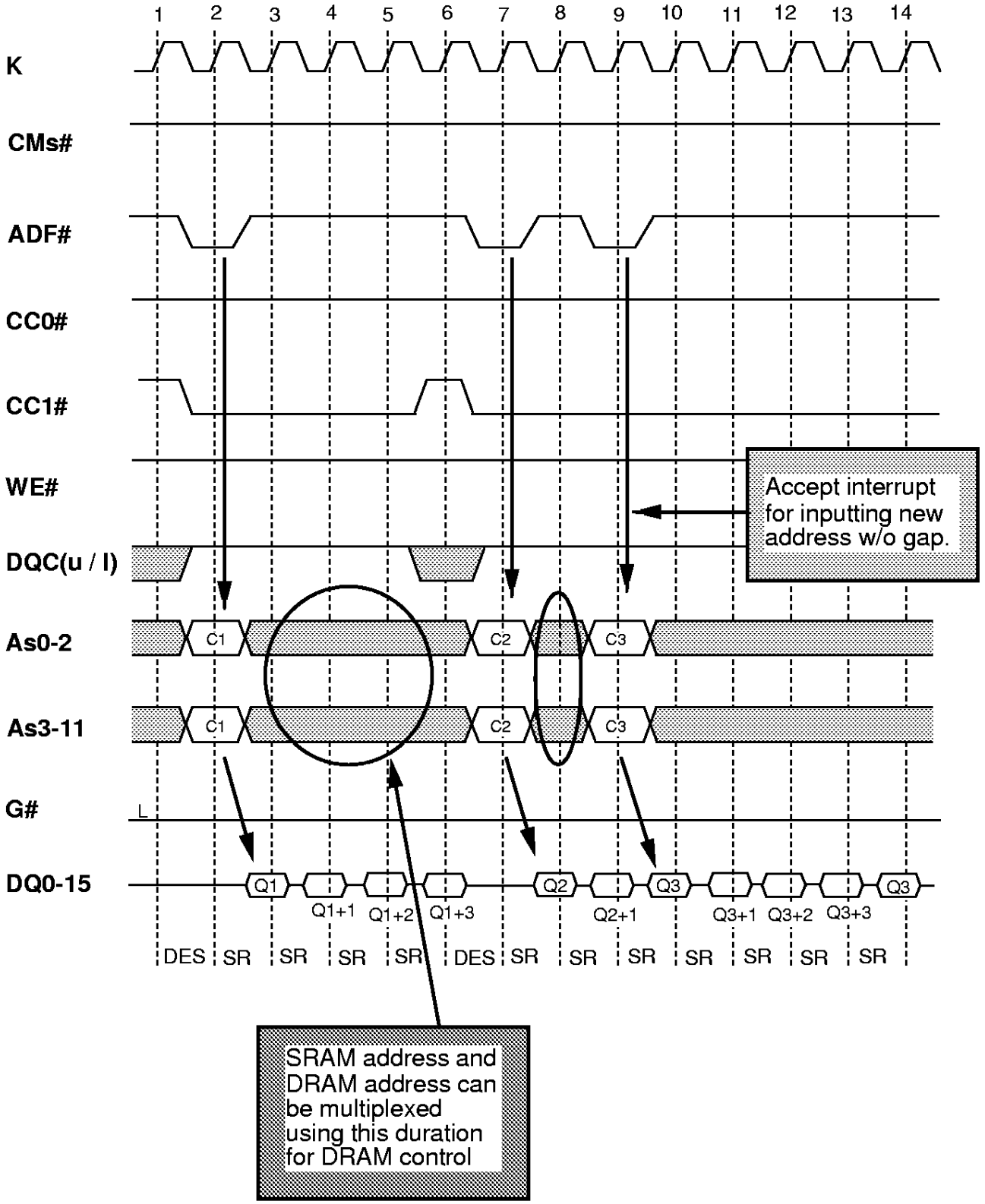
Write / Mask logic



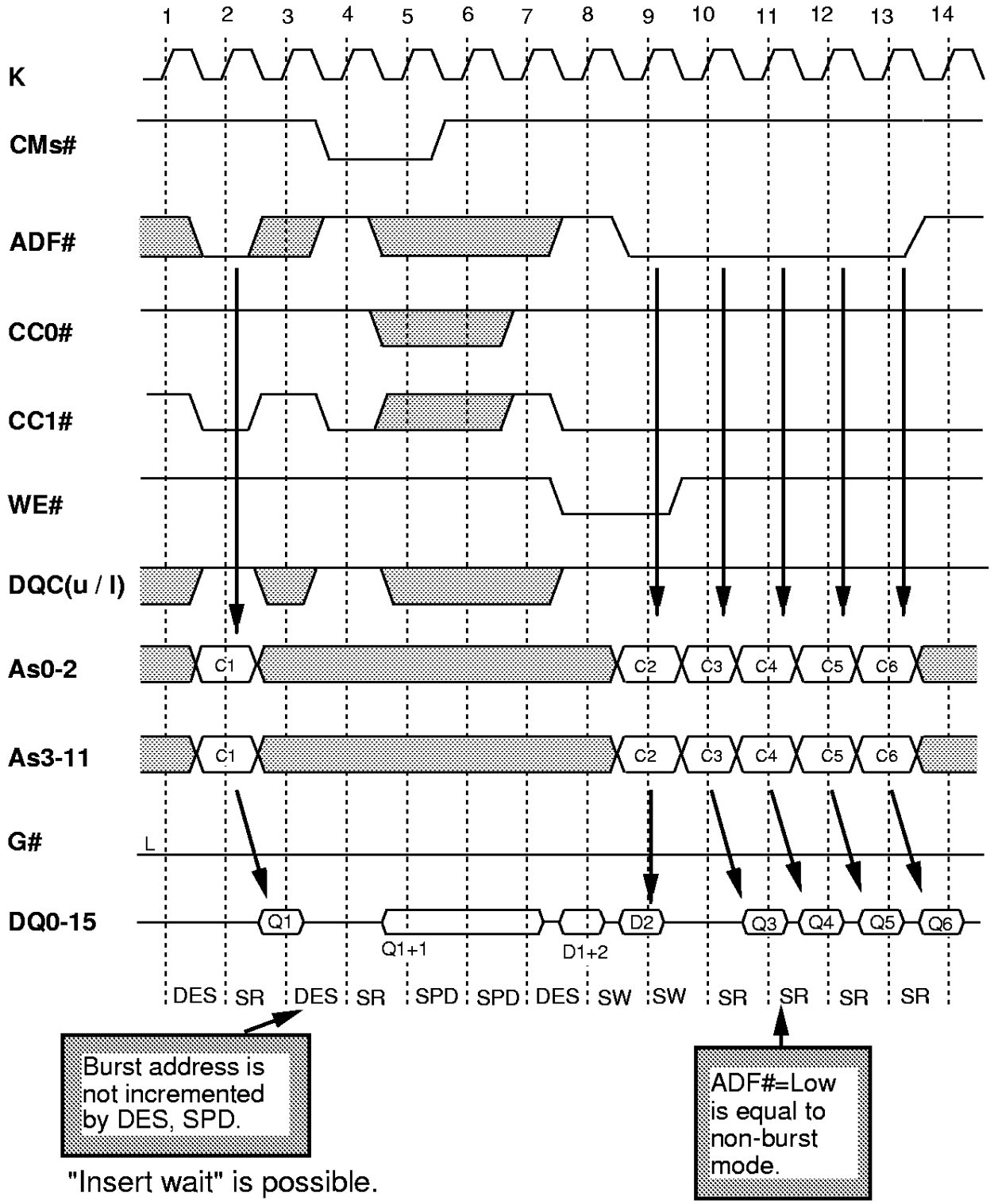
DWT3-DWT4 for Window clear(Block Write)



Burst Mode (1)


1 2 3 4 5 6 7 8 9 10 11 12 13 14
K
CMs#
ADF#
CC0#
CC1#
WE#
DQC(u / l)
As0-2
As3-11
G#
DQ0-15
L
C1
C2
C3
Q1
Q1+1
Q1+2
Q1+3
Q2
Q2+1
Q3
Q3+1
Q3+2
Q3+3
DES SR SR SR SR DES SR SR SR SR SR SR SR
Accept interrupt for inputting new address w/o gap.
SRAM address and DRAM address can be multiplexed using this duration for DRAM control

Burst Mode (2)



"Insert wait" is possible.

M5M4V16169D keeps compatibility setting ADF# low or setting Burst length=1 by SCR cycle. (Ad7, Ad8 and Ad9=0)

**-15 spec is the same as M5M4V16169TP/RT-15

ABSOLUTE MAXIMUM RATINGS

(Ta=0~70°C , Vdd=3.3±0.3V for -8,and -10, Vdd=3.3±0.15V for -7
Vss=0V, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply Voltage	With respect to Vss	-0.5 ~ 4.6	V
V_I	Input Voltage		-0.5 ~ 4.6	V
VO	Output Voltage		-0.5 ~ 4.6	V
IO	Output Current		50	mA
Pd	Power Dissipation		1000	mW
Topr	Operating Temperature		0 ~ 70	°C
Tstg	Storage Temperature		-65 ~ 150	°C

RECOMMENDED OPERATING CONDITIONS

(Ta=0~70°C , Vdd=3.3±0.3V for -8,and -10, Vdd=3.3±0.15V for -7
Vss=0V, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max	
Vcc	Supply Voltage	3.0	3.3	3.6	V
Vss	Supply Voltage	0	0	0	V
VccQ	Supply Voltage for Output	3.0	3.3	3.6	V
VIH (LVTTL)	High-level Input Voltage clock and add.	2.0		Vdd+0.3	V
VIH (LVTTL)	High-level Input Voltage master clock (K)	2.2		Vdd+0.3	V
VIH (LVTTL)	High-level Input Voltage data pin	2.0		VddQ+0.3	V
VIL (LVTTL)	Low-level Input Voltage all inputs	-0.3		0.8	V

CAPACITANCE

(Ta=0~70°C , Vdd=3.3±0.3V for -8,and -10, Vdd=3.3±0.15V for -7
Vss=0V, unless otherwise noted)

Symbol	Parameter	Test Condition	Limits (MAX)	Unit
CI(A)	Input Capacitance, Address pin	VI=Vss f=1MHz V_I =25mVrms	5	pF
CI(C)	Input Capacitance, Clock pin		5	pF
CI/O	Input Capacitance, I/O pin		7	pF

**-15 spec is the same as M5M4V16169TP/RT-15

AVERAGE SUPPLY CURRENT from Vcc

(Ta=0~70°C , Vdd=3.3±0.3V for -8,and -10, Vdd=3.3±0.15V for -7
Vss=0V, unless otherwise noted)

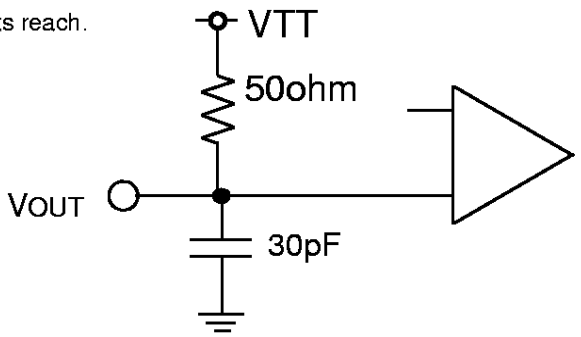
Symbol	Condition	Limits (MAX)				Unit
		-7	-8	-10	-15	
IccS	Average supply current of SRAM operating, tK=min. DRAM=DPD output open data input=H or L	260	240	200	140	mA
IccD	Average supply current of DRAM operating, tRC=min. SRAM=SPD	160	150	130	100	mA
IccD(PG)	Average supply current of DRAM page-mode tPC=min. SRAM=SPD	140	130	110	80	mA
Icc(STN1)	LVTTL standby, tK=min, DRAM=DNOP&SRAM=DES, or NOP all input=stable. output open data input=H or L	60	60	50	30	mA
Icc(STN2)	CMOS standby, tK=min, DRAM=DNOP&SRAM+DES, or NOP all input=stable. output open data input=H or L	50	50	40	25	mA
Icc(PD)	CMOS Power Down current, CMd#=CMs#=L,tK=min.	5	5	5	5	mA
Icc(SRF)	CMOS Self Refresh current, CMd#=CMs#=L,tK=∞	1	1	1	1	mA

AC OPERATING CONDITIONS AND CHARACTERISTICS

(Ta=0~70°C , Vdd=3.3±0.3V for -8,and -10, Vdd=3.3±0.15V for -7
Vss=0V, unless otherwise noted)

Symbol	Parameter	Test Condition	Limits		Unit
			Min.	Max	
VOH(DC)*(LVTTL)	High-level Output Voltage (DC)	IOH= -2mA	2.4	-	V
VOL(DC)*(LVTTL)	Low-level Output Voltage (DC)	IOL= 2mA	-	0.4	V
IOZ	Off-state Output Current	Q floating V_O=0 ~VddQ	-10	10	uA
II	Input Current	V_{IH}=0 ~ VddQ+0.3V	-10	10	uA

* VOH(AC) and VOL(AC) are the reference levels for AC measurements.
VOH(DC) and VOL(DC) are the final levels the outputs reach.



AC Condition
(Access Time)

**-15 spec is the same as M5M4V16169TP/RT-15

TIMING REQUIREMENTS (CLK pulse, input signals setup / hold time to CLK edge)

(Ta=0~70°C , Vdd=3.3±0.3V for -8,and -10, Vdd=3.3±0.15V for -7
Vss=0V, unless otherwise noted)

Input Pulse Levels: VIH=3.0V,VIL=0.0V (LVTTL)
Input Timing Measurement Reference Level: 1.5V (LVTTL)

Symbol	Parameter	Limits								Unit
		-7		-8		-10		-15		
		Min.	Max	Min.	Max	Min.	Max	Min.	Max	
tK	**Clock Cycle Time**	**7**		8		10		15		ns
tKH	Clock High Pulse Width	3		3		3.5		5		ns
tKL	Clock Low Pulse Width	3		3		4		5		ns
tS	**Setup Time for Inputs**	**3**		3		3		4		ns
tH	**Hold Time for Inputs**	**1**		1		1		1		ns

**-15 spec is the same as M5M4V16169TP/RT-15

TIMING REQUIREMENTS (Read, Write, Refresh)

(Ta=0~70°C , Vdd=3.3±0.3V for -8,and -10, Vdd=3.3±0.15V for -7
Vss=0V, unless otherwise noted)

Input Pulse Levels: VIH=3.0V,VIL=0.0V (LVTTL)

Input Timing Measurement Reference Level: 1.5V (LVTTL)

Symbol	Parameter	Limits								Unit
		-7		-8		-10		-15		
		Min.	Max	Min.	Max	Min.	Max	Min.	Max	
tREF	Refresh Cycle Time		64		64		64		64	ms
tRP	Precharge Time	**21**		24		30		40		ns
tRCD	Delay Time, Add Strb. Row to Col.	**21**		24		30		30		ns
tRC*	DRAM Activate-Read Cycle Time	**70**		80		90		120		ns
tWC*	DRAM Activate-Write Cycle Time	**70**		80		90		120		ns
tPC	Page Cycle Time	**14**		16		20		30		ns
tRAS	Activate Time	**49**	10,000	56	10,000	60	10,000	70	12,000	ns
tRASP	Page mode Activate Time	**49**	100,000	56	100,000	60	100,000	70	100,000	ns
tRWL	Write to Precharge Lead Time	**14**		16		20		20		ns
tRSH	Read to Precharge Hold Time	**14**		16		20		20		ns

*Note: When tRP and tRAS = Min. values, tRC and tWC = tRP + tRAS.

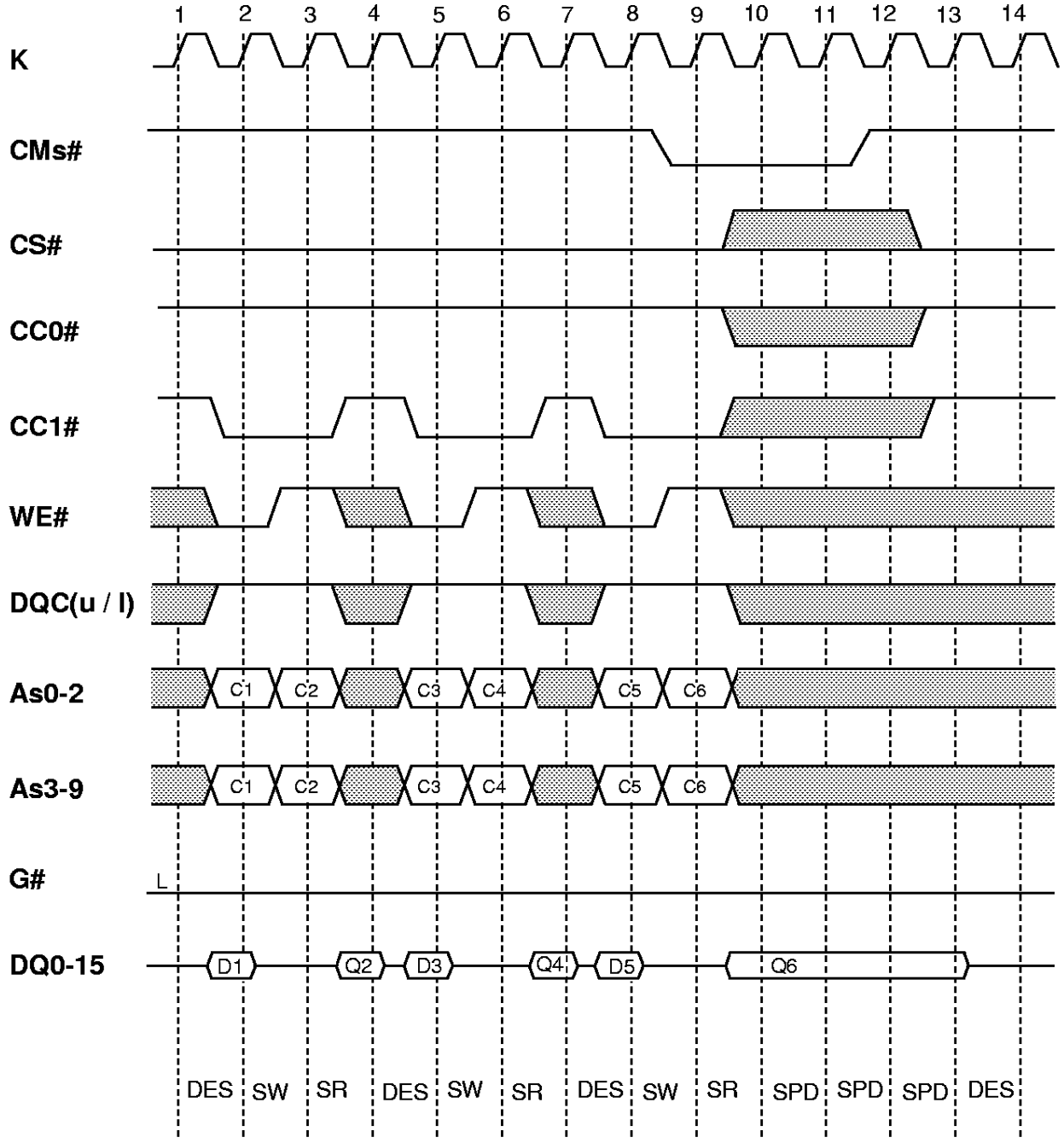
**-15 spec is the same as M5M4V16169TP/RT-15

SWITCHING CHARACTERISTICS

(Ta=0~70°C , Vdd=3.3±0.3V for -8,and -10, Vdd=3.3±0.15V for -7
Vss=0V, unless otherwise noted)

Symbol	Parameter	Limits								Unit
		-7		-8		-10		-15		
		Min.	Max	Min.	Max	Min.	Max	Min.	Max	
tCBF	**Buffer-Fill from DRAM Read Transfer**		**20**		**20**		**20**		**20**	ns
tKHA	Access Time from K-High Edge						10		15	ns
tKHQX	Output Active Time from K-High Edge					2		3		ns
tKHQZ	Output Disable Time from K-High Edge					2	10	3	5	ns
tKHAR	Access Time from K-High Edge		**5.6**		**6.4**		**7**	**12**		ns
tKHQXR	Output Active Time from K-High Edge	2		2		2		3		ns
tKHQZR	Output Disable Time from K-High Edge	2	7	2	8	2	10	3		ns
tGLA	Access Time from G#-Low Edge		5.6		6.4		7			ns
tGLQ	Output Active Time from G#-Low Edge	0		0		0				ns
tGHQ	Output Disable Time from G#-High Edge	2	5.6	2	6.4	2	8			ns

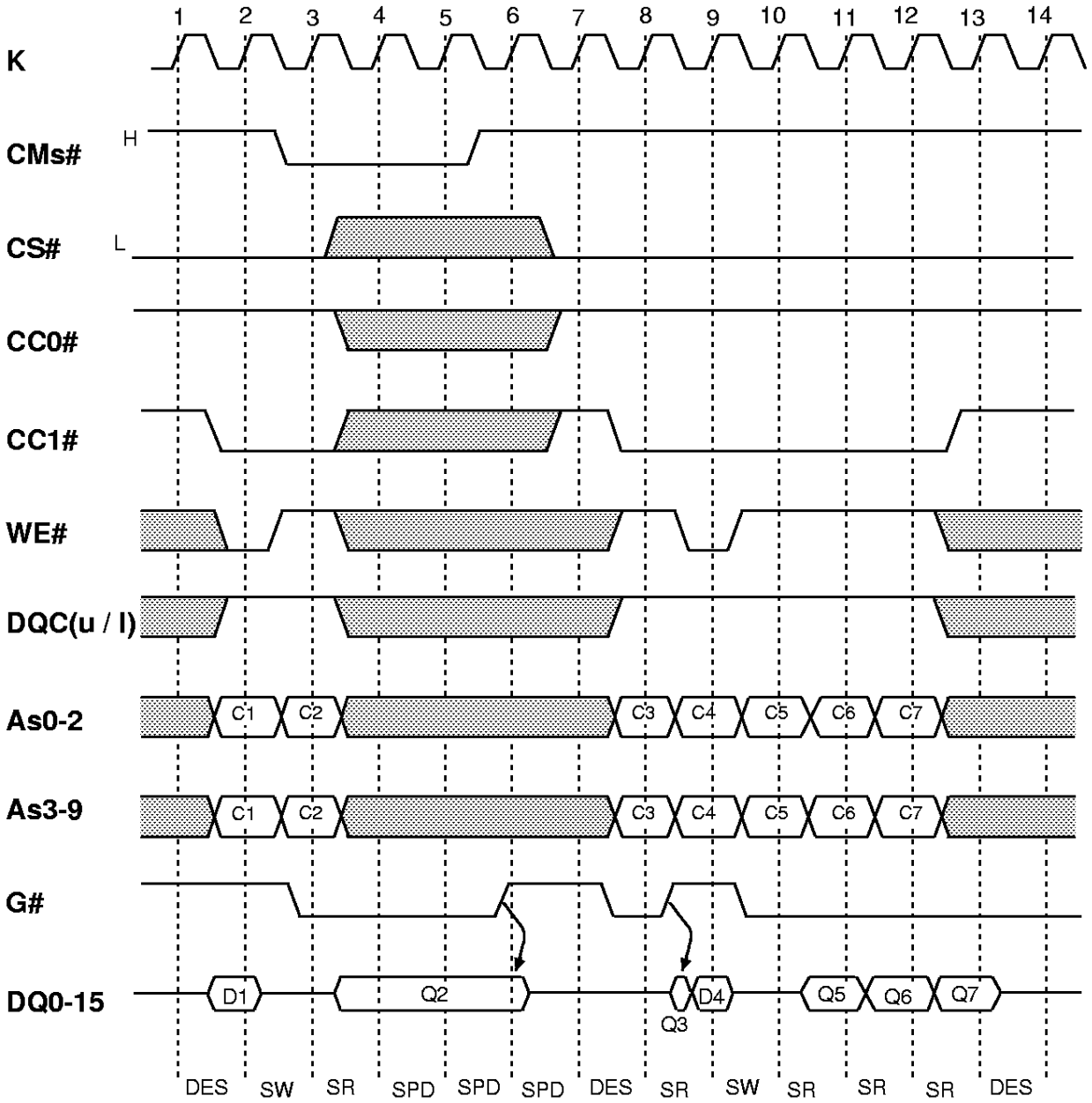
non-G# controlled Write & Read (DES control)
(SRAM Read/Deselect SRAM/SRAM Write/SRAM Power-down)



Note : Output is transparent. DRAM operation can be freely performed.

G# controlled Write & Read

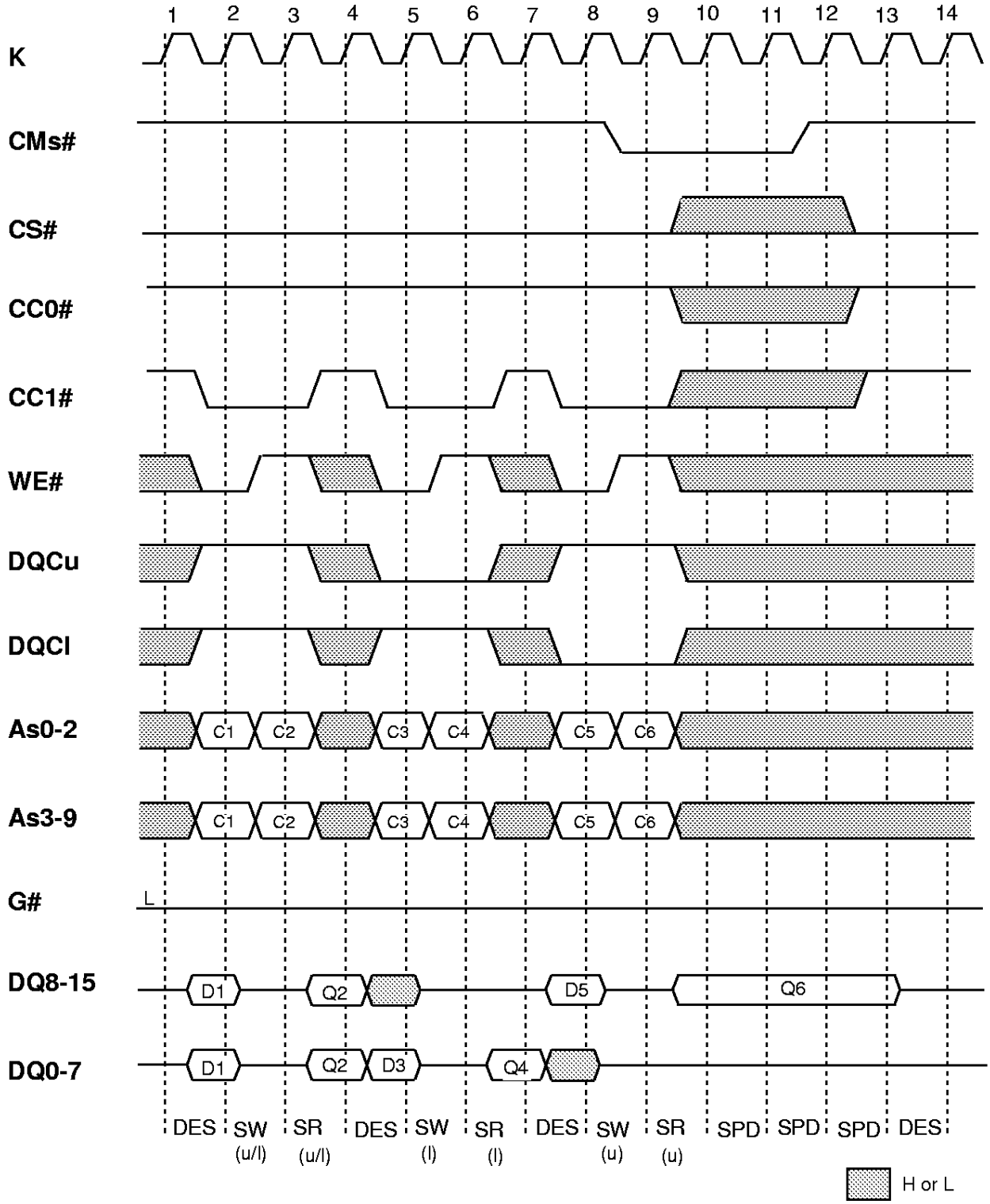
(SRAM Read/Deselect SRAM/SRAM Write/SRAM Power-down)



Note : Output is transparent. DRAM operation can be freely performed.

DQC controlled Write & Read

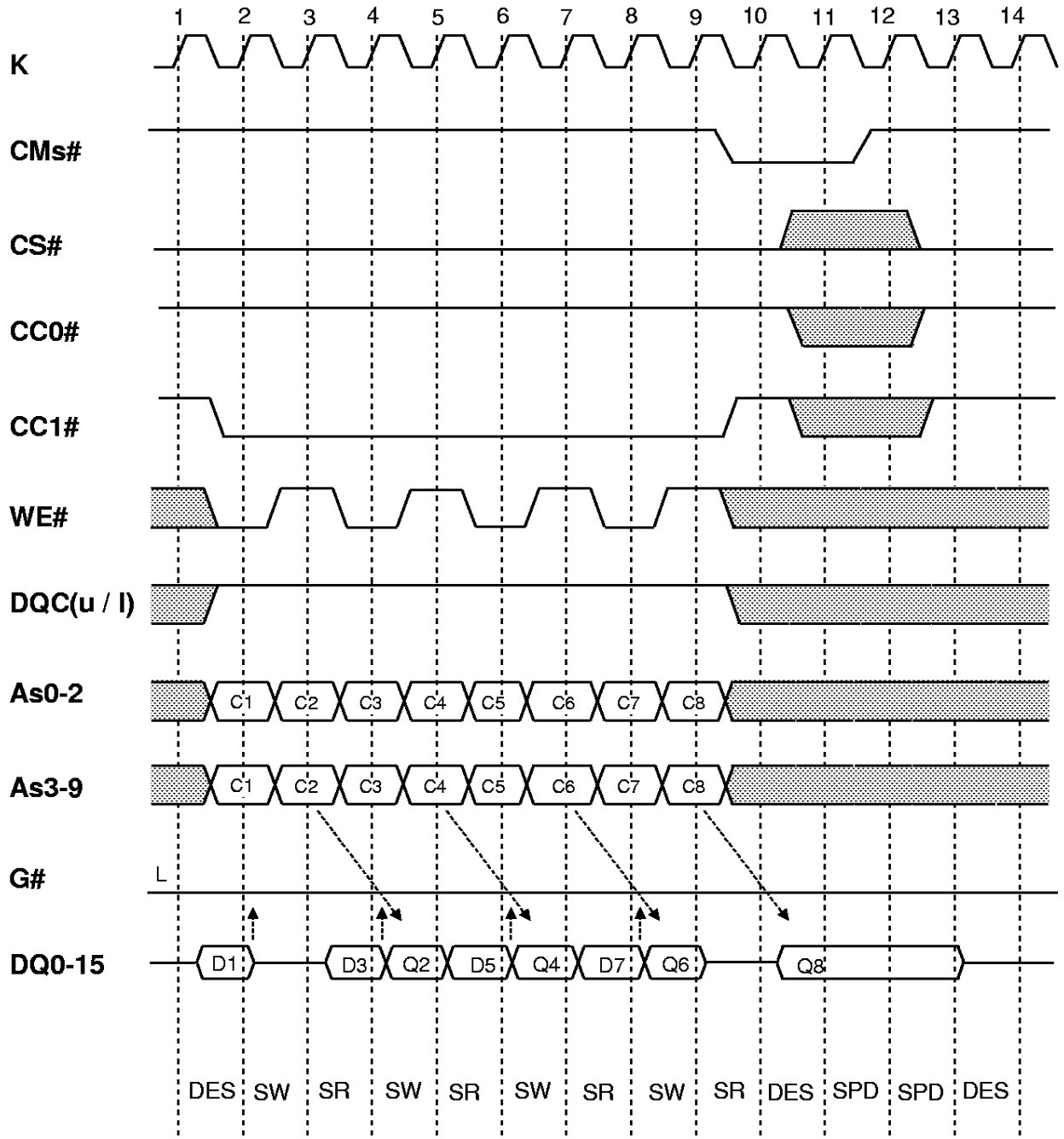
(SRAM Read/Deselect SRAM/SRAM Write/SRAM Power-down)



Note : Output is transparent. DRAM operation can be freely performed.

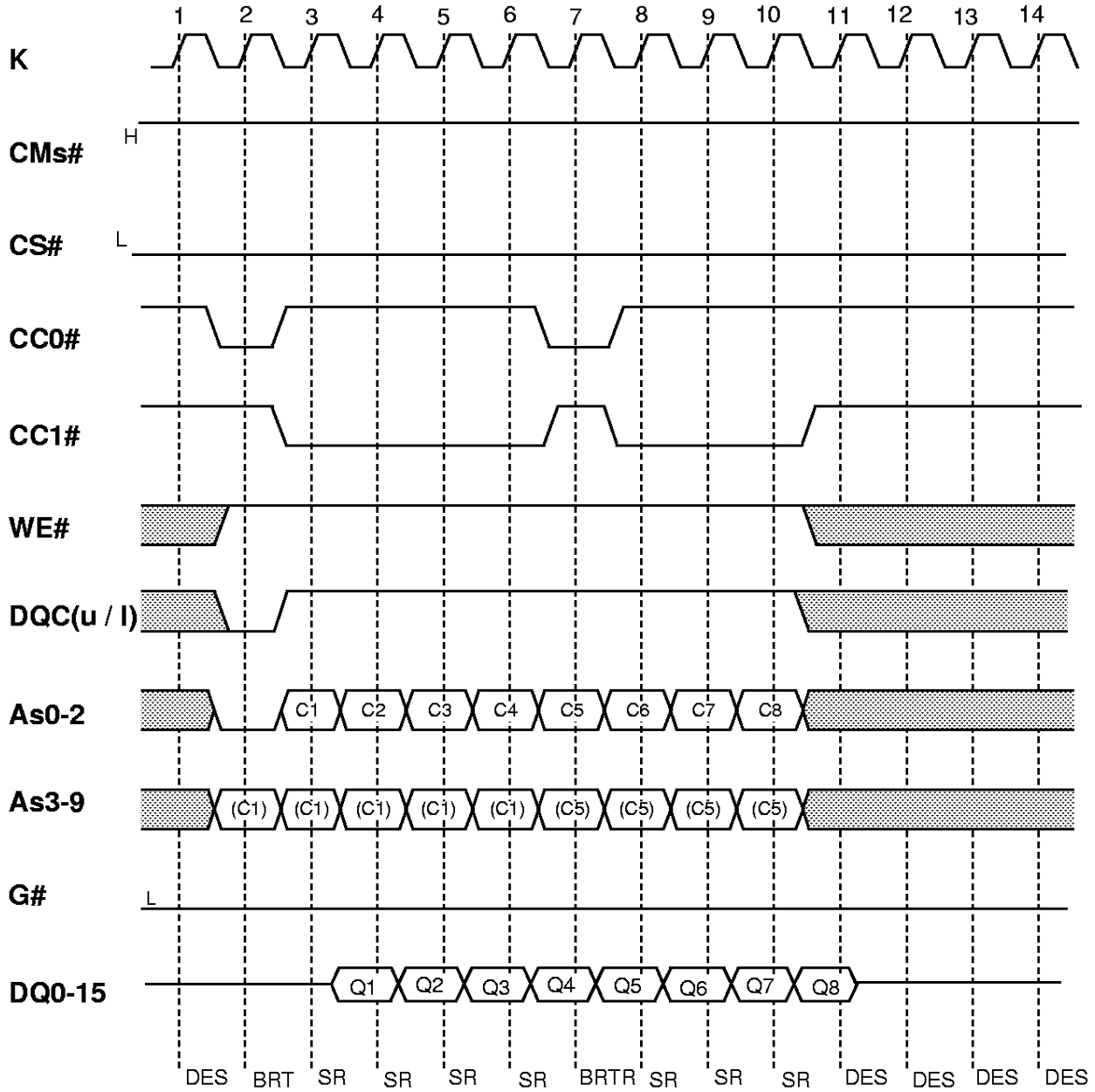
Registered Output control

(SRAM Read/Deselect SRAM/SRAM Write/SRAM Power-down)



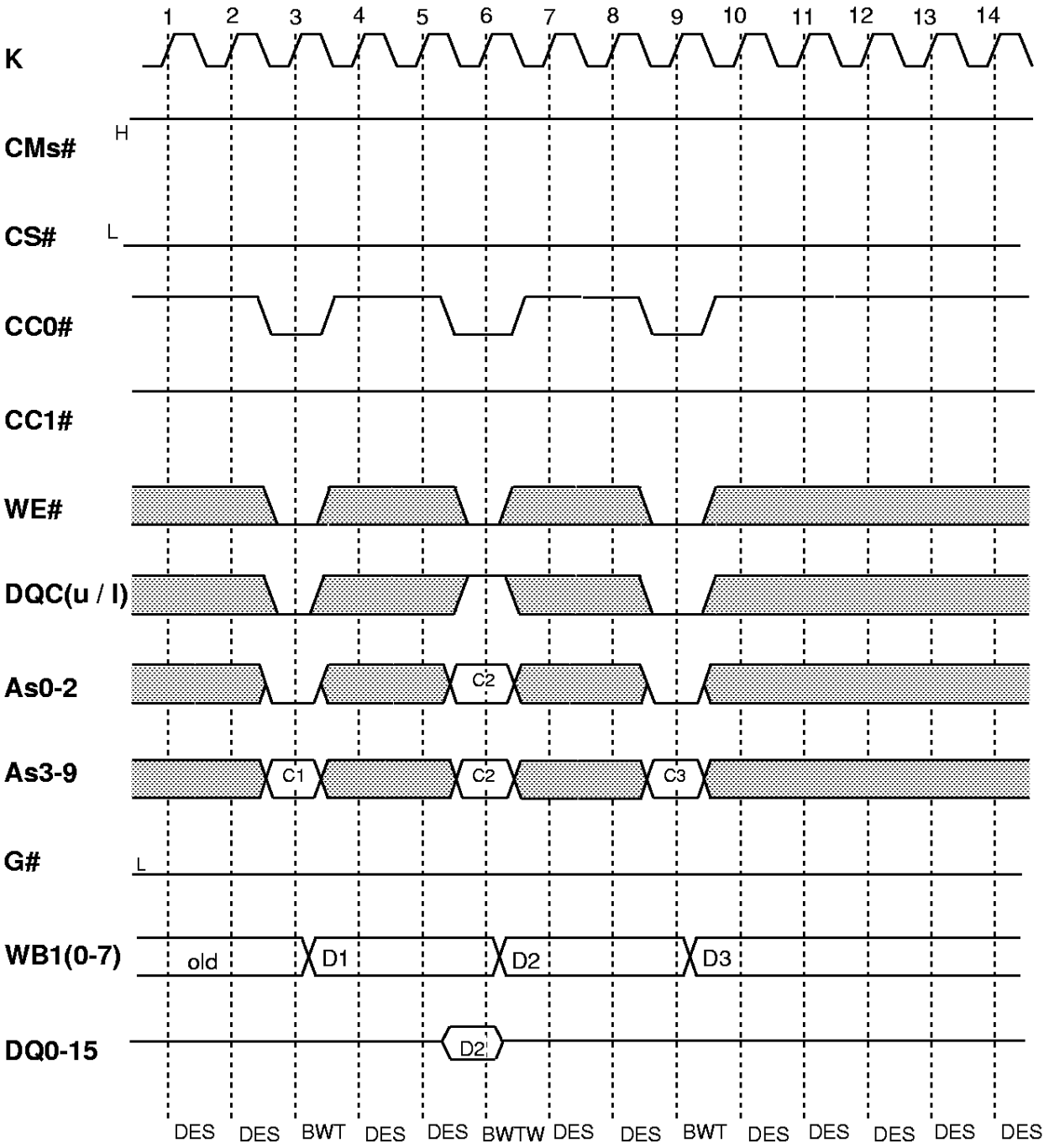
Note : Output is registered. DRAM operation can be freely performed.

Buffer Read Transfer (RB2 -> SRAM)
Buffer Read Transfer & SRAM Read (RB2 -> SRAM -> Output)



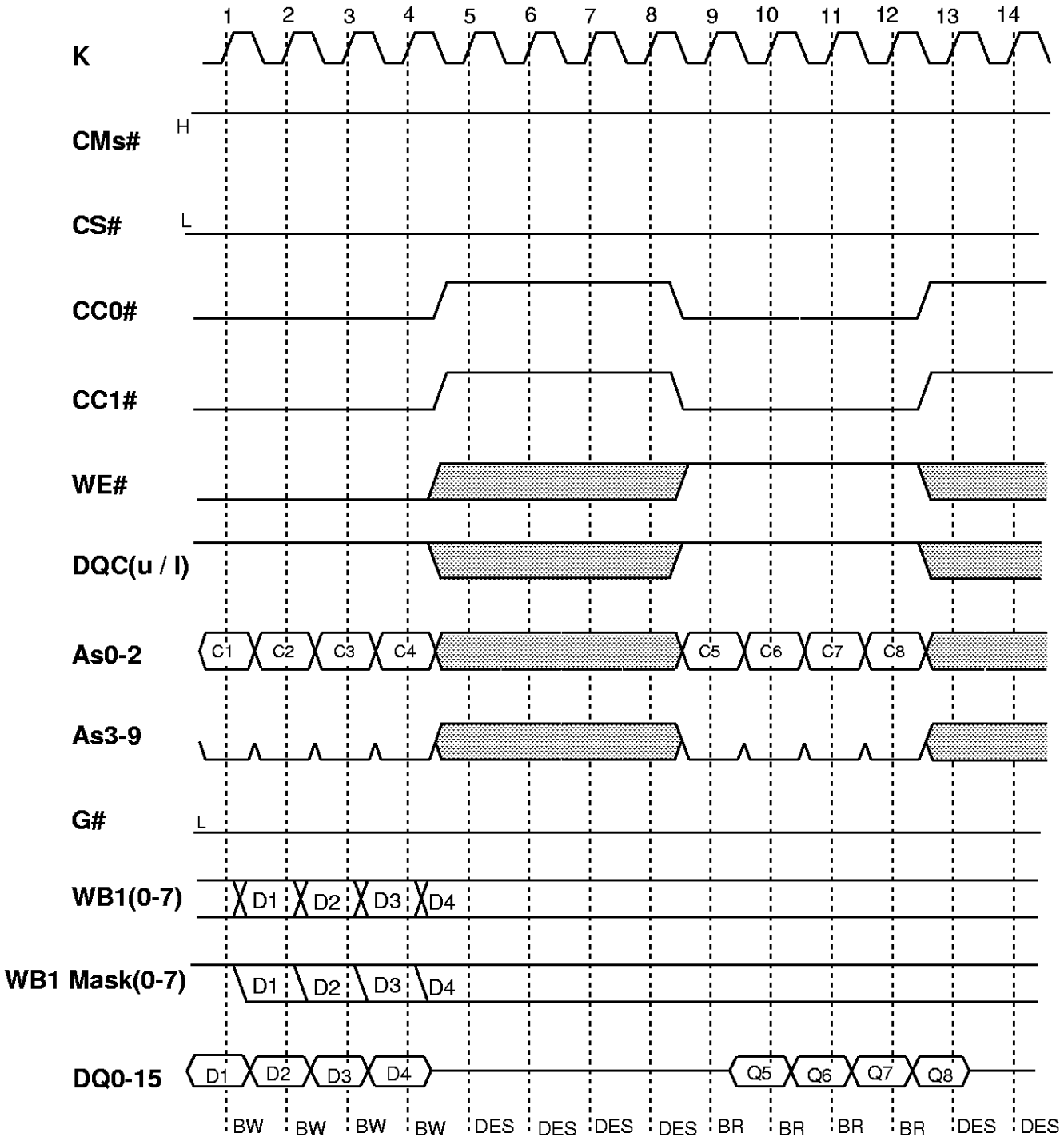
Note : Output is transparent. DRAM operation can be freely performed.

Buffer Write Transfer (SRAM -> WB1)
Buffer Write Transfer & SRAM Write (Input -> SRAM -> WB1)



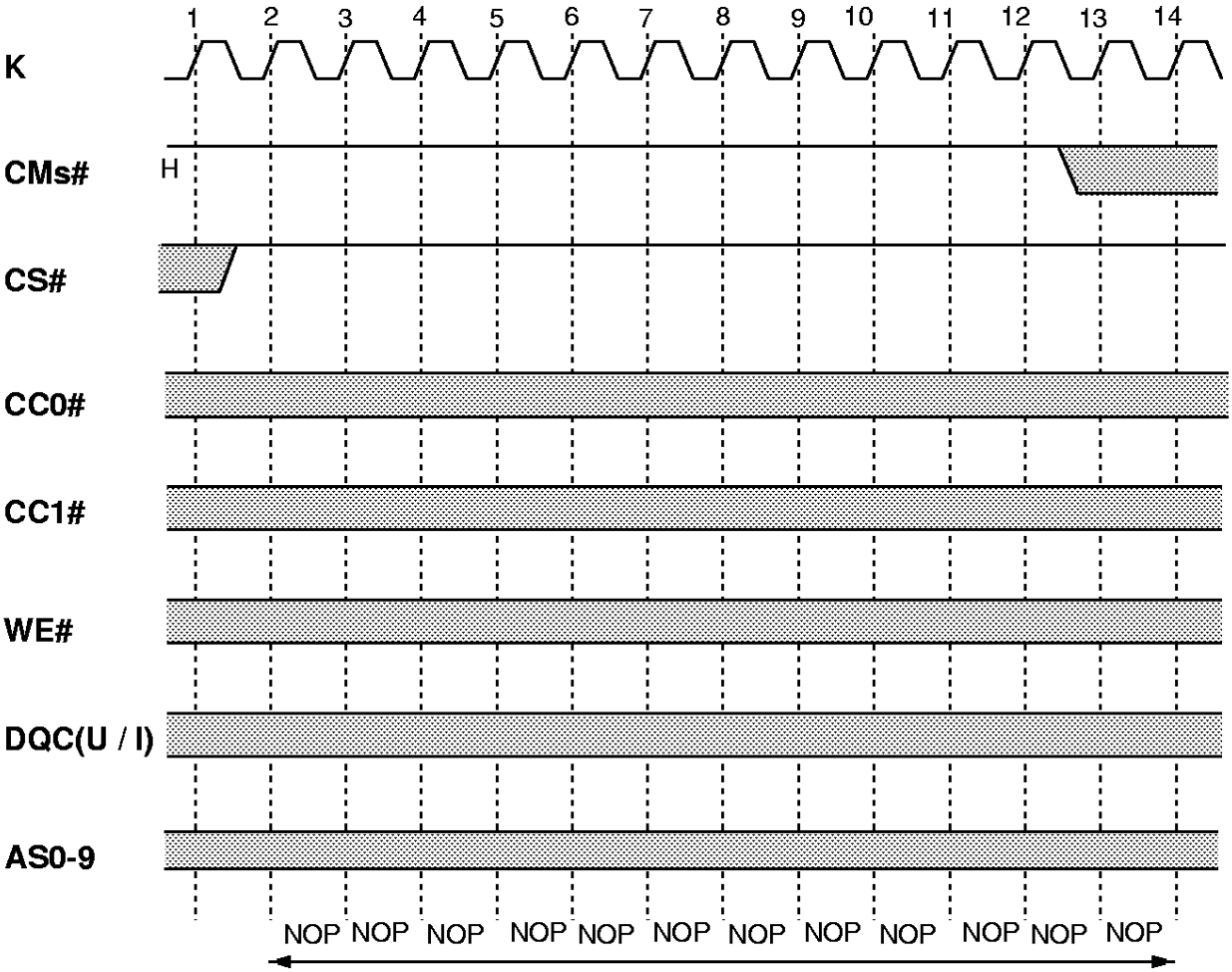
Note : Output is transparent. DRAM operation can be freely performed.

Buffer Write (Input -> WB1)
Buffer Read (RB2 -> Output)



Note : Output is transparent. DRAM operation can be freely performed.

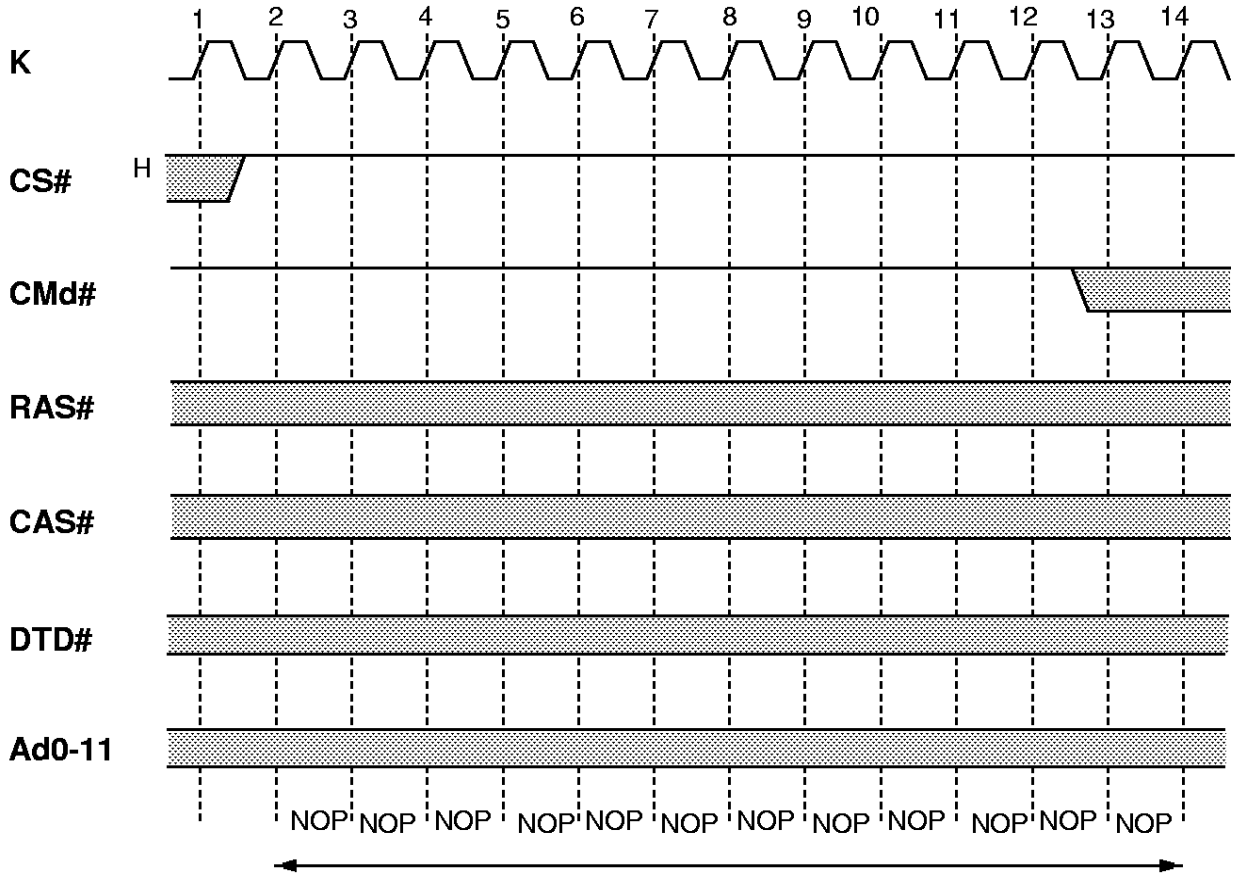
NO - Operation of SRAM



CMd#
RAS#
CAS#
DTD#
Ad0-11

DRAM operation can be freely performed.

NO - Operation of DRAM

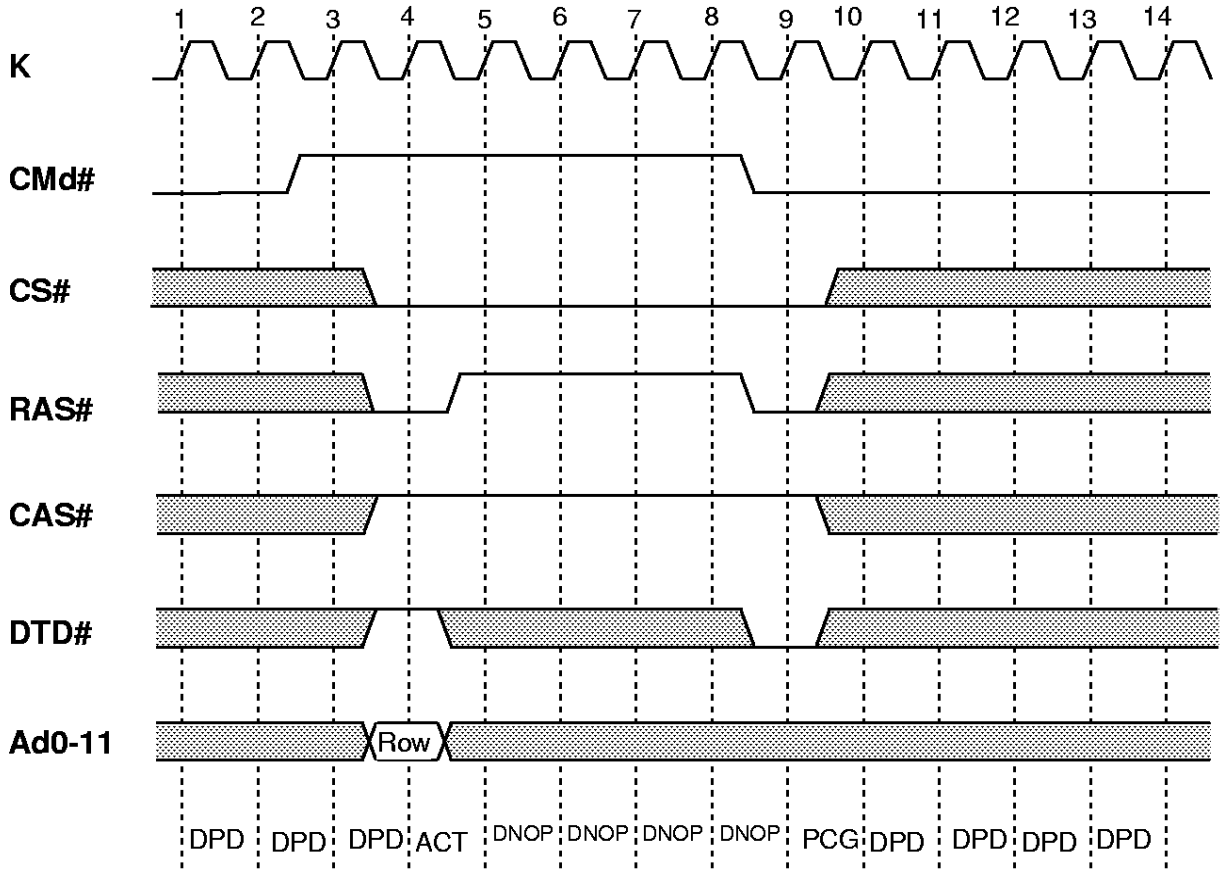


NO-Operation Mode

CMs#
CC0#
CC1#
WE#
DQC(u/l)
G#
As0-9
DQ0-15

SRAM operation can be freely performed.

DRAM Power Down / DRAM Activate / DRAM Precharge

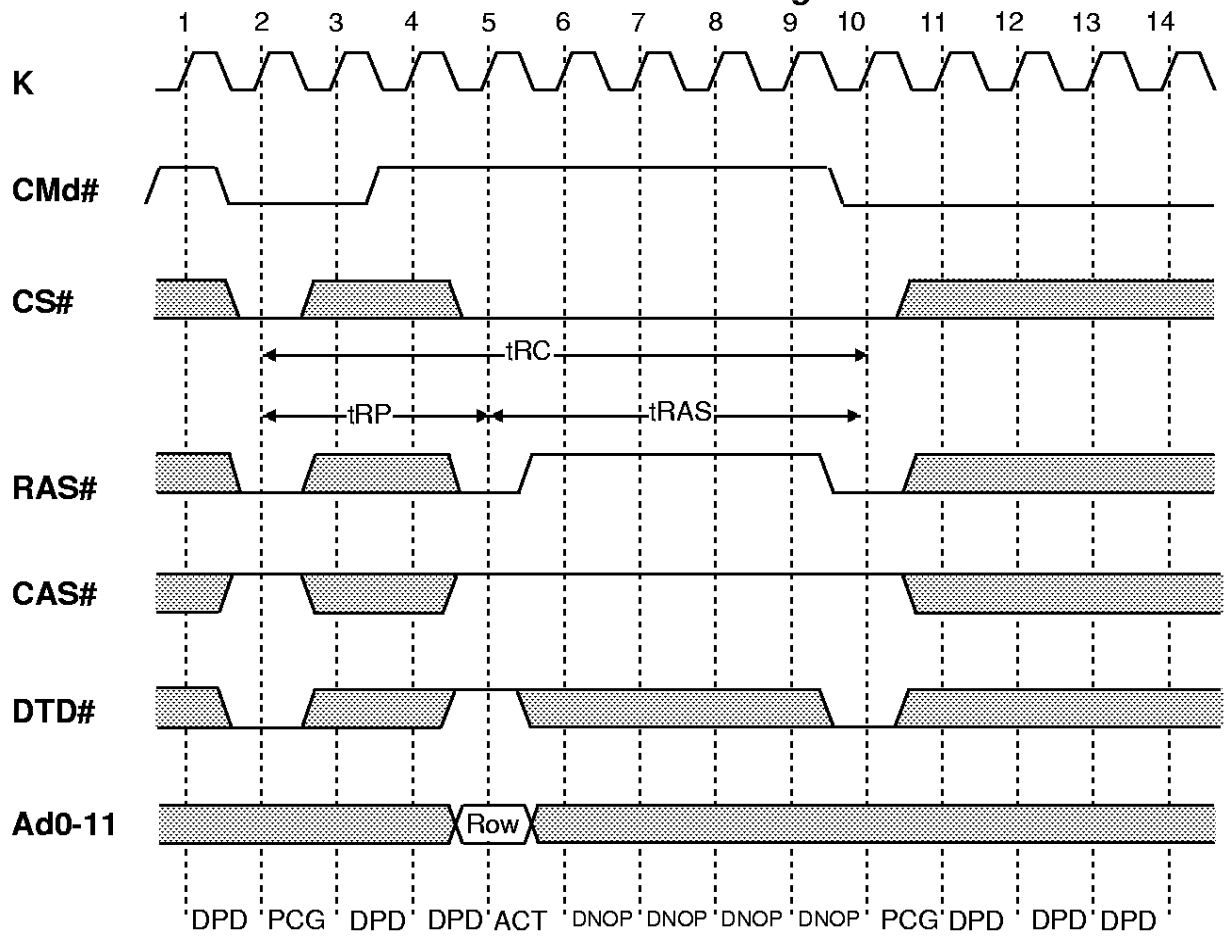


CMs#
CC0#
CC1#
WE#
DQC(u/l)
G#
As0-9
DQ0-15

SRAM operation can be freely performed.

DPD is recommended during no operation to save power.

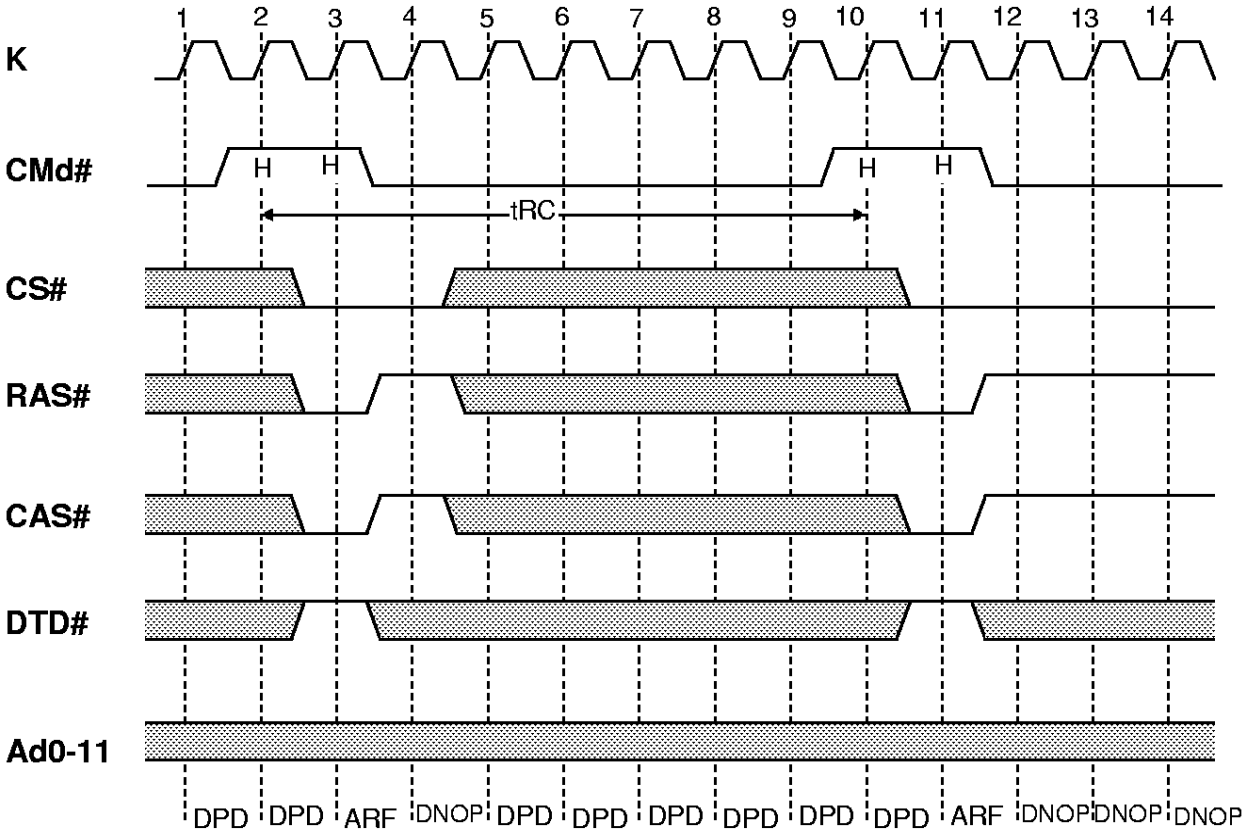
RAS only Refresh cycle
DRAM Power Down / DRAM Activate / DRAM Precharge



CMs#
CC0#
CC1#
WE#
DQC(u/l)
G#
As0-9
DQ0-15

SRAM operation can be freely performed.

DRAM Auto Refresh

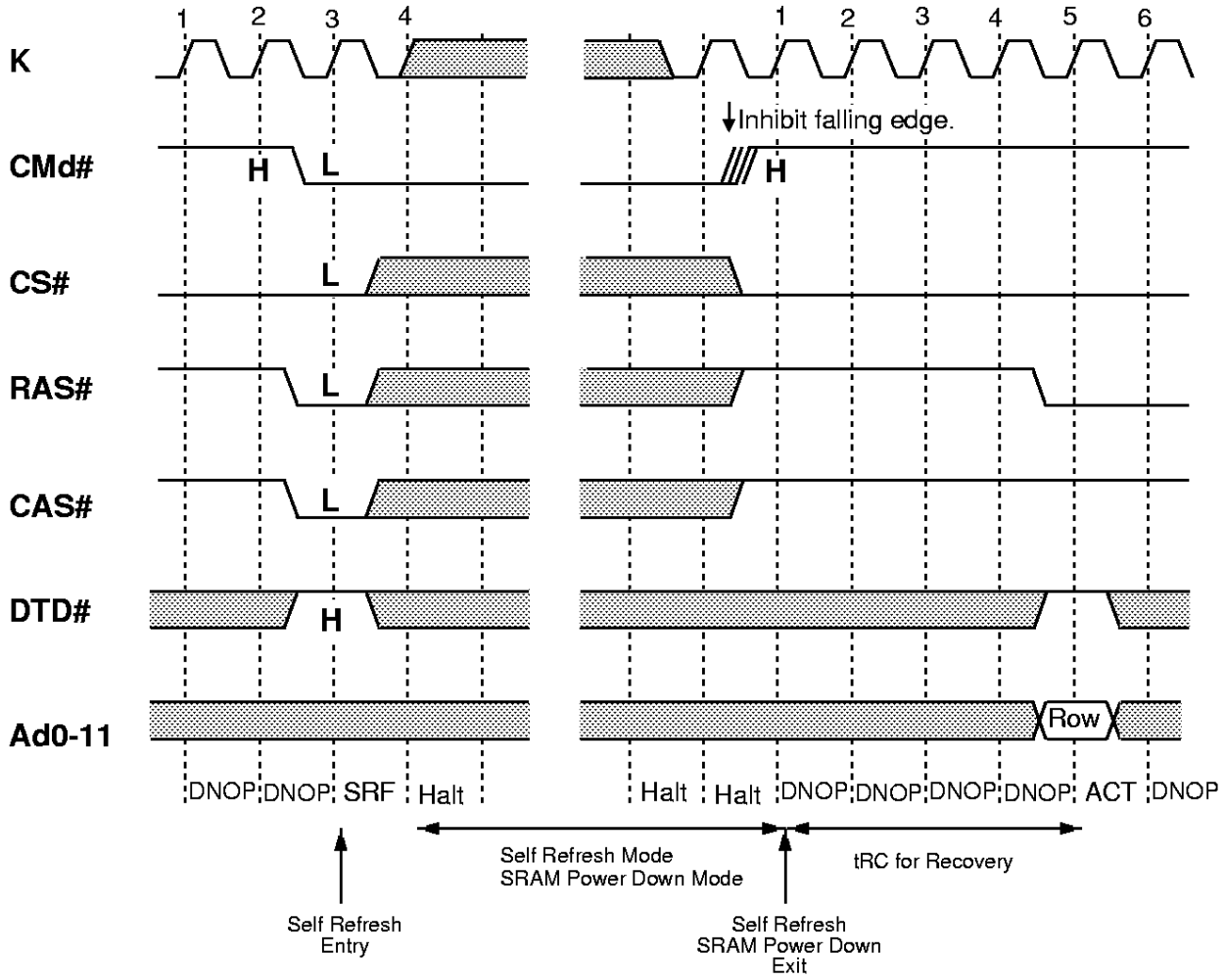


Note: DRAM must be in Precharge state prior to Auto-Refresh cycle.
DRAM new commands except for NOP,DNOP and DPD can be set after tRC later from ARF command input.

CMs#
CC0#
CC1#
WE#
DQC(u/l)
G#
As0-9
DQ0-15

SRAM operation can be freely performed.

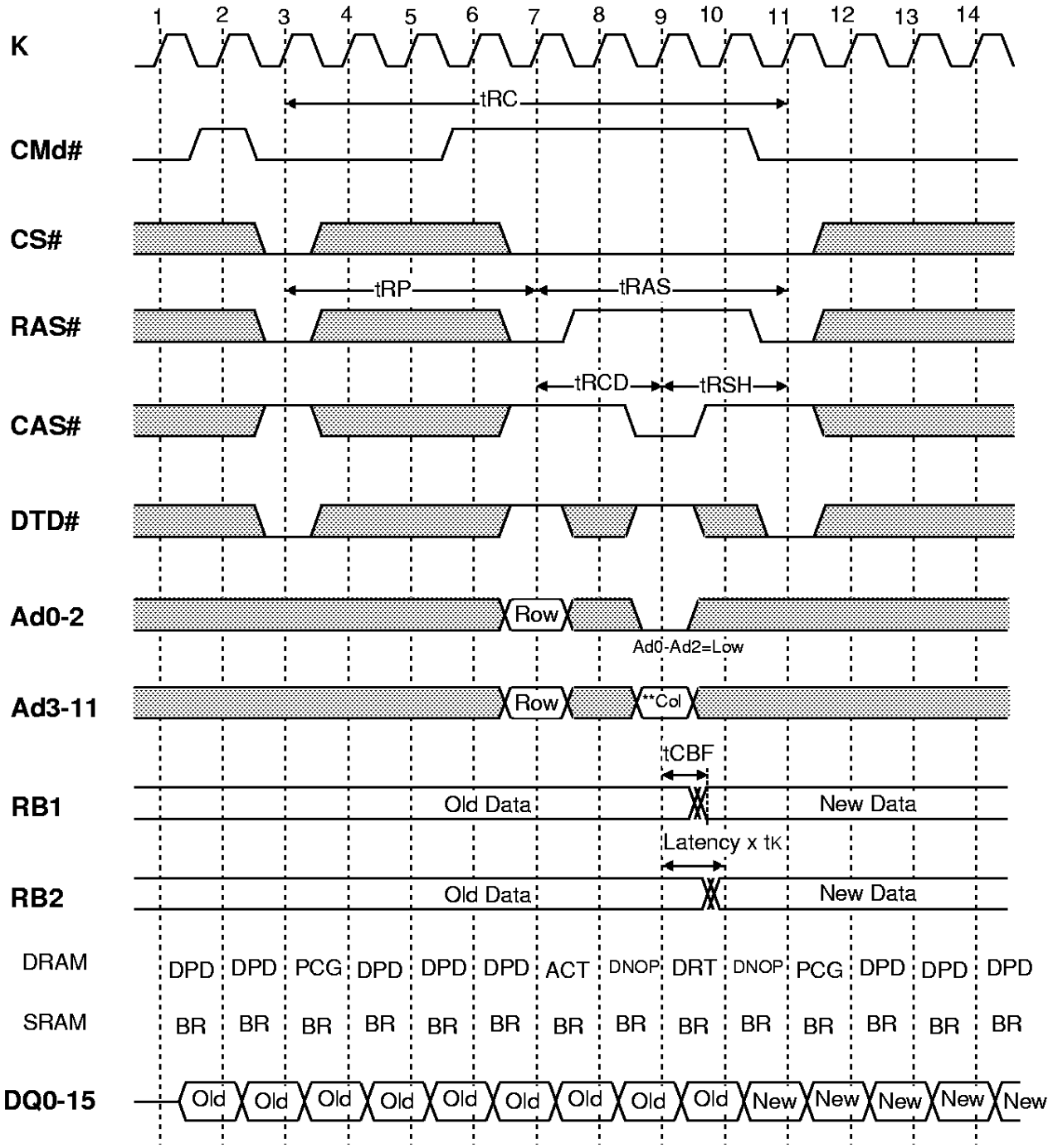
DRAM Self Refresh



Self Refresh Entry: (Note: DRAM must be in Precharge state prior to Self-Refresh Entry)
Previous CMd#=H, Present CMd#=L, CS#=RAS#=CAS#=L, DTD#=H
(CMd# must remain low to maintain Self Refresh).

Self Refresh Exit (in order):
a) resume K clock
b) CMd#=H
c) Wait tRC for recovery
d) Resume normal operation

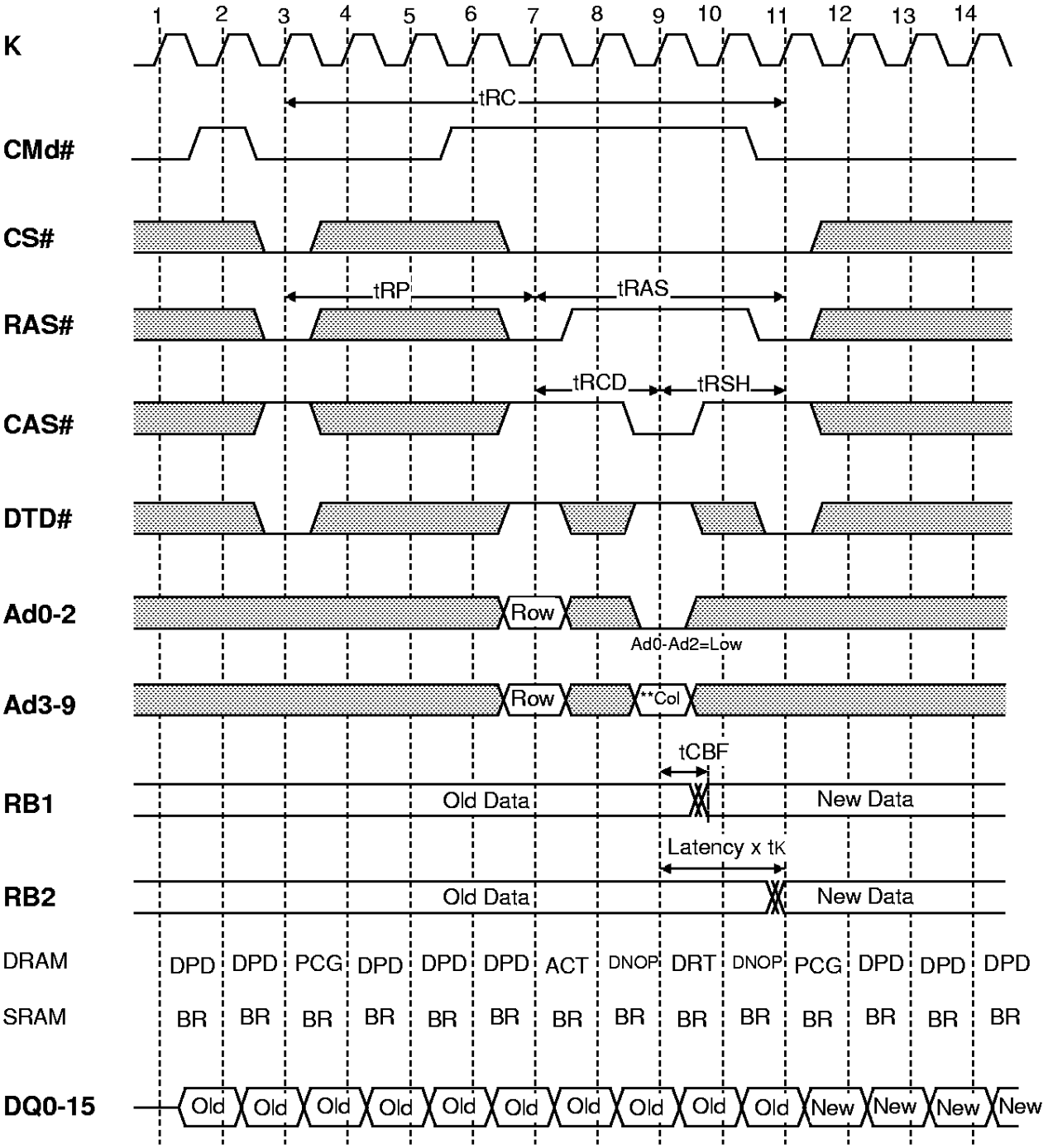
DRAM Read Transfer (DRAM -> RB1-> RB2) Latency set=1



SRAM operation can be freely performed.

** Ad3-Ad7 are column block addresses (Ad8~Ad11=Low).

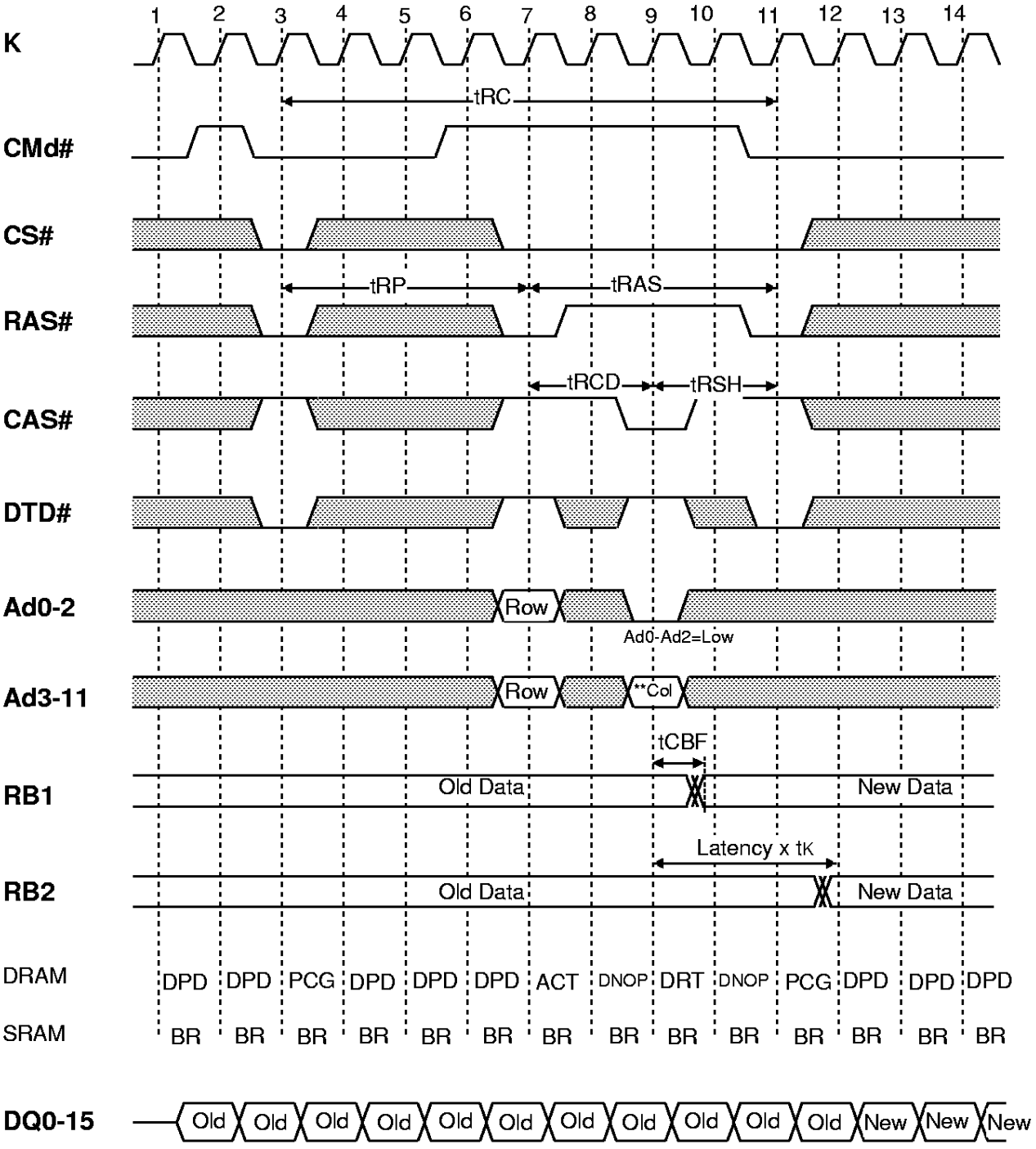
DRAM Read Transfer (DRAM -> RB1-> RB2) Latency set=2



SRAM operation can be freely performed.

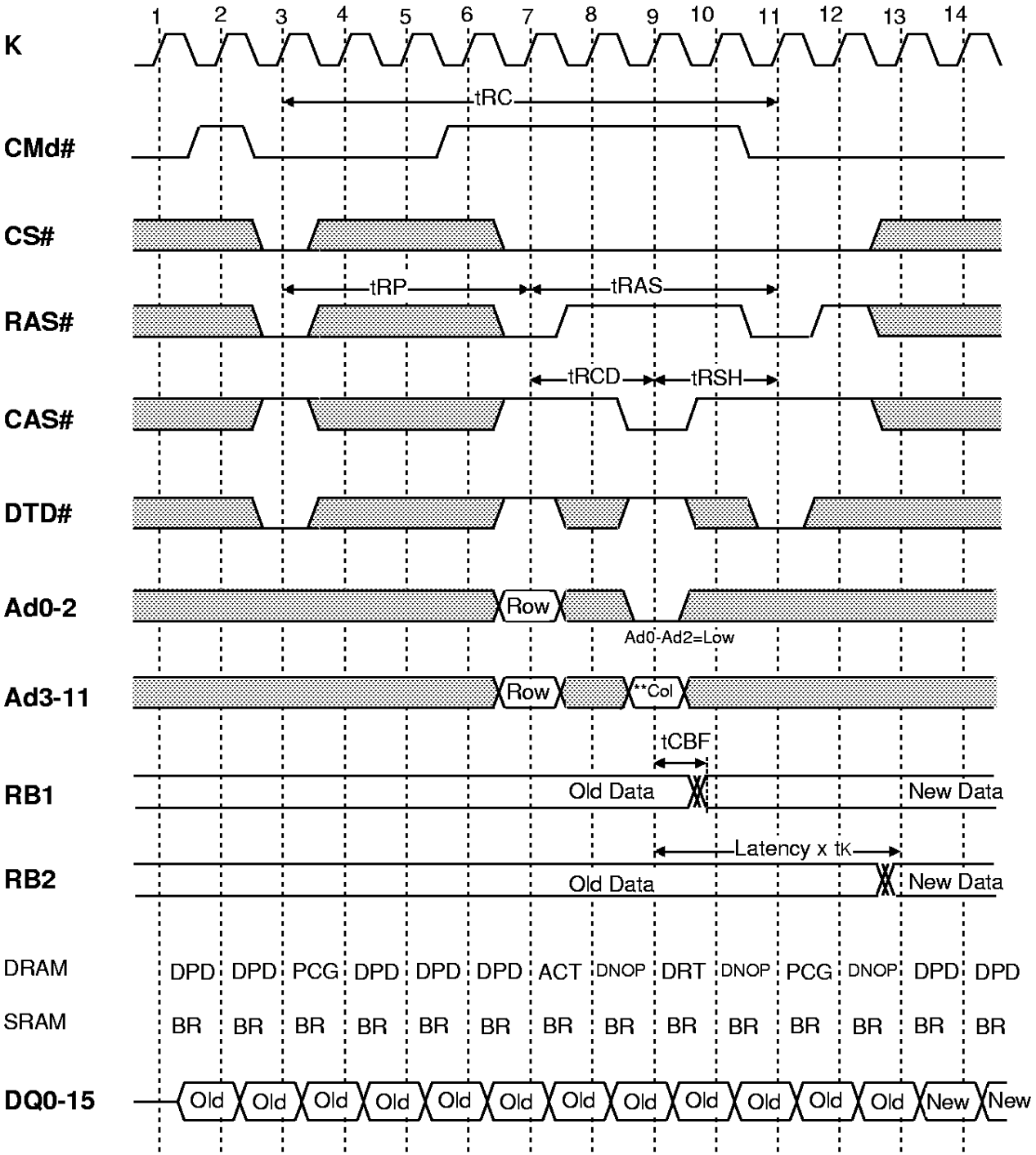
** Ad3-Ad7 are column block addresses (Ad8~Ad11=Low).

DRAM Read Transfer (DRAM -> RB1-> RB2) Latency set=3



SRAM operation can be freely performed. ** Ad3-Ad7 are column block addresses (Ad8~Ad11=Low).

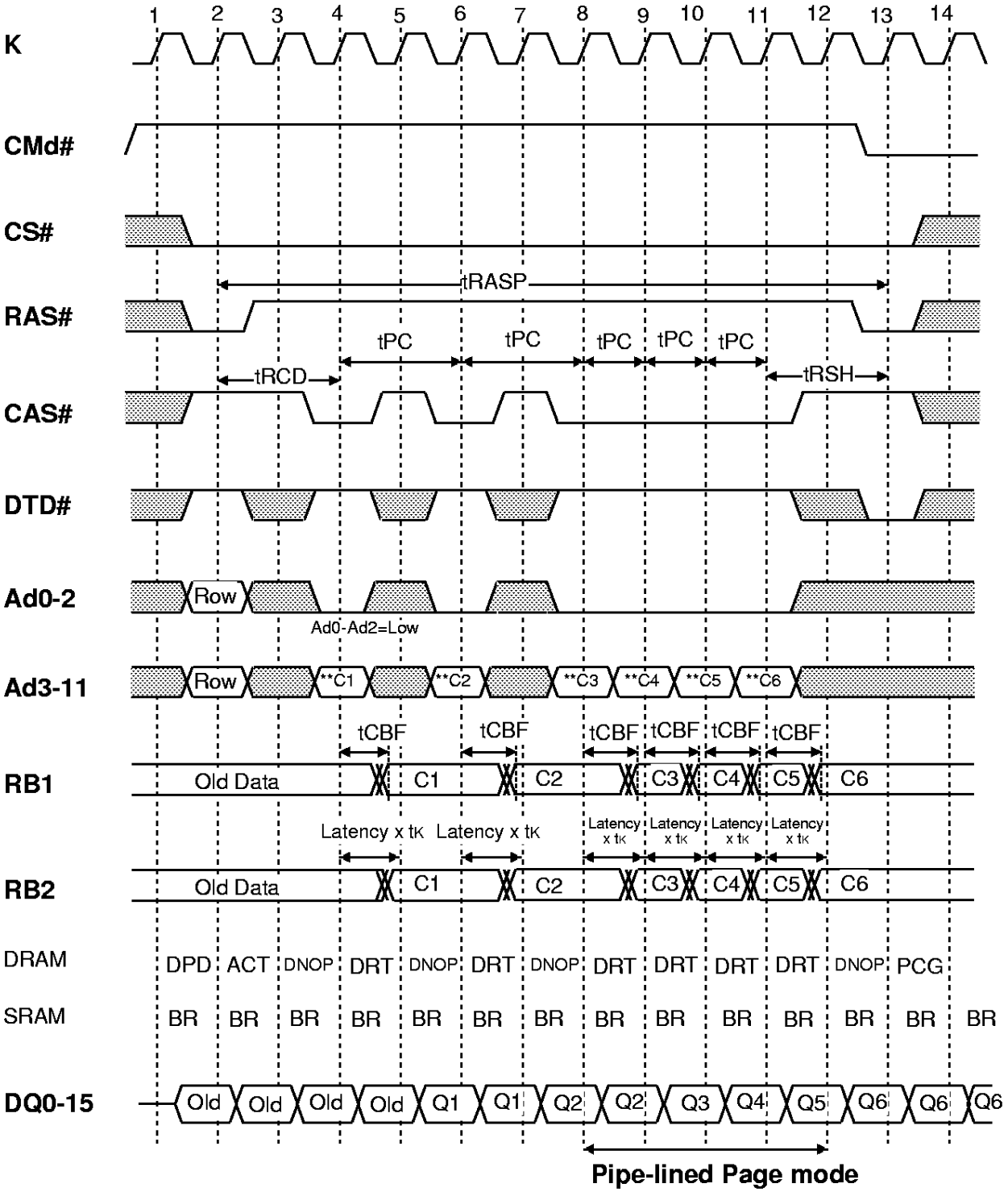
DRAM Read Transfer (DRAM -> RB1-> RB2) Latency set=4



SRAM operation can be freely performed.

** Ad3-Ad7 are column block addresses (Ad8~Ad11=Low).

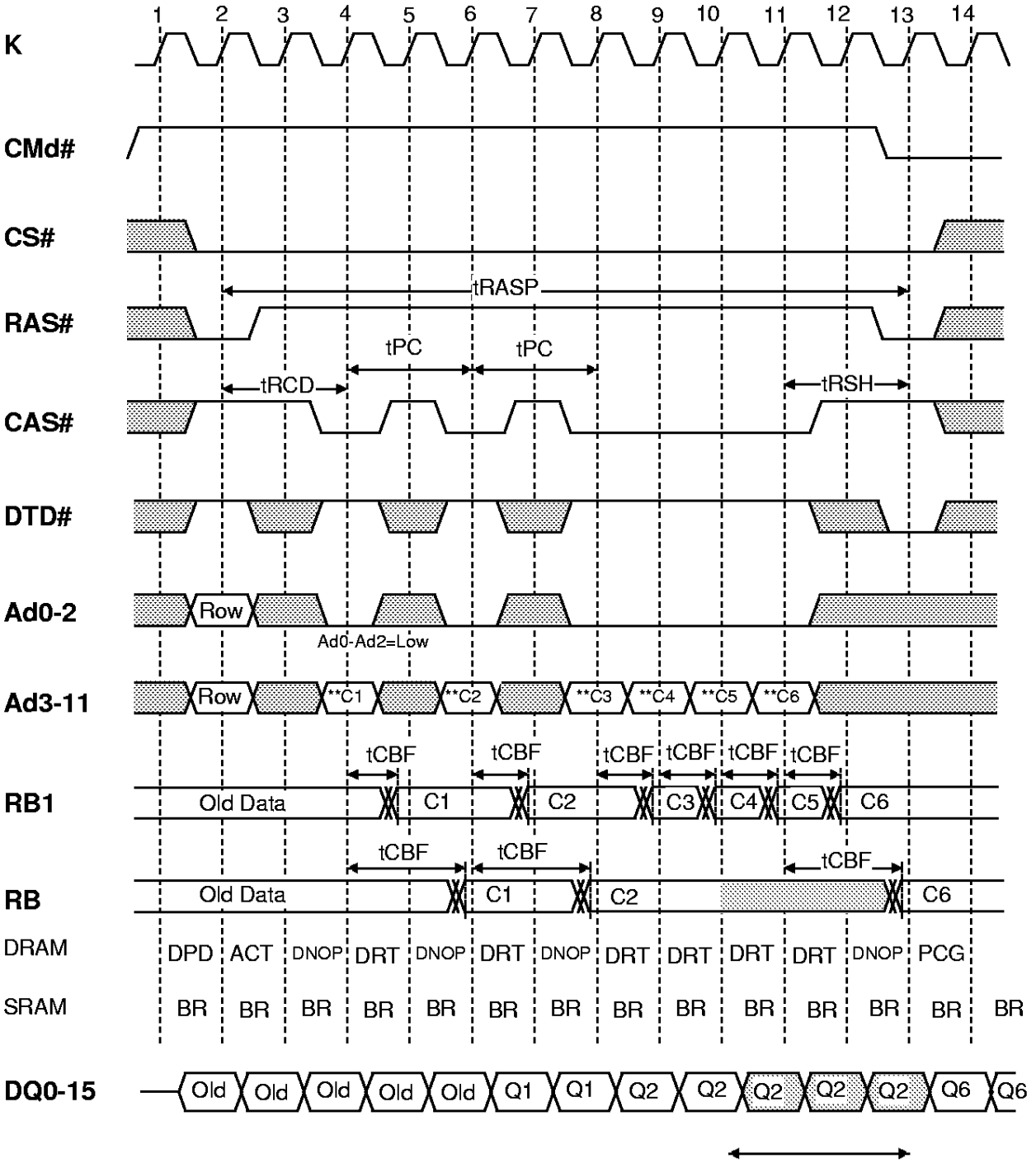
Page-Mode DRAM Read Transfer (Pipe-lined Page-Mode) Latency set=1



SRAM operation can be freely performed.

** Ad3-Ad7 are column block addresses (Ad8~Ad11=Low).

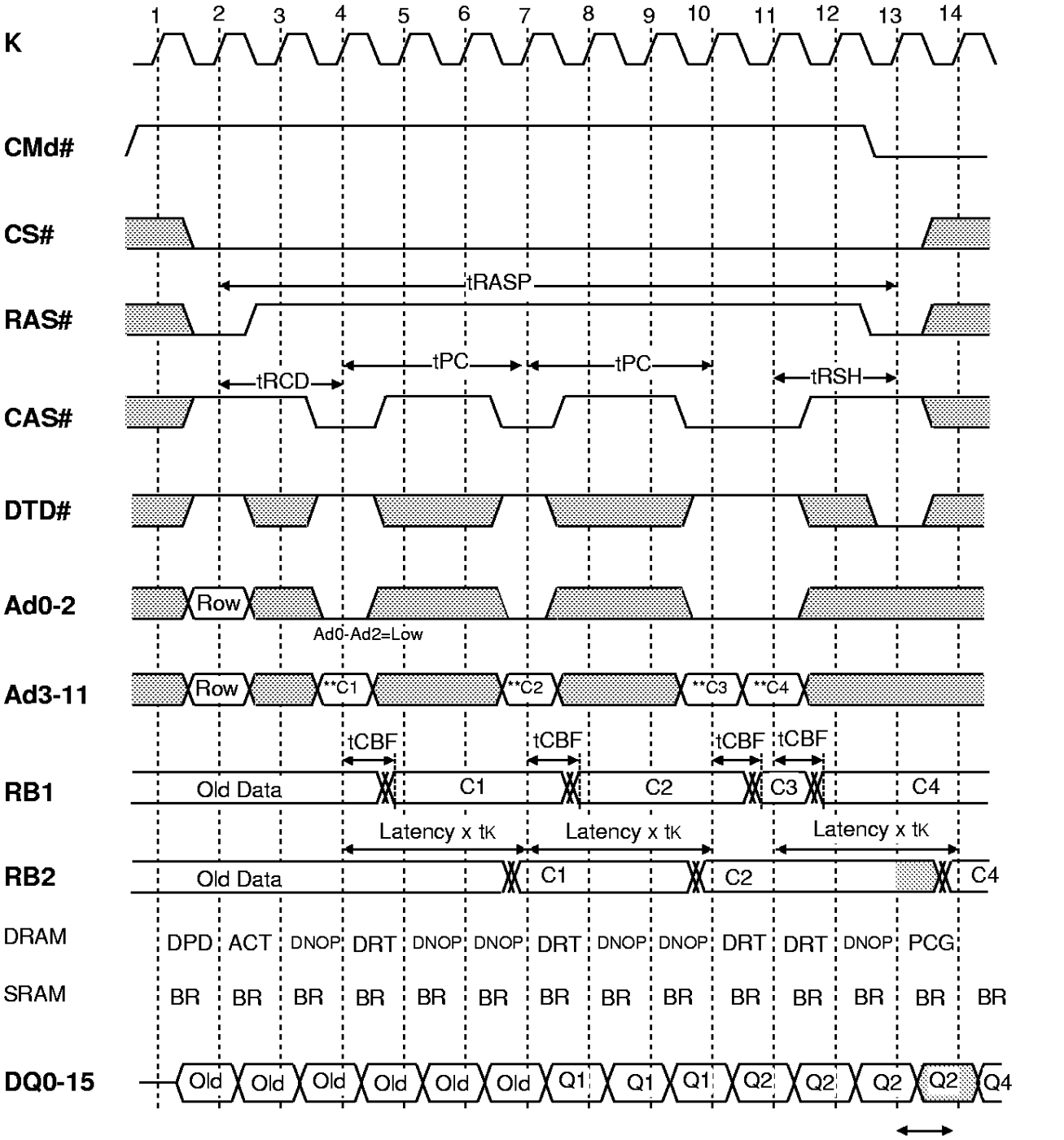
Page-Mode DRAM Read Transfer Latency set=2



If next DRT happens within the latency, new data does not transferred to RB. However this operation is not guaranteed.

SRAM operation can be freely performed. ** Ad3-Ad7 are column block addresses (Ad8~Ad11=Low).

Page-Mode DRAM Read Transfer Latency set=3

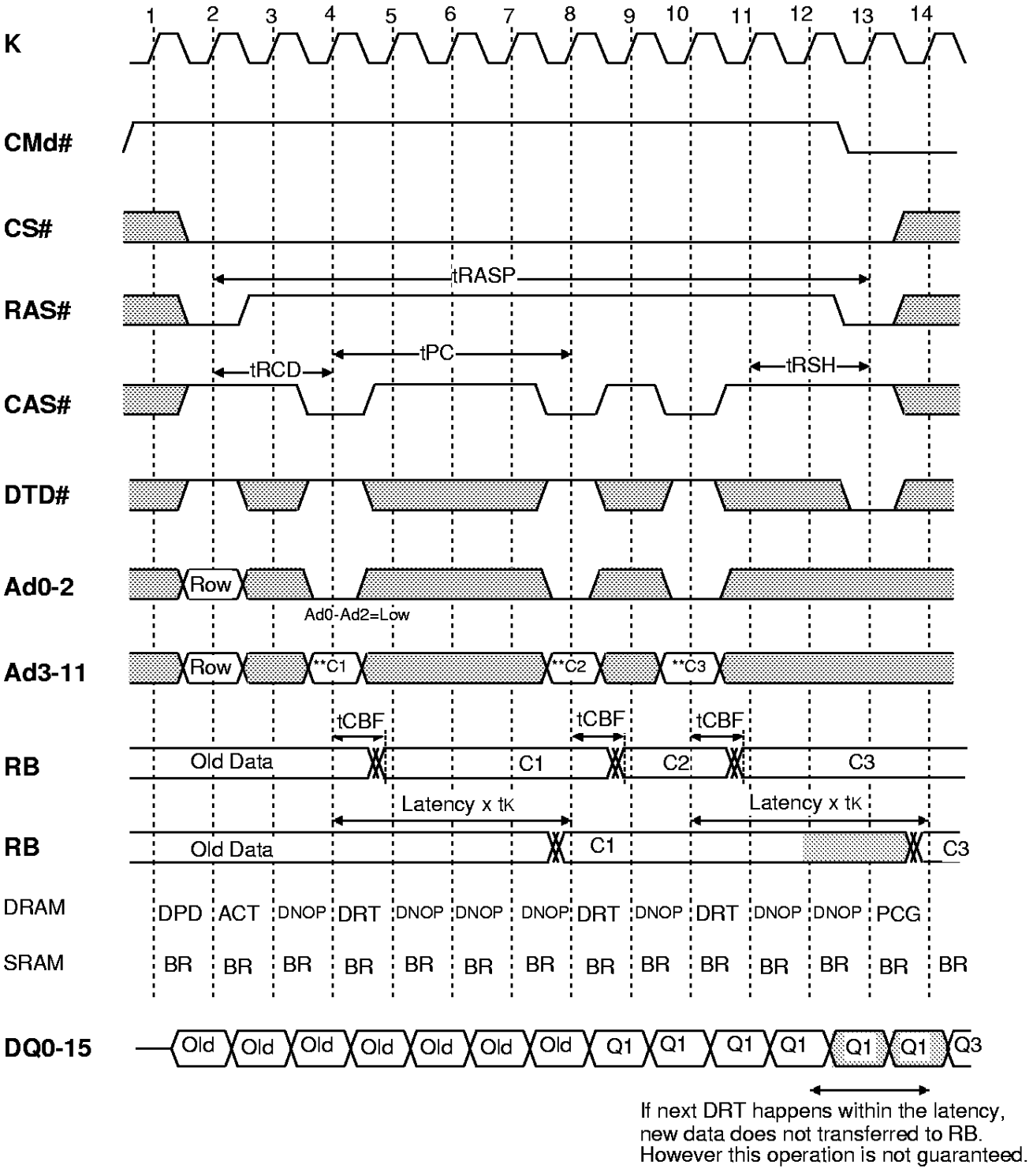


If next DRT happens within the latency, new data does not transferred to RB. However this operation is not guaranteed.

SRAM operation can be freely performed.

** Ad3-Ad7 are column block addresses (Ad8~Ad11=Low).

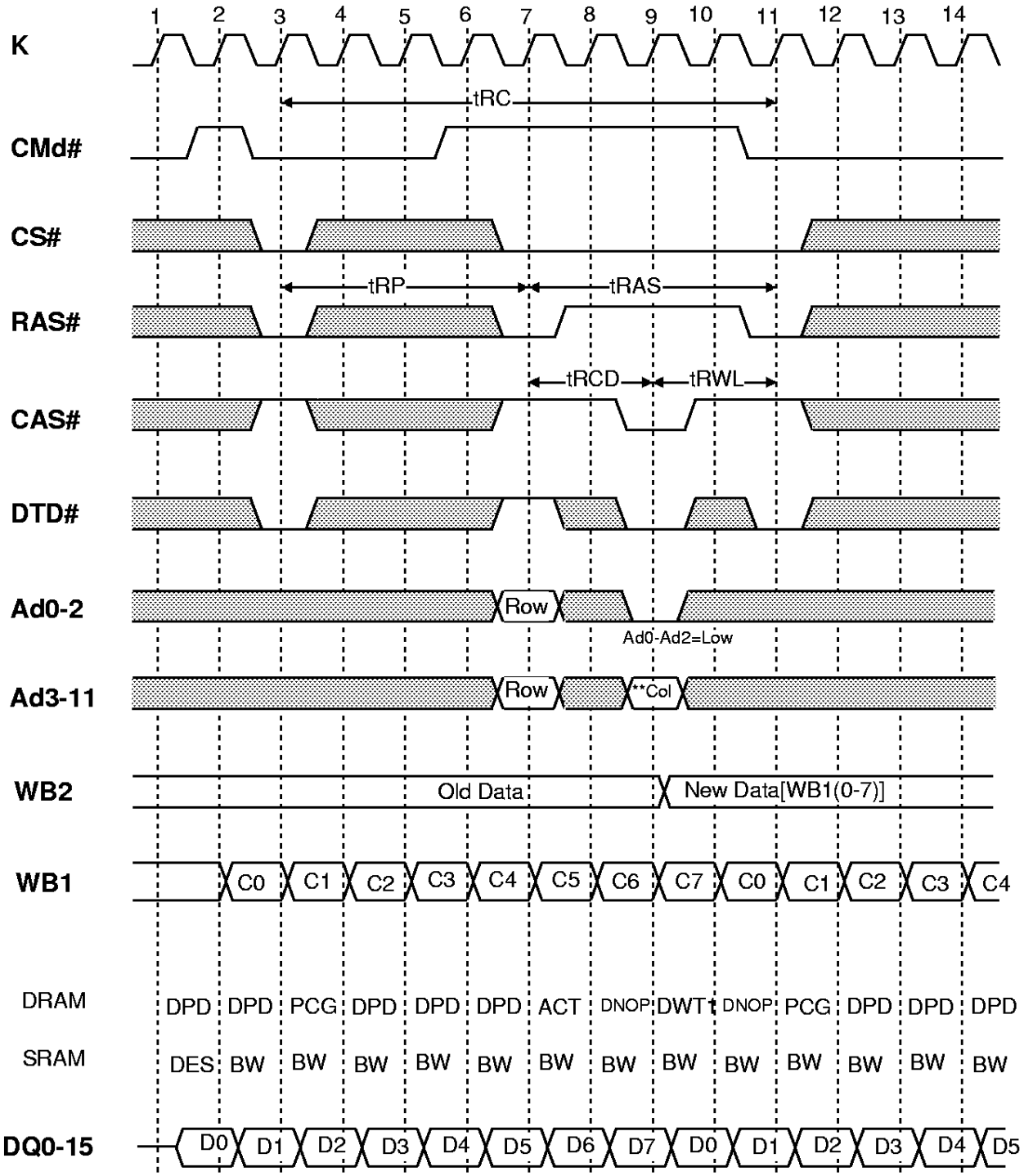
Page-Mode DRAM Read Transfer Latency set=4



SRAM operation can be freely performed.

** Ad3-Ad7 are column block addresses (Ad8~Ad11=Low).

DRAM Write Transfer 1 (WB1->WB2->DRAM)
Buffer Write (DIN->WB1)



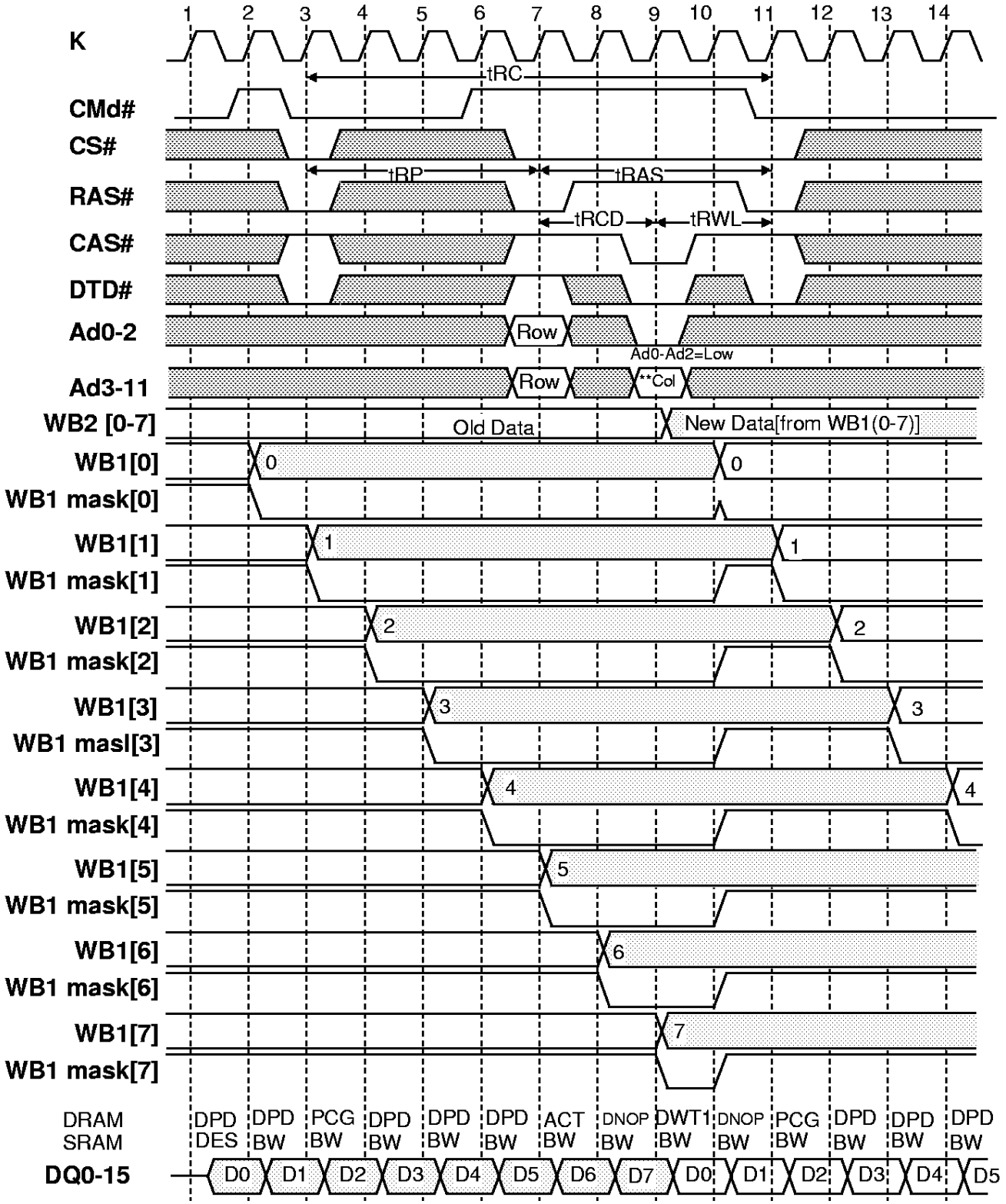
Please refer to next page in detail.

SRAM operation can be freely performed.

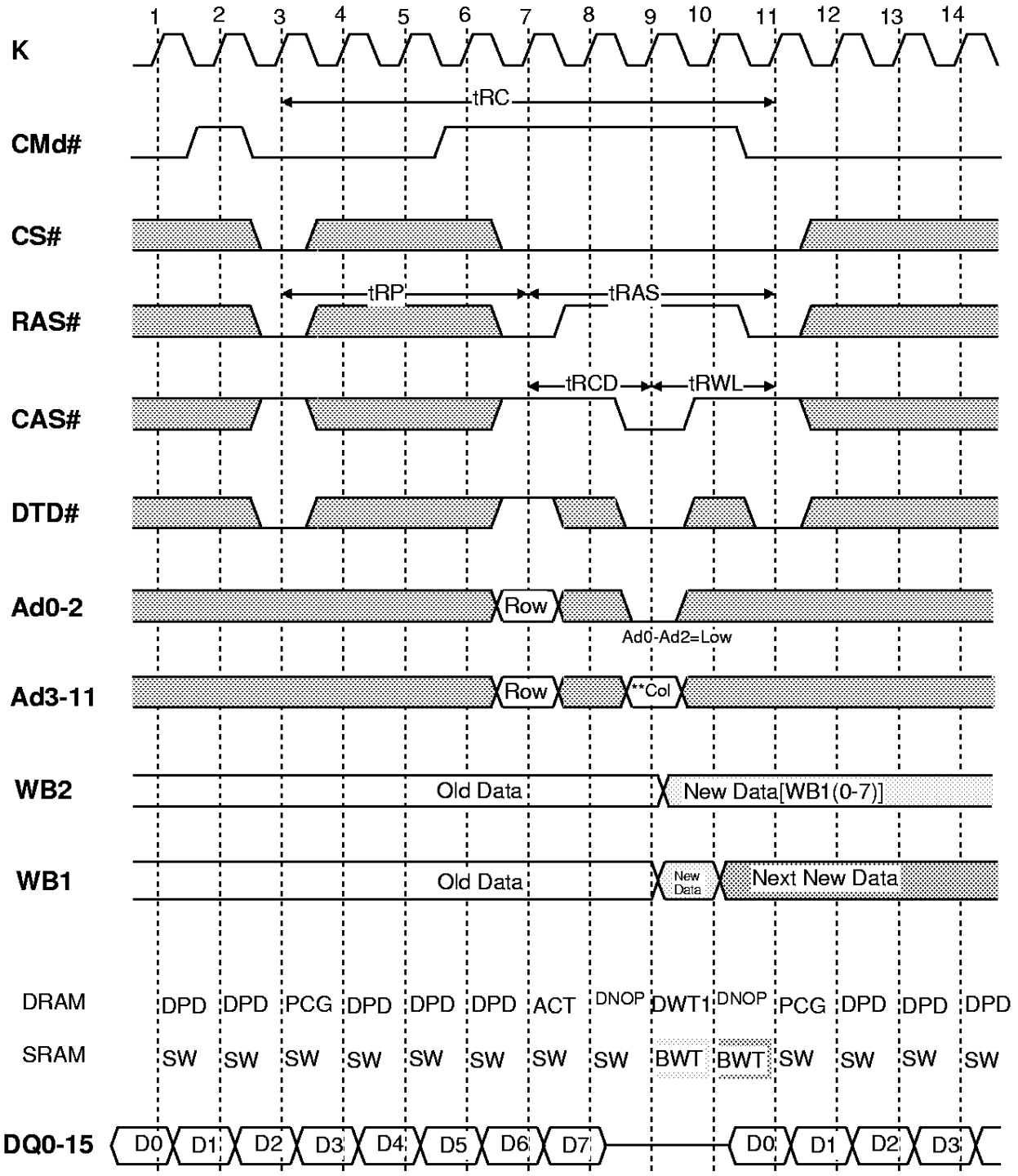
** Ad3-Ad7 are column block addresses (Ad8~Ad11=Low).

DRAM Write Transfer 1 (WB1->WB2->DRAM)
Buffer Write (DIN->WB1)

detail



DRAM Write Transfer 1 (WB1->WB2->DRAM)
Buffer Write Transfer (SRAM->WB1)



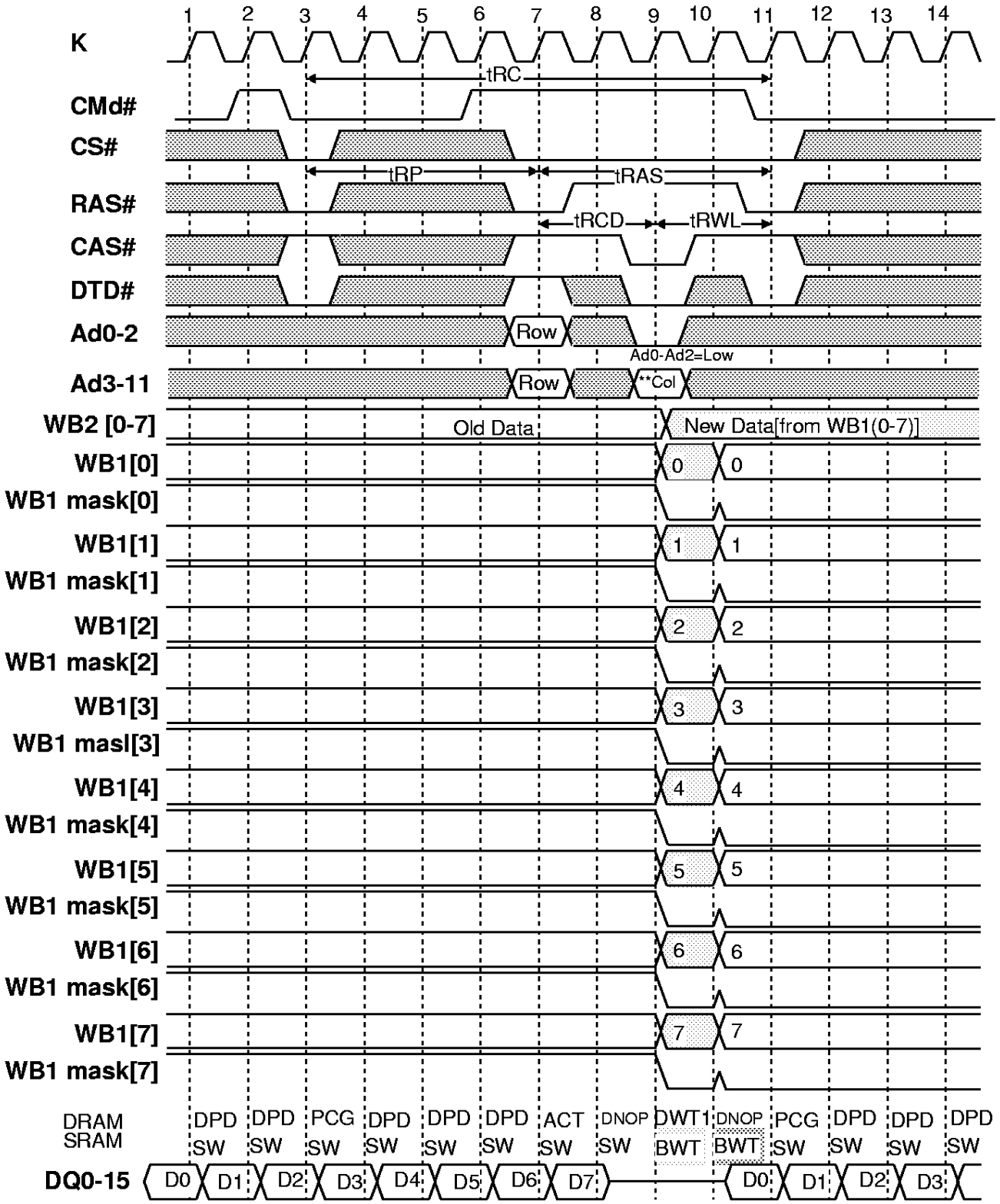
Please refer to next page in detail.

SRAM operation can be freely performed.

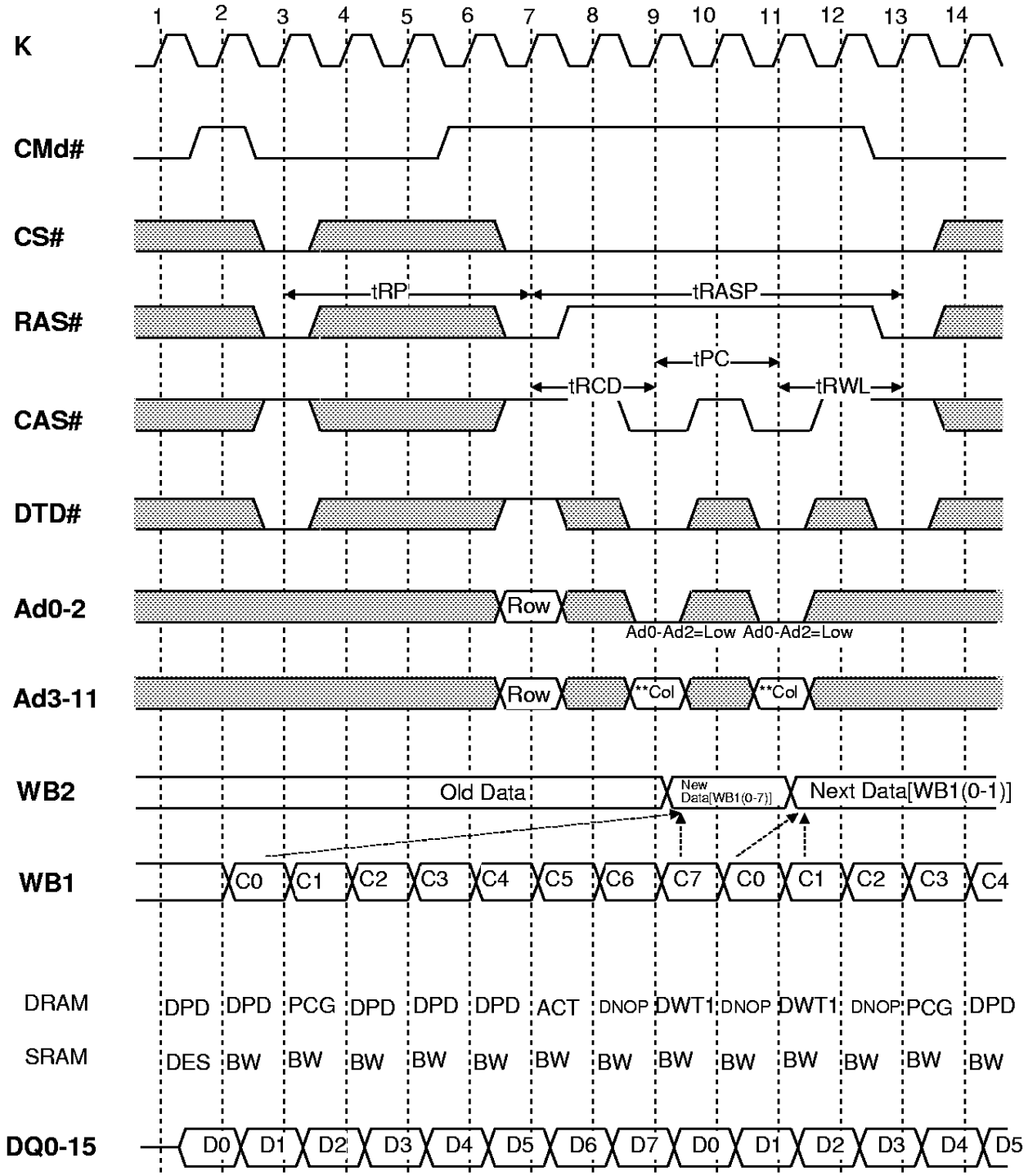
** Ad3-Ad7 are column block addresses (Ad8~Ad11=Low).

DRAM Write Transfer 1 (WB1->WB2->DRAM)
Buffer Write Transfer (SRAM->WB1)

detail



Page-Mode DRAM Write Transfer 1 (WB1->WB2->DRAM)
Buffer Write (DIN->WB1)

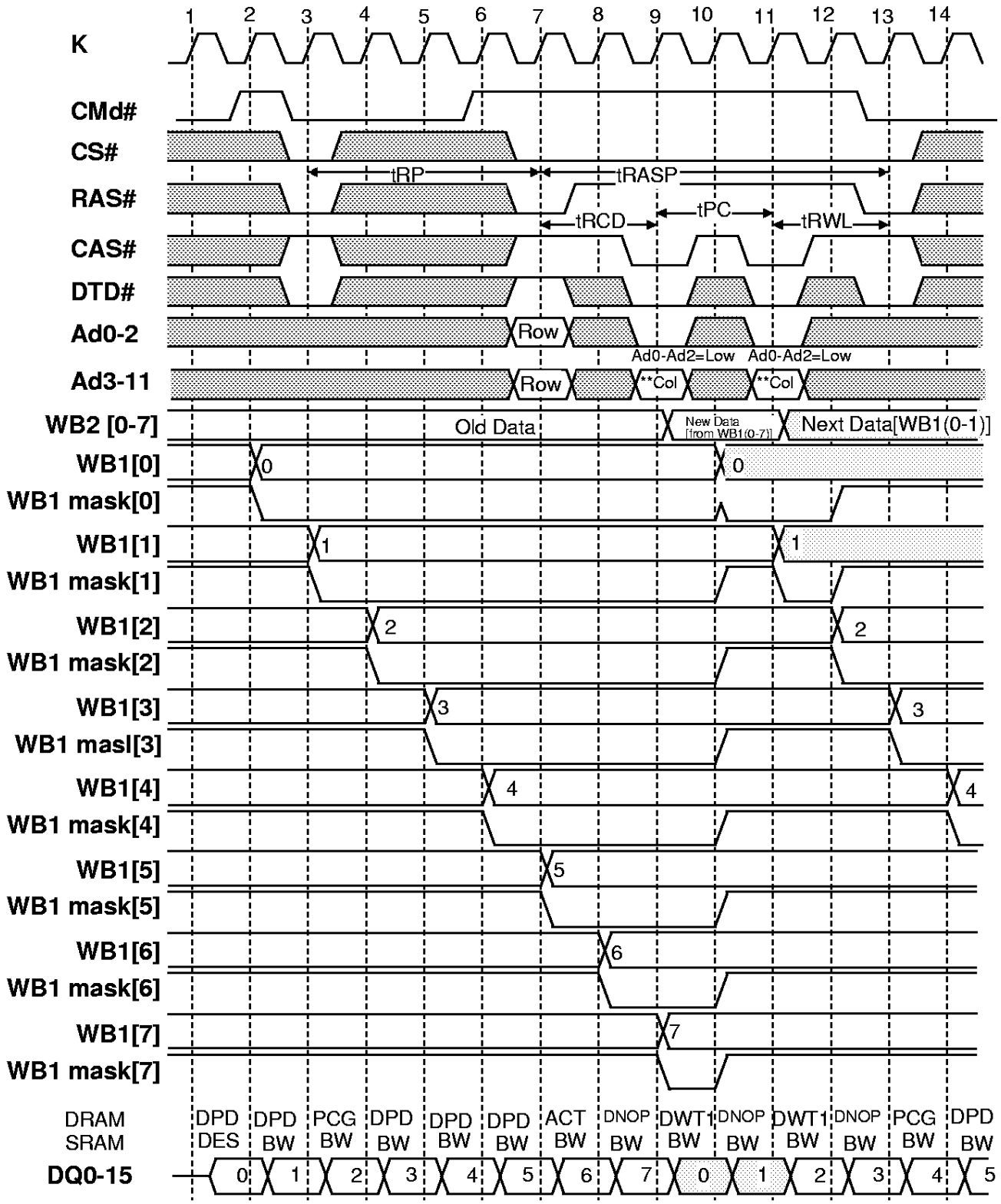


Please refer to next page in detail.

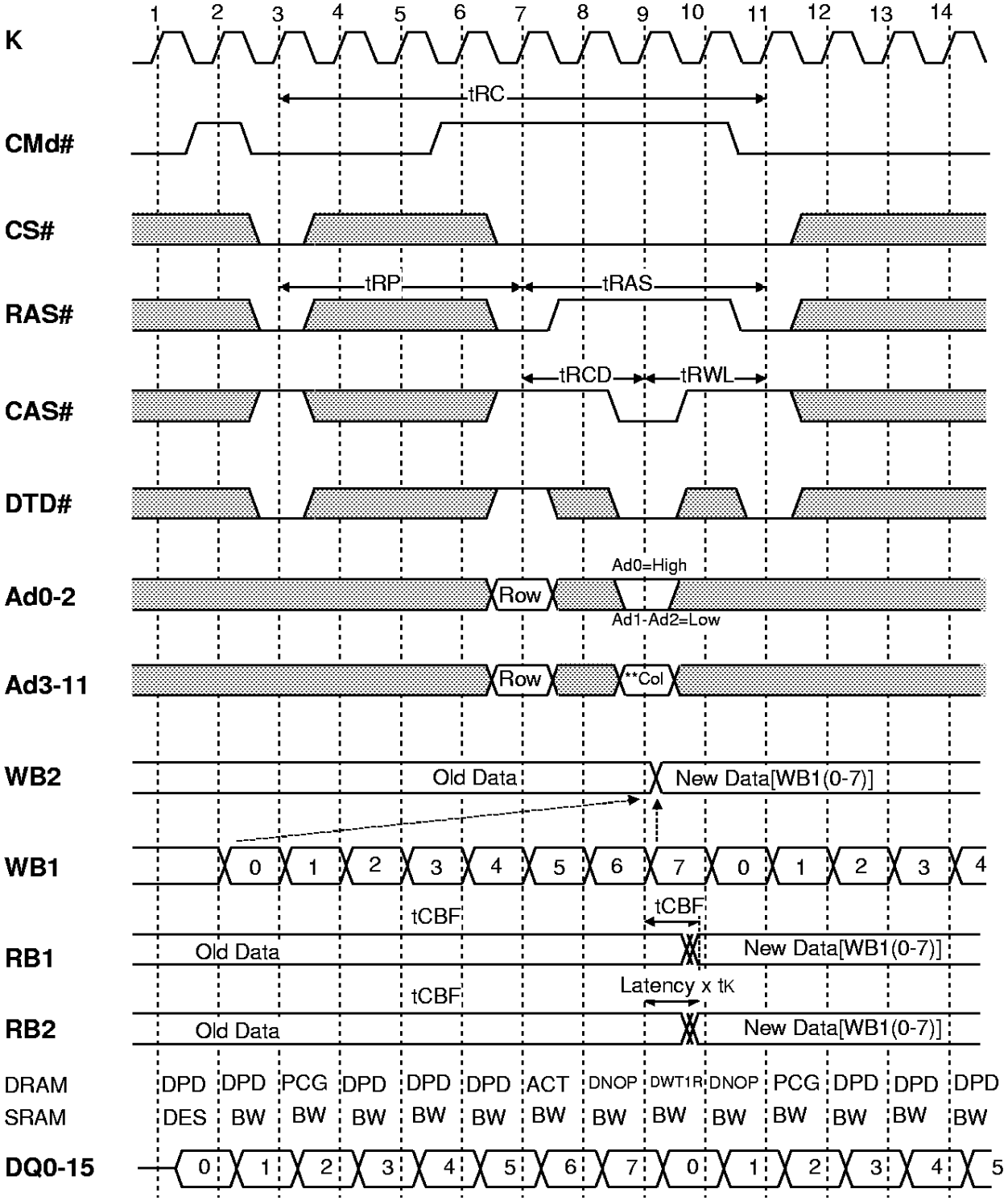
SRAM operation can be freely performed. ** Ad3-Ad7 are column block addresses (Ad8~Ad11=Low).

Page-Mode DRAM Write Transfer 1 (WB1->WB2->DRAM)
Buffer Write (DIN->WB1)

detail



DRAM Write Transfer 1&Read (WB1->WB2->DRAM->RB) Latency set=1
Buffer Write (DIN->WB1)

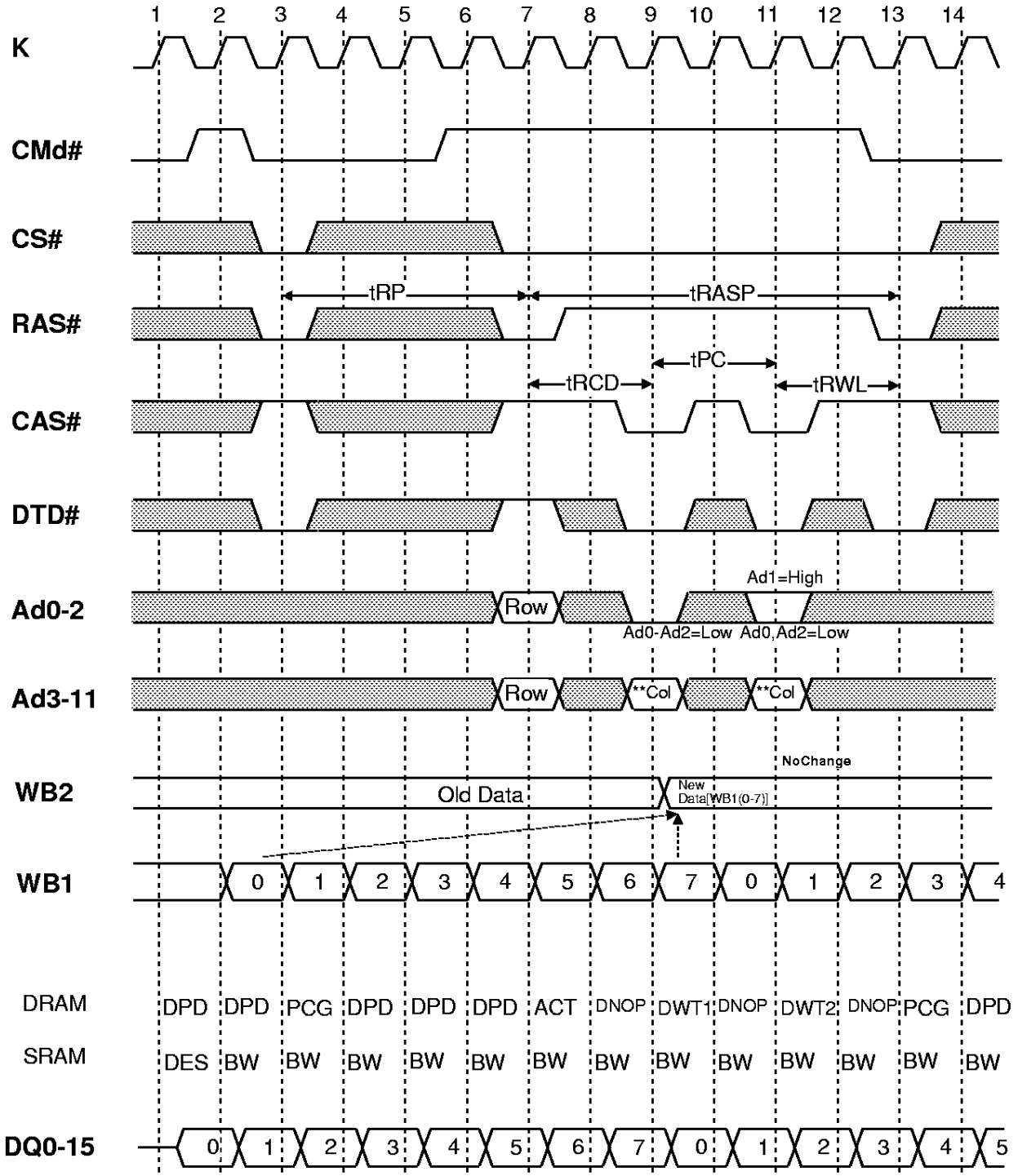


New Data on RB appears as to latency set count. See DRT timing chart.

SRAM operation can be freely performed.

** Ad3-Ad7 are column block addresses (Ad8~Ad11=Low).

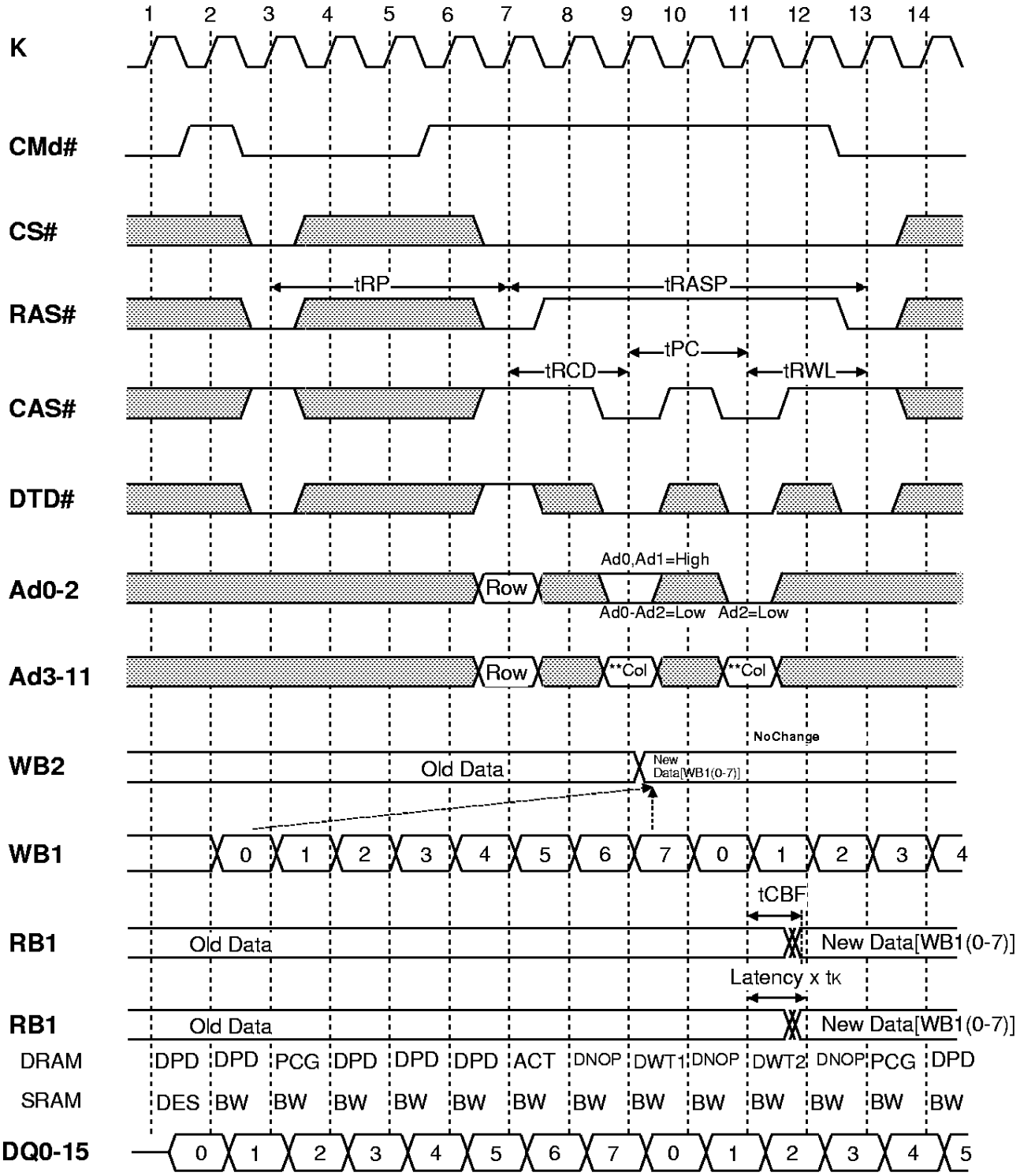
DRAM Write Transfer 2 (WB2->DRAM)



SRAM operation can be freely performed.

** Ad3-Ad7 are column block addresses (Ad8~Ad11=Low).

DRAM Write Transfer2 & Read (WB2->DRAM->RB1-> RB2) Latency set=1

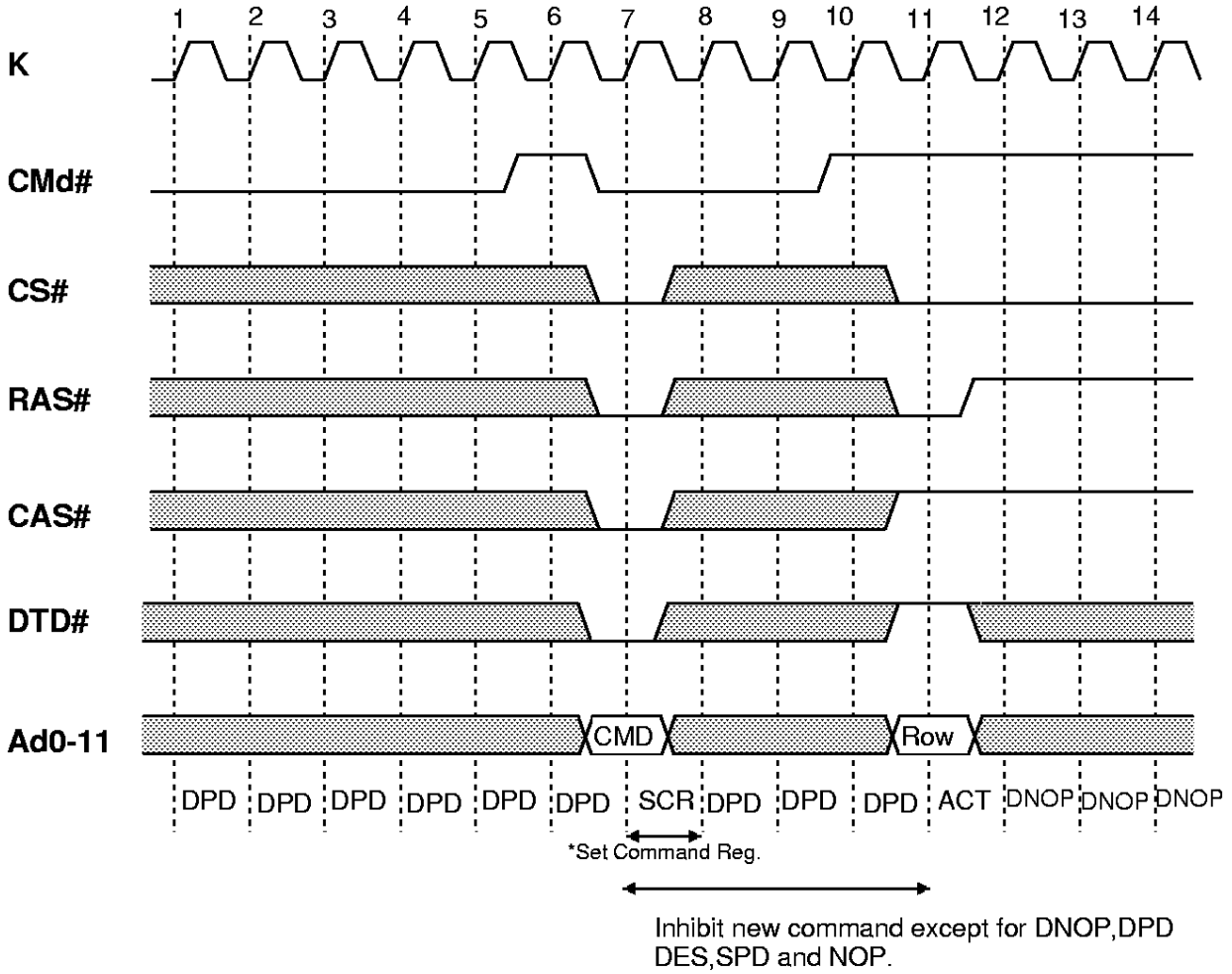


New Data on RB appears as to latency set count. See DRT timing chart.

SRAM operation can be freely performed. ** Ad3-Ad7 are column block addresses (Ad8~Ad11=Low).

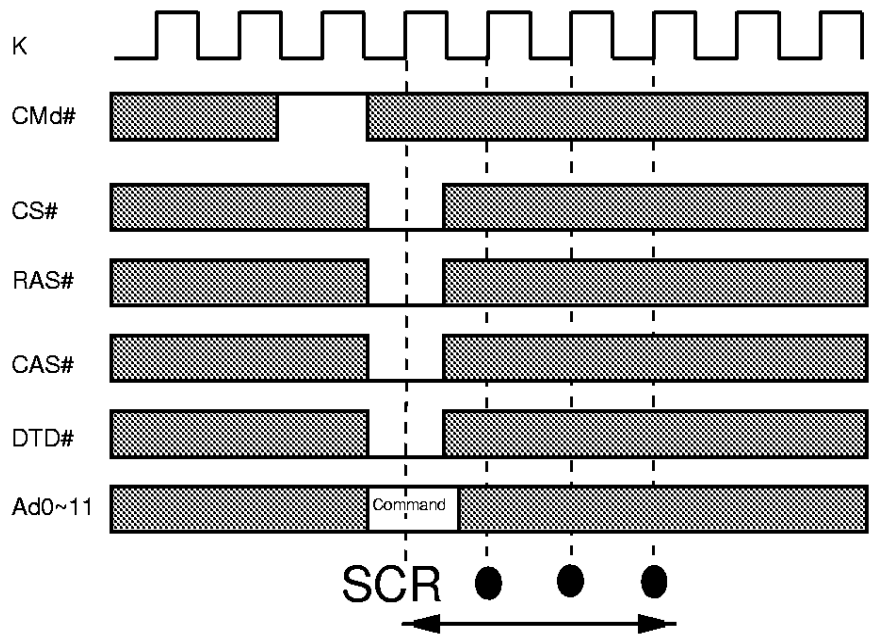
This page is left blank, so that the Set Command Register Timing Diagram on the next spread can be seen conveniently.

Set Command Register (1)



Set Command Register(2)

Address Input												Command
Ad11	Ad10	Ad9	Ad8	Ad7	Ad6	Ad5	Ad4	Ad3	Ad2	Ad1	Ad0	
L	L				L					L	L	**No operation**
L	L				L					L	H	**Set All WB1 Xfer Masks**
L	L				L					L		**Default**
L	L				L			L	L	L		**Output ModeTransparent**
~~L~~	~~L~~				~~L~~			~~L~~	~~H~~	~~L~~		~~**Output Mode Latched**~~
L	L				L			H	L	L		**Output Mode Registered**
L	L				L	L	L			L		Latency 1
L	L				L	L	H			L		Latency 2
L	L				L	H	L			L		Latency 3
L	L				L	H	H			L		Latency 4
L	L				L					L		**Default**
L	L		L	L	L					L		**BL=1**
L	L		L	H	L					L		**BL=2**
L	L		H	L	L					L		**BL=4**
L	L		H	H	L					L		**BL=8**
L	L	L			L					L		**Sequential**
L	L	H			L					L		**Interleave**
L	L				L					L		**Default**
L	L				L					L		**Default**



* **Latency** is the number of clock cycles required to transfer new data from the DRAM to the Read Buffer . Therefore, it can be adjusted to the clock frequency of the system.
(Latency) x (tK) should meet tCBF min. timing requirement.

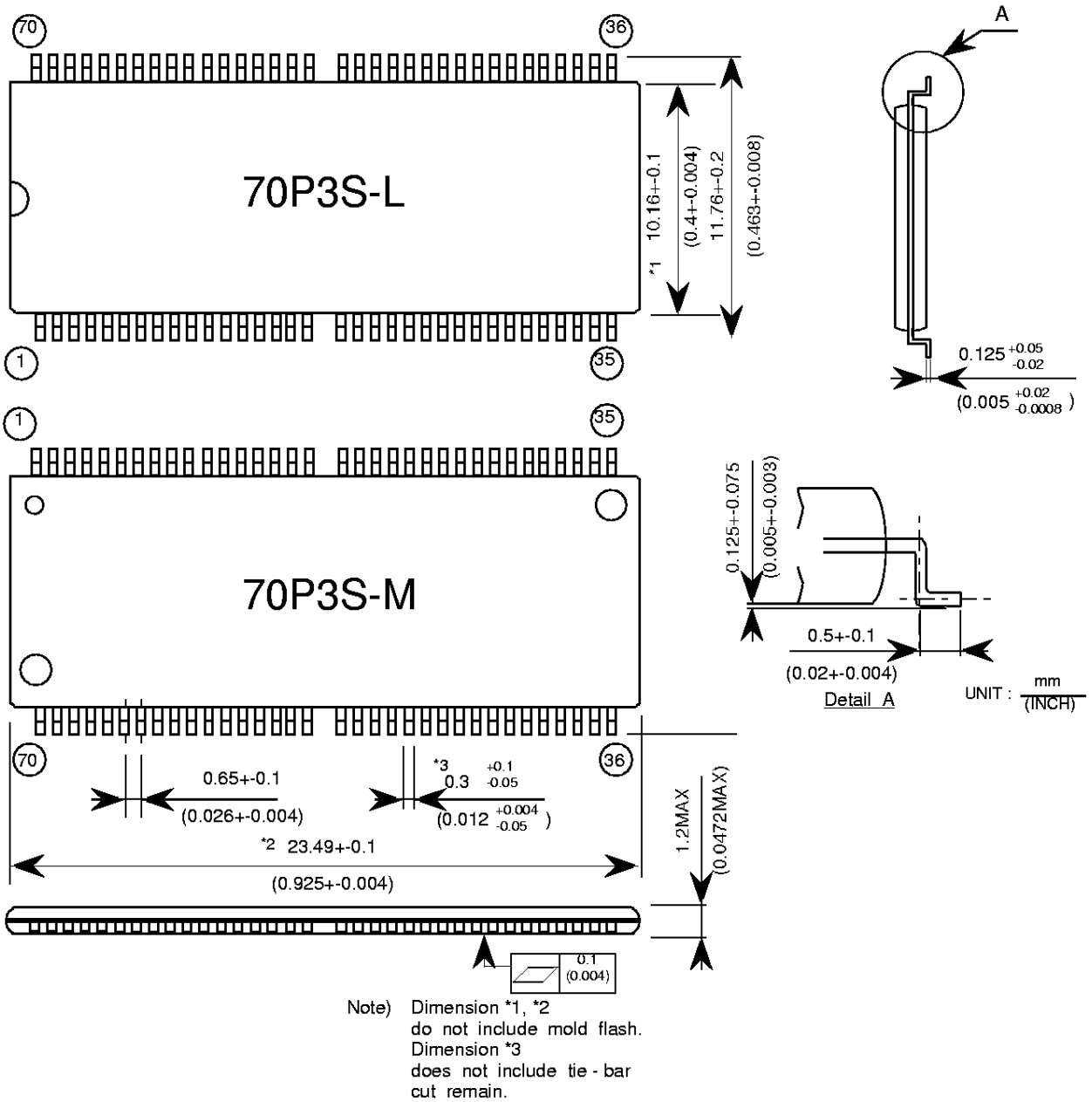
Inhibit new read or write function during these 4 clocks.

Burst Mode Address

Initial Address			BL	Sequential								Interleaved							
As2	As1	As0		Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
0	0	0	8	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
0	0	1		1	2	3	4	5	6	7	0	1	0	3	2	5	4	7	6
0	1	0		2	3	4	5	6	7	0	1	2	3	0	1	6	7	4	5
0	1	1		3	4	5	6	7	0	1	2	3	2	1	0	7	6	5	4
1	0	0		4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3
1	0	1		5	6	7	0	1	2	3	4	5	4	7	6	1	0	3	2
1	1	0		6	7	0	1	2	3	4	5	6	7	4	5	2	3	0	1
1	1	1		7	0	1	2	3	4	5	6	7	6	5	4	3	2	1	0
0	0	0	4	0	1	2	3					0	1	2	3				
-	0	1		1	2	3	0					1	0	3	2				
-	1	0		2	3	0	1					2	3	0	1				
-	1	1		3	0	1	2					3	2	1	0				
-	-	0	2	0	1							0	1						
-	-	1		1	0							1	0						

Note: When SRAM command is executed more than burst length, the Address repeats with the same sequence.

70P3S Package Dimension



Note) Dimension *1, *2
do not include mold flash.
Dimension *3
does not include tie - bar
cut remain.