



High-Speed CMOS 4Kx4 SRAM with Common I/O

QS8768

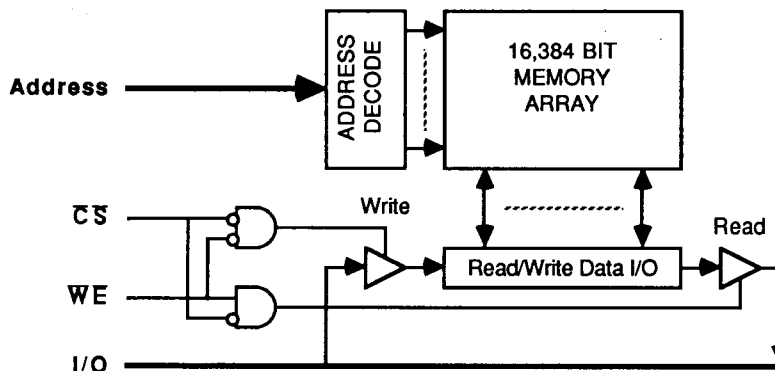
FEATURES/BENEFITS

- High Speed Access and Cycle times
- 10ns/12ns/15ns/20ns/25ns Commercial
- 15ns/20ns/25ns/35ns Military
- TTL compatible I/O
- Low power, high-speed QCMOS™ technology
- Military product compliant to MIL-STD-883, Class B
- 6-Transistor cell for high reliability
- Ideal for reliable,dense memory systems
- Available in 20-pin DIP, 20-Pin ZIP
- 20-pin 300 mil SOJ & 20-pin LCC
- Low Standby current
- JEDEC standard pinout

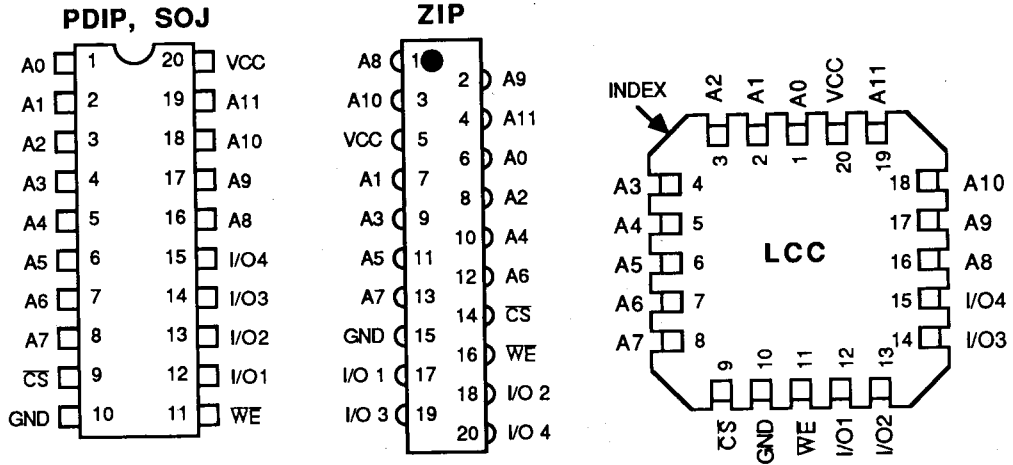
DESCRIPTION

The QS8768 is a high-speed 16K SRAM organized as 4Kx4 . It is manufactured in a high-performance CMOS process, and it based on a 6-transistor cell design for high reliability of data retention. The high-speed access times of the QS8768 make it useful in cache data RAM, cache tag RAMs, high-speed scratchpad memories, look-up tables, pipelined DSP and bit-slice systems. Low operating power and excellent latch-up and ESD protection are provided.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS



ALL PINS TOP VIEW

PIN DESCRIPTION

Pin	Name	I/O	Function
A		I	Address
I/O1 - I/O4		I/O	Data
CS		I	Chip Select
WE		I	Write Enable

FUNCTION TABLE

CS	WE	I/O	Power	Function
H	X	High Z	Standby	Deselect
L	H	Data Out	Active	Read
L	L	Data In	Active	Write

ABSOLUTE MAXIMUM RATINGS

Supply Voltage to Ground.....	-0.5V to +7.0V
DC Output Voltage V_O	-0.5V to $V_{CC} + 0.5V$
DC Input Voltage V_I	-0.5V to $V_{CC} + 0.5V$
AC Input Voltage (for a pulse width ≤ 20 ns).....	-3.0V
DC Output Current Max. sink current/pin.....	50 mA
DC Output Current Max. source current/pin.....	30 mA
TBIAS Temperature Under Bias, COM.....	-65° to +125°C
TSTG Storage Temperature, COM.....	-65° to +125°C
TBIAS Temperature Under Bias, MIL.....	-65° to +135°C
TSTG Storage Temperature, MIL.....	-65° to +155°C

Note: Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to the maximum ratings for extended periods may affect reliability.

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CAPACITANCE

$T_a = +25^\circ\text{C}$, $f = 1$ MHz

Name	Description	Conditions	Typ	Max	Unit
Cin	Input Capacitance	$V_{in} = 0$ V PDIP Pkg.	3	6	pF
Cin	Input Capacitance	$V_{in} = 0$ V SOJ Pkg.	2.5	5	pF
Cout	Output Capacitance	$V_{out} = 0$ V PDIP Pkg.		7	pF
Cout	Output Capacitance	$V_{out} = 0$ V SOJ Pkg.		7	pF

Note: Capacitance is measured at characterization but not tested at final production.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Commercial TA = 0° C to 70°C, Vcc = 5.0V±10% Military TA = -55°C to 125° C, Vcc = 5.0V±10%

Symbol	Parameter	Test Conditions	Commercial		Military		Unit
			Min	Max	Min	Max	
Vih	Input HIGH Voltage	Logic High for All Inputs	2.2	6.0	2.2	6.0	Volts
Vil	Input LOW Voltage (1)	Logic Low for All Inputs		0.8		0.8	
Voh	Output HIGH Voltage	Ioh = -4 mA, Vcc = MIN	2.4		2.4		
Vol	Output LOW Voltage	Iol = 8 mA, Vcc = MIN		0.4		0.4	
Ii	Input Leakage	Vcc = MAX, Vin = GND to Vcc		5		10	μA
Io	Output Leakage	Vcc = MAX, Vout = GND to Vcc		5		10	

Notes:

1. Transient inputs with Vil not more negative than -3.0 volts are permitted for pulse widths < 20 ns.

POWER SUPPLY CHARACTERISTICS

Commercial TA = 0° C to 70°C, Vcc = 5.0V±10% Military TA = -55°C to 125° C, Vcc = 5.0V±10%
Vlc = 0.2 V, Vhc = Vcc - 0.2V At f = 0, no input lines switch; At f = f MAX, RAM is cycling at 1 / t RC

Symbol	Parameter	-10		-12		15		-20		-25/-35		Unit
		C	M	C	M	C	M	C	M	C	M	
Icc1	Static Operating Current, Vcc = MAX Outputs open CS ≤ Vil, f = 0	100	120	100	120	100	120	100	120	100	120	mA
Icc2	Dynamic Operating Current, Vcc = MAX Outputs open CS ≤ Vil, f = f MAX	145	165	135	155	125	145	120	140	110	130	
Isb	TTL Standby Current, Vcc = MAX Outputs open CS ≥ Vih, f = f MAX	60	70	60	70	60	70	60	70	60	70	
Isb1	Full Standby Current, Vcc = MAX Outputs open CS ≥ Vhc, f = 0 Vin ≤ Vlc or Vin ≥ Vhc	15	20	15	20	15	20	15	20	15	20	

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Commercial TA = 0° C to 70° C, Vcc = 5.0V±10% Military TA = -55° C to 125° C, Vcc = 5.0V±10%
See Read Timing Diagrams. All values in nanoseconds unless otherwise noted

Symbol	Parameter (1)	-10(3)		-12 (3)		-15		-20		-25		-35	
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
READ CYCLE													
t RC	Read Cycle Time	10	-	12	-	15	-	19	-	25	-	35	-
t AA	Address Access Time	-	10	-	12	-	15	-	19	-	25	-	35
t ACS	Chip Select Access Time	-	10	-	12	-	15	-	19	-	25	-	35
t OH	Output Hold from Address Change	2	-	2	-	2	-	3	-	3	-	3	-
t CLZ	Chip Select to Output in Low Z (2)	2	-	2	-	2	-	2	-	2	-	3	-
t CHZ	Chip Select to Output in High Z (2)	-	4	-	5	-	7	-	8	-	10	-	15
t PU	Chip Select to Power Up Time (2)	0	-	0	-	0	-	0	-	0	-	0	-
t PD	Chip Select to Power Down Time (2)	-	10	-	12	-	15	-	19	-	25	-	35

Notes:

- 1) See Test Circuit and Waveforms. Minimums guaranteed but not tested.
- 2) This parameter is guaranteed by design but not tested.
- 3) For Vcc±5%. Commercial Only-Preliminary Data.

QS8768

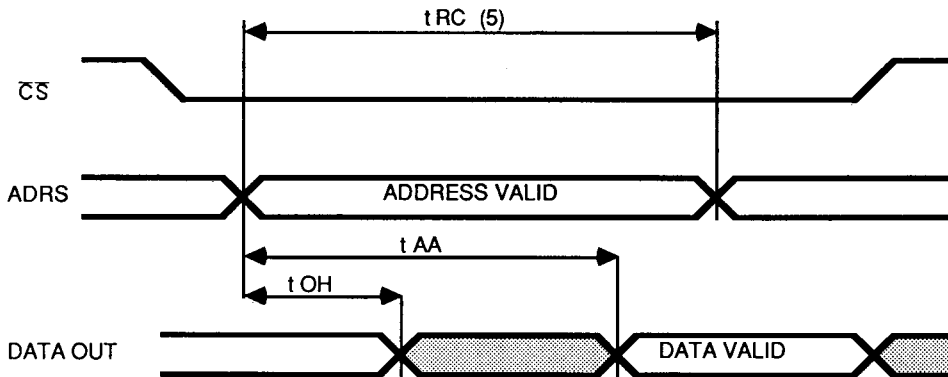
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See Write Timing Diagrams. All values in nanoseconds unless otherwise noted

See Write Timing Diagrams. All values in nanoseconds unless otherwise noted.													
Symbol	Parameter (1)	-10(3)		-12 (3)		-15		-20		-25		-35	
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
WRITE CYCLE													
t WC	Write Cycle Time	10	-	12	-	15	-	19	-	25	-	35	-
t CW	Chip Select Valid to End of Write	8	-	10	-	13	-	17	-	20	-	30	-
t AW	Address Valid to End of Write	8	-	10	-	13	-	17	-	20	-	30	-
t AS	Address Setup Time	0	-	0	-	0	-	0	-	0	-	0	-
t WP	Write Pulse width	8	-	10	-	12	-	16	-	20	-	30	-
t WR	Write Recovery Time	0	-	0	-	0	-	0	-	0	-	0	-
t DW	Data Valid to End of Write	5	-	7	-	8	-	10	-	13	-	18	-
t DH	Data Hold Time	0	-	0	-	0	-	0	-	0	-	0	-
t WZ	Write Enable to Output in High Z (2)	-	4	-	5	-	6	-	7	-	8	-	12
t OW	Output Active from End of Write (2)	2	-	2	-	2	-	2	-	2	-	3	-

Notes:

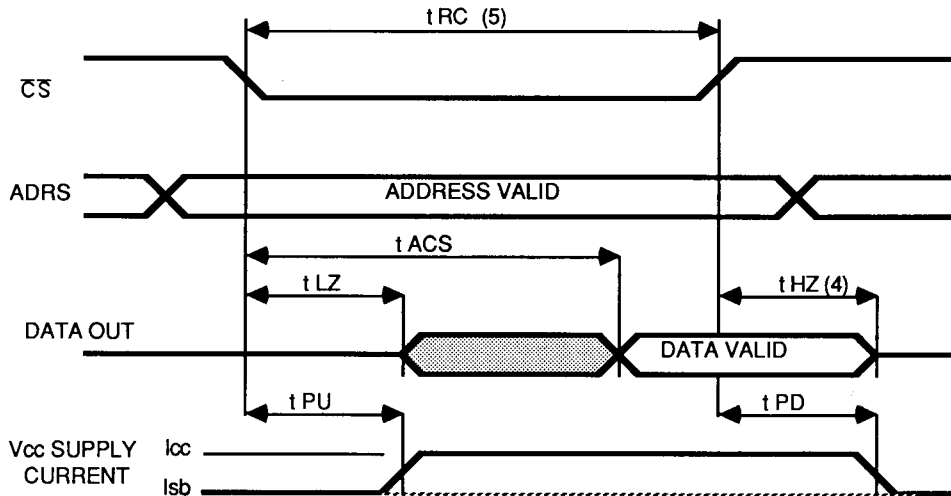
- 1) See Test Circuit and Waveforms. Minimums guaranteed but not tested.
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TIMING WAVEFORMS - READ CYCLE NO. 1 (1,2)



2

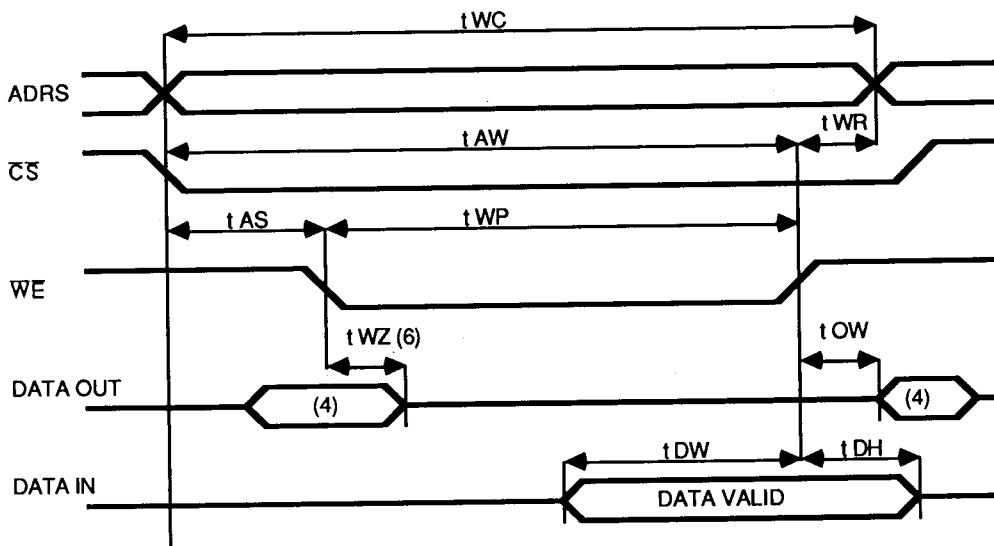
TIMING WAVEFORMS - READ CYCLE NO. 2 (1,3)



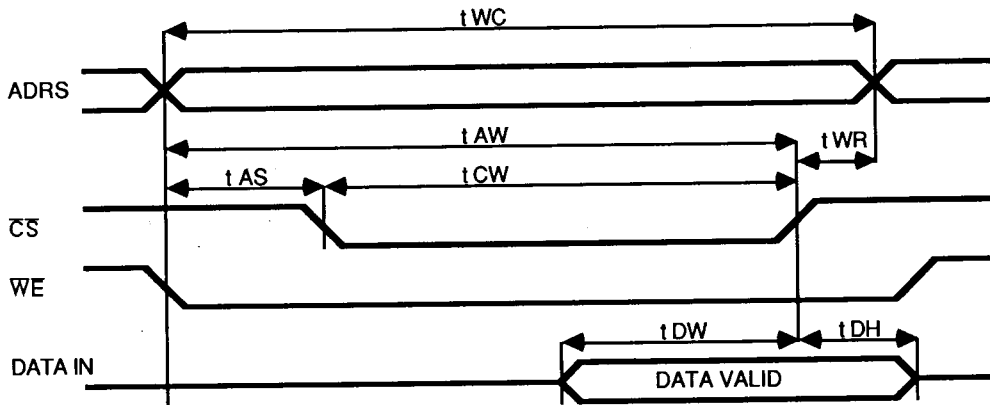
Notes:

1. $\overline{WE}$ is high for Read cycle.
2. $\overline{CS}$ is low for Read cycle #1.
3. Address is valid to or coincident with $\overline{CS}$ transition time for Read Cycle #2.
4. Transition to Hi-Z is measured ± 200 mV change from the prior steady state voltage.
5. All read timings are referenced from the last valid address to the first transitioning address.

TIMING WAVEFORMS-WRITE CYCLE No. 1 (1,2,3 WE controlled timing)



TIMING WAVEFORMS-WRITE CYCLE No. 2 (1,2,3,5 CS controlled timing)



Notes:

1. WE or CS must be high during address transitions.
2. A write occurs during the overlap of a low CS and a low WE.
3. t_{WR} is measured from the earlier of CS and WE going high to end of the write cycle.
4. During this period the I/O pins are in the output state and input signals must not be applied.
5. If the CS low transition occurs simultaneously with or after the WE low transition, the output remains in the high impedance state.
6. Transition to Hi-Z is measured ± 200 mV change from the previous steady state voltage.