



The Future of Analog IC Technology®

LN60A01

600V, Triple N-Channel MOSFET
with Common Gate Control

DESCRIPTION

The LN60A01 is a three channel, 600V N-Channel, enhancement mode power FET manufactured in MPS's proprietary, high-voltage DMOS technology.

This advanced technology has been especially tailored to minimize the on-state resistance, provide superior switching performance, and withstand high energy pulses in the avalanche and commutation modes. This device is well suited for high efficiency switched mode power supplies and active power factor correction.

The LN60A01 is available in PDIP8 and SOIC8 package.

FEATURES

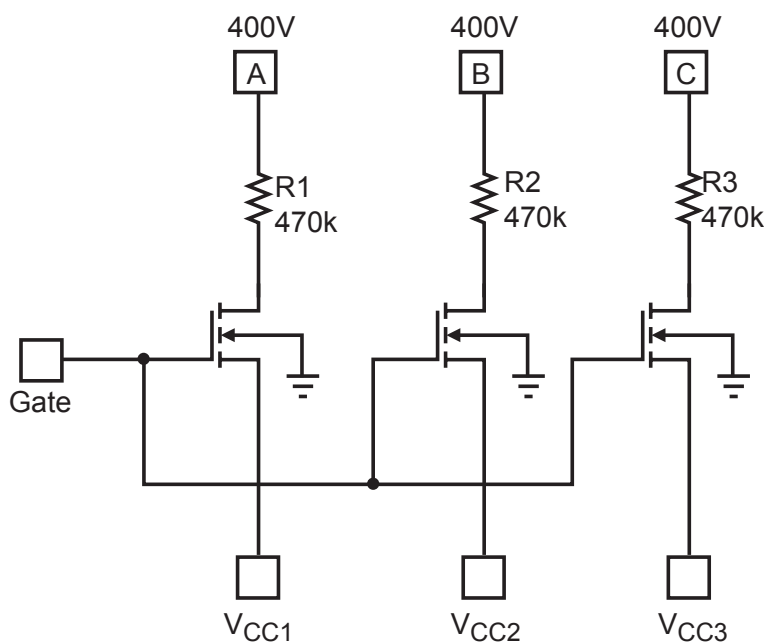
- 600V Breakdown Voltage
- Three N-Channel MOSFETs
- One Gate control to All Three FETs
- $R_{ds(on)}=200\Omega$ at $V_{gs}=10V$
- Switching Current $>0.1A$
- Fast Switching

APPLICATIONS

- High Efficiency AC/DC Adaptor
- Offline Switching Power Supply
- Active Power Factor Correction

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TYPICAL APPLICATION



ORDERING INFORMATION

Part Number*	Package	Top Marking	Free Air Temperature (T _A)
LN60A01EP	PDIP-8	LN60A01E	-20°C to 85°C
Part Number**	Package	Top Marking	Free Air Temperature (T _A)
LN60A01ES	SOIC-8	LN60A01E	-20°C to 85°C

*For RoHS compliant packaging, add suffix -LF (e.g. LN60A01EP-LF)

** For Tape & Reel, add suffix -Z (e.g. LN60A01ES-Z).

For RoHS compliant packaging, add suffix -LF (e.g. LN60A01ES-LF-Z)

PACKAGE REFERENCE

TOP VIEW	TOP VIEW
Diagram of PDIP-8 package top view. Pin 1 is at the top left, pin 8 at the top right. Pin 2 is below pin 1, pin 7 below pin 2. Pin 3 is below pin 2, labeled 'Gate'. Pin 4 is below pin 3, labeled 'S3'. Pin 5 is at the bottom right, labeled 'GND'. Pin 6 is above pin 5, labeled 'D3'. Pin 7 is above pin 6, labeled 'D2'. Pin 8 is above pin 7, labeled 'D1'. A circle is shown inside the package outline.	Diagram of SOIC-8 package top view. Pin 1 is at the top left, pin 8 at the top right. Pin 2 is below pin 1, pin 7 below pin 2. Pin 3 is below pin 2, labeled 'Gate'. Pin 4 is below pin 3, labeled 'S3'. Pin 5 is at the bottom right, labeled 'GND'. Pin 6 is above pin 5, labeled 'D3'. Pin 7 is above pin 6, labeled 'D2'. Pin 8 is above pin 7, labeled 'D1'. A circle is shown inside the package outline.
PDIP-8	SOIC-8

ABSOLUTE MAXIMUM RATINGS ⁽¹⁾

Drain-Source Voltage V_{DS} 600V
 Gate-Source Voltage V_{GS} 15V
 Continuous Drain Current ⁽¹⁾ I_D 0.08A
 Pulsed Drain Current ⁽²⁾ I_{DM} 0.4A
 Power Dissipation ^{(1) (2)} P_D 1.3W
 Storage Temperature -55°C to +150°C

Recommended Operating Conditions

Operating Junction Temp (T_J) -20°C to +125°C

Thermal Resistance ⁽³⁾

	θ_{JA}	θ_{JC}
SOIC8	90 ... 45 ...	°C/W
PDIP8	105 ... 45 ...	°C/W

Notes:

- 1) Surface Mounted on 1"×1" FR4 Board..
- 2) Pulse width limited by maximum junction temperature.
- 3) Measured on JESD51-7, 4-layer PCB

ELECTRICAL CHARACTERISTICS

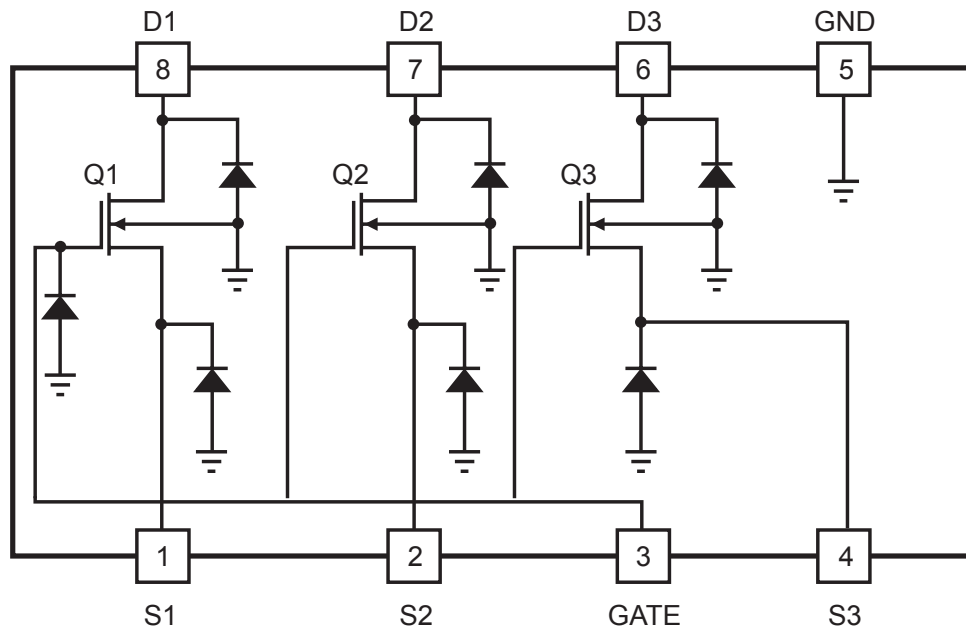
 $T_A = +25^{\circ}\text{C}$, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=30\mu A$		600		V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	0.8	1.0	1.2	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=400V, V_{GS}=0V$		15		μA
Drain-Source On-Resistance	$r_{DS(on)}$	$V_{GS}=10V, I_D=10mA$		190		Ω
		$V_{GS}=5V, I_D=10mA$		200		
Switching Parameter						
Turn-On Delay Time	$t_{(on)}$	$V_{DS}=350V, I_{DS}=10mA$		50		ns
Turn-Off Delay Time	$t_{(off)}$			3000		

PIN FUNCTIONS

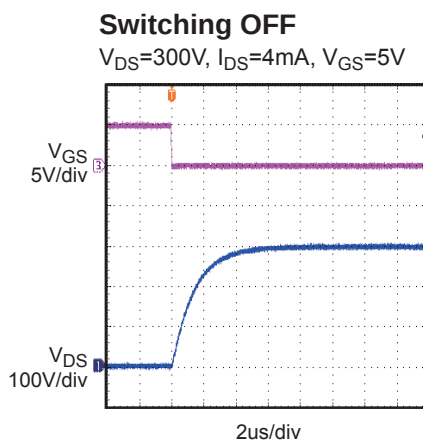
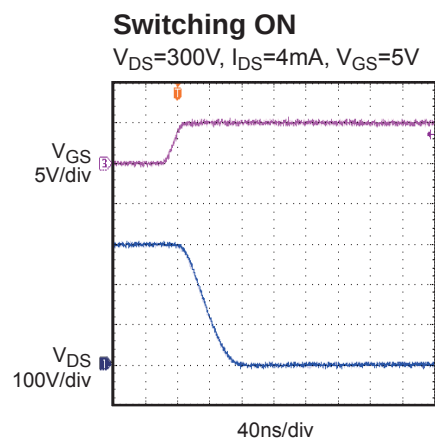
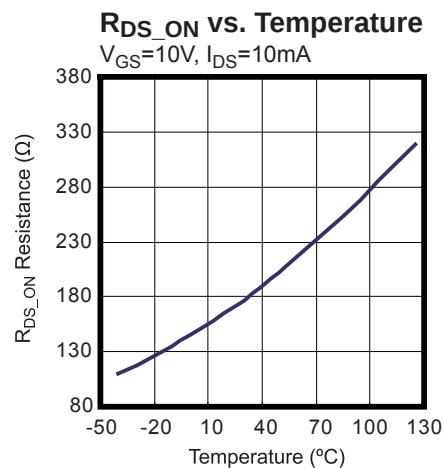
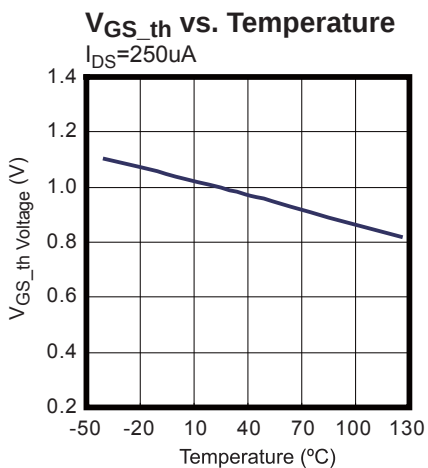
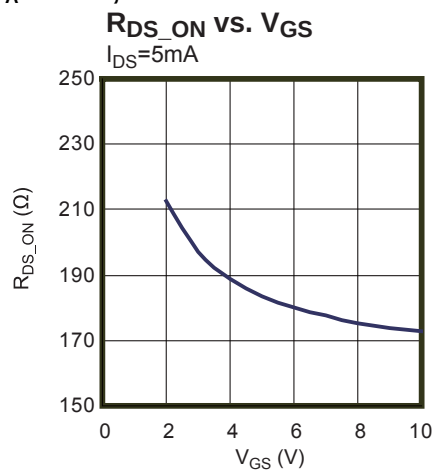
Pin Number	Pin Name	Description
1	S1	Source 1
2	S2	Source 2
3	Gate	Gate
4	S3	Source 3
5	GND	Ground
6	D3	Drain 3
7	D2	Drain 2
8	D1	Drain 1

DEVICE CIRCUIT



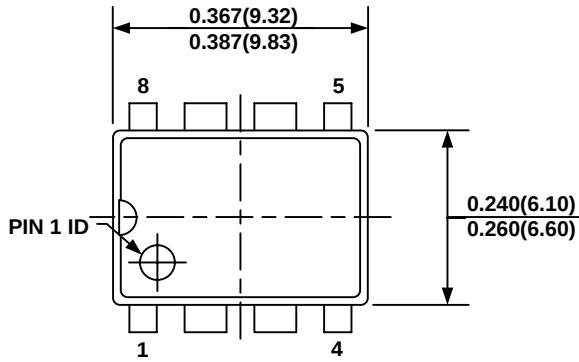
TYPICAL PERFORMANCE CHARACTERISTICS

$T_A = 25^\circ\text{C}$, unless otherwise noted.

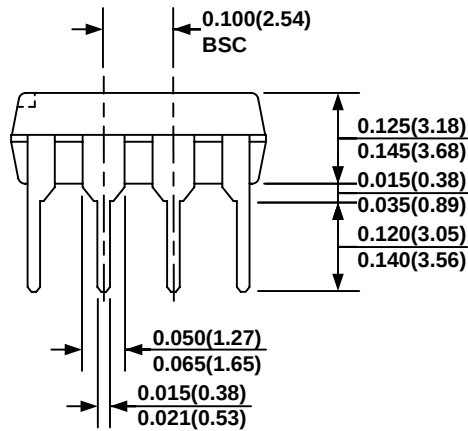


PACKAGE INFORMATION

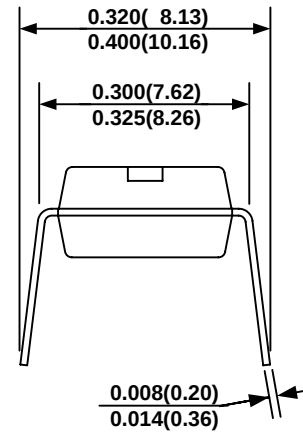
PDIP-8



TOP VIEW



FRONT VIEW

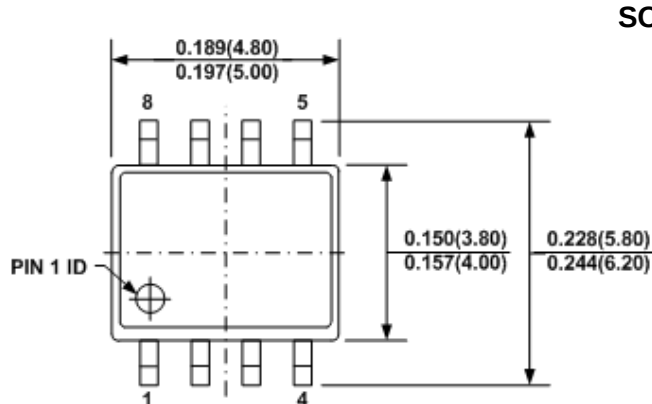


SIDE VIEW

NOTE:

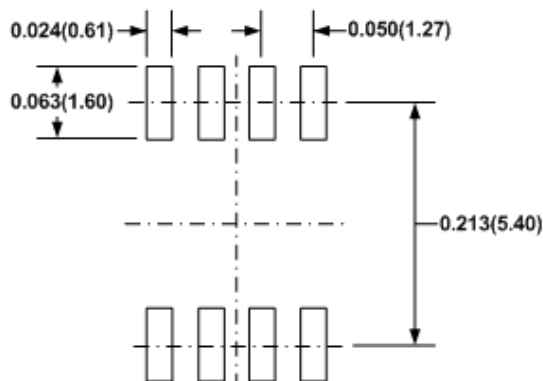
- 1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
- 2) PACKAGE LENGTH AND WIDTH DO NOT INCLUDE MOLD FLASH, OR PROTRUSIONS.
- 3) DRAWING CONFORMS TO JEDEC MS-001, VARIATION BA.
- 4) DRAWING IS NOT TO SCALE.

PACKAGE INFORMATION

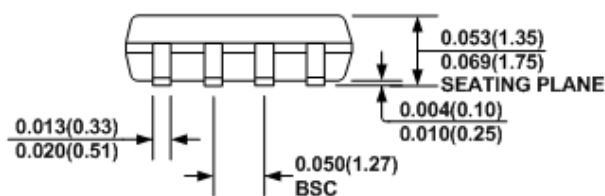


TOP VIEW

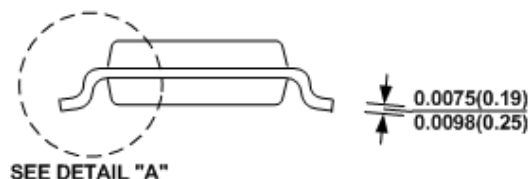
SOIC8



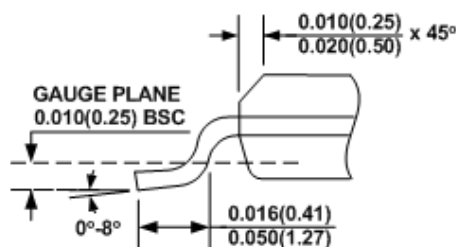
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL "A"

NOTE:

- 1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
- 2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
- 3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
- 4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
- 5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION AA.
- 6) DRAWING IS NOT TO SCALE.

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