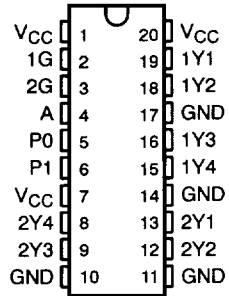


- Low Output Skew, Low Pulse Skew for Clock-Distribution and Clock-Generation Applications
- TTL-Compatible Inputs and Outputs
- Distributes One Clock Input to Eight Outputs
- Distributed V_{CC} and Ground Pins Reduce Switching Noise
- High-Drive Outputs ($-48\text{-mA } I_{OH}$, $48\text{-mA } I_{OL}$)
- State-of-the-Art EPIC-II B™ BiCMOS Design Significantly Reduces Power Dissipation
- Package Options Include Plastic Small-Outline (DW) and Shrink Small-Outline (DB) Packages

DB OR DW PACKAGE
(TOP VIEW)



description

The CDC340 is a high-performance clock-driver circuit that distributes one (A) input signal to eight (Y) outputs with minimum skew for clock distribution. Through the use of the control pins (1G and 2G), the outputs can be placed in a high state regardless of the A input.

The CDC340's propagation delays are adjusted at the factory using the P0 and P1 pins. These pins are not intended for customer use and should be strapped to GND.

The CDC340 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

INPUTS			OUTPUTS	
1G	2G	A	1Y1–1Y4	2Y1–2Y4
X	X	L	H	H
L	L	H	H	H
L	H	H	H	L
H	L	H	L	H
H	H	H	L	L

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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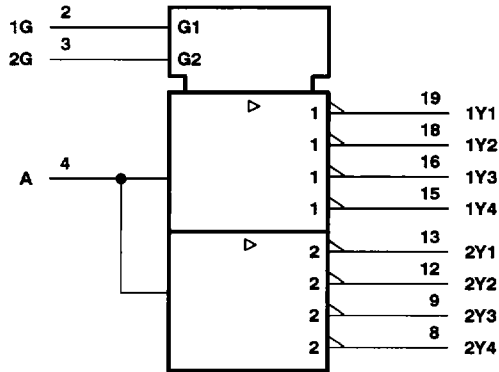
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CDC340

1-LINE TO 8-LINE CLOCK DRIVER

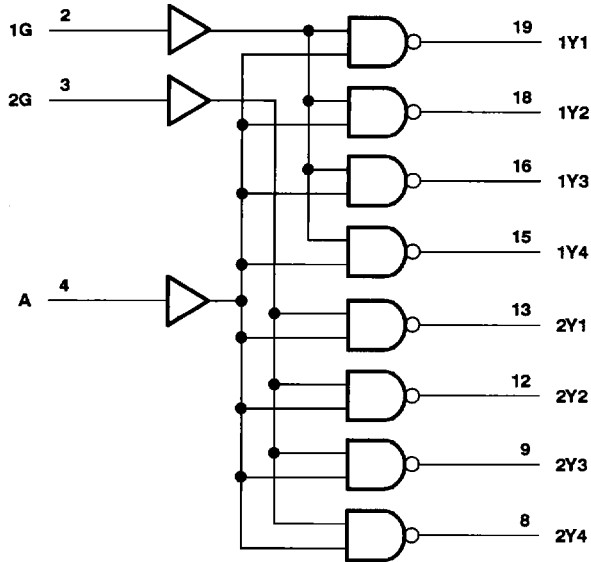
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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	-0.5 V to 7 V
Input voltage range, V_I (see Note 1)	-0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O	-0.5 V to $V_{CC} + 0.5$ V
Current into any output in the low state, I_O	96 mA
Input clamp current, I_{IK} ($V_I < 0$)	-18 mA
Storage temperature range	-65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and negative-voltage rating may be exceeded if the input clamp-current rating is observed.

recommended operating conditions (see Note 2)

	MIN	MAX	UNIT
V_{CC} Supply voltage	4.75	5.25	V
V_{IH} High-level input voltage	2		V
V_{IL} Low-level input voltage		0.8	V
V_I Input voltage	0	V_{CC}	V
I_{OH} High-level output current		-48	mA
I_{OL} Low-level output current		48	mA
f_{clock} Input clock frequency		80	MHz
T_A Operating free-air temperature	0	70	°C

NOTE 2: Unused pins (input or I/O) must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
		MIN	TYP [‡]	MAX			
V_{IK}	$V_{CC} = 4.75$ V, $I_I = -18$ mA			-1.2	-1.2		V
V_{OH}	$V_{CC} = 4.75$ V, $I_{OH} = -3$ mA	2.5			2.5		V
	$V_{CC} = 5$ V, $I_{OH} = -3$ mA	3			3		
	$V_{CC} = 4.75$ V, $I_{OH} = -48$ mA	2			2		
V_{OL}	$V_{CC} = 4.75$ V, $I_{OL} = 48$ mA				0.5		V
I_I	$V_{CC} = 5.25$ V, $V_I = V_{CC}$ or GND		± 1		± 1		μA
I_O^{\S}	$V_{CC} = 5.25$ V, $V_O = 2.5$ V	-50	-100	-200	-50	-200	mA
I_{CC}	$V_{CC} = 5.25$ V, $V_I = V_{CC}$ or GND, $I_O = 0$.	Outputs high	2		3.5		mA
		Outputs low	24		33		
C_i	$V_I = 2.5$ V or 0.5 V	3					pF

[‡] All typical values are at $V_{CC} = 5$ V.

^{\S} Not more than one output should be tested at a time, and the duration of the test should not exceed one second.



CDC340

1-LINE TO 8-LINE CLOCK DRIVER

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switching characteristics, $C_L = 50$ pF (see Figures 1 and 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5$ V, $T_A = 25^\circ$ C			$V_{CC} = 4.75$ V to 5.25 V, $T_A = 0^\circ$ C to 70° C		UNIT
			MIN	TYP	MAX	MIN	MAX	
t_{PLH}	A	Y	3.4		4.5	3	4.8	ns
t_{PHL}			3.2		4.3	2.8	4.7	
t_{PLH}	G	Y	2		3.8	2	4	ns
t_{PHL}			2		3.8	2	4	
$t_{sk(o)}$	A	Y		0.3	0.5		0.6	ns
$t_{sk(p)}$				0.6	0.8		0.9	
$t_{sk(pr)}$					1.1		1.1	
t_r	A	Y				1.5	ns	
t_f	A	Y				1.5	ns	

t_{pd} performance information relative to V_{CC} and temperature variation (see Note 3)

$Dt_{PLH}(T_A)^\dagger$	Temperature drift of t_{PLH} from 0° C to 70° C	-53 ps/ 10° C
$Dt_{PHL}(T_A)^\dagger$	Temperature drift of t_{PHL} from 0° C to 70° C	-58 ps/ 10° C
$Dt_{PLH}(V_{CC})^\ddagger$	V_{CC} drift of t_{PLH} from 4.75 V to 5.25 V	+43 ps/100 mV
$Dt_{PHL}(V_{CC})^\ddagger$	V_{CC} drift of t_{PHL} from 4.75 V to 5.25 V	-33 ps/100 mV

† Virtually independent of V_{CC}

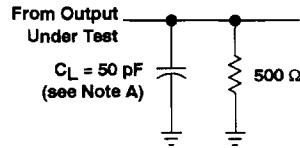
‡ Virtually independent of temperature

NOTE 3: The data extracted is from a wide range of characterization material.

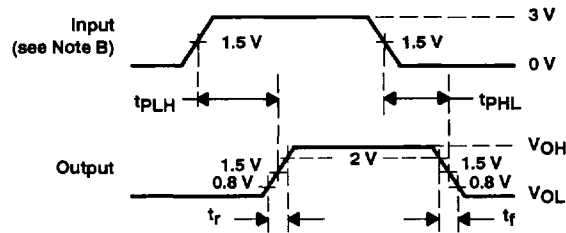


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PARAMETER MEASUREMENT INFORMATION



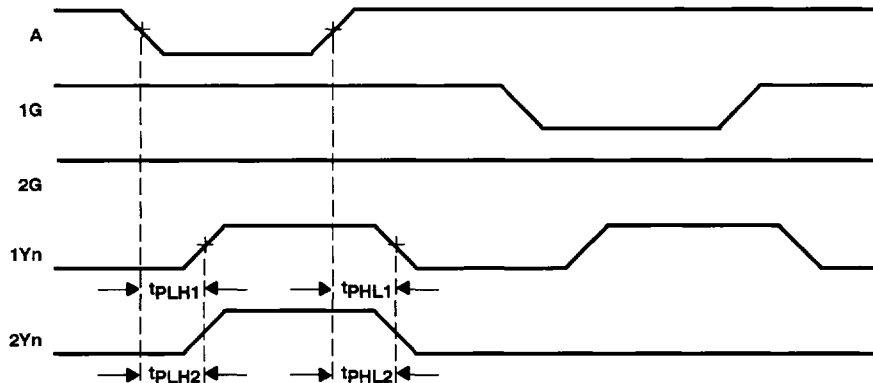
LOAD CIRCUIT FOR OUTPUTS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

- NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10$ MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.

Figure 1. Load Circuit and Voltage Waveforms



- NOTES: A. Output skew, $t_{sk(o)}$, is calculated as the greater of:
 - The difference between the fastest and slowest of t_{PLHn} ($n = 1, 2$)
 - The difference between the fastest and slowest of t_{PHLn} ($n = 1, 2$)
 B. Pulse skew, $t_{sk(p)}$, is calculated as the greater of $|t_{PLHn} - t_{PHLn}|$ ($n = 1, 2$).
 C. Process skew, $t_{sk(pr)}$, is calculated as the greater of:
 - The difference between the fastest and slowest of t_{PLHn} ($n = 1, 2$) across multiple devices under identical operating conditions
 - The difference between the fastest and slowest of t_{PHLn} ($n = 1, 2$) across multiple devices under identical operating conditions

Figure 2. Waveforms for Calculation of $t_{sk(o)}$, $t_{sk(p)}$, $t_{sk(pr)}$