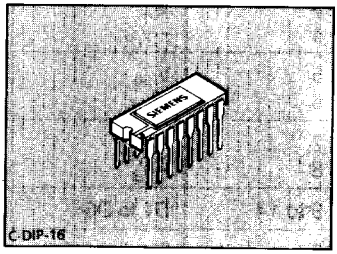
6-Bit A/D Converter, 50 MHz

SDA 6020

Bipolar IC

Features

- Conversion up to Nyquist frequency (25 MHz)
- 6-bit resolution (1.6%), simple extension to 8 bits
- 50 MHz strobe frequency
- ±1/2 LSB max. linearity error
- No sample and hold required
- Dynamic driving of reference inputs for analog addition and multiplication
- ECL-compatible (ECL → TTL matching possible, e.g. with SH 100.255
- Low power dissipation of 450 mW
- Logic-compatible supply voltage +5 V; −5.2 V



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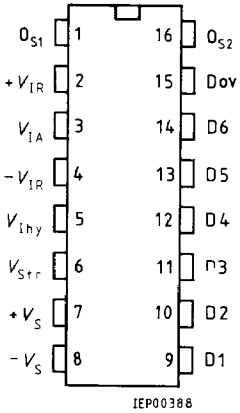
Type	Ordering Code	Package
■ S SDA 6020	Q67000-Y584	C-DIP-16

■ Not for new design

Pin Configuration

top view



Pin Definitions and Functions

Pin	Symbol	Function
1	0_{S1}	Digital ground
2	$+V_{IR}$	Positive reference voltage (< 2.5 V)
3	V_{IA}	Analog signal input (max. ± 2.5 V)
4	$-V_{IR}$	Negative reference voltage (> −2.5 V)
5	V_{Ihy}	Hysteresis control (0 V to +2.5 V)
6	V_{Str}	Strobe input (ECL)
7	$+V_S$	Positive supply voltage (+5 V)
8	$-V_S$	Negative supply voltage (−5.2 V)
9 to 14	D1 to D6	Data outputs, bits 1 to 6 (ECL)
15	D ov	Overflow
16	0_{S2}	Digital ground of output stages

Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Supply voltage	$+V_S$	−0.3	6.0	V
Supply voltage	$-V_S$	−6.0	0.3	V
Input voltages	$V_{IA}, +V_{IR} - V_{IR}$	−3.0	3.0	V
Strobe	V_{Str}	$-V_S$	0	V
Hysteresis control	V_{Ihy}	0	3.0	V
Voltage difference	$0_{S1} - 0_{S2}$	−0.5	0.5	V
Ambient temperature	T_A	0	70	°C
Junction temperature	T_j		150	°C
Storage temperature	T_{stg}	−55	125	°C
Thermal resistance System – air	$R_{th\ SA}$		70	K/W

Characteristics

Parameter	Symbol	Limit Values min.	typ.	max.	Unit
Power Supply					
Positive supply voltage	$+V_S$	4.5	5.0	5.5	V
Negative supply voltage	$-V_S$	−5.7	−5.2	−4.7	V
Current consumption					
at $+V_S = +5.0$ V; $V_{IA} \leq -V_{IR}$	I_S		30	60	mA
at $-V_S = -5.2$ V; $V_{IA} \leq -V_{IR}$	I_S		55	80	mA
Analog Section					
$T_A = 25\,°C$; $+V_S = 5$ V; $-V_S = 5.2$ V					
Signal Input					
Maximum input voltage	$V_{IA\,max}$	$-V_{IR\,min}$		$+V_{IR\,max}$	V
$V_{IA\,max} = \lvert(+V_{IR\,max}) - (-V_{IR\,min})\rvert$				5	V
V_{IA} for 6-bit resolution	V_{IA}		0.3		V
V_{IA} for 1/2 LSB linearity	V_{IA}	1.2	0.6		V
V_{IA} for 1/4 LSB linearity	V_{IA}	2.4	1.2		V
Input current					
at $V_{IA} = +V_{IR}$ in sample mode	I_{IA}		200	800	µA
at $V_{IA} < -V_{IR}$ in sample mode	I_{IA}	−10		10	µA
$-V_{IR} < V_{IA} < +V_{IR}$ in hold mode	I_{IA}	−10		10	µA
Input capacitance					
at $V_{IA} < -V_{IR}$	C_{IA}			35	pF
Reference Input					
Positive reference voltage	$+V_{IR}$	−2		2.5	V
Negative reference voltage	$-V_{IR}$	−2.5		2	V
Reference resistance	$64\,R$	96	128	256	Ω
Digital Section					
Strobe Input					
H-input voltage	V_{IH}	−1.1	−0.9	−0.6	V
L-input voltage	V_{IL}	−2.0	−1.7	−1.5	V
H-input voltage	I_{IH}	5	30	100	µA
L-input voltage	I_{IL}	5	30	100	µA
Data Outputs					
100 Ω to −2 V					
H-output voltage	V_{QH}	−1.1	−0.9	−0.6	V
L-output voltage	V_{QL}	−2.0	−1.7	−1.5	V

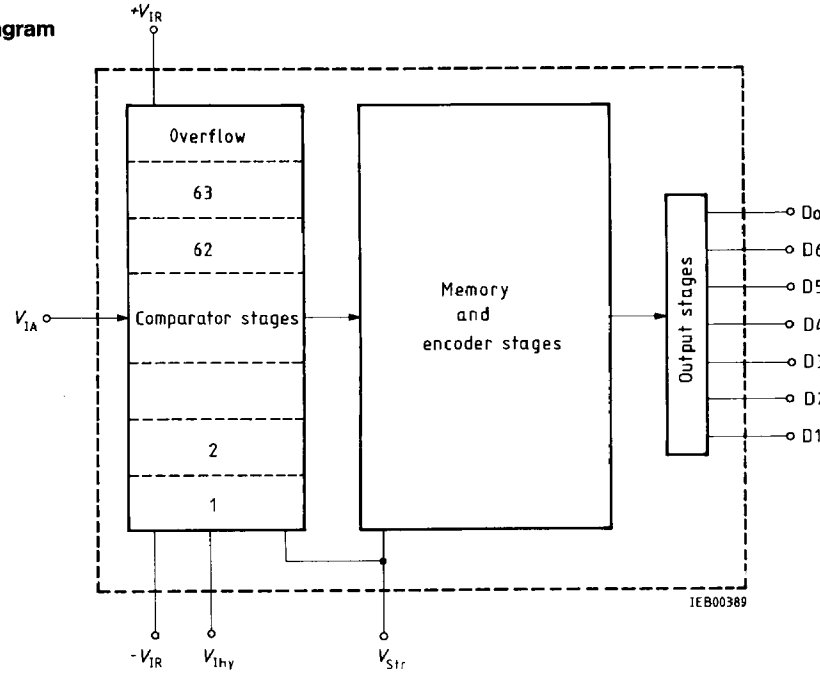
Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Dynamic Parameters					
Aperture time	t_D		2		ns
Aperture jitter			25		ps
Strobe	t_{strobe}		8	10[1]	ns
Signal transition time[2])	$t_{TLH\ Qmax}$		9		ns
Signal transition time[2])	$t_{THL\ Qmin}$		11		ns
Strobe frequency	f_{strobe}	50			MHz

1) Exceeding this value at strobe frequencies of less than 50 MHz is quite permissible as long as the remaining hold time is adequate for reliable data transfer.

2) The data transfer into the following circuit should occur with a delay t_D referred to the rising strobe edge in the range:

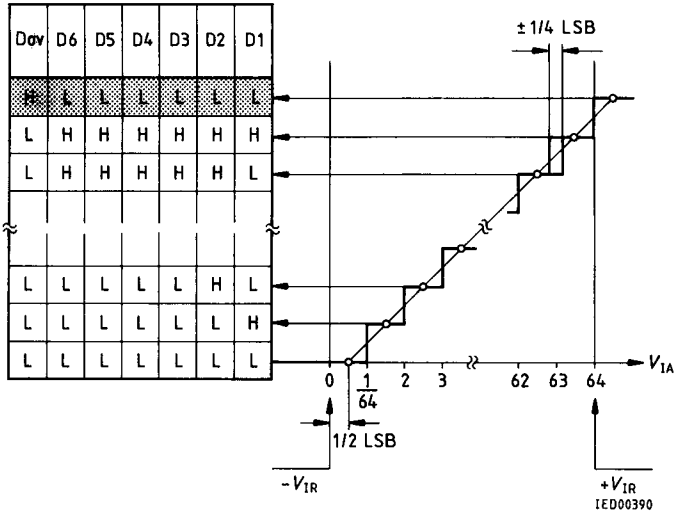
$$t_{TLH\ Qmax} + t_{hold/2} < t_D < t_{hold} + t_{THL\ Qmin}$$

Block Diagram

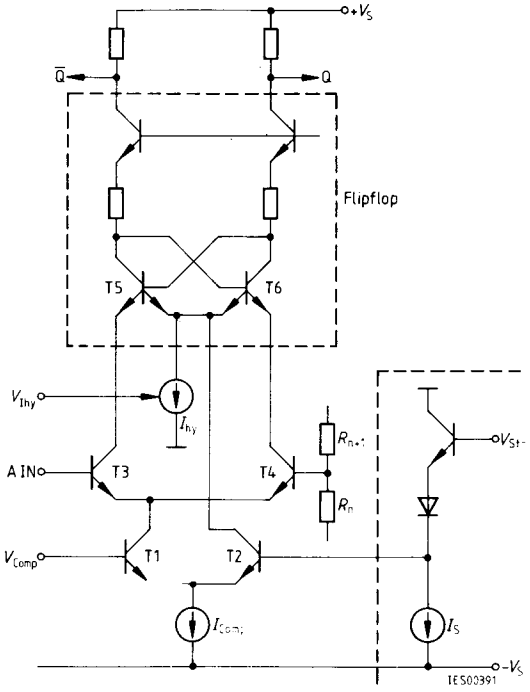


Transfer Characteristic and Truth Table

Dov	D6	D5	D4	D3	D2	D1
H	L	L	L	L	L	L
L	H	H	H	H	H	H
L	H	H	H	H	H	L
≈						≈
L	L	L	L	L	H	L
L	L	L	L	L	L	H
L	L	L	L	L	L	L

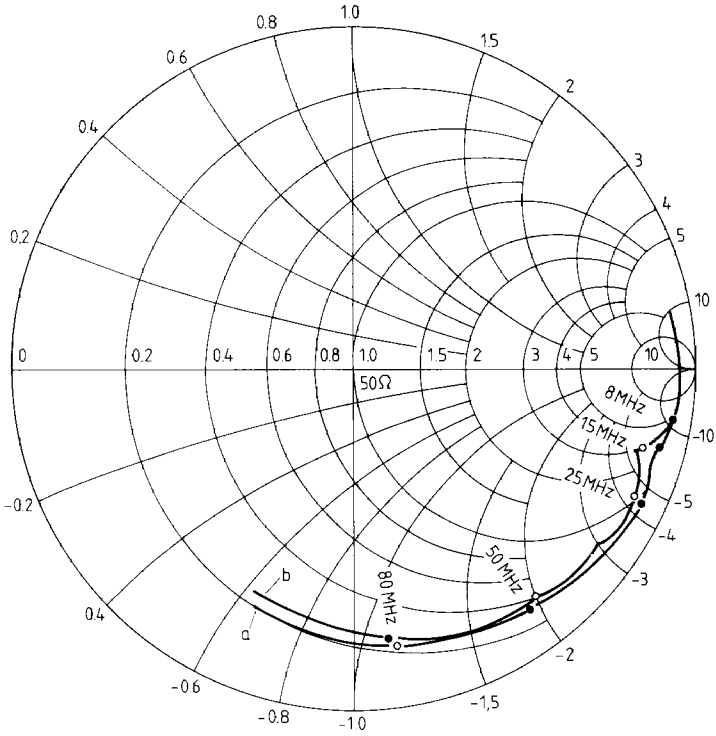


Input Stage

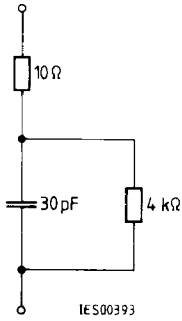


Smith Diagram

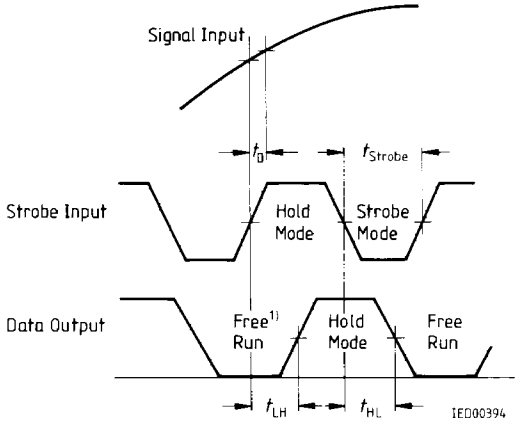
a) Nyquist plot of input impedance
b) Nyquist plot of equivalent circuit



Equivalent Circuit

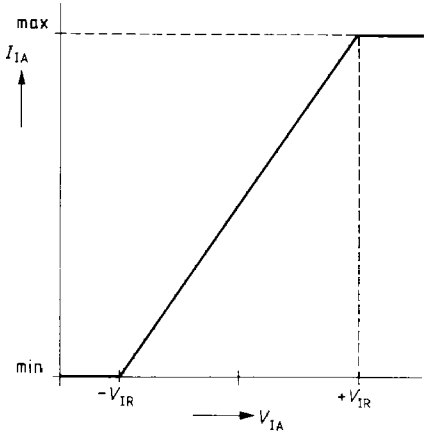


Pulse Diagram of Strobe Input and Data Outputs

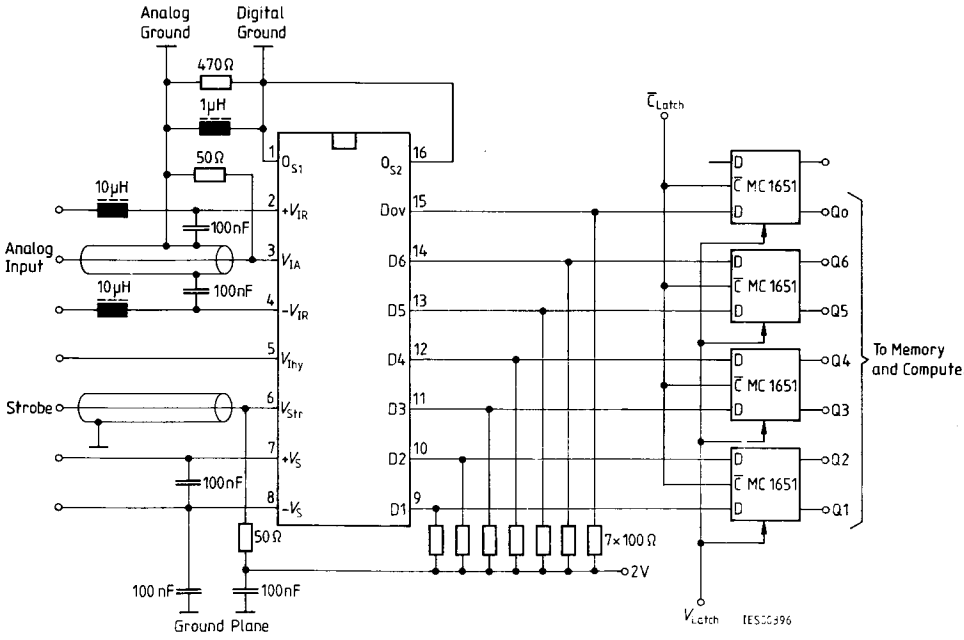


[1] undefined Output Levels

Input Current versus Input Voltage



Test Circuit



Test Circuit