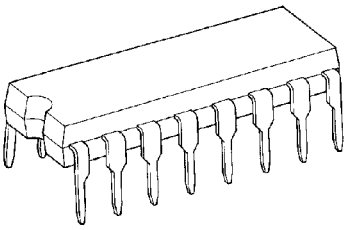
TENTATIVE TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC90A44P, TC90A44F

NTSC 2-LINE DIGITAL Y / C SEPARATION IC

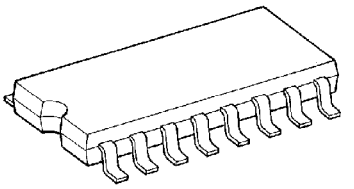
The TC90A44P, TC90A44F separates luminance (Y) and chrominance (C) signals from NTSC system composite video signal by using 2 horizontal (H) lines. It employs the Toshiba logical comb filter to reduce color dot interference and realizes high performance Y / C separation. The Y / C separation unit for TV and VCR set is able to assembled at low cost, because it requires few external parts and no adjustment.

TC90A44P



DIP16-P-300-2.54A

TC90A44F



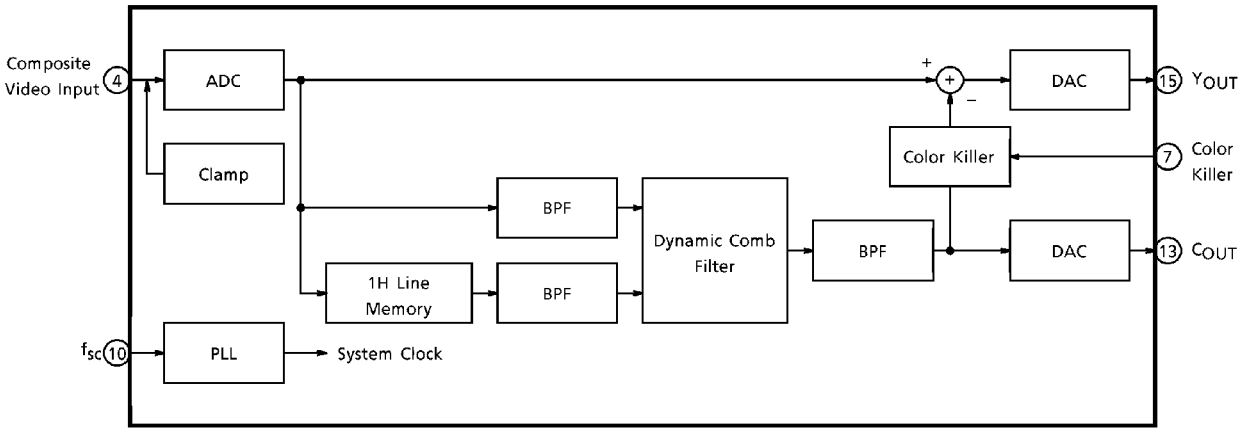
SOP16-P-300-1.27

Weight
DIP16-P-300-2.54A : 1.00g (Typ.)
SOP16-P-300-1.27 : 0.18g (Typ.)

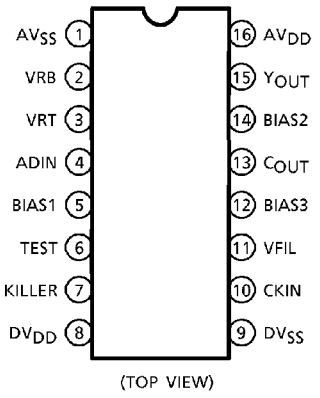
FEATURES

- TV system : NTSC
- PLL4 × multiplication circuit
- sync. tip clamping circuit
- Internal 8bit A / D converter
- Internal 8bit D / A converters (2ch.)
- 1H line memory
- Dynamic comb filter
- Color killer mode (Y / C separation OFF)
- DIP16 / SOP16 package
- 5V single power supply

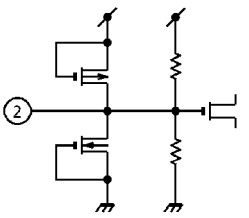
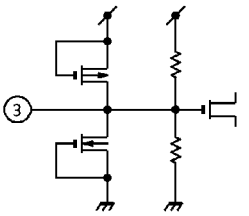
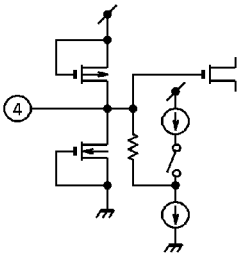
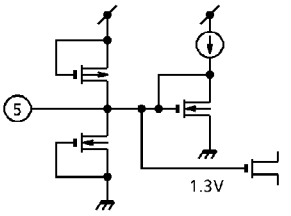
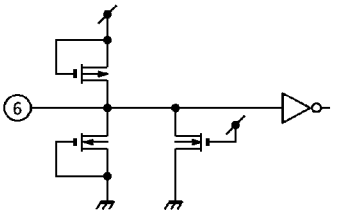
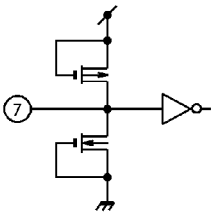
BLOCK DIAGRAM

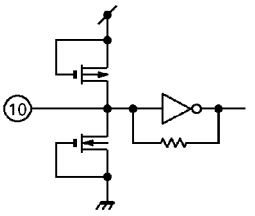
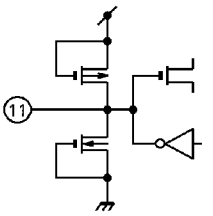
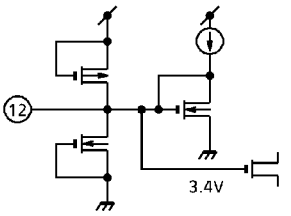
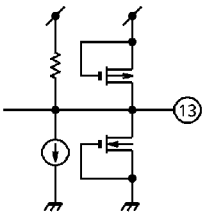
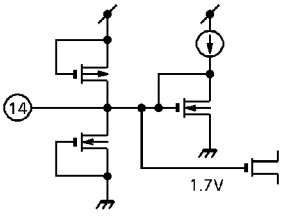
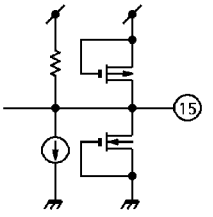


TERMINAL CONNECTION DIAGRAM



TERMINAL FUNCTION

PIN No.	NAME	FUNCTION	I/O	INTERFACE CIRCUIT
1	AV_{SS}	Ground for analog components.	—	—
2	VRB	ADC bias lower limit reference voltage. This defaults internally to approximately 2.25V, so this pin should normally be conected to ground (AV_{SS}) through a 0.01μF capacitor.	—	
3	VRT	ADC bias higher limit reference voltage. This defaults internally to approximately 2.8V, so this pin should normally be conected to ground (AV_{SS}) through a 0.01μF capacitor.	—	
4	ADIN	Composite video signal input.	I	
5	BIAS1	ADC bias voltage. This defaults internally to approximately 1.3V, so this pin should normally be conected to ground (AV_{SS}) through a 0.01μF capacitor.	—	
6	TEST	Test terminal. Normally connected to ground (DV_{SS}).	—	
7	KILLER	This pin is switch for color killer circuit. H : For B/W signal, Y/C separation OFF. L : Normal Y/C separation	I	

PIN No.	NAME	FUNCTION	I/O	INTERFACE CIRCUIT
8	DV_{DD}	Power supply for digital components (+5V).	—	—
9	DV_{SS}	Ground for digital components.	—	—
10	CKIN	Clock input. After applying capacitor for DC cut, input a color-burst-synchronized f_{sc} clock signal to this pin.	I	
11	VFIL	Connect a VCO filter to this pin.	—	
12	BIAS3	DAC bias voltage. This defaults internally to approximately 3.4V, so this pin should normally be conected to ground (AV_{SS}) through a 0.01μF capacitor.	—	
13	C_{OUT}	Chrominance signal output.	O	
14	BIAS2	DAC bias voltage. This defaults internally to approximately 1.7V, so this pin should normally be conected to ground (AV_{SS}) through a 0.01μF capacitor.	—	
15	Y_{OUT}	Luminance signal output.	O	
16	AV_{DD}	Power supply for analog components (+5V)	—	—

FUNCTION BLOCK DESCRIPTIONS

(1) Input clamp (CLAMP)

This is sync. tip clamp circuit for composite signal.
This circuit makes feedback so that the min. data after A / D converter at Y / C separation equal to internal DC bias level.

(2) A / D converter (ADC)

This is high speed series-parallel 8bit A / D converter. Input dynamic range is $1.0V_{p-p}$ (Typ.)

(3) Line memory

This block is DRAM line memory for 1H delay.

(4) Band-pass filter (BPF)

This filter extracts the signal of chrominance band from composite video signal. The center frequency is f_{SC}.

(5) Dynamic comb filter (DCF)

This block is logical comb filter to extract the chrominance signal. Filtering logic applies a correlation of two lines to reduce color dot crawl and cross color.

(6) Color killer circuit (KILLER)

This block is applied for black and white (B / W) signal white have no color burst. When pin 10 (KILLER) is "H", logic stop Y / C separation and output composite video signal from pin 14 (Y_{OUT}).

(7) PLL (4 times multiply clock generator)

This block is 4 times multiplier and makes $4f_{SC}$ as system clock.

(8) RTIM (Clock / memory timing generator)

This block supplies system clock ($4f_{SC}$) to each block via buffer and generates timing signal for memories.

(9) D / A converter (DAC)

This is high speed 8bit D / A converter. Output dynamic lange is $2.3V_{p-p}$ (Typ.).

MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC		SYMBOL	RATING	UNIT
Power Supply Voltage		V_{DD}	V_{SS}~V_{SS} + 6.5	V
Input Voltage		V_{IN}	− 0.3~V_{DD} + 0.3	V
Power Dissipation	TC90A44P	P_D (Note)	600	mW
	TC90A44F		440	
Storage Temperature		T_{stg}	− 55~125	°C

(Note) Ta = 70°C

RECOMMENDED OPERATING CONDITION

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Power Supply Voltage	V_{DD}	—	4.75	5.00	5.25	V
Input Voltage	V_{IN}	—	0	—	V_{DD}	V
Operating Temperature	T_{opr}	—	− 10	—	70	°C

ELECTRICAL CHARACTERISTICS

DC CHARACTERISTICS (Ta = 25°C, V_{DD} = 5V)

CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Power Supply Voltage		V_{DD}	1	CLOCK = 3.579545MHz V_{IN} = 0.75V_{p-p}	4.75	5.00	5.25	V
Supply Current		I_{DD}	1		45	60	75	mA
Output Voltage Level		Y_{OUT}	1		3.55	3.70	3.85	V
		C_{OUT}			3.70	3.85	4.00	
Terminal Voltage Level		VRB	1		2.15	2.25	2.35	V
		VRT			2.7	2.8	2.9	
		ADIN			2.35	2.45	2.55	
		BIAS1			1.0	1.3	1.7	
		BIAS2			1.2	1.7	2.1	
		BIAS3			3.0	3.4	4.0	
		VFIL			1.2	1.9	3.0	
		CKIN			1.8	2.3	2.8	
Input Voltage	High Level	V_{IH}	1		4	—	—	V
	Low Level	V_{IL}	1		—	—	1	V

AC CHARACTERISTICS

(1) Y output (Ta = 25°C, V_{DD} = 5V, input clock : 3.579545MHz 0.4V_{p-p}, S_1 = 1)

CHARACTERISTICS		SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Input Level		V_{IN}	1	0~140 IRE	—	0.75	—	V_{p-p}
Low Frequency Gain		G_V	1	S_2 = 1, S_3 = 1, S_4 = 2 V_{IN} = 15.73426kHz, 0.75V_{p-p}, Vdc = 2.5V	6.8	7.2	7.7	dB
Frequency Response	f_2 / f_1	MTF1	1	S_2 = 1, S_3 = 1, S_4 = 2 V_{IN} = 0.75V_{p-p}, Vdc = 2.5V	– 0.8	– 1.0	– 2.0	dB
	f_4 / f_1	MTF2			– 1.5	– 2.0	– 3.0	
Comb Characteristics	f_2 / f_3	COMBY	1		—	– 46	– 40	dB
Output Impedance		Zo	1	S_2 = 2, S_4 = 2 V_{IN} = 15.73426kHz, 0.75V_{p-p}, Vdc = 2.5V $Zo = \frac{V_1 - V_2}{V_2} \times 400$ V_1 : S_3 = 1, V_2 : S_3 = 2	250	400	700	Ω
Clock Leak ($4f_{sc}$ Components)		Lck	1	S_2 = 1, S_3 = 1, S_4 = 1 V_{IN} = No input	—	2	10	mV_{rms}
Clock Leak (f_{sc} Components)		Lsc	1	S_2 = 1, S_3 = 1, S_4 = 1 V_{IN} = No input	—	1	3	mV_{rms}

(Note) $f_1 = fH = 15.73426kHz$, $f_2 = f_{sc} = 3.579545MHz$, $f_3 = f_{sc} + 1/2fH = 3.587412MHz$,
$f_4 = 1/3\ (4f_{sc}) = 4.772727MHz$

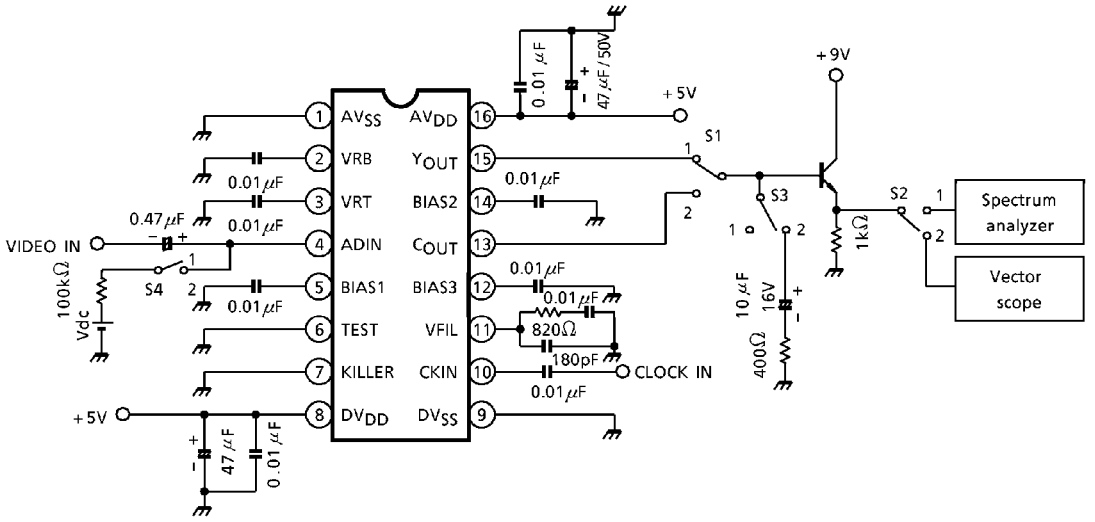
(2) C output (Ta = 25°C, V_{DD} = 5V, input clock : 3.579545MHz 0.4V_{p-p}, S_1 = 2)

CHARACTERISTICS	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Gain	C_V	1	S_2 = 1, S_3 = 1, S_4 = 1 V_{IN} = 0.75V_{p-p}	5.7	6.2	6.7	dB
BPF Characteristics	BWCW	1	S_2 = 2, S_3 = 1, S_4 = 2 V_{IN} = 0.75V_{p-p}, Vdc = 2.5V (f_{sc} – 503496Hz) – (f_{sc})	– 2.5	– 1.9	– 1.5	dB
Comb Characteristics	COMBC	1	S_2 = 1, S_3 = 1, S_4 = 2 V_{IN} = 0.75V_{p-p}, Vdc = 2.5V	—	– 38	– 35	dB
Differential Gain	DG	1	S_2 = 1, S_3 = 1, S_4 = 1 Modulated lamp signal 140 IRE : 0.75V	0	2	5	%
Differential Phase	DP			0	2	5	°
Output Impedance	Zo	1	S_2 = 2, S_4 = 2 V_{IN} = 15.73426kHz, 0.75V_{p-p}, Vdc = 2.5V $Zo = \frac{V_1 - V_2}{V_2} \times 400$ V_1 : S_3 = 1, V_2 : S_3 = 2	250	400	700	Ω
Clock Leak (4f_{sc} Components)	Lck	1	S_2 = 1, S_3 = 1, S_4 = 1 V_{IN} = No input	—	2	10	mV_{rms}
Fundamental Clock Leak (f_{sc} Components)	Lsc	1	S_2 = 1, S_3 = 1, S_4 = 1 V_{IN} = No input	—	1	3	mV_{rms}

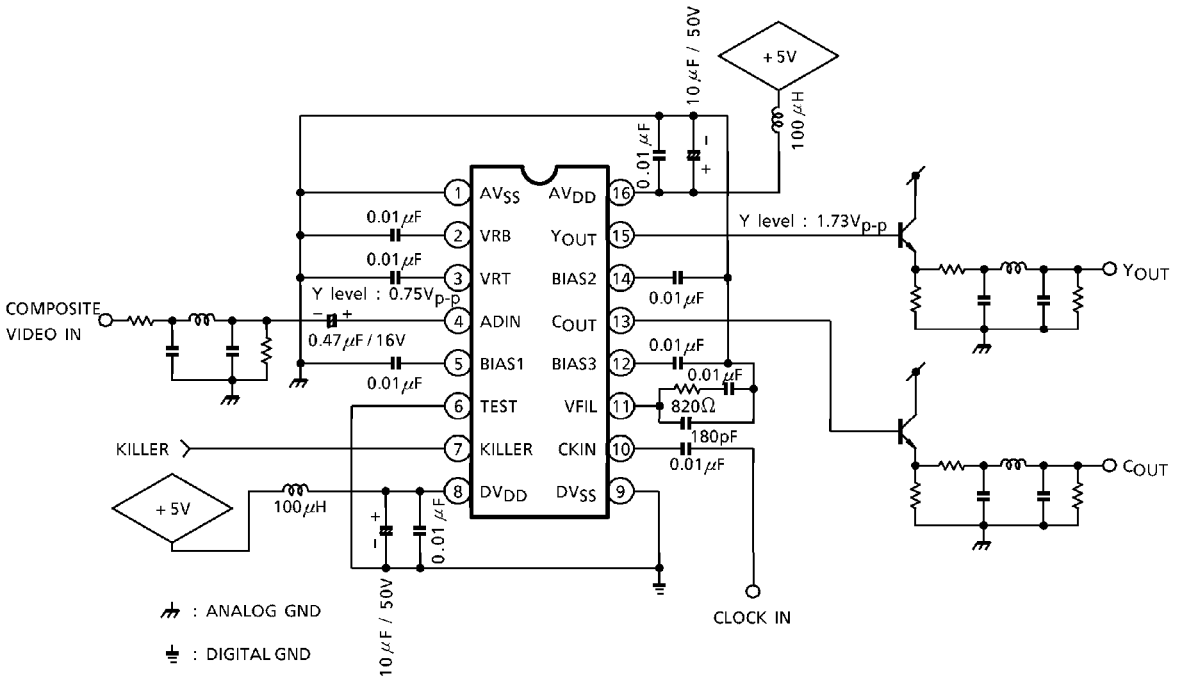
(3) PLL circuit characteristics

CHARACTERISTICS	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Pull-In Frequency Range	fck	1	—	3.5	3.6	3.7	MHz
Input Amplitude (f_{sc} Components)	Vck	1	—	0.35	0.5	—	V_{p-p}

TEST CIRCUIT 1



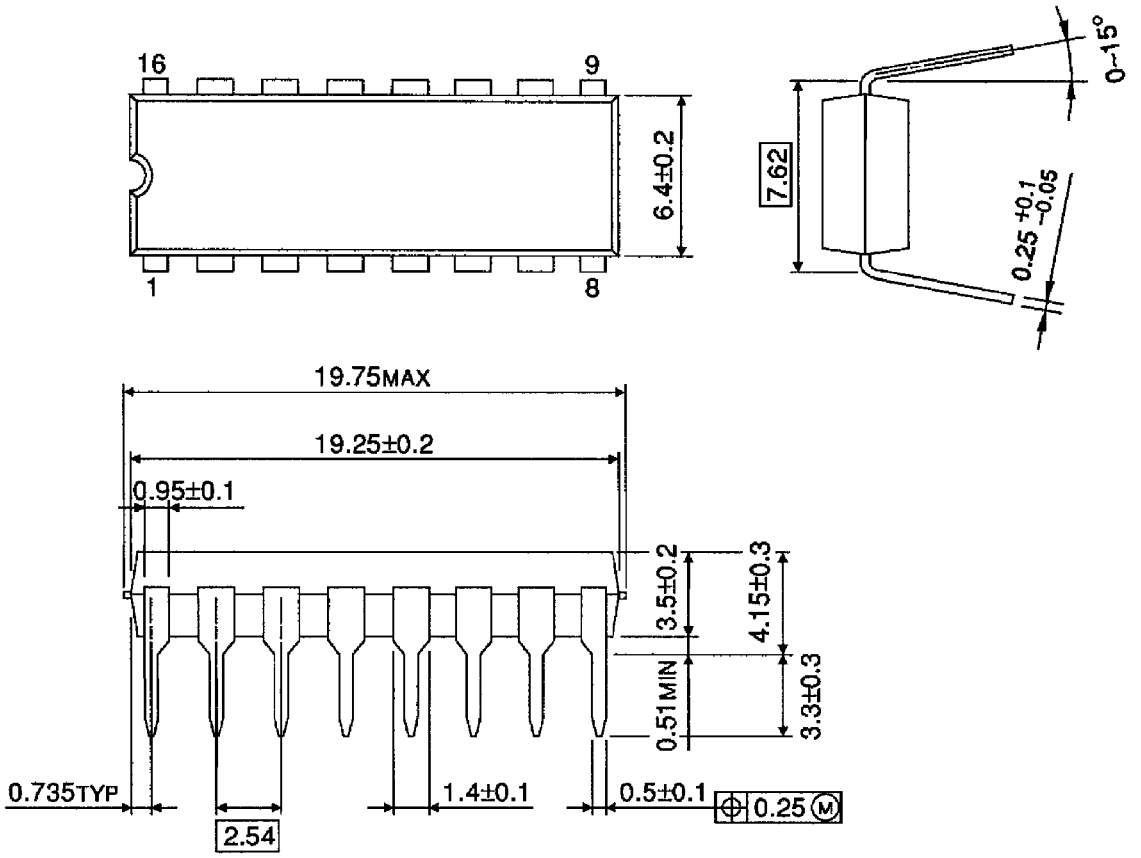
APPLICATION CIRCUIT



OUTLINE DRAWING

DIP16-P-300-2.54A

Unit : mm

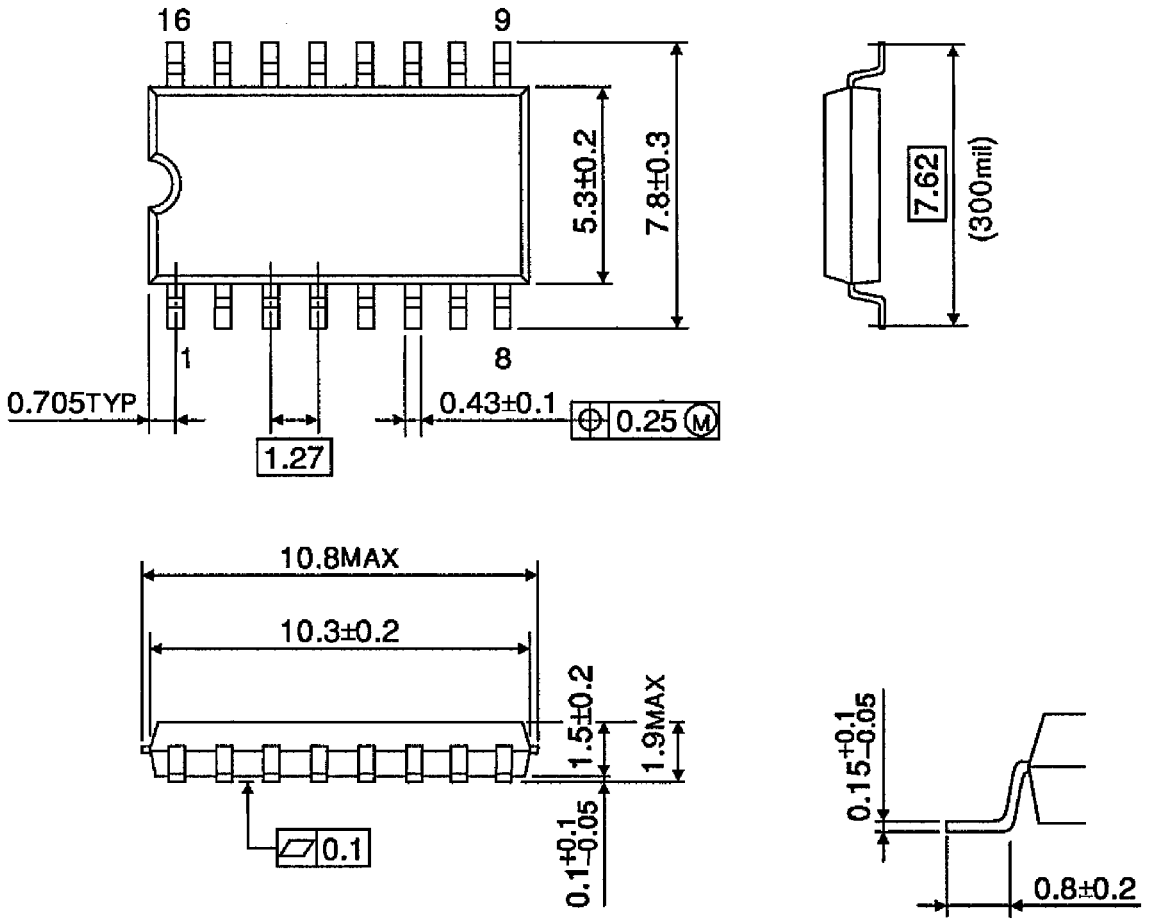


Weight : 1.00g (Typ.)

OUTLINE DRAWING

SOP16-P-300-1.27

Unit : mm



Weight : 0.18g (Typ.)