Integrated Device Technology, Inc.

2 x 16K x 60 DATA/INSTRUCTION WITH RESETTABLE TAG/VALID CACHE MODULE FOR IDT79R3000 CPU (MULTIPROCESSOR)

IDT7MB6061

FEATURES:

- High-speed 240K-Byte CMOS static RAM module constructed to support the IDT79R3000 CPU, in a multiprocessor system as a complete data and instruction cache
- Additional data and instruction address invalidation latches on-board to facilitate use in a multi-processor system
- $\overline{RESET}$ pin invalidates instruction cache in one operation
- Operating frequencies to support 12MHz, 16.7MHz, 20MHz, 25MHz and 33MHz IDT79R3000
- Available in a high density, low profile 120-pin QIP (Quad In-Line Package)
- Surface mounted SOs on a multilayer epoxy substrate
- Multiple ground pins for maximum noise immunity
- TTL compatible I/Os
- Single 5V (±10%) power supply

PIN CONFIGURATION

GND	1	61	GND	GND	120	60	Vcc
D_0	2	62	D_1	D_{58}	119	59	D_{59}
D_2	3	63	D_3	D_{56}	118	58	D_{57}
D_4	4	64	D_5	D_{54}	117	57	D_{55}
D_6	5	65	D_7	D_{52}	116	56	D_{53}
$\overline{WE_1}$	6	66	$\overline{OE_1}$	$\overline{WE_4}$	115	55	$\overline{OE_4}$
$\overline{CS_1}$	7	67	Vcc	GND	114	54	GND
D_8	8	68	D_9	D_{50}	113	53	D_{51}
D_{10}	9	69	D_{11}	D_{48}	112	52	D_{49}
$P1A_0$	10	70	$P1A_1$	$P2A_0$	111	51	$P2A_1$
$P1A_2$	11	71	$P1A_3$	$P2A_2$	110	50	$P2A_3$
$P1A_4$	12	72	$P1A_5$	$P2A_4$	109	49	$P2A_5$
P1LE1	13	73	P1LE2	P2LE1	108	48	GND
$P1A_6$	14	74	$P1A_7$	$P2A_6$	107	47	$P2A_7$
$P1A_8$	15	75	$P1A_9$	$P2A_8$	106	46	$P2A_9$
$P1A_{10}$	16	76	$P1A_{11}$	$P2A_{10}$	105	45	$P2A_{11}$
$P1A_{12}$	17	77	$P1A_{13}$	$P2A_{12}$	104	44	$P2A_{13}$
$\overline{P1OE_1}$	18	78	GND	$\overline{P21OE_1}$	103	43	$\overline{RESET}$
D_{12}	19	79	D_{13}	D_{46}	102	42	D_{47}
D_{14}	20	80	D_{15}	D_{44}	101	41	D_{45}
D_{16}	21	81	D_{17}	D_{42}	100	40	D_{43}
D_{18}	22	82	D_{19}	D_{40}	99	39	D_{41}
$\overline{WE_2}$	23	83	$\overline{OE_2}$	$\overline{WE_3}$	98	38	$\overline{OE_3}$
GND	24	84	GND	Vcc	97	37	$\overline{CS_2}$
D_{20}	25	85	D_{21}	D_{38}	96	36	D_{39}
D_{22}	26	86	D_{23}	D_{36}	95	35	D_{37}
D_{24}	27	87	D_{25}	D_{34}	94	34	D_{35}
D_{26}	28	88	D_{27}	D_{32}	93	33	D_{33}
D_{28}	29	89	D_{29}	D_{30}	92	32	D_{31}
Vcc	30	90	Vcc	Vcc	91	31	GND

QIP
TOP VIEW

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DESCRIPTION:

The IDT7MB6061 is a 240K-byte high-speed CMOS static RAM cache module constructed on a multilayer epoxy substrate (FR-4). The data cache uses the IDT6198 (16K x 4) SRAMs while the instruction cache uses both the IDT6198 and the IDT6178 (4K x 4) Resettable SRAMs; both cache sharing the 60-bit data bus.

Both cache also have a set of IDT74FCT373 latches to interface with the address bus. The data cache has an additional set of latches so each processor within the multiprocessor system has the ability to invalidate the data cache.

The instruction cache uses the IDT6178 (4K x 4) Cache Tag SRAMs for D_{36}-D_{59}. These bits cover the Tag and Valid bit fields. Address bits A_2-A_{13} are used for this portion of the instruction cache (i.e. there are four words per line in this cache). Asserting $\overline{RESET}$ will clear D_{36}-D_{59} to zeros in a single operation.

All inputs and outputs of the IDT7MB6061 are TTL-compatible and operate from a single 5V supply. Fully asynchronous circuitry is used, reqiring no clocks or refreshing for operation.

PIN NAMES

D_0–D_{59}	Data Inputs/Outputs
$P1A_0$–$P1A_{11}$	Address Inputs
$P2A_0$–$P2A_{11}$	Invalidate Address
$P1LE_1$	Data Address Latch Enable
$P1LE_2$	Instruction Address Latch Enable
$\overline{P1OE}$	Data Address Enable
$\overline{P2OE}$	Instruction Address Enable
P2LE	Invalidate Data Address Latch Enable
$\overline{RESET_1}$	Data Cache Reset
$\overline{RESET_2}$	Instruction Cache Reset
$\overline{WE_1}$–$\overline{WE_4}$	Write Enables
$\overline{OE_1}$–$\overline{OE_4}$	Output Enables
GND	Ground
Vcc	Power Supply

2755 bl 01

NOTE:

1. For module dimensions, please refer to drawing M27 in the packaging section.

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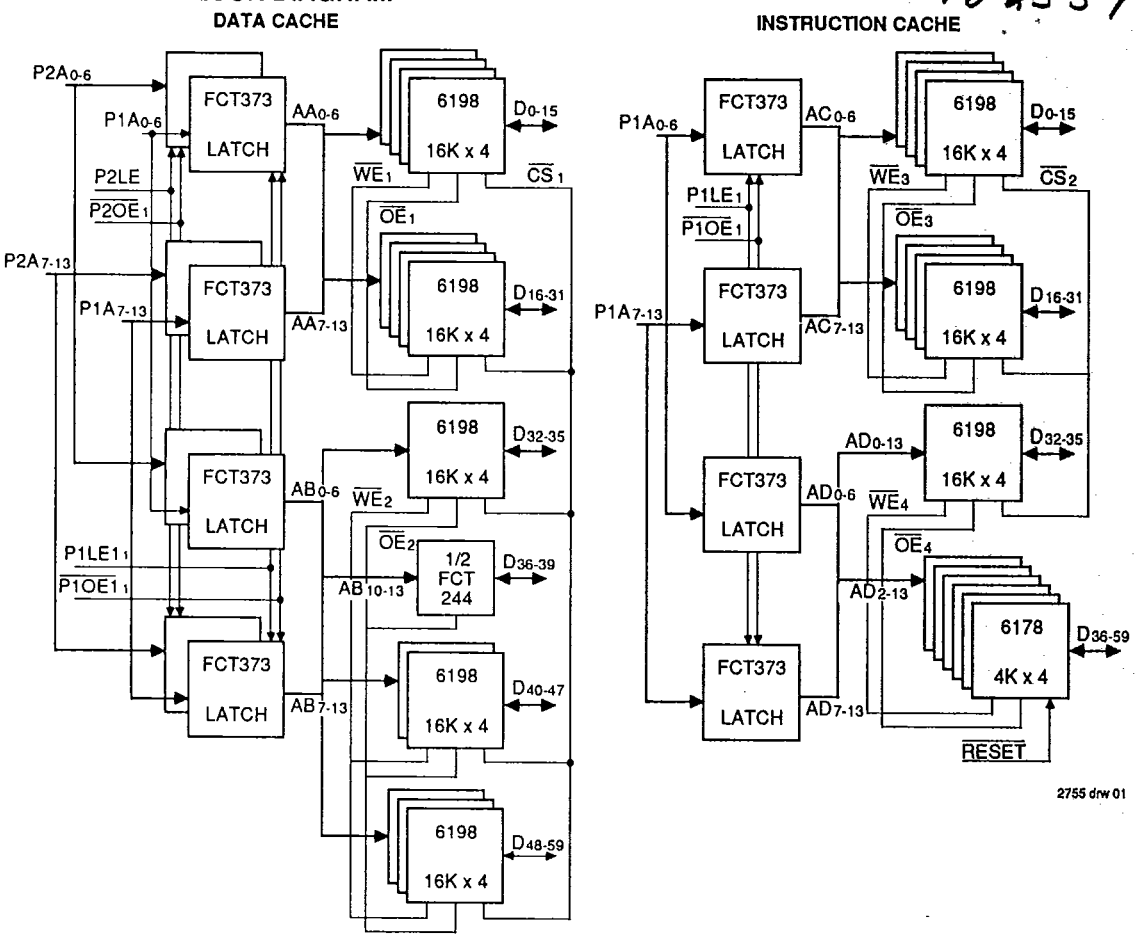
FUNCTIONAL BLOCK DIAGRAM



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RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6	V
V_{IL}	Input Low Voltage	-0.5[1]	—	0.8	V

NOTE: 2755 tbl 04
1. V_{IL} = -3.0V for pulse width less than 20ns.

CAPACITANCE

Symbol	Parameter[1]	Conditions	Typ.	Unit
$C_{IN(D)}$	Input Capacitance (Data)	V_{IN} = 0V	20	pF
$C_{IN(A)}$	Input Capacitance (Address)	V_{IN} = 0V	40	pF
$C_{IN(C)}$	Input Capacitance ($\overline{OE}$, $\overline{WE}$)	V_{IN} = 0V	50	pF
$C_{IN(C)}$	Input Capacitance ($\overline{CS}$)	V_{IN} = 0V	100	pF
$C_{IN(C)}$	Input Capacitance (LE, $\overline{PxOE}$)	V_{IN} = 0V	30	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	20	pF

NOTE: 2755 tbl 03
1. This parameter is guaranteed by design, but not tested.

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Value	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	–10 to +85	°C
T_{STG}	Storage Temperature	–55 to +125	°C
I_{OUT}	DC Output Current	50	mA

NOTE: 2755 tbl 02
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	5V ± 10%

2755 tbl 05

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	10ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

2755 tbl 06

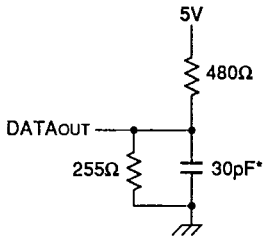

Figure 1. Output Load

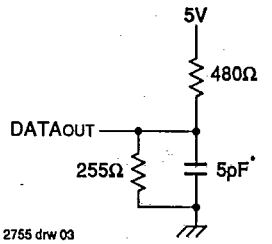

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Figure 2. Output Load (for tOLZ and tOHZ)

* Including scope and jig.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_A = 0°C to +70°C)

Symbol	Parameter	Test Conditions	12MHz		16.7MHz		20MHz		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
$\|I_{LI}\|$	Input Leakage	V_{CC} = Max., V_{IN} = GND to V_{CC}	—	20	—	20	—	20	µA
$\|I_{LO}\|$	Output Leakage	V_{CC} = Max., $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	—	10	—	10	—	10	µA
I_{CC1}	Operating Current	f = 0, $\overline{CS}$ = V_{IL}; V_{CC} = Max., Outputs Open	—	2925	—	2925	—	2925	mA
I_{CC2}	Dynamic Operating Current	V_{CC} = Max., $\overline{CS}$ = V_{IL}; f = f_{MAX}, Outputs Open	—	3850	—	3900	—	4150	mA
I_{SB1}	Full Standby Supply Current	$\overline{CS}$ ≥ V_{CC} - 0.2V, V_{IN} ≥ V_{CC} - 0.2V or ≤ 0.2V	—	450	—	450	—	450	mA
I_{SB}	Standby Power Supply Current	V_{CC} = Max., $\overline{CS}$ ≥ V_{IH}; f = f_{MAX}, Outputs Open	—	1300	—	1425	—	1575	mA
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = -4mA	2.4	—	2.4	—	2.4	—	V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 8mA	—	0.4	—	0.4	—	0.4	V

NOTE:
1. I_{CC1}, I_{CC2} in the case for all devices selected (i.e. both instruction and data cache selected).

2755 tbl 07

DC ELECTRICAL CHARACTERISTICS (Continued)

(V_{CC} = 5V ± 10%, T_A = 0°C to +70°C)

Symbol	Parameter	Test Conditions	25MHz		33MHz		Unit
			Min.	Max.	Min.	Max.	
$\|I_{LI}\|$	Input Leakage	V_{CC} = Max., V_{IN} = GND to V_{CC}	—	20	—	20	µA
$\|I_{LO}\|$	Output Leakage	V_{CC} = Max., $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	—	10	—	10	µA
I_{CC1}	Operating Current	f = 0, $\overline{CS}$ = V_{IL}; V_{CC} = Max., Outputs Open	—	3400	—	3700	mA
I_{CC2}	Dynamic Operating Current	V_{CC} = Max., $\overline{CS}$ = V_{IL}; f = f_{MAX}, Outputs Open	—	4675	—	4900	mA
I_{SB1}	Full Standby Supply Current	$\overline{CS}$ ≥ V_{CC} - 0.2V, V_{IN} ≥ V_{CC} - 0.2V or ≤ 0.2V	—	600	—	960	mA
I_{SB}	Standby Power Supply Current	V_{CC} = Max., $\overline{CS}$ ≥ V_{IH}; f = f_{MAX}, Outputs Open	—	1700	—	2000	mA
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = -4mA	2.4	—	2.4	—	V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 8mA	—	0.4	—	0.4	V

NOTE:
1. I_{CC1}, I_{CC2} in the case for all devices selected (i.e. both instruction and data cache selected).

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AC ELECTRICAL CHARACTERISTICS

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(V_{CC} = 5V ± 10%, T_A = 0°C to +70°C)

Symbol	Parameter	12MHz		16.7MHz		20MHz		25MHz		33MHz		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE												
t_{LE}	Latch Enable Width	6	—	6	—	6	—	6	—	6	—	ns
t_{AS}	Address Setup Time to LE	2	—	2	—	2	—	2	—	2	—	ns
t_{AH}	Address Hold Time from LE	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
t_{AA}[2]	Address Access Time	—	45	—	35	—	30	—	25	—	20	ns
t_{ACS}	Chip Select Time	—	40	—	30	—	25	—	20	—	15	ns
t_{OE}[3]	Output Enable to Output Valid	—	22	—	17	—	11	—	8	—	5	ns
t_{OHZ}[1]	Output Disable to Output in High Z	2	16	2	14	2	10	2	8	2	6	ns
t_{OLZ}[1]	Output Enable to Output in Low Z	5	—	5	—	5	—	5	—	5	—	ns
WRITE CYCLE												
t_{LE}	Latch Enable Width	6	—	6	—	6	—	6	—	6	—	ns
t_{AS}	Address Setup Time to LE	2	—	2	—	2	—	2	—	2	—	ns
t_{AH}	Address Hold Time to LE	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
t_{AW}[2]	Address Valid to End of Write	40	—	30	—	25	—	23	—	20	—	ns
t_{CW}	Chip Select to End of Write	35	—	25	—	20	—	18	—	15	—	ns
t_{WP}	Write Pulse Width	30	—	25	—	20	—	17	—	12	—	ns
t_{DW}	Data Valid to End of Write	20	—	13	—	13	—	11	—	8	—	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	0	—	0	—	ns
t_{LOE}[4]	Latch Output Enable	—	7	—	7	—	7	—	7	—	7	ns
RESET CYCLE												
t_{CLPW}	$\overline{RESET}$ Pulse Width	40	—	40	—	30	—	30	—	25	—	ns
t_{CLRC}	$\overline{RESET}$ High to $\overline{WE_4}$ Low	5	—	5	—	5	—	5	—	5	—	ns

NOTE:
1. This parameter is guaranteed by design, but not tested.
2. LE asserted.
3. $\overline{OE_1}$, $\overline{OE_2}$, $\overline{OE_3}$, $\overline{OE_4}$.
4. P1OE1 and P2OE1.

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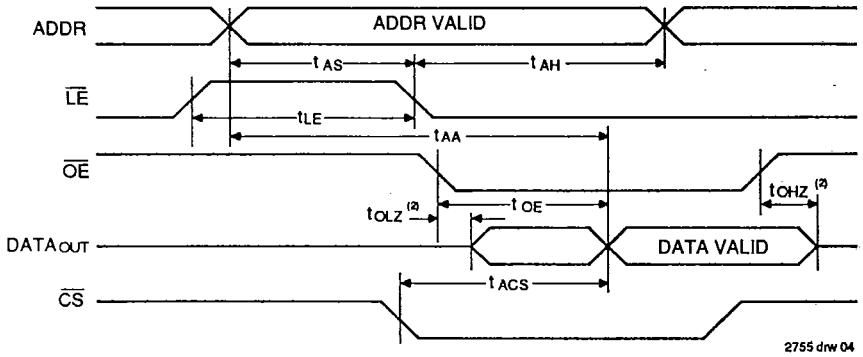
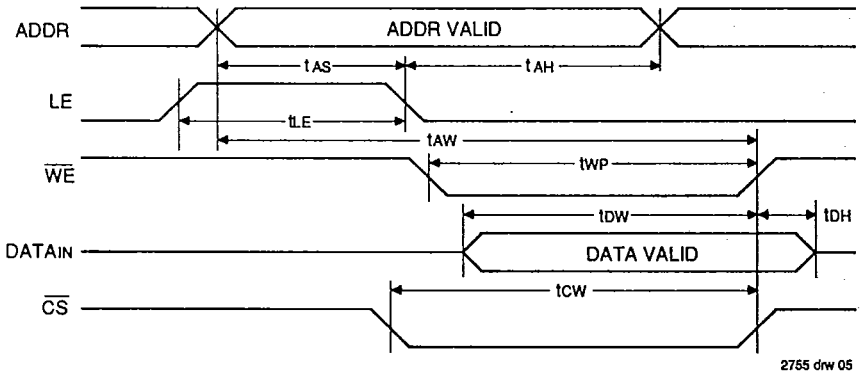
TIMING WAVEFORM OF READ CYCLE(1)

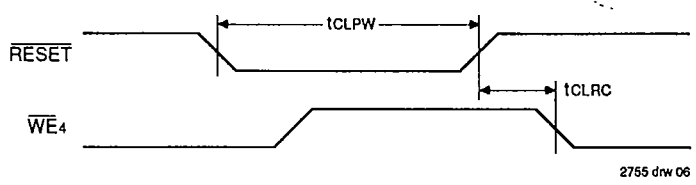


NOTE:
1. Assume $\overline{WE}$ is active high throughout this cycle.
2. This parameter is guaranteed by design but not tested.

TIMING WAVEFORM OF WRITE CYCLE



TIMING WAVEFORM OF $\overline{RESET}$ CYCLE



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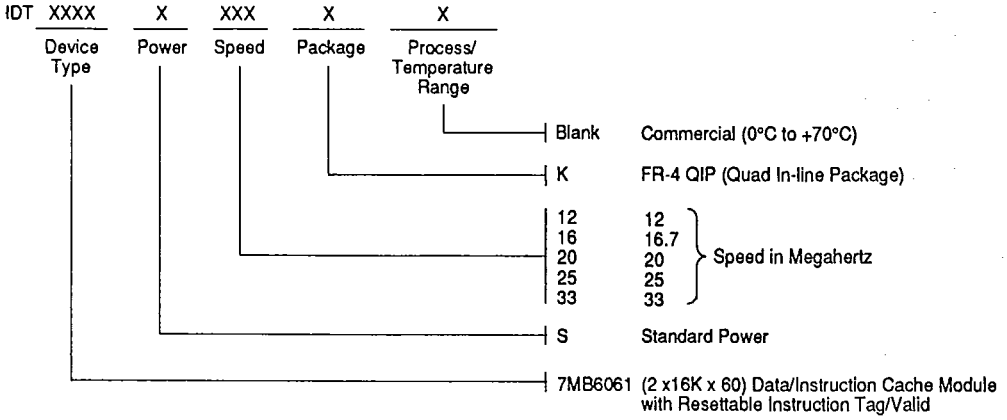
ORDERING INFORMATION



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