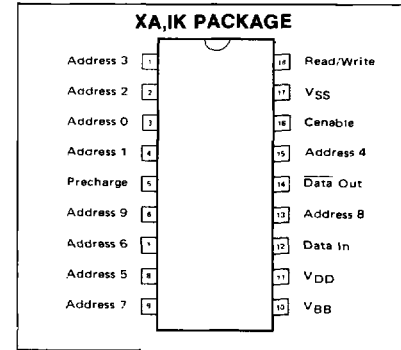


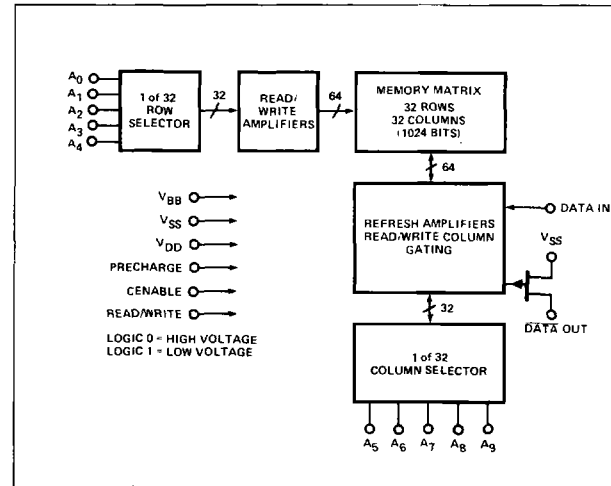
**DESCRIPTION**

The 1103 is designed for main memory applications where high performance, low cost and large bit storage are important design objectives. It is a 1024 word by 1 bit random access memory element using enhancement mode P-channel MOS devices integrated on a monolithic array. It is fully decoded, permitting the use of an 18-pin dual in-line package. The dynamic circuitry dissipates significant power only during precharge. Information stored in the memory is nondestructively read. Refreshing of all 1024 bits is accomplished in 32 read cycles and is required every two milliseconds. A separate cenable (chip enable) lead allows easy selection of an individual package when outputs are OR-tied. Use Signetics 8T25 Sense Amp, and 3207 Clock Driver.

**PIN CONFIGURATION**



**BLOCK DIAGRAM**



**MEMORIES**

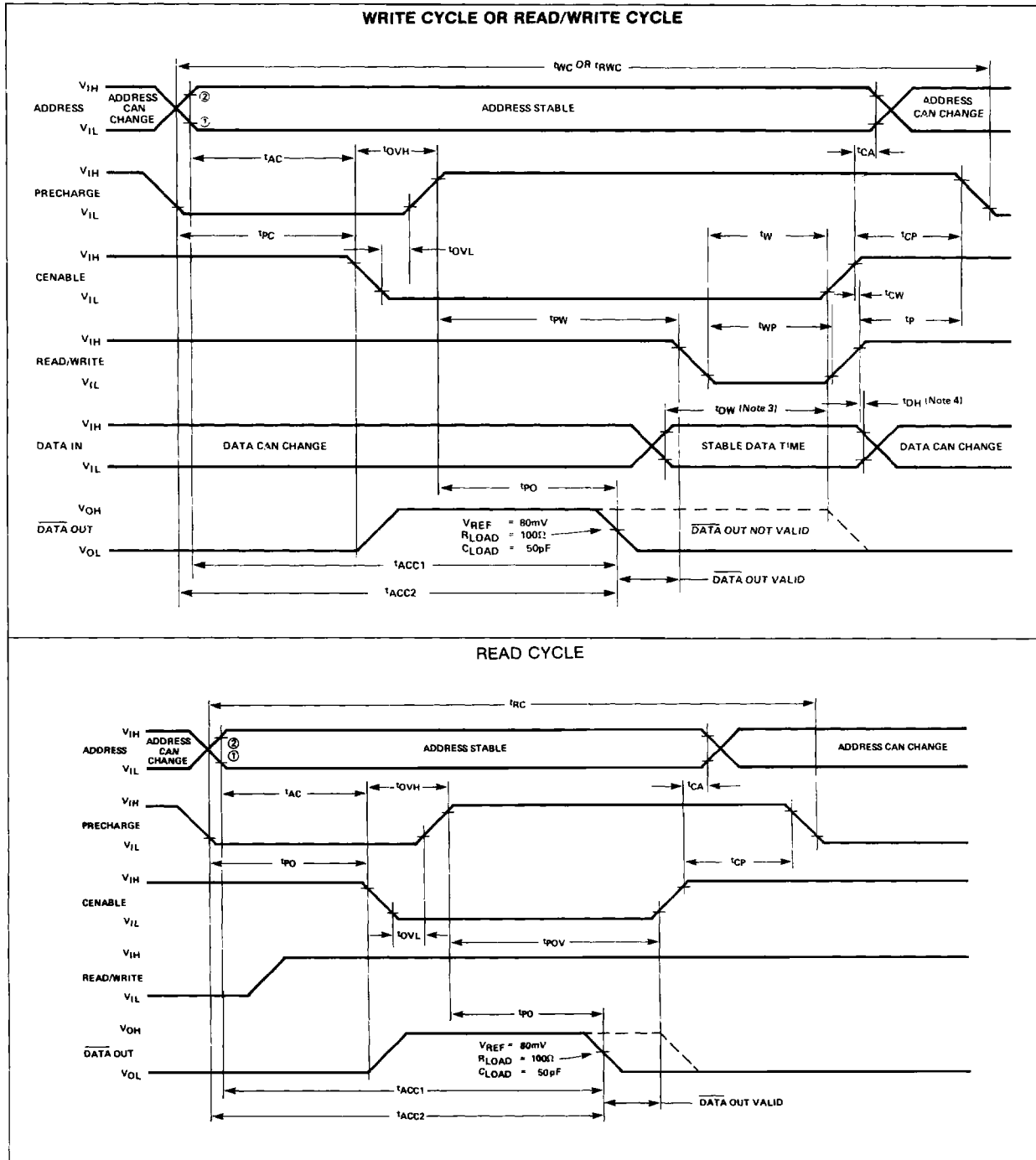
## AC CHARACTERISTICS

READ, WRITE, AND READ/WRITE CYCLE		1103 <sup>(1)</sup>		1103-1 <sup>(3)</sup>		UNIT	
		TA = 0°C to +70°C VSS = 16V ± 5% (VBB - VSS) = 3V to 4V VDD = 0V		TA = 0°C to +55°C VSS = 19V ± 5% (VBB - VSS) = 3V to 4V VDD = 0V			
PARAMETER	CONDITIONS	MIN	MAX	MIN	MAX	UNIT	
tREF Time Between Refresh			2		1	ms	
tAC Address to Cenable Set Up Time		115		30		ns	
tCA Cenable to Address Hold Time		20		10		ns	
tPC Precharge to Cenable Delay		125		60		ns	
tOVL Precharge & Cenable Overlap, Low		25	75	5	30	ns	
tCP Cenable to Precharge Delay		85		40		ns	
tOVH Precharge & Cenable Overlap, High			140		85	ns	
<b>READ CYCLE</b>							
tRC Read Cycle	$t_{ACmin} + t_{OVLmin}$ $+ t_{POmax} = 2t_r$ $t_{PCmin} + t_{OVLmin}$ $+ t_{POmax} + 2t_r$	480		300		ns	
tPOV Precharge to End of Cenable		165	500	115	500	ns	
tPO End of Precharge to Output Delay				120		75	ns
tACC1 Address to Output Access			300		150		ns
tACC2 Precharge to Output Access			310		180		ns
<b>WRITE OR READ/WRITE CYCLE</b>							
tWC Write Cycle	$t_r = 20 \text{ ns}$  $C_{LOAD} = 50 \text{ pF (100pF)}$ $R_{LOAD} = 100$ $V_{REF} = 80 \text{ mV (40mV)}$ <b>*1103 only</b>	580		340		ns	
tRWC Read/Write Cycle		580		340		ns	
tPW Precharge to Read/Write Delay		165	500	115	500	ns	
tWP Read/Write Pulse Width		50		20		ns	
tW Read/Write Set Up Time		80		20		ns	
tDW Data Set Up Time		105		40		ns	
tDH Data Hold Time		10		10		ns	
tPO End of Precharge to Output Delay				120		75	ns
tPO End of Precharge to Output Delay				120		75	ns
tp Time to Next Precharge			0		0		ns
tCW Read/Write Hold Time			10		15	ns	
<b>CAPACITANCE</b> <sup>(2)</sup>							
CAD Address Capacitance	VIN = VSS		7		7	pF	
CPR Precharge Capacitance	VIN = VSS		18		18	pF	
CCE Cenable Capacitance	VIN = VSS		18		18	pF	
CRW Read/Write Capacitance	VIN = VSS		15		15	pF	
CIN1 Data Input Capacitance	Cenable = 0V	f = 1MHz	5		5	pF	
CIN2 Data Input Capacitance	VIN = VSS	All Unused Pins are at A.C. Ground	4		4	pF	
COUT Data Output Capacitance	VIN = VSS VOUT = 0V		3		3	pF	

## NOTES:

- These times will degrade by 40ns (worst case) if the maximum values for VIL (for precharge, cenable and read/write inputs) go to VSS - 14.2V @ 0°C and VSS - 14.5V @ 70°C.
- This parameter is periodically sampled and is not 100% tested. It is measured at worst case operating conditions. Capacitance measurements for plastic package only.
- These times will degrade by 35ns if VREF point of 40mV is chosen instead of the 80mV point defined in this specification.

## TIMING DIAGRAM



## NOTES:

- 1  $V_{DD} + 2V$  }  $t_r$  is defined as the transitions between these two points.
- 2  $V_{SS} - 2V$  }
- 3  $t_{DW}$  is referenced to point 1 of the rising edge of enable or read/write whichever occurs first.
- 4  $t_{DH}$  is referenced to point 2 of the rising edge of enable or read/write whichever occurs first.