Product Brief
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microelectronics group

Lucent Technologies
Bell Labs Innovations

LUC4AC01
ATM Crossbar Element (ACE)

Introduction

The ACE IC is part of the ATLANTA chip set consisting of four devices that provide a highly integrated, innovative, and complete VLSI solution for implementing the ATM layer core of an ATM switch system. The chip set enables construction of high-performance, feature-rich, and cost-effective ATM switches, scalable over a wide range of switching capacities. This document discusses the ACE device.

Features

- Functions as a highly efficient, 5 Gbits/s, ATM crossbar element.
  - — Allows construction of nonblocking, lossless, and self-routing three-stage switch fabrics.
  - — Supports variable configurations for more compact fabric design with higher port density. Each ACE can be programmed to provide 1, 2, or 4 crossbars of different sizes.
- Supports I/O port speeds up to 622 Mbits/s of ATM traffic.
- Incorporates independent clocking of input ports to facilitate robust system designs by eliminating clock trees and allowing for varied clock skews.
- Uses differential clocking to provide noise immunity.
- Provides system diagnostic features, including detection and reporting of the following error conditions:
  - — Input port parity error.
  - — Loss of input port clock.
- Supports a generic *Intel** or *Motorola*† compatible 16-bit microprocessor interface with interrupt.
- Facilitates circuit board testing with on-chip *IEEE*‡ standard boundary scan.
- Low-power monolithic IC fabricated in 0.5 µm, 3.3 V CMOS technology, with 5 V tolerant and TTL-level compatible I/O.
- Available in a 352-pin PBGA package.

Description

Figure 1 shows the architecture of an ATM switch designed with the ATLANTA chip set. This document summarizes ATLANTA switch fabrics and the LUC4AC01 ATM Crossbar Element (ACE). The ATLANTA ACE device provides the switching crossbar function for a three-stage ATM switch fabric. This 8 x 8 crossbar element is a key building block for larger scalable three-stage switch fabrics (up to 40 x 40 OC-12 equivalent ports, 25 Gbits/s systems). The ACE interfaces directly to the ATLANTA LUC4AS01 ATM Switch Element (ASX) device and is used for linking switch elements. Nonblocking, lossless, and self-routing switch fabrics can be constructed using the ATLANTA chip set.

Each ACE is configurable to provide four crossbars of a 2 x 2 configuration, two crossbars of up to a 4 x 4 configuration, or a single crossbar of up to an 8 x 8 configuration. It supports the novel internal backpressure and routing algorithms of the companion ASX device and provides fail-safe access to the output ports.

The ACE also provides system diagnostic features. Diagnostic reports include parity errors on inputs, and loss of input port clock.

* *Intel* is a registered trademark of Intel Corporation.
† *Motorola* is a registered trademark of Motorola, Inc.

‡ *IEEE* is a registered trademark of The Institute of Electrical and Electronics Engineers, Inc.

Description (continued)

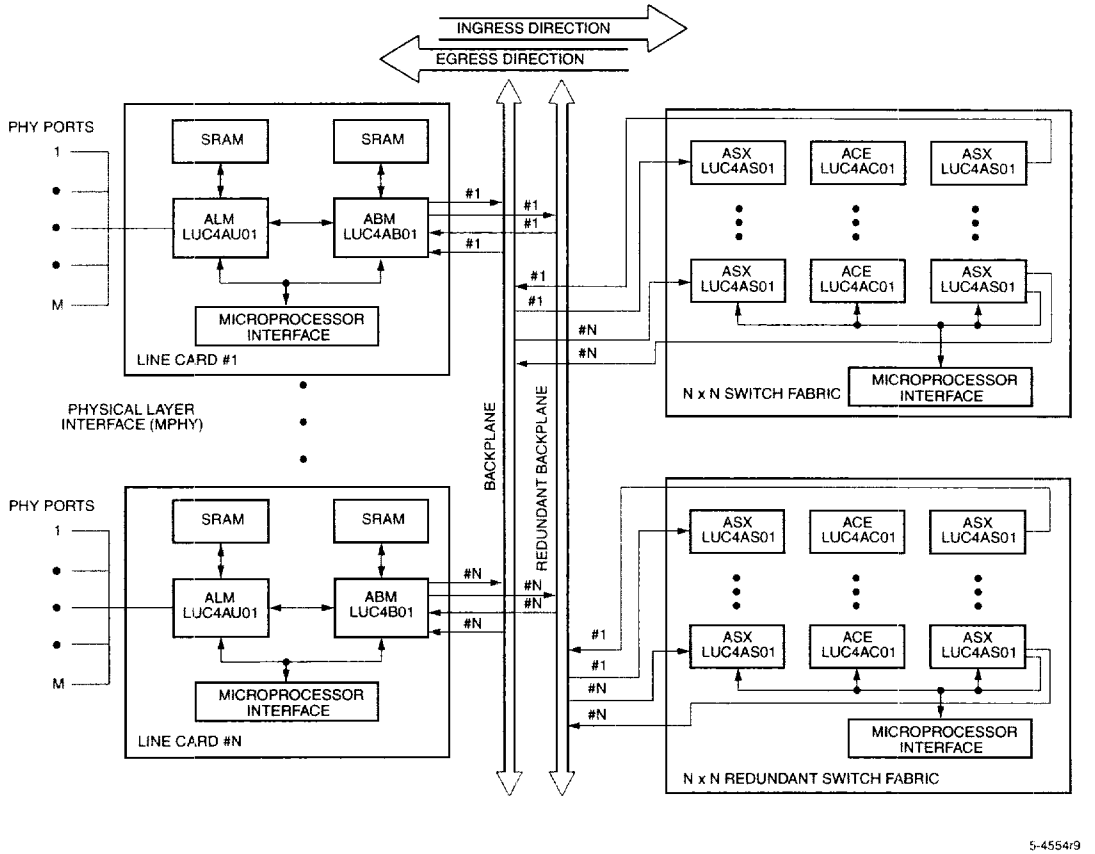

Figure 1. Architecture of an ATM Switch Using the ATLANTA Chip Set

SECTION 4.4

Description (continued)

The ACE block diagram and a brief description of the functionality of each block follows.

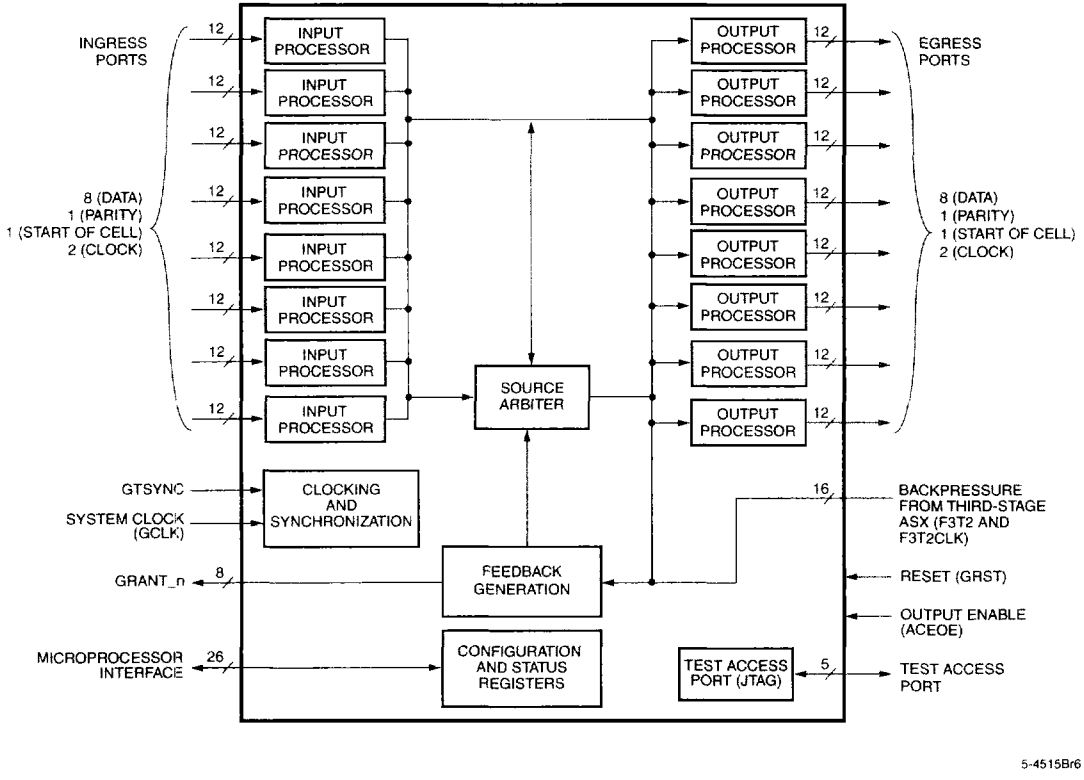

Figure 2. ACE Block Diagram

SECTION 4.4

Description (continued)

Overview

As shown in Figure 2, data for each port is clocked into an input processor, and then routed to the appropriate output processor. The routing and arbitration circuit, and backpressure feedback generation circuit control the movement of data into and out of the crossbar elements. Control and status is communicated through a 16-bit asynchronous microprocessor interface.

Figure 3 shows an example 16 x 16 ATLANTA-based switch fabric. The switch fabric will switch any of the 16 inputs to any of the 16 outputs. This is achieved by staging devices and is referred to as a three-stage switch fabric. The input stage is called the **first stage** (expander), and the output stage is called the **third stage** (concentrator). The ACE is functionally similar to the ASX, but without the internal cell buffer (a handshake protocol between the ASX and the ACE ensures that the ACE need not store data). Conceptually, the first stage ASX expands the number of paths available for switching the data, while the third stage concentrates data from the center stage.

A three-stage ASX/ACE based switch fabric can support up to 40 ports with 622 Mbits/s I/O rates. A 40-port (25 Gbits/s total ATM throughput) fabric design would use eight devices per stage in a 5:8 expansion mode.

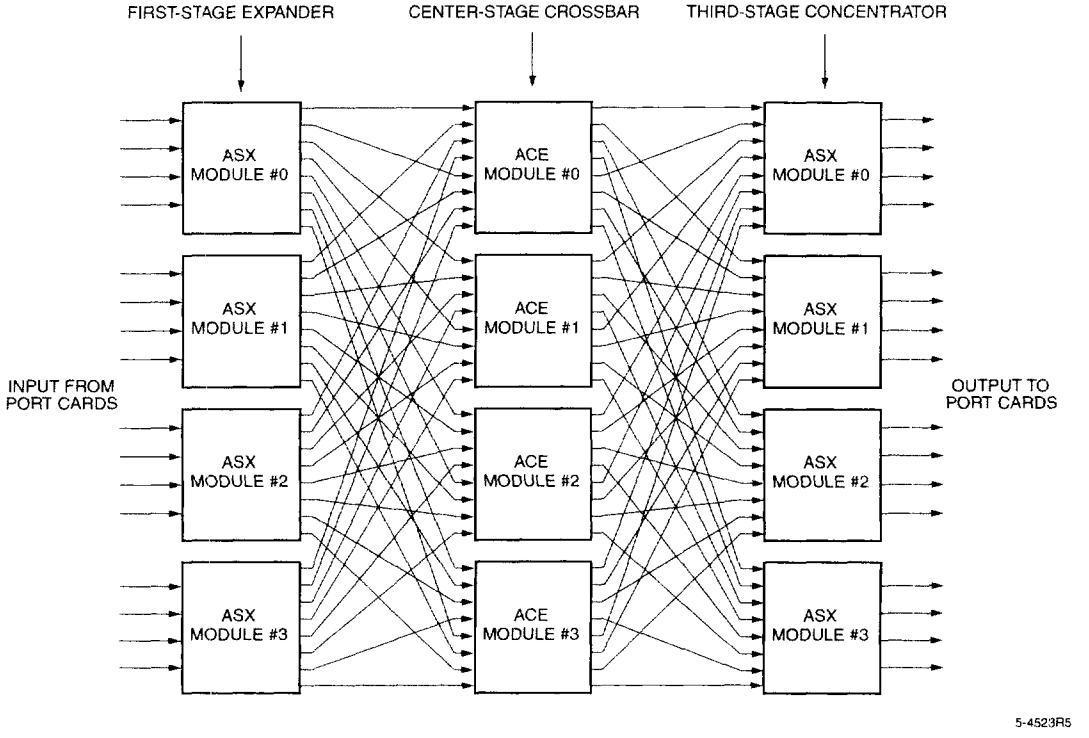

Figure 3. Example 16 x 16 @ 622 Mbits/s Switch Fabric (10 Gbits/s throughput)

Description (continued)

Input Processors

The input processors are responsible for accepting data into the device. There are eight input processors, one for each port. Each input port has eight data bits, one parity bit, one start of cell bit, and a differential clock. The microprocessor must enable the appropriate input ports. The input processor shifts data in and checks parity. Input ports are clocked independently.

The input port interface is designed to minimize the risk of undetected errors. The differential clock provides system noise immunity to prevent errors. In addition, the input processor detects the presence of an input clock and reports when the input clock is lost. The input processor also checks for incoming parity errors. Parity errors and loss of clock are reported through the microprocessor interface.

Output Processors

The output processors perform the opposite functions of the input processors. They handle the shifting out of the data. The microprocessor can disable any output port.

Source Arbiter

The source arbiter arbitrates access to the crossbar outputs of the center-stage ACE module. The source arbiter receives requests from the first-stage ASX modules. The source arbiter then determines which of these requests are granted or denied, taking into consideration any output contention in the center-stage or congestion in the third-stage ASX modules in the switch fabric.

Microprocessor Interface

The microprocessor interface (MPI) provides a general 16-bit asynchronous interface to an external processor for accessing the ASX configuration and status registers and internal memory. The MPI also supports per-function, maskable interrupts. The interface operates identically to the interface in the ALM, ABM, and ASX.

The MPI is designed to support various 16-bit microprocessors with minimal glue logic, and to directly interface to popular *Intel* and *Motorola* microprocessors.

Test Access Port

The ACE incorporates logic to support a standard five-pin test access port (TAP), compatible with the *IEEE* P1149.1 standard (JTAG), used for boundary scan. TAP contains instruction registers, data registers, and control logic, and has its own set of instructions. It is controlled externally by a JTAG bus master. The TAP gives the ACE board-level test capability.