AAA1M304 Fast Page Mode CMOS 256K × 4 Dynamic RAM

DESCRIPTION

The AAA1M304 is a high performance CMOS Dynamic Random Access Memory organized as 262,144 words by 4 bits. The AAA1M304 is fabricated with advanced CMOS technology and designed with innovative design techniques resulting in high speed, extremely low power and wide operating margins at both component and system levels.

The AAA1M304 features a high speed page mode operation in which high speed read, write or read-write is performed on any of the 1,024 bits defined by the column address. The asynchronous column address eases the system level timing constraints associated with a multiplexed address scheme with an extremely short row address capture time. The output is tri-stated by $\overline{CAS}$ which, in essence, acts as an output enable independent of $\overline{RAS}$ with very fast $\overline{CAS}$ to output access time.

Refresh is accomplished by performing $\overline{RAS}$ only refresh cycles, hidden refresh cycles, $\overline{CAS}$ before $\overline{RAS}$ refresh cycles, or normal read or write cycles on the 512 address combinations of A0 to A8 during an 8ms period.

Multiplexed address inputs permit AAA1M304 to be packaged in a standard 20-pin plastic DIP, 26-pin plastic SOJ and 20-pin plastic ZIP. The package sizes provide high system bit densities and are compatible with widely available automated testing and insertion equipment. System level features include single power supply of 5V ±10% tolerance and direct interface with high performance TTL logic families.

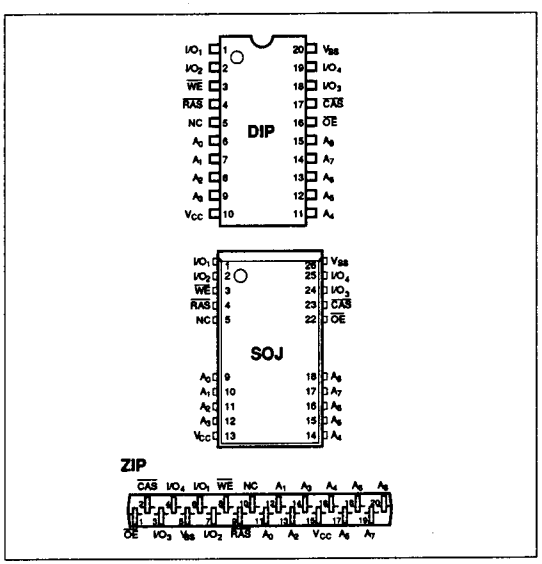
FEATURES

- 262,144 × 4 bit Organization
- Single 5V ±10% Power Supply
- Performance Ranges:

Parameter	-06	-07	-08
Max. $\overline{RAS}$ Access Time	60ns	70ns	80ns
Max. $\overline{CAS}$ Access Time	15ns	20ns	20ns
Max. Column Address Access Time	30ns	35ns	40ns
Min. Read/Write Cycle Time	110ns	130ns	150ns

- Low Power Operation
  - — Standby current (CMOS) 1mA
  - — Operating current 60mA
- 512 Refresh cycles distributed across 8ms
- In slow refresh version 512 cycles (A_0~A_8)/64 msec during data retention.
- All input and output clocks are fully TTL and CMOS compatible
- Refresh modes:
  $\overline{RAS}$ only, $\overline{CAS}$ before $\overline{RAS}$ and hidden refresh
- High reliability plastic 20 pin 300 mil wide DIP, plastic 26pin SOJ, and plastic 20pin ZIP.

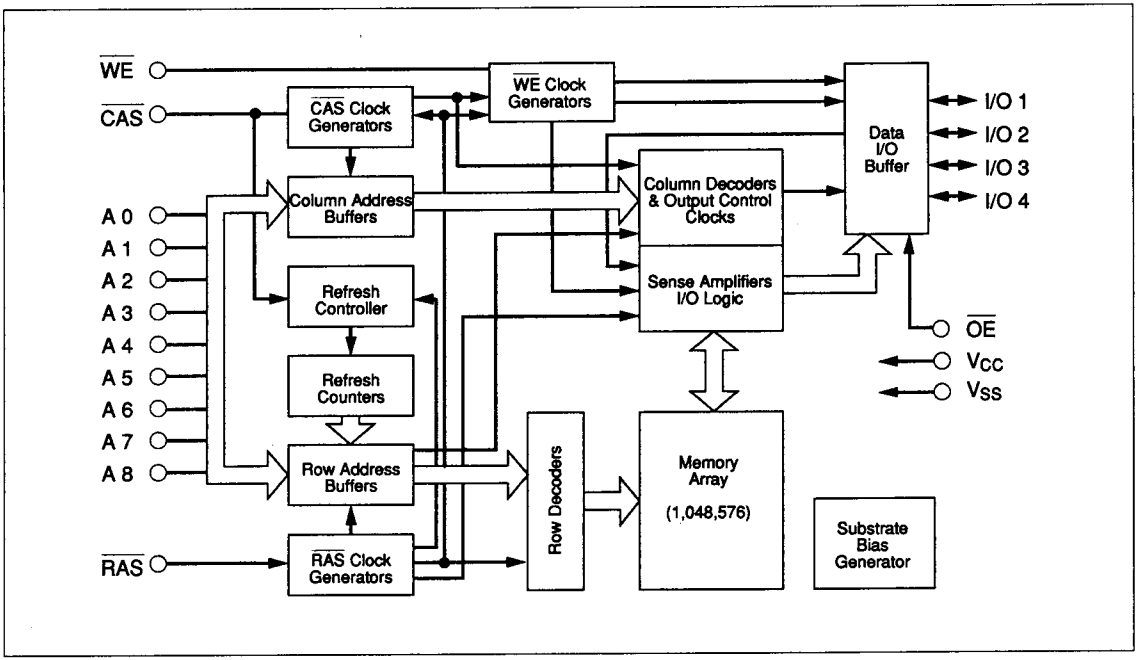
PIN CONFIGURATION



PIN NAMES

A0~A8	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{OE}$	Output Enable
I/01~I/04	Data-in / Data-out
$\overline{WE}$	Write Enable
Vcc	+5V Supply
Vss	Ground
NC	No Connection

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

RATING	SYMBOL	VALUE	UNIT
Voltage on Any Pin Relative to V_{SS}	Vin, Vout	–1 to 7	V
Voltage on Vcc Relative to V_{SS}	V_{CC}	–1 to 7	V
Storage Temperature (Plastic)	Tstg	–55 to 125	°C
Power Dissipation	Pd	600	mW
Ambient Operating Temperature	Ta	0 to + 70	°C

* Permanent device damage can occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods can affect device reliability.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{SS}	Supply Voltage		0		V
V_{IH}	Input High Voltage, All Inputs	2.4		6.5	V
V_{IL}	Input Low Voltage, All Inputs	–1.0		0.8	V

Note: All voltage values in this data sheet are with respect to V_{SS}.

DC ELECTRICAL CHARACTERISTICS (0°C ≤ Ta ≤ 70°C, V_{cc} = 5.0 V ±10%)

SYMBOL	PARAMETER	SPEED	MIN.	MAX.	UNIT	TEST CONDITIONS	NOTE
I_{CC1}	Average V_{CC} Power Supply Current (Operating)	-06 -07 -08		80 70 60	mA mA mA	$t_{RC} = t_{RC}$ (min.) $\overline{RAS}$, $\overline{CAS}$, Address cycling	1, 2
I_{CC2}	V_{CC} Supply Current (TTL standby)			2	mA	$\overline{RAS}$ and $\overline{CAS}$ at V_{IH}. All Other Inputs ≥ V_{SS}	
I_{CC3}	V_{CC} Supply Current ($\overline{RAS}$ only Refresh)	-06 -07 -08		80 70 60	mA mA mA	$t_{RC} = t_{RC}$ (min.) $\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}	1
I_{CC4}	V_{CC} Supply Current (Fast page mode)	-06 -07 -08		50 40 30	mA mA mA	$t_{PC} = t_{PC}$ (min.) $\overline{RAS}$ = V_{IL} $\overline{CAS}$, Address cycling	1, 2
I_{CC5}	Vcc Supply Current ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	-06 -07 -08		80 70 60	mA mA mA	$t_{RC} = t_{RC}$ (min.) $\overline{RAS}$, $\overline{CAS}$ cycling	1
I_{CC6}	V_{CC} Supply Current (CMOS standby)			1	mA	$\overline{RAS}$ and $\overline{CAS}$ ≥ V_{CC}-0.2V All Other Inputs ≥ V_{SS}	
I_{CC7}	Slow Refresh Operating Current (T_{RC}=125µsec, T_{RAS} ≤ 1µsec)			1	mA	All Inputs Stable at CMOS Standby level during $\overline{RAS}$ precharge	
$\|I_{LI}\|$	Input Leakage Current (Any input pin)		-10	10	µA	0V ≥ V_{IH} ≥ 5.5V, Others = 0V	
$\|I_{LO}\|$	Output Leakage Current (For high impedance state)		-10	10	µA	$\overline{RAS}$ at V_{IH}, $\overline{CAS}$ at V_{IH} 0V ≤ V_{OUT} ≤ 5.5V	
V_{OH}	Output High Voltage		2.4		V	I_{OH} = –5.0 mA	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 4.2 mA	

Notes:
1. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC5} depend on cycle rate.
2. I_{CC1} and I_{CC4} depend on output loading. Specified values are obtained with outputs open.

CAPACITANCE (0°C ≤ Ta ≤ 70°C, V_{cc} = 5.0 V ±10%, f = 1 MHz)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{IN}	Address	—	4	pF
C_{IN}	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$	—	4	pF
C_{OUT}	I/01,I/02,I/03,I/04	—	6	pF

A.C. OPERATING CONDITIONS ($0°C \leq Ta \leq 70°C$, $V_{cc} = 5\ V \pm 10\%$, $V_{ss} = 0\ V$) (NOTES 3, 4, 5)

NO.	SYMBOL		PARAMETER	MM1M304-06		MM1M304-07		MM1M304-08		UNIT	NOTE
	JEDEC	STD		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	t_{CL1QV}	t_{CAC}	Access Time from $\overline{CAS}$	—	15	—	20	—	20	ns	6
2	t_{CH2QV}	t_{CPA}	Access Time from $\overline{CAS}$ Precharge	—	30	—	35	—	40	ns	13
3	t_{AVQV}	t_{AA}	Access Time from Column Address	—	30	—	35	—	40	ns	7
4	t_{RL1QV}	t_{RAC}	Access Time from $\overline{RAS}$	—	60	—	70	—	80	ns	6
5	t_{RL1CH1}	t_{CSH}	$\overline{CAS}$ Hold Time	60	—	70	—	80	—	ns	
6	t_{RL1CH1}	t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	30	—	30	—	30	—	ns	
7	t_{CH2CL2}	t_{CPN}	$\overline{CAS}$ Precharge Time	10	—	10	—	10	—	ns	
8	t_{CH2CL2}	t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test)	30	—	40	—	40	—	ns	
9	t_{CH2CL2}	t_{CP}	$\overline{CAS}$ Precharge Time (Fast Page Mode)	10	—	10	—	10	—	ns	
10	t_{CL1CH1}	t_{CAS}	$\overline{CAS}$ Pulse Width	15	10K	20	10K	20	10K	ns	
11	t_{CL1RL2}	t_{CSR}	$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	10	—	10	—	10	—	ns	
12	t_{CL1QV}	t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	—	0	—	0	—	ns	8
13	t_{CH2RL2}	t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	—	5	—	5	—	ns	
14	t_{CL1WL2}	t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay Time	40	—	50	—	50	—	ns	11
15	t_{CL1AX}	t_{CAH}	Column Address Hold Time	10	—	15	—	15	—	ns	
16	t_{RL1AX}	t_{AR}	Column Address Hold Time Referenced to $\overline{RAS}$	25	—	35	—	35	—	ns	
17	t_{AVCL2}	t_{ASC}	Column Address Setup Time	0	—	0	—	0	—	ns	
18	t_{AVRH1}	t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	30	—	35	—	40	—	ns	
19	t_{AVWL2}	t_{AWD}	Column Address to $\overline{WE}$ Delay Time	60	—	65	—	70	—	ns	11
20	t_{CL1DX} t_{WL1DX}	t_{DH}	Data Hold Time	10	—	15	—	15	—	ns	13
21	t_{RL1DX}	t_{DHR}	Data Hold Time Referenced to $\overline{RAS}$	50	—	55	—	60	—	ns	
22	t_{DVCL2} t_{DVWL2}	t_{DS}	Data Setup Time	0	—	0	—	0	—	ns	13
23	t_{OL1QV}	t_{OEA}	$\overline{OE}$ Access Time	—	15	—	20	—	20	ns	
24	t_{WL1OL2}	t_{OEH}	$\overline{OE}$ Command Hold Time	15	—	20	—	20	—	ns	
25	t_{OH2OV}	t_{OED}	$\overline{OE}$ to Data Delay Time	15	—	20	—	20	—	ns	
26	t_{CH2QX}	t_{OFF}	Output Buffer Turn-off Delay Time	0	10	0	10	0	10	ns	10
27	t_{OH2QX}	t_{OEZ}	Output Buffer Turn-off Delay Time Referenced to $\overline{OE}$	0	15	0	20	0	20	ns	
28	t_{CL1RH1}	t_{RSH}	$\overline{RAS}$ Hold Time	15	—	20	—	20	—	ns	
29	t_{OL1RH1}	t_{ROH}	$\overline{RAS}$ Hold Time Referenced to $\overline{OE}$	10	—	10	—	10	—	ns	
30	t_{RH2RL2}	t_{RP}	$\overline{RAS}$ Precharge Time	40	—	50	—	60	—	ns	
31	t_{RL1RH1}	t_{RAS}	$\overline{RAS}$ Pulse Width	60	100K	70	100	80	100K	ns	
32	t_{RL1RH1}	t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	60	100K	70	100	80	100K	ns	
33	t_{RL1CL1}	t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	15	45	20	50	20	60	ns	6
34	t_{RH2CL2}	t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0	—	0	—	0	—	ns	
35	t_{RL1AV}	t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	30	15	35	15	40	ns	7

NO.	SYMBOL		PARAMETER	MM1M304-06		MM1M304-07		MM1M304-08		UNIT	NOTE
	JEDEC	STD		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
36	t_{RL1WL2}	t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time	90	—	100	—	110	—	ns	11
37	t_{CH2WL2}	t_{RCH}	Read Command Hold Time	0	—	0	—	0	—	ns	9
38	t_{RH2WL2}	t_{RRH}	Read Command Hold Time Referenced to $\overline{RAS}$	0	—	0	—	0	—	ns	9
39	t_{WH2CL2}	t_{RCS}	Read Command Setup Time	0	—	0	—	0	—	ns	
40	t_{RL2RL2}	t_{RC}	Random Read or Write Cycle Time	110	—	130	—	150	—	ns	
41	t_{CL2CL2}	t_{PC}	Read or Write Cycle Time (Fast Page Mode)	35	—	40	—	45	—	ns	13,14
42	t_{RL2RL2}	t_{RMW}	Read-Modify-Write Cycle Time	165	—	185	—	205	—	ns	
43	t_{CL2CL2}	t_{PRMW}	Read-Modify-Write Cycle Time (Fast Page Mode)	90	—	95	—	100	—	ns	13,14
44	t_{REF}	t_{REF}	Refresh Period	—	8	—	8	—	8	ms	15
45	t_{RL1AX}	t_{RAH}	Row Address Hold Time	10	—	10	—	10	—	ns	
46	t_{AVRL2}	t_{ASR}	Row Address Setup Time	0	—	0	—	0	—	ns	
47	t_T	t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	4, 5
48	t_{CL1WH1}	t_{WCH}	Write Command Hold Time	10	—	15	—	15	—	ns	
49	t_{RL1WH1}	t_{WCR}	Write Command Hold Time Referenced to $\overline{RAS}$	50	—	55	—	60	—	ns	
50	t_{WL1WH1}	t_{WP}	Write Command Pulse Width	10	—	10	—	15	—	ns	
51	t_{WL1CL2}	t_{WCS}	Write Command Setup Time	0	—	0	—	0	—	ns	11
52	t_{WL1CH1}	t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	15	—	20	—	20	—	ns	
53	t_{WL1RH1}	t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	15	—	20	—	20	—	ns	

Notes:

3. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required. Eight initialization cycles are required after extended periods of bias without clocks (greater than 8ms).
4. AC measurements assume t_T=5ns. All AC parameters are measured with V_{IL}(min.)≥V_{SS} and V_{IH}(max.)≤V_{CC} and with a load equivalent to two TTL loads and 100pF.
5. V_{IH}(min.) and V_{IL}(max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
6. Operation within the t_{RCD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RCD}(max.) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then access time is controlled by t_{CAC}.
7. Operation within the t_{RAD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RAD}(max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then access time is controlled exclusively by t_{AA}.
8. Assumes three state test load (5pF and a 380 Ohm Thevenin equivalent).
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. t_{OFF}(max.) defines the time at which the output achieves an open circuit condition and is not referenced to output voltage levels.
11. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If t_{WCS}≥t_{WCS}(min.), the cycle is an early write cycle and data-out pins will remain open circuit (high impedance) throughout the entire cycle. If t_{RWD}≥t_{RWD}(min.), t_{CWD}≥t_{CWD}(min.) and t_{AWD}≥t_{AWD}(min.), the cycle is a read-modify-write cycle and the data-out will contain data read from the selected cell. If neither of the above conditions is satisfied, the condition of the data-out (at access time) is indeterminate.
12. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in read-modify-write cycles.
13. Access time is determined by the longer of t_{AA}, t_{CAC}, or t_{CPA}.
14. t_{ASC}≥t_{CP} to achieve t_{PC}(min.) and t_{CPA}(max.) values.
15. In slow refresh version, 512 cycles (A_0~A_8)/64msec is possible during data retention.

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AAA1M304-53 Fast Page Mode CMOS 256K × 4 Dynamic RAM

DESCRIPTION

The AAA1M304 is a high performance CMOS Dynamic Random Access Memory organized as 262,144 words by 4 bits. The AAA1M304 is fabricated with advanced CMOS technology and designed with innovative design techniques resulting in high speed, extremely low power and wide operating margins at both component and system levels.

The AAA1M304 features a high speed page mode operation in which high speed read, write and read-write is performed on any of the 1,024 bits defined by the column address. The asynchronous column address eases the system level timing constraints associated with a multiplexed address scheme with an extremely short row address capture time. The output is tri-stated by $\overline{CAS}$ which, in essence, acts as an output enable independent of $\overline{RAS}$ with very fast $\overline{CAS}$ to output access time.

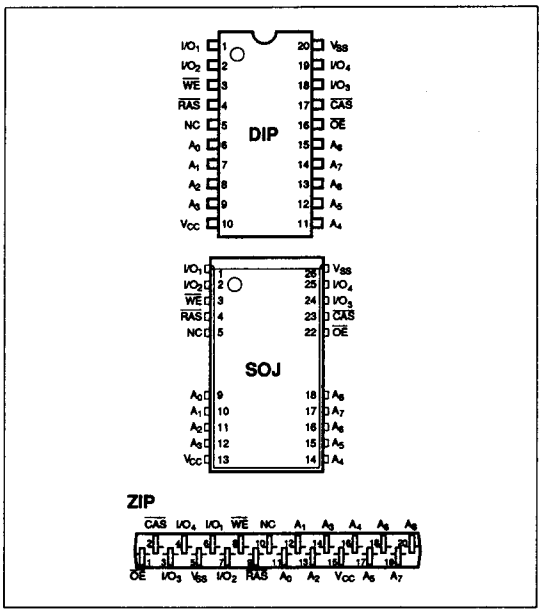
Refresh is accomplished by performing $\overline{RAS}$ only refresh cycles, hidden refresh cycles, $\overline{CAS}$ before $\overline{RAS}$ refresh cycles, or normal read or write cycles on the 512 address combinations of A0 to A8 during an 8ms period.

Multiplexed address inputs permit AAA1M304 to be packaged in a standard 20-pin plastic DIP, 26-pin plastic SOJ and 20-pin plastic ZIP. The package sizes provide high system bit densities and are compatible with widely available automated testing and insertion equipment. System level features include single power supply of 5V ±5% tolerance and direct interface with high performance TTL logic families.

FEATURES

- 262,144 x 4 bit Organization
- Single 5V ±5% Power Supply
- High Speed Operation
  - Min. $\overline{RAS}$ cycle time 100ns
  - Max. $\overline{RAS}$ Access Time 53ns
  - Max. Power Dissipation 420mw
- Fast page mode operation
- Low Power Operation
  - — Standby current (CMOS) 1mA
  - — Operating current 80mA
- 512 Refresh cycles distributed across 8ms
- In slow refresh version 512 cycles (A_0~A_8)/64 msec during data retention.
- All input and output clocks are fully TTL and CMOS compatible
- Refresh modes:
  $\overline{RAS}$ only, $\overline{CAS}$ before $\overline{RAS}$ and hidden refresh
- High reliability plastic 20 pin 300 mil wide DIP, plastic 26pin SOJ, and plastic 20pin ZIP.

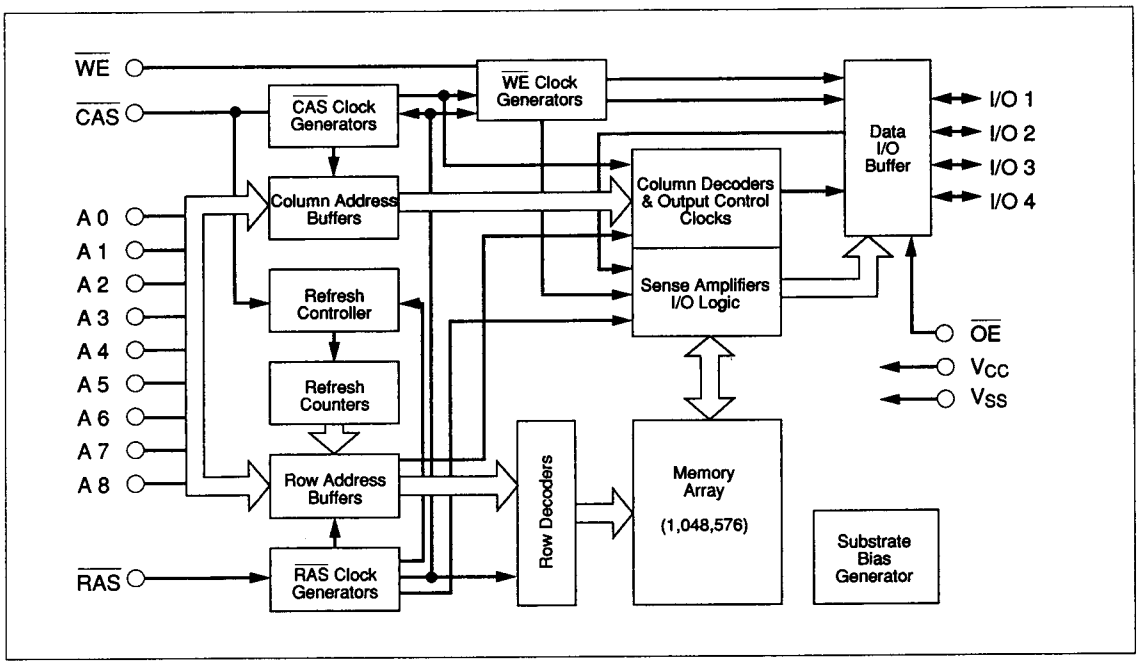
PIN CONFIGURATION



PIN NAMES

A0~A8	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{OE}$	Output Enable
I/01~I/04	Data-in / Data-out
$\overline{WE}$	Write Enable
Vcc	+5V Supply
Vss	Ground
NC	No Connection

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

RATING	SYMBOL	VALUE	UNIT
Voltage on Any Pin Relative to V_{ss}	Vin, Vout	–1 to 7	V
Voltage on Vcc Relative to V_{ss}	V_{cc}	–1 to 7	V
Storage Temperature (Plastic)	Tstg	–55 to 125	°C
Power Dissipation	Pd	600	mW
Ambient Operating Temperature	Ta	0 to + 70	°C

* Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{cc}	Supply Voltage	4.75	5.0	5.25	V
V_{ss}	Supply Voltage		0		V
V_{IH}	Input High Voltage, All Inputs	2.4		6.5	V
V_{IL}	Input Low Voltage, All Inputs	–1.0		0.8	V

Note: All voltage values in this data sheet are with respect to V_{ss}.

DC ELECTRICAL CHARACTERISTICS (0°C ≤ Ta ≤ 70°C, V_{cc} = 5.0V ±5%)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	TEST CONDITIONS	NOTE
I_{CC1}	Average V_{CC} Power Supply Current (Operating)		80	mA	$t_{RC} = t_{RC}$ (min.) $\overline{RAS}$, $\overline{CAS}$, Address Cycling	1, 2
I_{CC2}	V_{CC} Supply Current (TTL standby)		2	mA	$\overline{RAS}$ and $\overline{CAS}$ at V_{IH}. All Other Inputs ≥ V_{SS}	
I_{CC3}	V_{CC} Supply Current ($\overline{RAS}$ only refresh)		80	mA	$t_{RC} = t_{RC}$ (min.) $\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}	1
I_{CC4}	V_{CC} Supply Current (Fast page mode)		50	mA	$t_{PC} = t_{PC}$ (min.) $\overline{RAS}$=V_{IL} $\overline{CAS}$, Address cycling	1, 2
I_{CC5}	Vcc Supply Current ($\overline{CAS}$ before $\overline{RAS}$ refresh)		80	mA	$t_{RC} = t_{RC}$ (min.) $\overline{RAS}$, $\overline{CAS}$ Cycling	1
I_{CC6}	VCC Supply Current (CMOS standby)		1	mA	$\overline{RAS}$ and $\overline{CAS}$ ≥ V_{CC}-0.2V All Other Inputs ≥ V_{SS}	
I_{CC7}	Slow Refresh Operating Current (T_{RC}=125µsec, T_{RAS} ≤ 1µsec)		1	mA	All Inputs Stable at CMOS Standby level during $\overline{RAS}$ precharge	
$\|I_{LI}\|$	Input Leakage Current (Any input pin)	-10	10	µA	0V ≥ V_{IH} ≥ 5.5V, Others = 0V	
$\|I_{LO}\|$	Input Leakage Current (For high impedance state)	-10	10	µA	$\overline{RAS}$ at V_{IH}, $\overline{CAS}$ at V_{IH} 0V ≤ V_{OUT} ≤ 5.5V	
V_{OH}	Output High Voltage	2.4		V	I_{OH} = –5.0 mA	
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 4.2 mA	

Notes:
1. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC5} depend on cycle rate.
2. I_{CC1} and I_{CC4} depend on output loading. Specified values are obtained with the output open.

CAPACITANCE (0°C ≤ Ta ≤ 70°C, V_{cc} = 5.0V ±5%, f = 1MHz)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{IN}	Address	—	4	pF
C_{IN}	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$	—	4	pF
C_{OUT}	I/01,I/02,I/03,I/04	—	6	pF

A.C. OPERATING CONDITIONS (0 °C≤Ta≤70°C, V_{CC} = 5 V ± 5%, V_{SS} = 0 V) (NOTES 3, 4, 5)

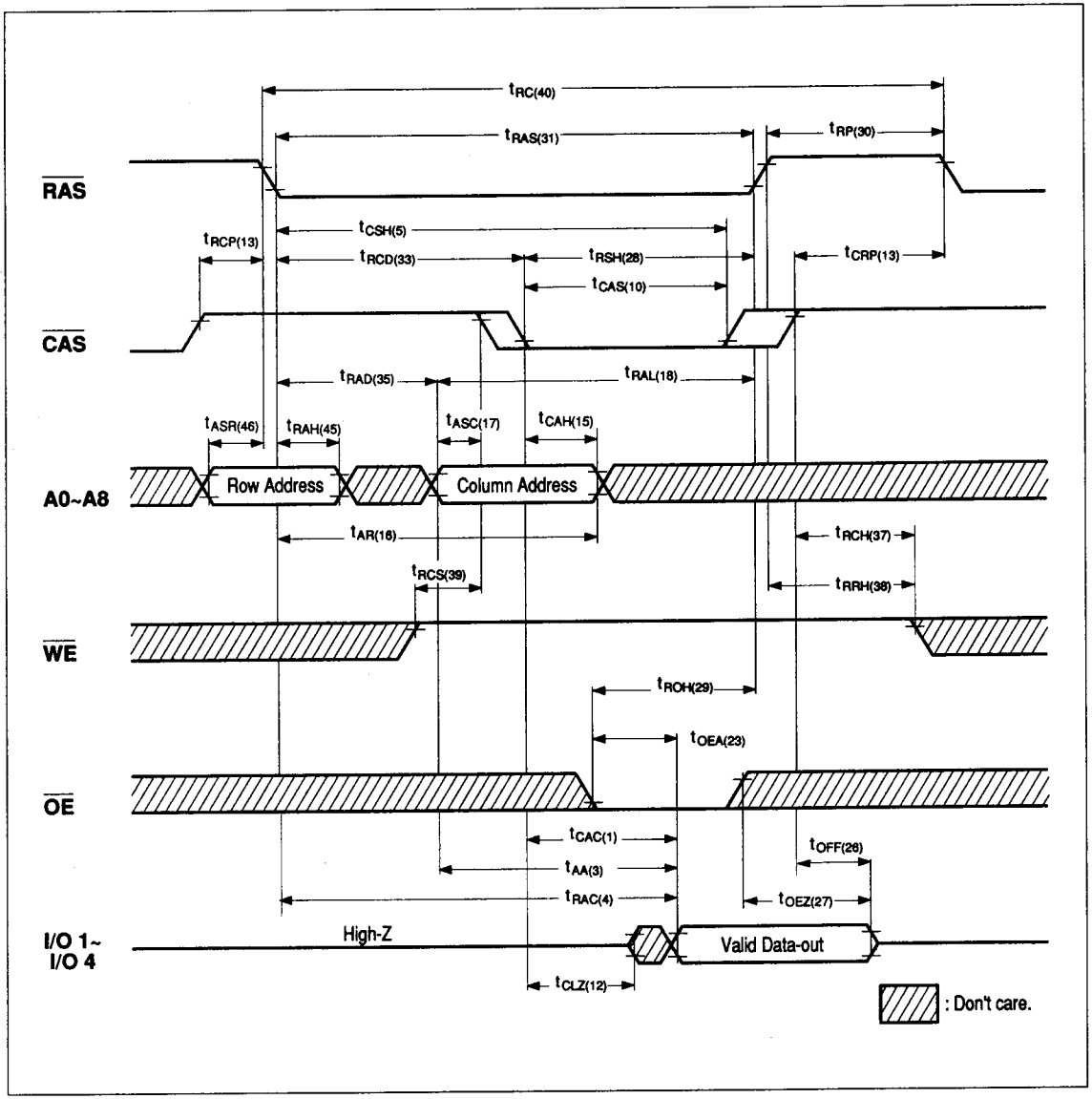
NO.	SYMBOL		PARAMETER	AAA1M304-53		UNIT	NOTE
	JEDEC	STD.		MIN.	MAX.		
1	t_{CL1QV}	t_{CAC}	Access Time from $\overline{CAS}$	—	15	ns	6
2	t_{CH2QV}	t_{CPA}	Access Time from $\overline{CAS}$ Precharge	—	26	ns	13
3	t_{AVQV}	t_{AA}	Access Time from Column Address	—	26	ns	7
4	t_{RL1QV}	t_{RAC}	Access Time from $\overline{RAS}$	—	53	ns	6
5	t_{RL1CH1}	t_{CSH}	$\overline{CAS}$ Hold Time	53	—	ns	
6	t_{RL1CH1}	t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	30	—	ns	
7	t_{CH2CL2}	t_{CPN}	$\overline{CAS}$ Precharge Time	10	—	ns	
8	t_{CH2CL2}	t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test)	30	—	ns	
9	t_{CH2CL2}	t_{CP}	$\overline{CAS}$ Precharge Time (Fast Page Mode)	10	—	ns	
10	t_{CL1CH1}	t_{CAS}	$\overline{CAS}$ Pulse Width	15	10K	ns	
11	t_{CL1RL2}	t_{CSR}	$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	10	—	ns	
12	t_{CL1QV}	t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	—	ns	8
13	t_{CH2RL2}	t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	—	ns	
14	t_{CL1WL2}	t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay Time	40	—	ns	11
15	t_{CL1AX}	t_{CAH}	Column Address Hold Time	10	—	ns	
16	t_{RL1AX}	t_{AR}	Column Address Hold Time Referenced to $\overline{RAS}$	23	—	ns	
17	t_{AVCL2}	t_{ASC}	Column Address Setup Time	0	—	ns	
18	t_{AVRH1}	t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	26	—	ns	
19	t_{AVWL2}	t_{AWD}	Column Address to $\overline{WE}$ Delay Time	54	—	ns	11
20	t_{CL1DX} t_{WL1DX}	t_{DH}	Data Hold Time	10	—	ns	13
21	t_{RL1DX}	t_{DHR}	Data Hold Time Referenced to $\overline{RAS}$	50	—	ns	
22	t_{DVCL2} t_{DVWL2}	t_{DS}	Data Setup Time	0	—	ns	13
23	t_{OL1OV}	t_{OEA}	$\overline{OE}$ Access Time	—	15	ns	
24	t_{WL1OL2}	t_{OEH}	$\overline{OE}$ Command Hold Time	15	—	ns	
25	t_{OH2QV}	t_{OED}	$\overline{OE}$ to Data Delay Time	15	—	ns	
26	t_{CH2QX}	t_{OFF}	Output Buffer Turn-off Delay Time	0	7	ns	10
27	t_{OH2QX}	t_{OEZ}	Output Buffer Turn-off Delay Time Referenced to $\overline{OE}$	0	7	ns	
28	t_{CL1RH1}	t_{RSH}	$\overline{RAS}$ Hold Time	15	—	ns	
29	t_{OL1RH1}	t_{ROH}	$\overline{RAS}$ Hold Time Referenced to $\overline{OE}$	10	—	ns	
30	t_{RH2RL2}	t_{RP}	$\overline{RAS}$ Precharge Time	30	—	ns	
31	t_{RL1RH1}	t_{RAS}	$\overline{RAS}$ Pulse Width	53	100K	ns	
32	t_{RL1RH1}	t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	53	100K	ns	
33	t_{RL1CL1}	t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	13	45	ns	6
34	t_{RH2CL2}	t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0	—	ns	
35	t_{RL1AV}	t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	13	27	ns	7

NO.	SYMBOL		PARAMETER	AAA1M304-53		UNIT	NOTE
	JEDEC	STD.		MIN.	MAX.		
36	t_{RL1WL2}	t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time	83	—	ns	11
37	t_{CH2WL2}	t_{RCH}	Read Command Hold Time	0	—	ns	9
38	t_{RH2WL2}	t_{RRH}	Read Command Hold Time Referenced to $\overline{RAS}$	0	—	ns	9
39	t_{WH2CL2}	t_{RCS}	Read Command Setup Time	0	—	ns	
40	t_{RL2RL2}	t_{RC}	Random Read or Write Cycle Time	100	—	ns	
41	t_{CL2CL2}	t_{PC}	Read or Write Cycle Time (Fast Page Mode)	30	—	ns	13, 14
42	t_{RL2RL2}	t_{RMW}	Read-Modify-Write Cycle Time	155	—	ns	
43	t_{CL2CL2}	t_{PRMW}	Read-Modify-Write Cycle Time (Fast Page Mode)	84	—	ns	13, 14
44	t_{REF}	t_{REF}	Refresh Period	—	8	ms	15
45	t_{RL1AX}	t_{RAH}	Row Address Hold Time	8	—	ns	
46	t_{AVRL2}	t_{ASR}	Row Address Setup Time	0	—	ns	
47	t_T	t_T	Transition Time (Rise and Fall)	2	50	ns	4, 5
48	t_{CL1WH1}	t_{WCH}	Write Command Hold Time	10	—	ns	
49	t_{RL1WH1}	t_{WCR}	Write Command Hold Time Referenced to $\overline{RAS}$	50	—	ns	
50	t_{WL1WH1}	t_{WP}	Write Command Pulse Width	10	—	ns	
51	t_{WL1CL2}	t_{WCS}	Write Command Setup Time	0	—	ns	11
52	t_{WL1CH1}	t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	15	—	ns	
53	t_{WL1RH1}	t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	15	—	ns	

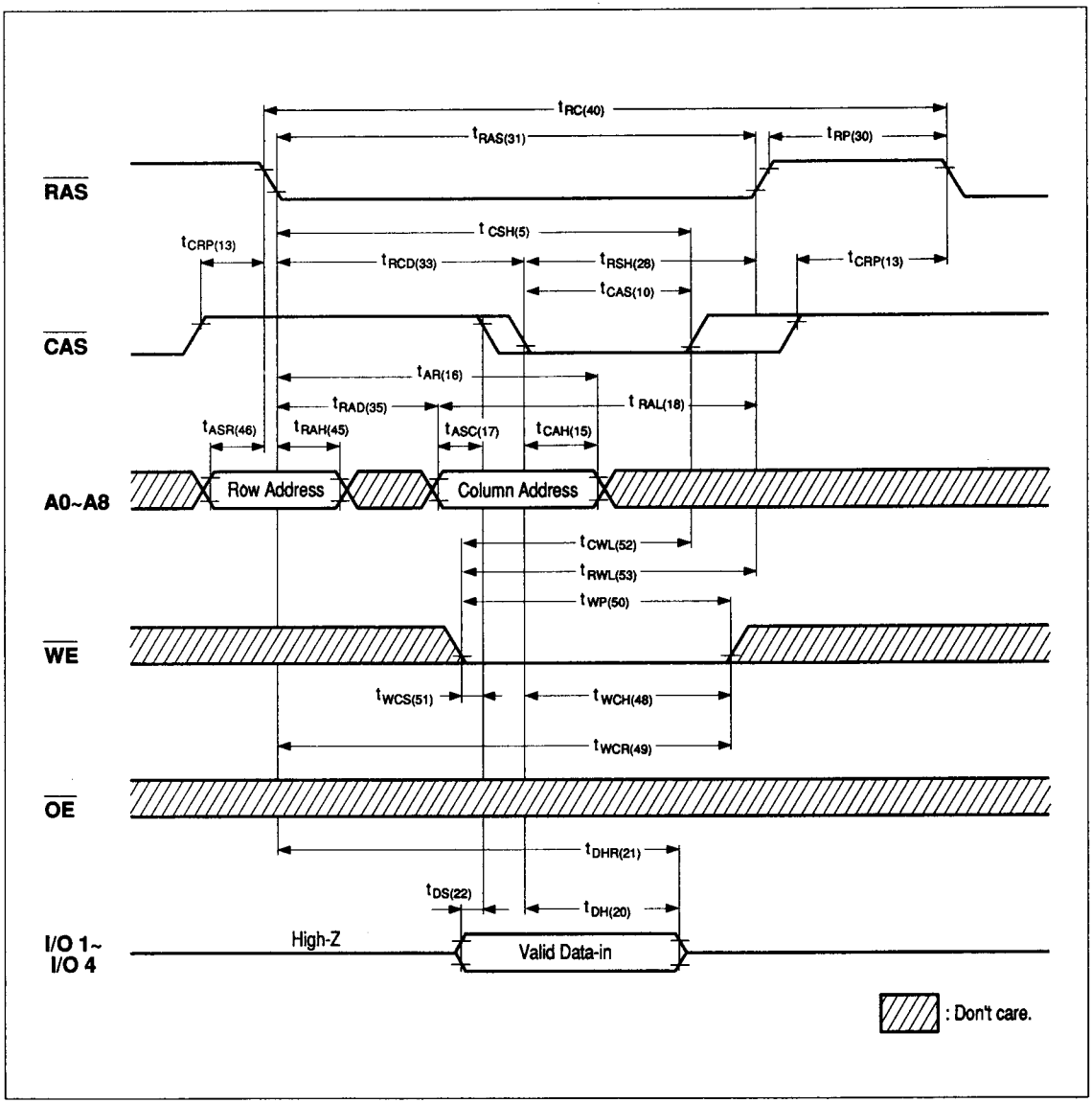
Notes:

3. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required. Eight initialization cycles are required after extended periods of bias without clocks (greater than 8ms).
4. AC measurements assume t_T=5ns. All AC parameters are measured with V_{IL}(min.)≥V_{SS} and V_{IH}(max.)≤V_{CC} and with a load equivalent to two TTL loads and 100pF.
5. V_{IH}(min.) and V_{IL}(max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
6. Operation within the t_{RCD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RCD}(max.) is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD(max.)}$ limit, then access time is controlled by t_{CAC}.
7. Operation within the t_{RAD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RAD}(max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then access time is controlled exclusively by t_{AA}.
8. Assumes three state test load (5pF and a 380 Ohm Thevenin equivalent).
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. t_{OFF}(max.) defines the time at which the output achieves an open circuit condition and is not referenced to output voltage levels.
11. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If t_{WCS}≥t_{WCS}(min.), the cycle is an early write cycle and data-out pins will remain open circuit (high impedance) throughout the entire cycle. If t_{RWD}≥t_{RWD}(min.), t_{CWD}≥t_{CWD}(min.) and t_{AWD}≥t_{AWD}(min.), the cycle is a read-modify-write cycle and the data-out will contain data read from the selected cell. If neither of the above conditions is satisfied, the condition of the data-out (at access time) is indeterminate.
12. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in read-modify-write cycles.
13. Access time is determined by the longer of t_{AA}, t_{CAC}, or t_{CPA}.
14. t_{ASC}≥t_{CP} to achieve t_{PC}(min.) and t_{CPA}(max.) values.
15. In slow refresh version, 512 cycles (A_0~A_8)/64 msec is possible during data retention.

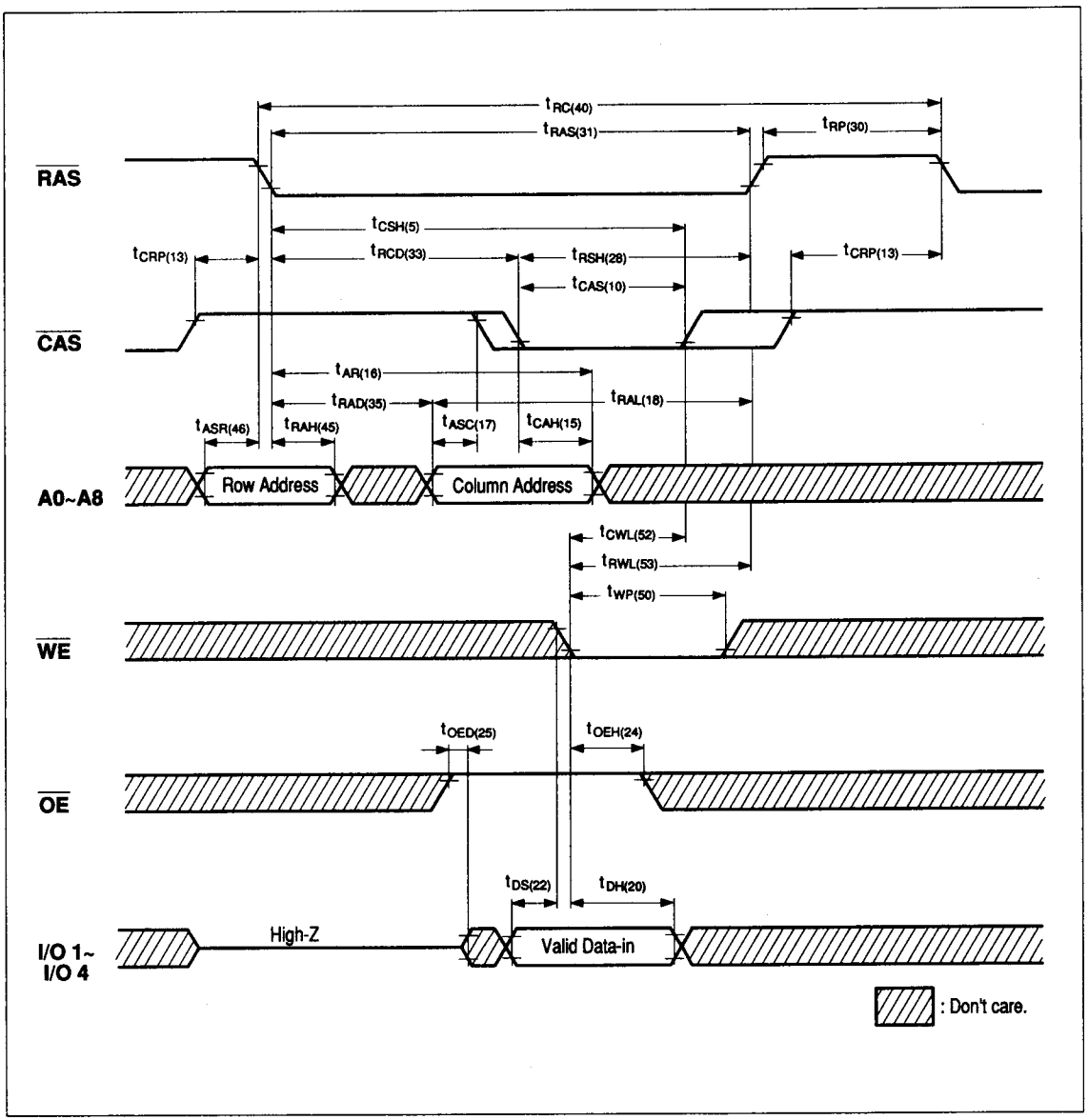
READ CYCLE


tRC(40)
tRAS(31)
tRP(30)
RAS
tCSH(5)
tRCP(13)
tRCD(33)
tRSH(28)
tCRP(13)
tCAS(10)
CAS
tRAD(35)
tRAL(18)
tASR(46)
tRAH(45)
tASC(17)
tCAH(15)
A0~A8
Row Address
Column Address
tAR(16)
tRCH(37)
tRCS(39)
tRRH(38)
WE
tROH(29)
tOEA(23)
OE
tCAC(1)
tOFF(28)
tAA(3)
tRAC(4)
tOEZ(27)
I/O 1~
I/O 4
High-Z
Valid Data-out
tCLZ(12)
: Don't care.

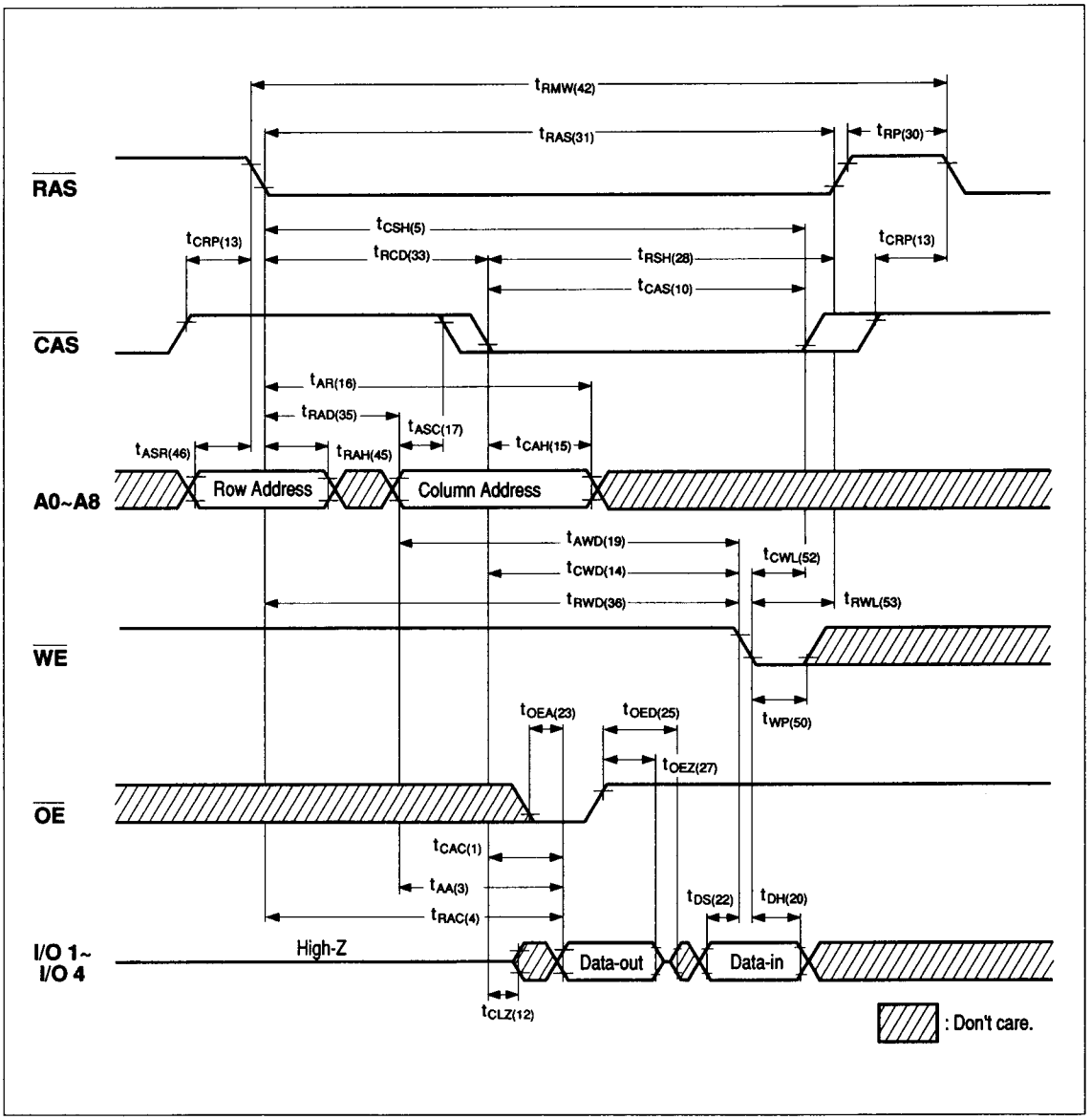
WRITE CYCLE (EARLY WRITE)



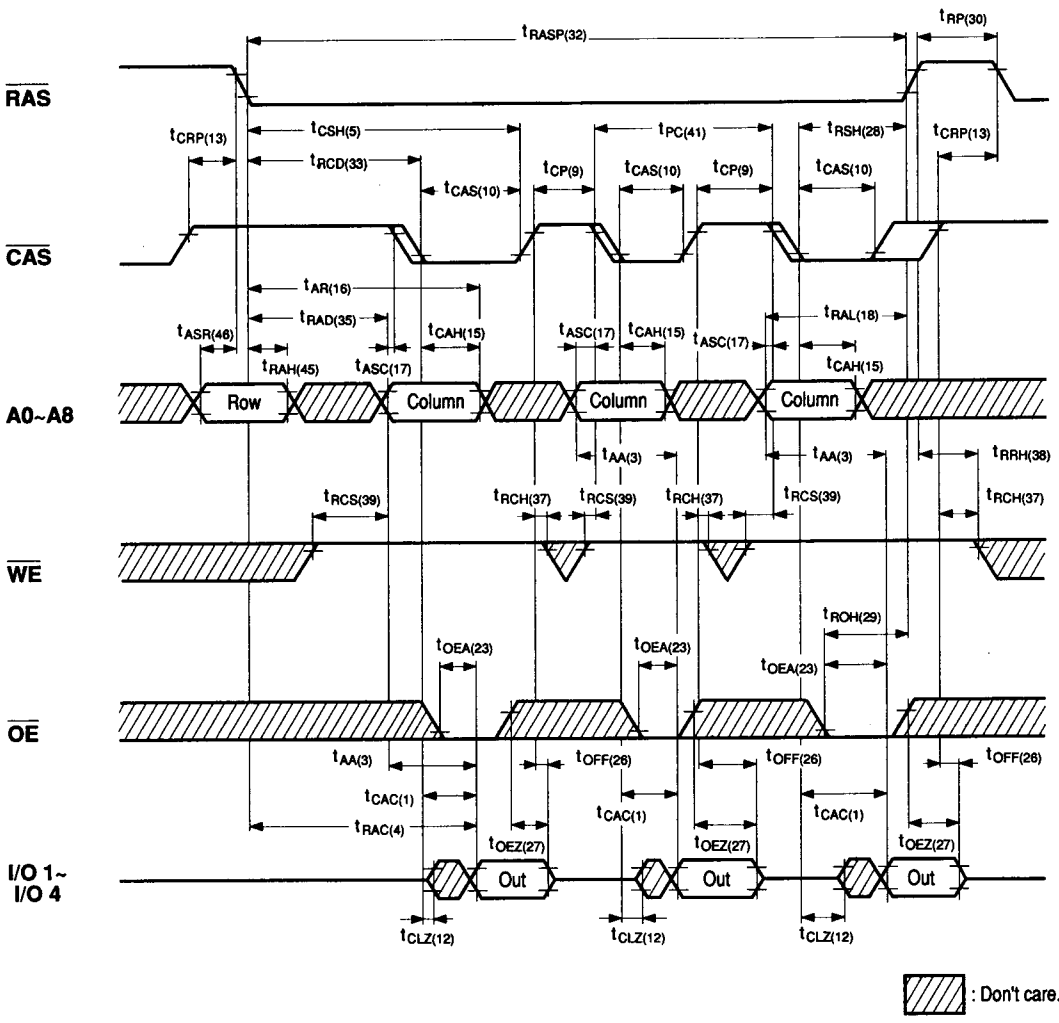
WRITE CYCLE ($\overline{OE}$-CONTROLLED WRITE)



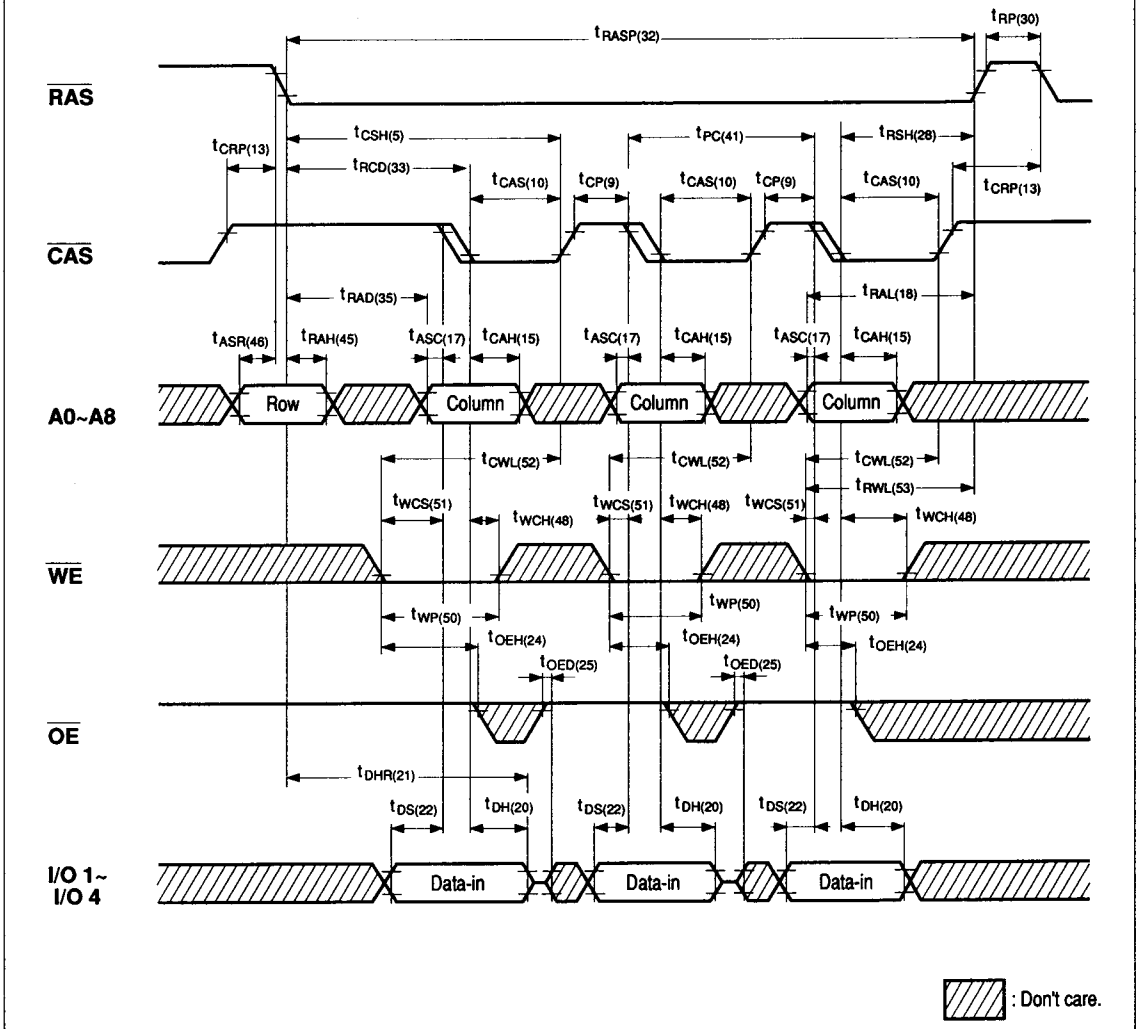
READ-MODIFY-WRITE CYCLE



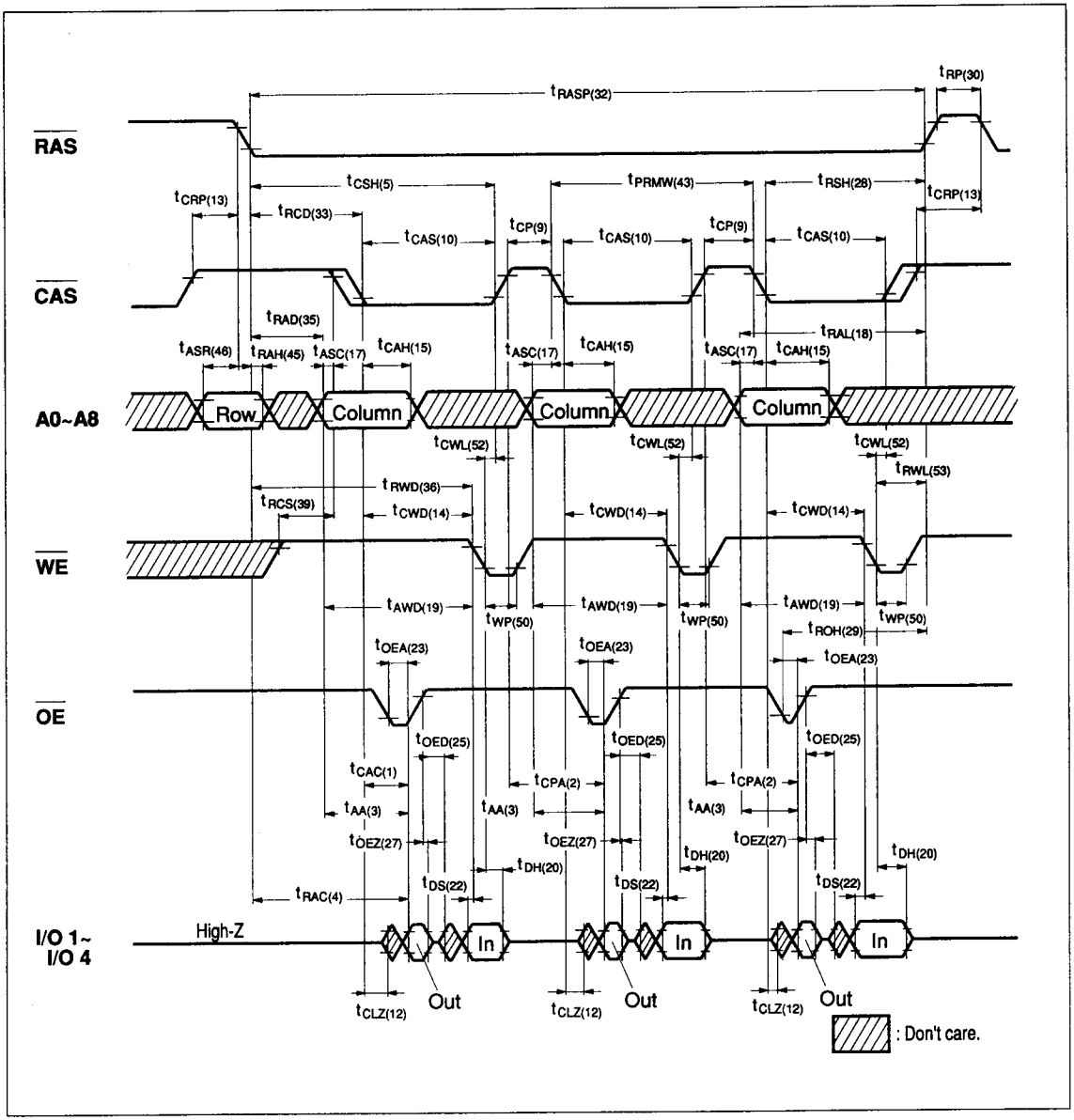
FAST PAGE MODE READ CYCLE



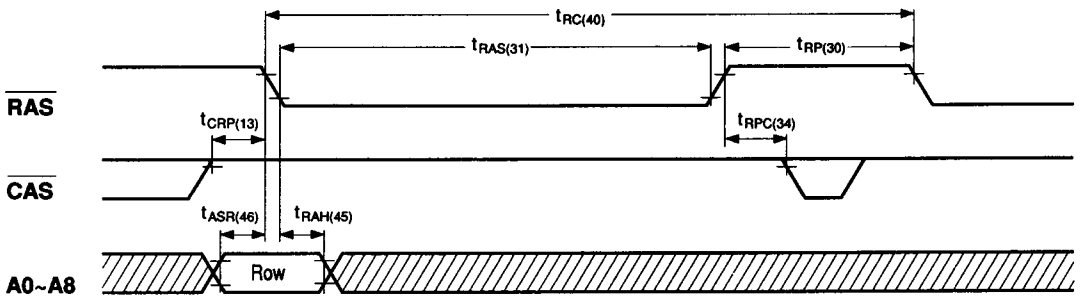
FAST PAGE MODE EARLY WRITE CYCLE



FAST PAGE MODE READ-MODIFY-WRITE CYCLE

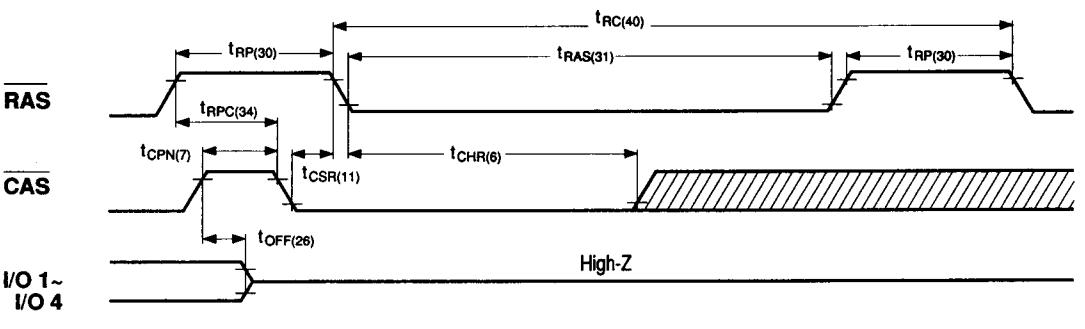


$\overline{RAS}$ ONLY REFRESH CYCLE



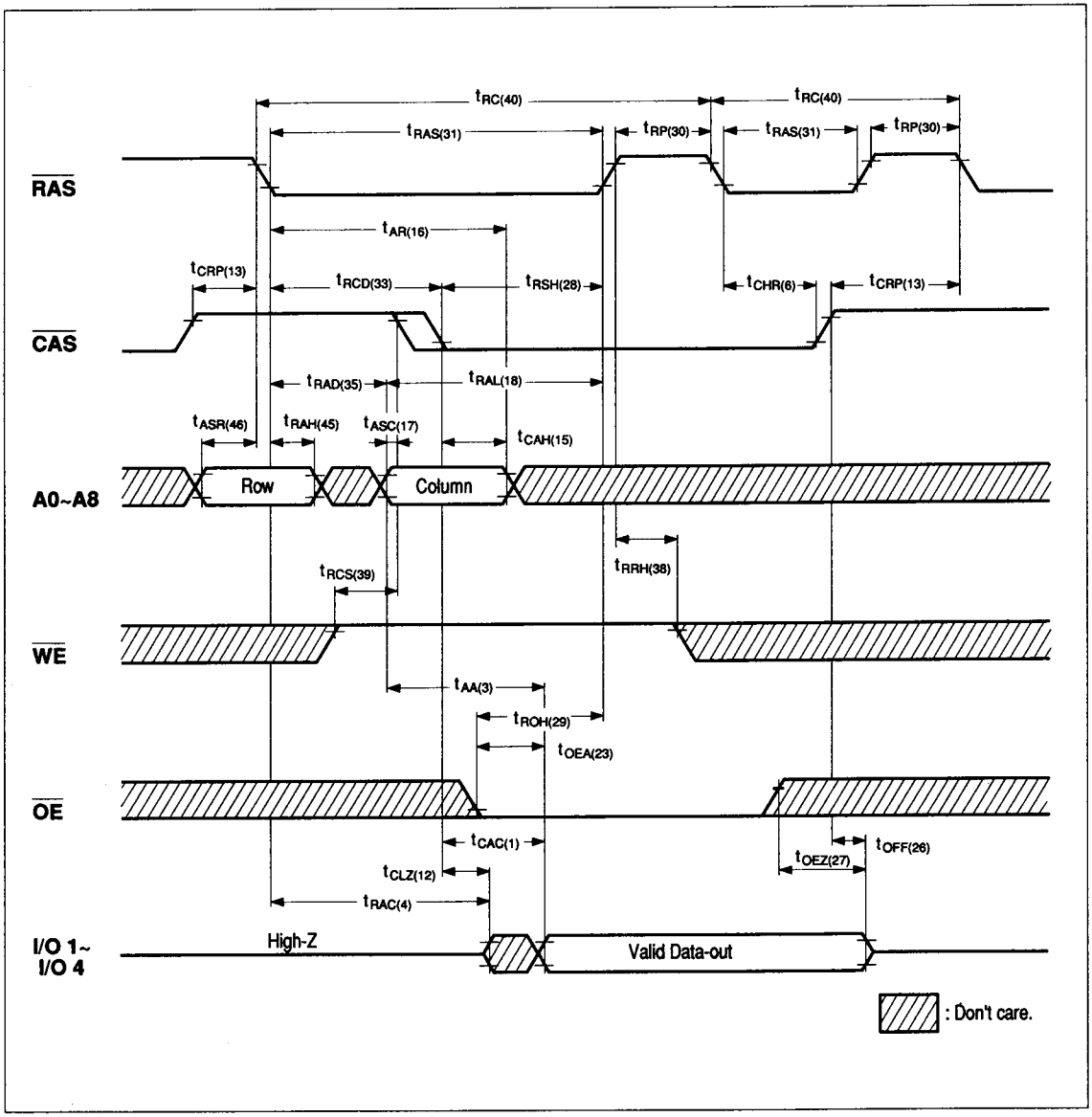
Note: $\overline{WE}$, $\overline{OE}$ = Don't care. : Don't care.

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE

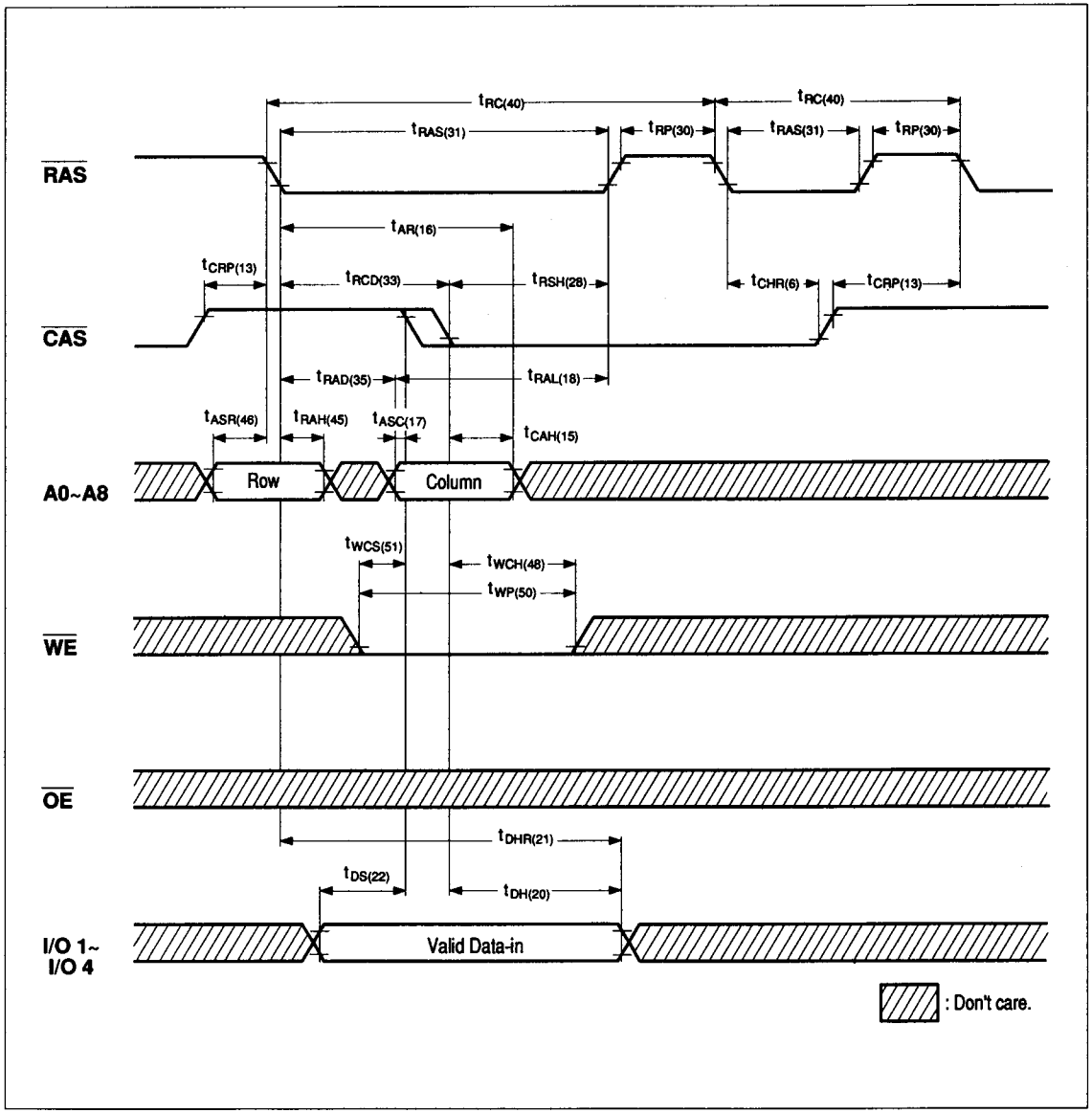


Note: $\overline{WE}$, $\overline{OE}$, A0~A8 = Don't care. : Don't care.

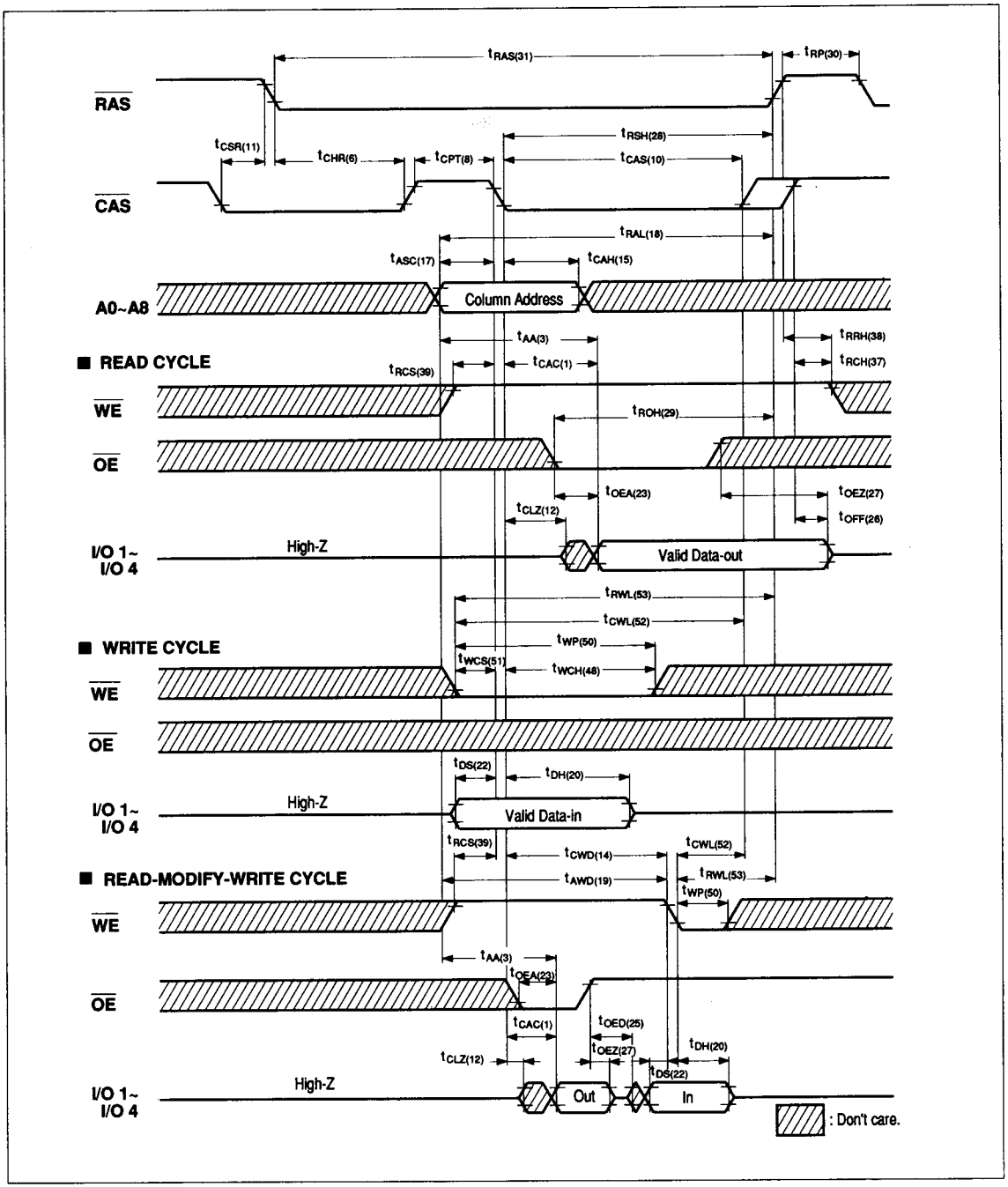
HIDDEN REFRESH CYCLE (READ)



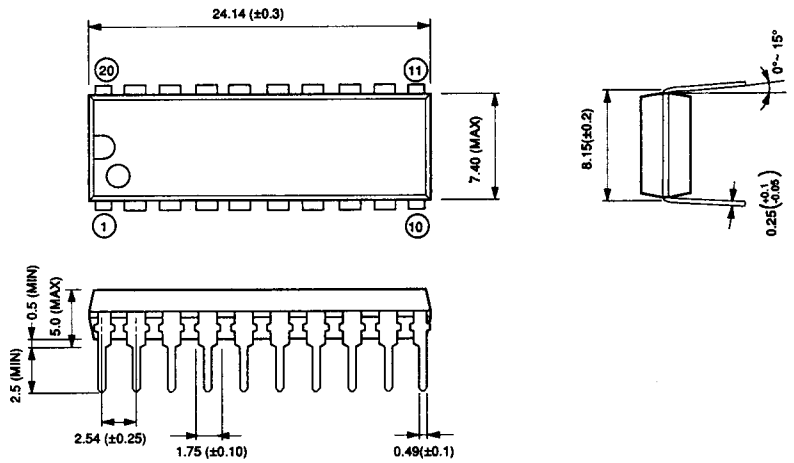
HIDDEN REFRESH CYCLE (EARLY WRITE)



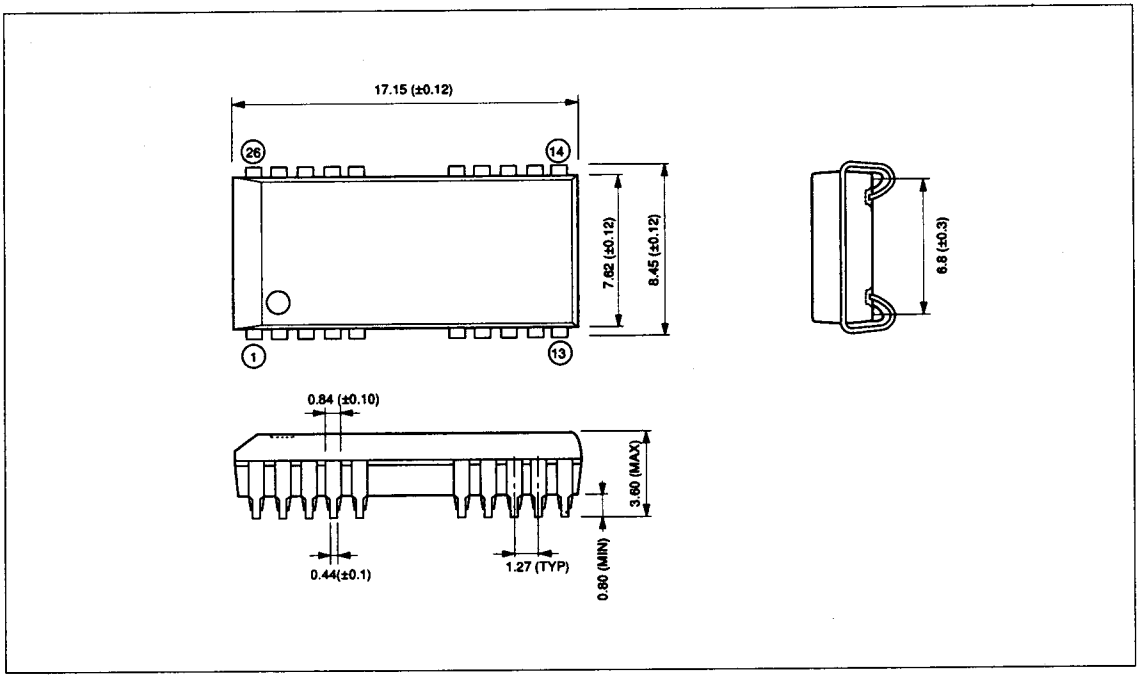
$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST CYCLE



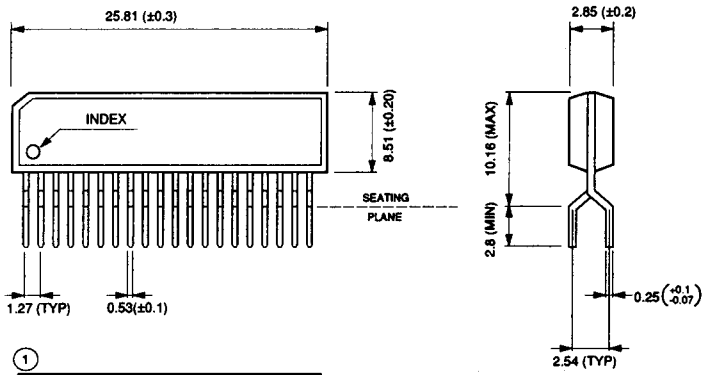
20 PIN PLASTIC DIP (300 mil) (Unit: mm)



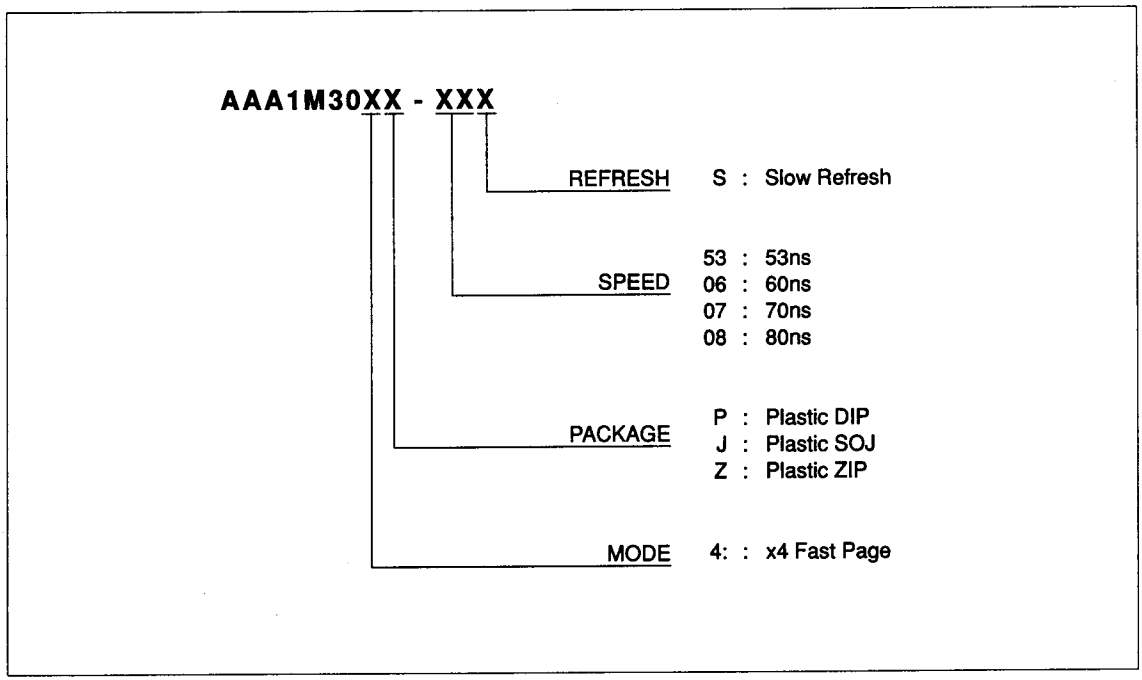
26 PIN PLASTIC SOJ (Unit: mm)



20 PIN PLASTIC ZIP (Unit: mm)



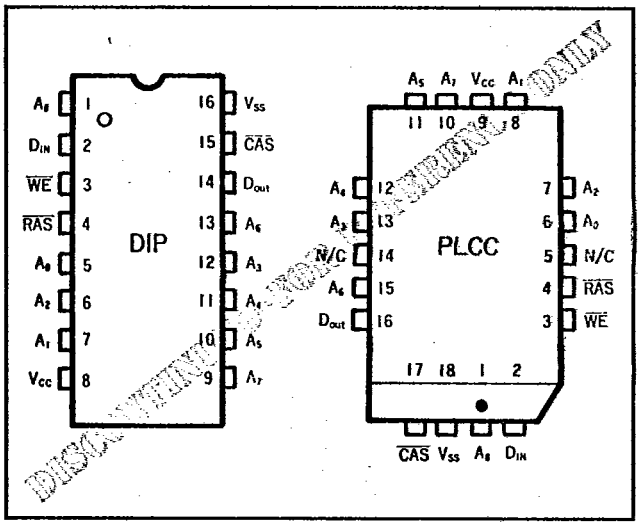
ORDERING INFORMATION



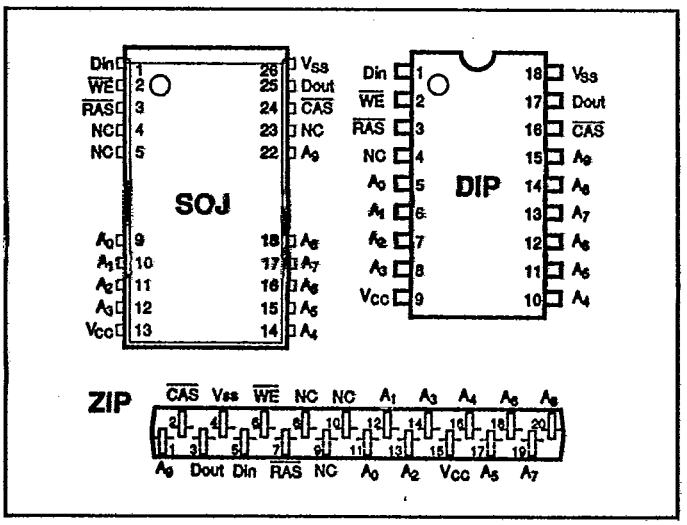
PACKAGE AND PINOUT DETAILS

T-91-20

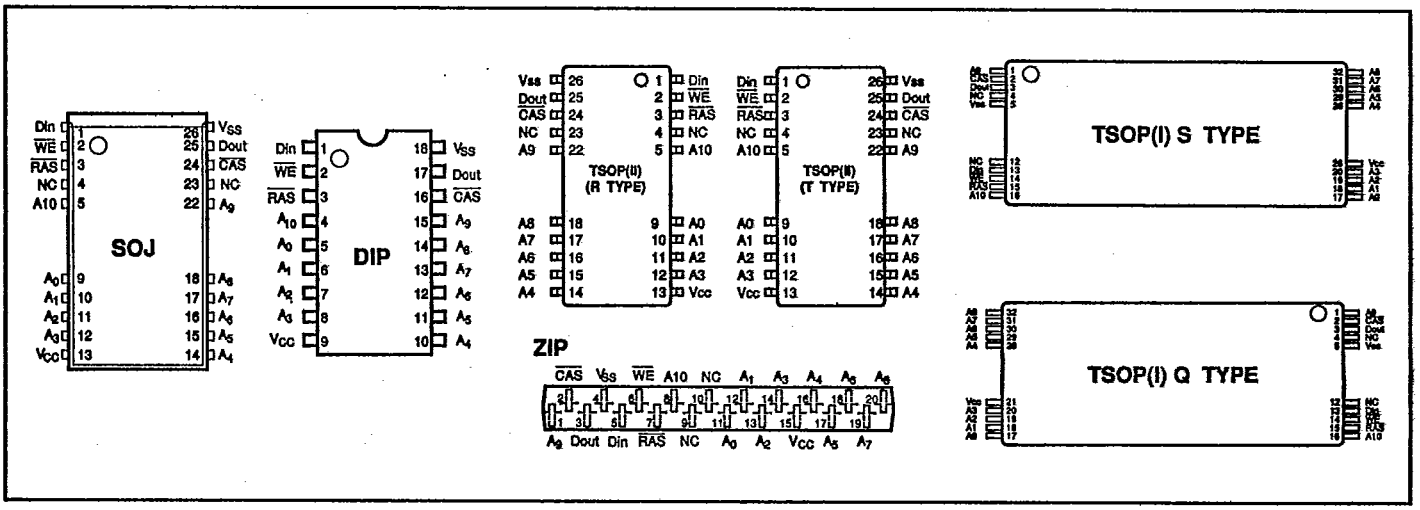
AAA2800 SERIES - 256K x 1



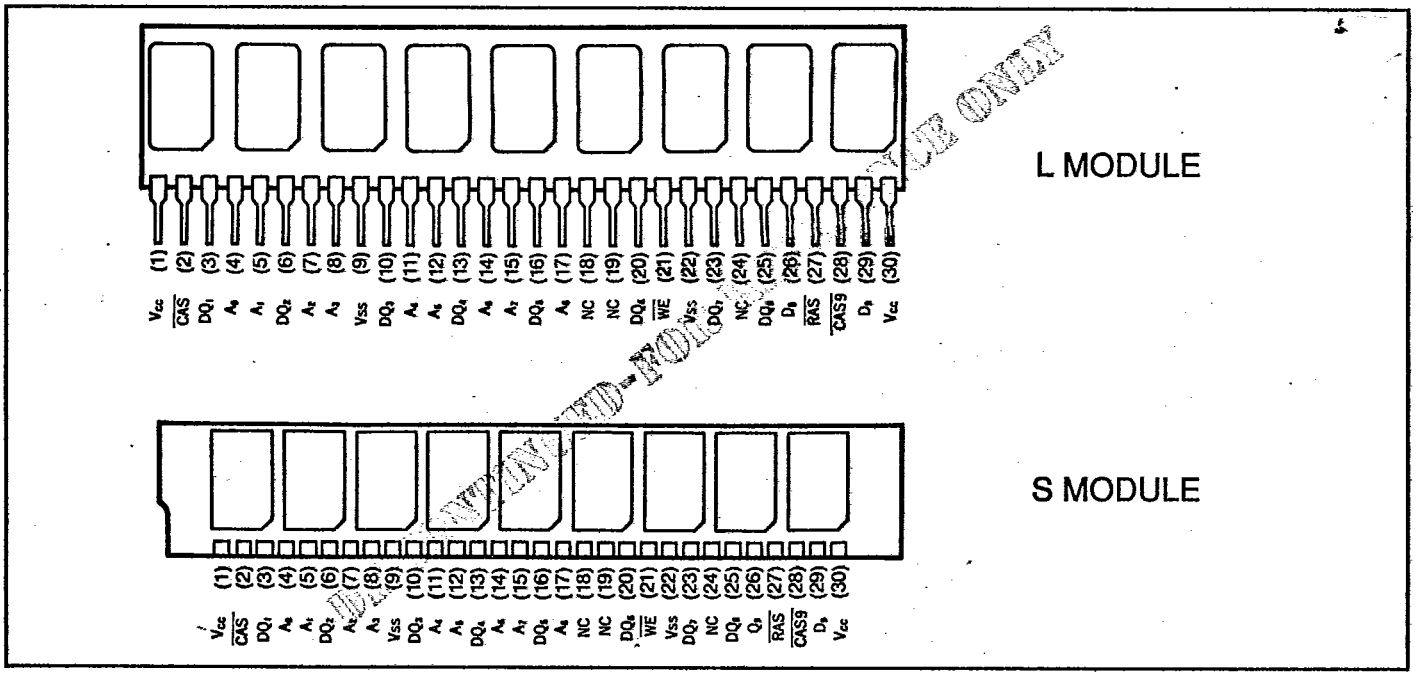
AAA1M300 SERIES - 1M x 1



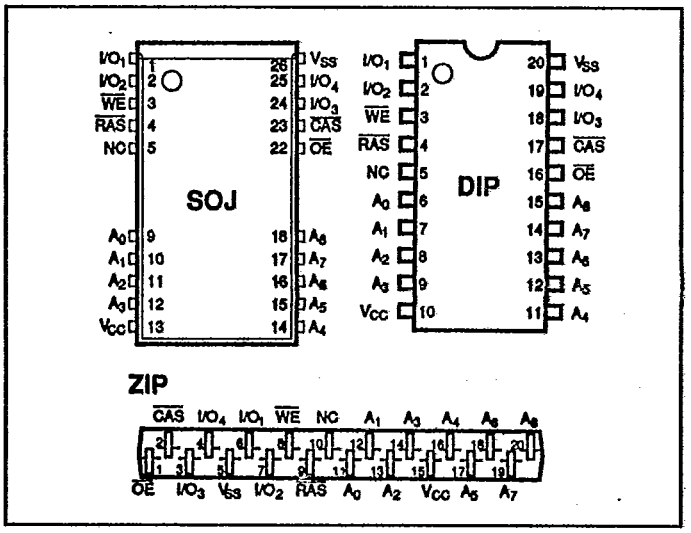
AAA4M200 SERIES - 4M x 1



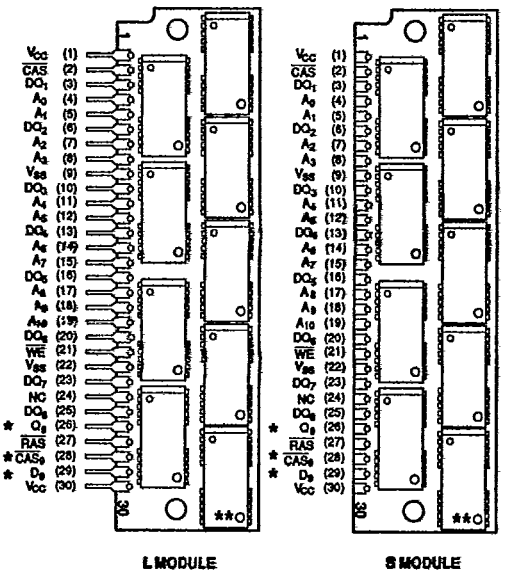
MM2800 J8/J9 SERIES - 256K x 8/9



AAA1M300 SERIES - 256K x 4

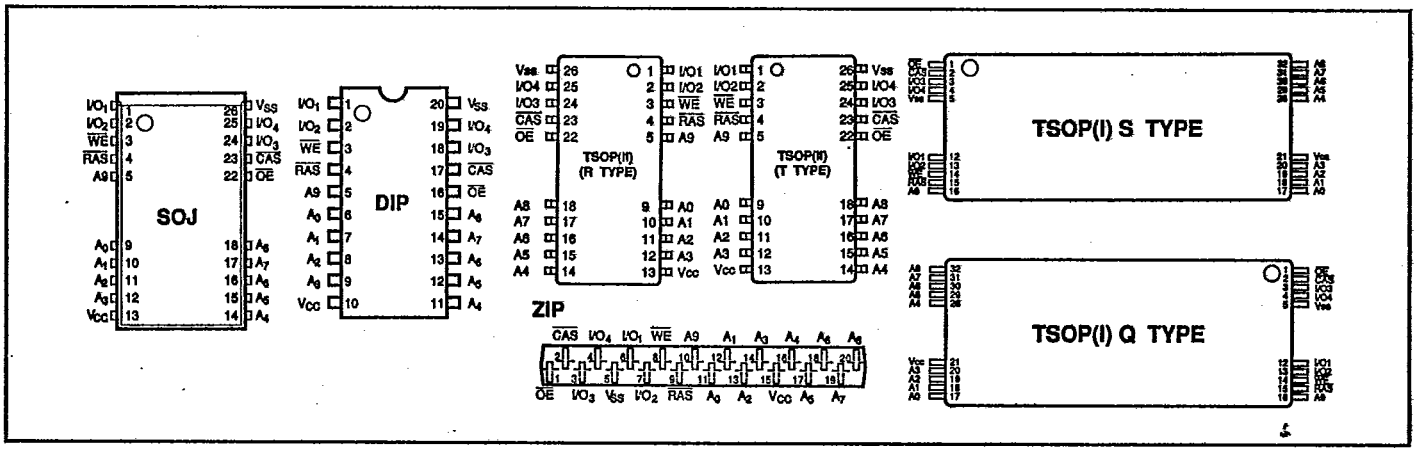


MM4M200 J8/J9 SERIES - 4M x 8/9

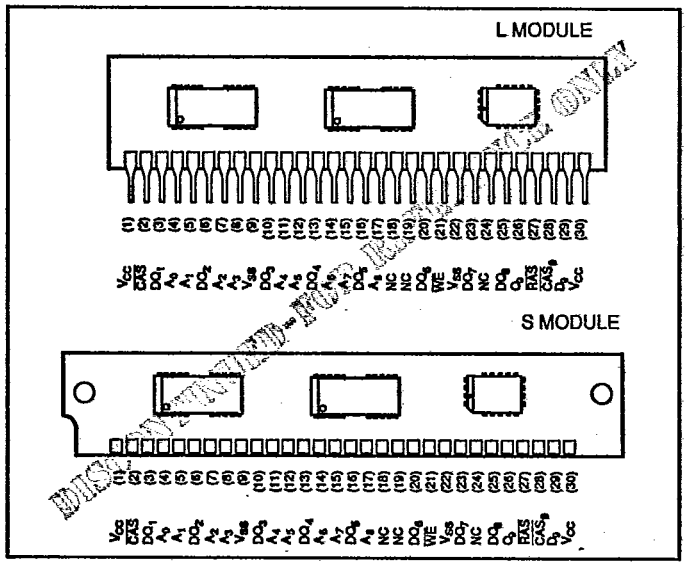


Notes:
1. * No connection (NC) for 4M x 8 bit module.
2. ** This chip is not mounted on 4M x 8 bit module.

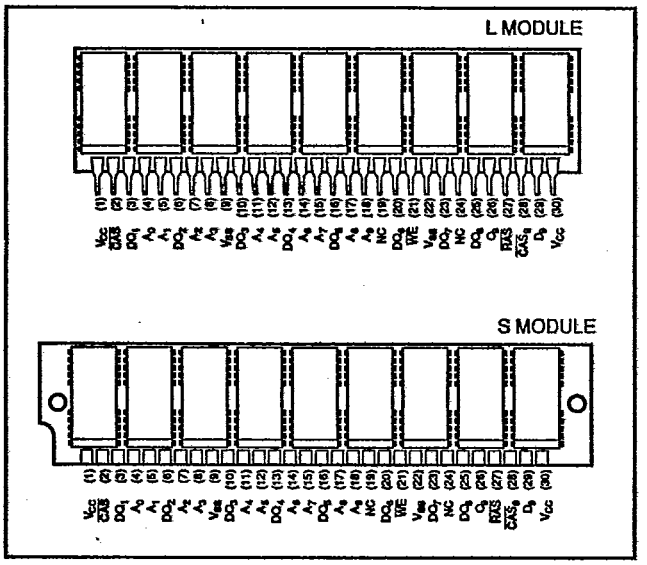
AAA4M200 SERIES - 1M x 4



MM256K0J9 SERIES - 256K x 9 (3 CHIP VERSION)



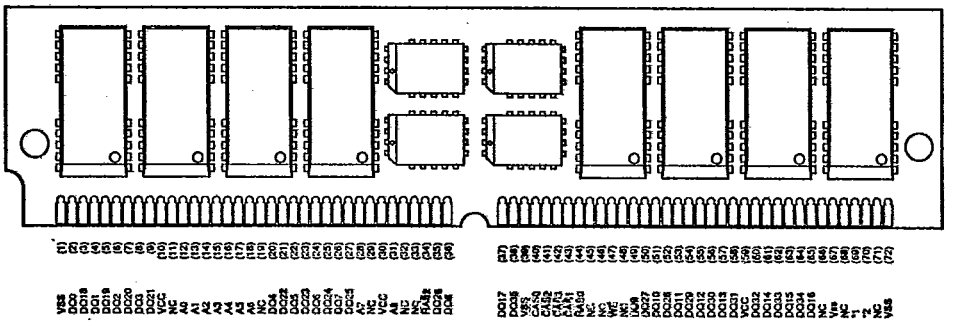
MM1M300J8/J9 SERIES - 1M x 8/9



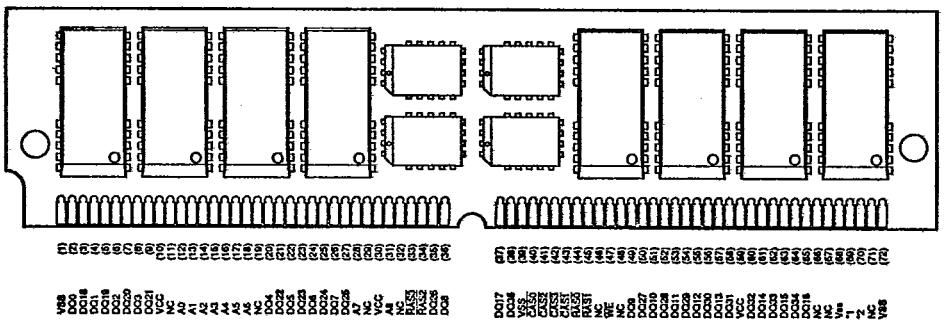
PACKAGE AND PINOUT DETAILS

MM256K0J36/MM512K0J36 SERIES - 256K x 36 and 512K x 36

256K x 36
(Components on one side of PCB)



512K x 36
(Components on both sides of PCB)



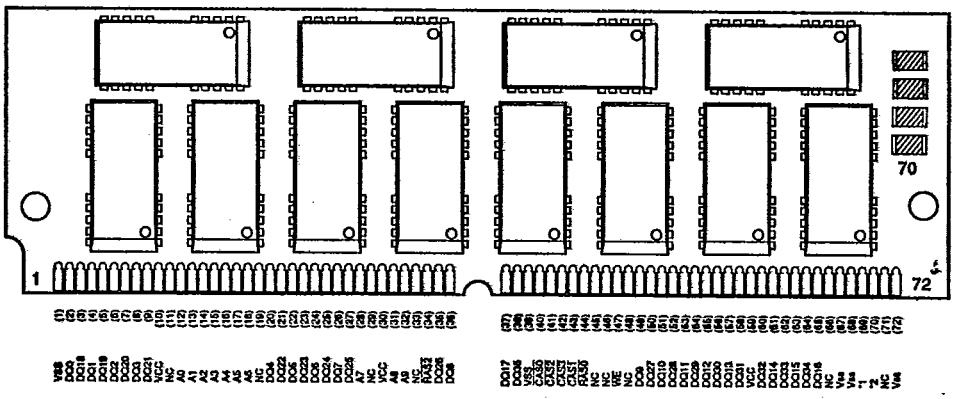
Pinout Variations

	-06	-07	-08
*1	TBD	Vss	NC
*2	TBD	NC	Vss

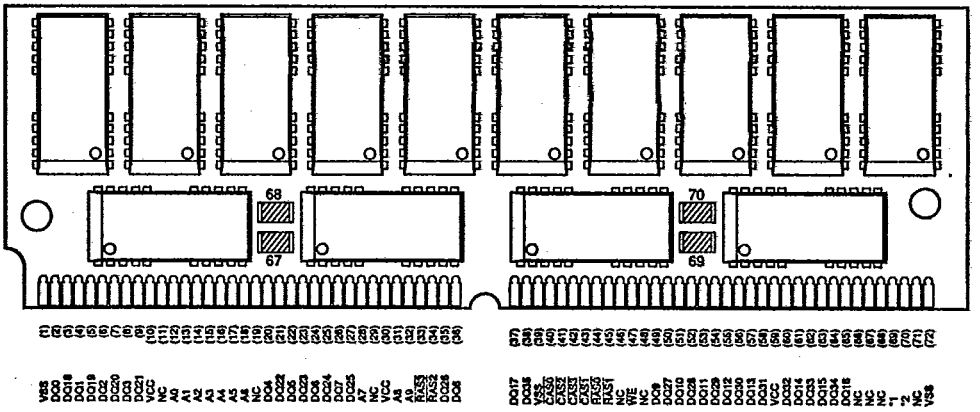
Note: TBD: To be determined

MM1M0J36/MM2M0J36 - 1M x 36 and 2M x 36

1M x 36
(Components on one side of PCB)



2M x 36
(Components on both sides of PCB)



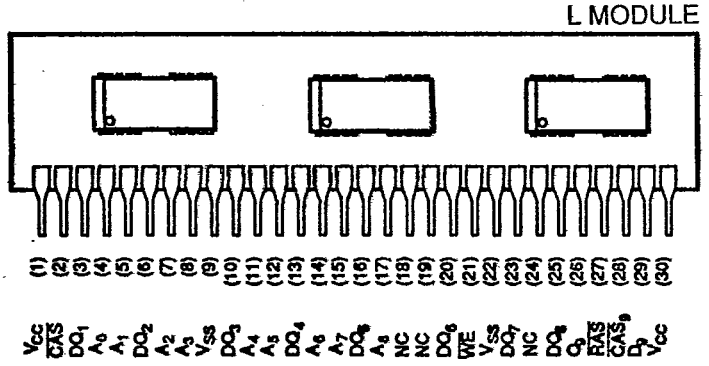
Pinout Variations

	-06	-07	-08
*1	TBD	Vss	NC
*2	TBD	NC	Vss

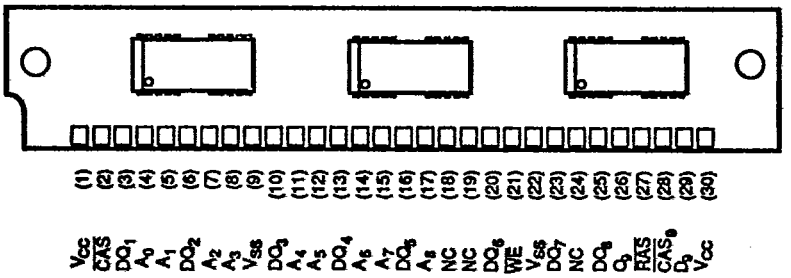
Note: TBD: To be determined

MM256K0J8R/J9R SERIES - (3 CHIP "R" VERSION)
MM1M0J8/J9 SERIES - (3 CHIP VERSION)
MM1M0J8R/J9R SERIES - (3 CHIP "R" VERSION)

L MODULE



S MODULE



Pinout 18 Variations

256K x 8/9	3 Chip "R"	N/C
1M x 8/9	3 Chip	A9
1M x 8/9	3 Chip "R"	A9