Integrated Device Technology, Inc.

CMOS CACHE CONTROLLER WITH TAG FOR INTEL® PENTIUM™ PROCESSORS

ADVANCE INFORMATION
IDT71V280

FEATURES

- Provides the Cache Tag, Status Bits, CPU interface control and Data SRAM control for Pentium CPU-based systems
- Supports 2-1-1-1 zero-wait state reads and writes for 50MHz Pentium CPU-based systems
- Offers 3-1-1-1 burst performance for 66MHz Pentium CPU-based systems
- Supports a write-back, look aside cache architecture
- 10-bit tag field for up to 512MB cacheable address space using four words per line
- Provides Pentium address pipelining support for optimum burst performance
- Supports cache sizes of 256KB, 512KB, and 1MB
- 2 status bits offer four encoded combinations:
  - Invalid
  - Shared (valid clean, write-through)
  - Exclusive (valid clean, write-back)
  - Modified (valid dirty)
- Supports asynchronous and burst data SRAMs
- 3.3V (±5%) power supply voltage
- Packaged in a 128-lead TQFP for optimum board density

DESCRIPTION

The IDT71V280 provides the Cache Tag SRAM, Status Bits, CPU interface control, and Data SRAM control for a Pentium secondary cache implementation. Combining these elements in a single, cost-effective CMOS chip provides the system designer with greatly enhanced cache performance by reducing cache-subsystem delays. The IDT71V280 provides 2-1-1-1 zero-wait state secondary cache performance at frequencies up to 50MHz and 3-1-1-1 performance at 60 and 66MHz in Pentium applications.

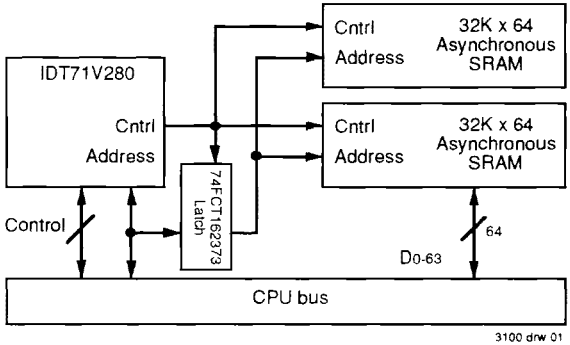
The IDT71V280 supports a number of different system configurations and performance levels. Cache size, cache wait-state performance, Data SRAM type, and Data SRAM size offer the system designer a wide range of cache choices to optimize the cache configuration to his exact system needs. Four mode pins determine the cache subsystem configuration and performance levels, with both asynchronous and burst data SRAM support options offered.

The IDT71V280 uses a single 3.3V power supply to provide full JEDEC LVTTL compatibility in 3.3V applications. Multiple GND pins provide excellent noise immunity at high frequencies, and the space saving 14mm x 20mm 128-pin Thin Quad Flat Pack offers a small board footprint and profile for maximum packing density.

TYPICAL CACHE SUBSYSTEM CONFIGURATIONS

FUNCTIONAL BLOCK DIAGRAM

1. Aynchronous SRAM—Interleaved



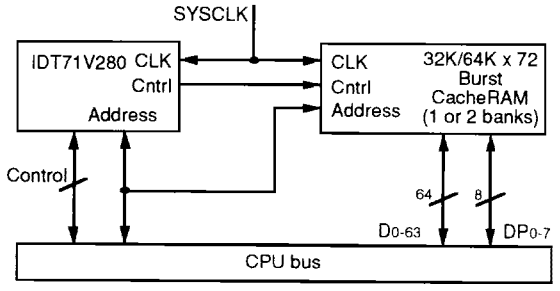
3100 drw 01

FUNCTIONAL DESCRIPTION

When used with two interleaved banks of asynchronous data SRAMs, the IDT71V280 supports zero wait-state bursts on read and write cycles for 50MHz systems and one wait-state bursts at 66MHz. All control for the SRAMs, including separate least significant address bits, are provided by the IDT71V280 to support this configuration.

FUNCTIONAL BLOCK DIAGRAM

2. Burst SRAM



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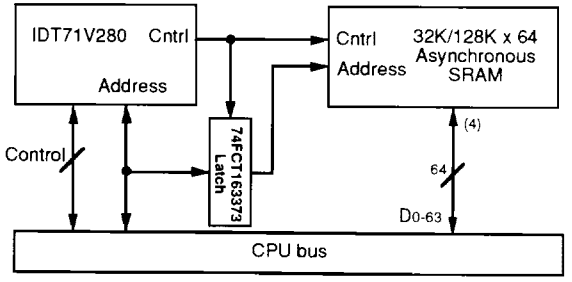
3. Asynchronous SRAM—Single Bank



3100 drw 03

FUNCTIONAL DESCRIPTION

The IDT71V280 can also be used with Burst CacheRAMs. The IDT71V280 provides all control signals necessary for up to 128K depth of data SRAM, using either one or two banks of data SRAMs. Therefore, all standard burst SRAM configurations may be used including 32K x 18, 32K x 36 and 64K x 18. For 50MHz, 2-1-1-1 zero wait-state operation can be achieved with 12ns burst SRAMs; for 66MHz, the IDT71V280 will operate with Pipelined Burst RAMs providing 3-1-1-1 performance.

The IDT71V280 will support a single bank of asynchronous SRAMs, allowing a minimum cost cache solution. With 15ns SRAMs this configuration provides 2-2-2-2 performance at 50MHz and 3-2-2-2 performance at 66MHz. This configuration will be especially useful for systems requring a minimum part count solution based on power and space constraints.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	3.15	3.3	3.45	V
GND	Supply Ground	0	0	0	V
V_{IH}	Input High Voltage	2.2	3.0	V_{CC}+0.3	V
V_{IL}	Input Low Voltage	–0.5(1)	—	0.8	V

NOTE: 3100 tbl 01

1. V_{IL} (min.) = –1.5V for pulse width of less than 10ns, once per cycle.

CAPACITANCE(1) (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Condition	IDT71V280	Unit
C_{IN}	Input Capacitance (Address, Control)	V_{IN} = 0V	5	pF
C_{IN}	Input Capacitance (CLK)	V_{IN} = 0V	5	pF
C_{OUT}	Output Capacitance (Control)	V_{IN} = 0V	7	pF
$C_{I/O}$	Data I/O Capacitance	V_{OUT} = 0V	7	pF

NOTE: 3100 tbl 02

1. These parameters are maximum values and guaranteed but not tested.

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Value	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +4.5	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	–0.5 to $+V_{CC}$+0.5	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	–65 to +135	°C
T_{STG}	Storage Temperature	–65 to +150	°C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current	20	mA

NOTES: 3100 tbl 03

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliabilty.
2. V_{CC} terminal only.
3. Input, Output, and I/O terminals; 4.5V maximum.

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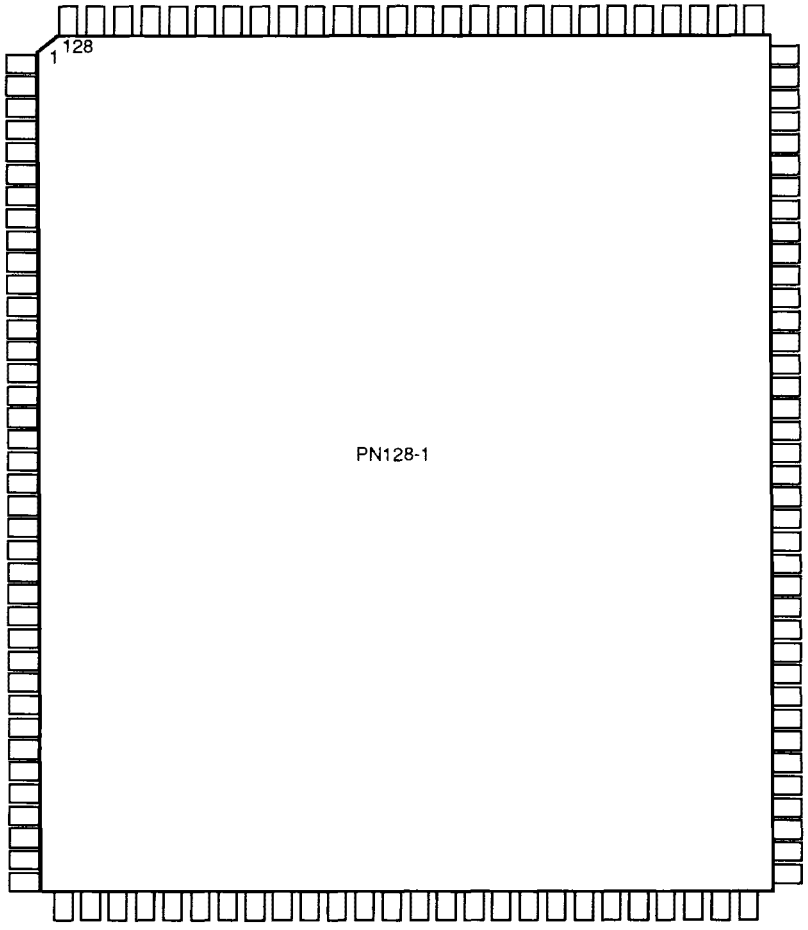
PIN CONFIGURATION



3100 drw 04

TQFP
TOP VIEW

MODE AND CONFIGURATION TABLE

M 3	M 2	M 1	M 0	Performance			Cache	SRAM	Number	
				Read Hit	Write/BurstWrite	Line Fill	Size (B)	Type[1]	of Banks	Notes
0	0	0	0	2-2-2-2	2/2-2-2-2	4-2-2-2	256K	32K x 8 A	1	
0	0	0	1	3-2-2-2	3/3-2-2-2	4-2-2-2	256K	32K x 8 A	1	
0	0	1	0	2-1-1-1	2/2-1-1-1	4-1-1-1	512K	32K x 8 A	2	Interleaved
0	0	1	1	3-2-2-2	3/3-2-2-2	4-2-2-2	512K	32K x 8 A	2	Interleaved
0	1	0	0	2-1-1-1	2/2-1-1-1	4-1-1-1	256K	Burst	1	32K deep Burst SRAMs
0	1	0	1	3-1-1-1	3/3-1-1-1	4-1-1-1	256K	Pipe-Burst	1	32K deep Pipelined Burst SRAMs
0	1	1	0	2-1-1-1	2/2-1-1-1	4-1-1-1	512K	Burst	1	64K deep Burst SRAMs
0	1	1	1	3-1-1-1	3/3-1-1-1	4-1-1-1	512K	Pipe-Burst	1	64K deep Pipelined Burst SRAMs
1	0	0	0	2-2-2-2	2/2-2-2-2	4-2-2-2	1M	128K x 8 A	1	
1	0	0	1	3-2-2-2	3/3-2-2-2	4-2-2-2	1M	128K x 8 A	1	
1	0	1	0	2-1-1-1	2/2-1-1-1	4-1-1-1	1M	Burst	2	2 banks of 64K deep Burst SRAMs
1	0	1	1	3-1-1-1	3/3-1-1-1	4-1-1-1	1M	Burst	2	2 banks of 64K deep Pipelined Burst SRAMs
1	1	0	0	—	—	—	—	—	—	Reserved
1	1	0	1	—	—	—	—	—	—	Reserved
1	1	1	0	—	—	—	—	—	—	Reserved
1	1	1	1	—	—	—	—	—	—	Reserved

NOTE:
1. A = Asynchronous.

3100 tbl 04

PIN DEFINITION

Symbol	Pin Function	I/O	Level	Description
CLK	Clock	I	N/A	This is the clock input to the IDT71V280. All timing references for the cache are made with respect to this input. If the clock input is to be disabled, PWRDN# must first be asserted.
PLL	PLL Output	O	N/A	This pin is a free running output that should be loaded the same as the WE# pins and is used to adjust the phase of the internal clock.
RESET	Reset	I	HIGH	If RESET is sampled HIGH by the IDT71V280, the control logic is reset to a known state. In addition, when RESET is sampled HIGH, the resettable status bits are forced to INVALID.
FLUSH#	Flush	I	LOW	When the FLUSH# input is sampled LOW, the IDT71V280 control logic is placed into a flush pending state. While the IDT71V280 is in a flush pending state, it does not alter how it handles CPU bus cycles. The IDT71V280 initiates a cache flush when it detects a CPU Flush Acknowledge special bus cycle.
SBOFF#	System Backoff	I	LOW	This input forces the IDT71V280 off of the CPU address and data buses. When SBOFF# is asserted, the IDT71V280 will only recognize invalidation and snoop cycles; however, the cache will not provide the data and address for an invalidation/snoop hit to a dirty line until SBOFF# is deasserted. When SBOFF# is sampled asserted, it causes the IDT71V280 to assert CBOFF# synchronously.
CBOFF#	Cache Backoff	O	LOW	This output is asserted by the cache to force the CPU off the bus when the IDT71V280 detects that a dirty line must be evicted from the IDT71V280. The IDT71V280 also asserts CBOFF# when its SBOFF# input is sampled asserted.
EADS#	External Address Strobe	I	LOW	This input is used by external devices to perform a snoop to a cache line in the IDT71V280. The IDT71V280 recognizes the initiation of a snoop access when EADS# is sampled LOW. The IDT71V280 ignores ADS# if it is sampled LOW concurrent with sampling EADS# LOW.
INV	Invalidate	I	HIGH	This input is used in conjunction with EADS# to snoop, or invalidate, a cache line. If INV is HIGH, the IDT71V280 will consider the access as an invalidation. If INV is LOW when EADS# is asserted the IDT71V280 will consider the access as a snoop.

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PIN DEFINITION (CONTINUED)

Symbol	Pin Function	I/O	Level	Description
ADS#	Address Strobe	I/O	LOW	This pin is used by external devices to inform the IDT71V280 that a valid address is present on the input of the cache. This pin is driven by the IDT71V280, while the IDT71V280 is asserting CBOFF#, to evict a dirty line from the cache or to supply dirty data for a snoop hit.
NA#	Next Address	I/O	LOW	This pin is driven LOW for one clock cycle by the IDT71V280 during burst read hits to pipeline the next CPU bus cycle into the current one. This pin is an input when the memory controller is servicing the memory cycle.
M/IO#	Memory/I/O	I/O	N/A	This pin is used by external devices to inform the IDT71V280 that a memory access is being made when this pin is HIGH, or that an I/O access is being made when this pin is LOW. I/O cycles are not considered cacheable. This pin is driven HIGH by the IDT71V280, while the IDT71V280 is asserting CBOFF#, to evict a dirty line from the cache or to supply dirty data for a snoop hit.
W/R#	Write/Read	I/O	N/A	This pin is used by external devices to inform the cache that either a write is being performed when this pin is HIGH, or that a read is being performed if this pin is LOW. This pin is driven HIGH by the IDT71V280, while the IDT71V280 is asserting CBOFF#, to evict a dirty line from the cache, or to supply dirty data for a snoop hit.
WRPT#	Write Pass Through	I	LOW	This input from the system is sampled concurrent with the beginning of a CPU bus cycle. If it is sampled LOW, the IDT71V280 passes control of servicing the write cycle to the system controller.
D/C#	Data/Control	I/O	N/A	This pin is used by the IDT71V280 in conjunction with the M/IO#, W/R#, BE_7#-BE_0# to determine when a special bus cycle is being executed, and the type of special bus cycle being executed. This pin is driven HIGH by the IDT71V280, while the IDT71V280 is asserting CBOFF#, to evict a dirty line from the cache or to supply dirty data for a snoop hit.
START#	Memory Start	O	LOW	This output is driven LOW by the IDT71V280 to inform the system that it must service the current memory cycle. START# is also driven LOW when the IDT71V280 is writing back a dirty line from the cache.
CBRDY#	Burst Ready Output	O	LOW	The IDT71V280 drives this signal to the CPU BRDY# at all times. It is driven LOW to indicate the successful transfer of data. CBRDY# is a combination of the internally generated logic (for read hits, and write hits that are not write through), and the SBRDY# input (all cache misses, non-cacheable and write through cycles). There is a register delay in the SBRDY# to CBRDY# path.
SBRDY#	Burst Ready Input	I	LOW	The system drives this signal into the IDT71V280 at all times. It is driven LOW to indicate the successful transfer of data to or from the system. CBRDY# is driven LOW in response to SBRDY# being sampled LOW. The IDT71V280 delays SBRDY# (through CBRDY#) to the CPU by one cycle.
CACHE#	Cacheability	I/O	LOW	This pin is sampled by the IDT71V280 at the beginning of a bus cycle to determine the length and cacheability of the cycle. If CACHE# is LOW at the beginning of a read cycle, the read is cacheable and contains four data words. If CACHE# is HIGH at the beginning of a read cycle, the cycle consists of a single data word. If CACHE# is LOW at the beginning of a write cycle, the CPU will execute a four word write back. If CACHE# is HIGH at the beginning of a write cycle, the CPU will write out a single word. When the IDT71V280 executes a write back to evict a dirty line this pin is driven LOW at the same time that CBOFF# is asserted. This pin is driven LOW when the IDT71V280 is performing a write cycle for either a line eviction, or to supply dirty data for a snoop hit.
A_{31}-A_3	Address	I/O	N/A	These are the CPU address bus lines. They are inputs to the IDT71V280, except when the IDT71V280 is performing a write cycle for either a line eviction or to supply dirty data for a snoop hit.
BE_7#-BE_0#	Byte Enable	I/O	LOW	These are the byte enable inputs to the IDT71V280. These inputs are sampled during write cycles to control byte writes, and they are used in conjunction with M/IO#, W/R#, and D/C# to determine when a special bus cycle is being executed. These pins are driven LOW when the IDT71V280 is performing a write cycle for either a line eviction, or to supply dirty data for a snoop hit.

PIN DEFINITION (CONTINUED)

Symbol	Pin Function	I/O	Level	Description
CS#	Cache Select	I	LOW	This input is used to disable the IDT71V280 from responding to any memory or snoop cycles. The IDT71V280 will not respond to a memory, or snoop, cycle unless it samples CS# LOW the clock cycle prior to and the clock concurrent with sampling either ADS# or EADS# LOW.
CWB/WT#	Write Back/Write Write Cache	O	N/A	Output from the IDT71V280 to the CPU. It is driven to reflect whether data being accessed during a cache hit is write back or write through in nature. CWB/WT# is also driven LOW when SWB/WT# is sampled LOW.
SWB/WT#	Write Back/Write Through System	I	N/A	Input to the IDT71V280 when a line of data is loaded into the cache. If PWT is sampled HIGH at the beginning of a read cycle that results in a cache miss, the value of this pin is ignored and the line returned is considered write through. If PWT is sampled LOW at the beginning of a read cycle, and SWB/WT# is sampled HIGH during the first work transfer of a line fill, the line is marked as write back. If PWT is sampled LOW at the beginning of a read cycle, and SWB/WT# is sampled LOW during the first work transfer of a line fill, the line is marked as write through. If the line is marked as write back, the cache will update its memory contents without passing the cycle on to other devices during a memory write cycle. If the line is marked as write through, the cache will update its memory contents when the write cycle is serviced by the system. When SWB/WT# is sampled LOW, it forces CWB/WT# LOW synchronously.
HITM#	Hit-Modified Input	I	LOW	This input is used to indicate to the IDT71V280 that a dirty line is hit in the CPU level 1 cache during inquire (snoop or invalidate) cycles. When HITM# is sampled asserted, it causes the IDT71V280 to assert CHITM# synchronously.
CHITM#	Hit-Modified Output	O	LOW	IDT71V280 asserted output to indicate that an inquire (snoop or invalidate) cycle hits a dirty line in the cache. The IDT71V280 also asserts CHITM# when its HITM# input is asserted.
MOD#	Modified Line	O	LOW	Output asserted by the IDT71V280 to indicate that a dirty line is being accessed during a memory read or write bus cycle. MOD# does not depend on hit or miss status.
SKEN#	Cacheable Data Input	I	LOW	This pin is sampled by the IDT71V280 to determine whether the data being returned during a read miss is cacheable. SKEN# must be sampled LOW at least one cycle before the first word is transferred to the cache. During Reset, SKEN# is used to indicate to the IDT71V280 whether write allocation is enabled or disabled. If asserted, write alloction is enabled.
PWT	Page Write Through	I/O	HIGH	This input is sampled by the IDT71V280 at the initiation of memory read and write cycles. If PWT is sampled HIGH at the initiation of a memory read that results in a cache miss, the line returned is automatically considered write through. If PWT is sampled HIGH at the initiation of memory write cycle, the cache ignores the value of its internal write back/write through flag, and it is forced to treat the write cycle as write through. The IDT71V280 drives this pin LOW, while CBOFF# is asserted, when the IDT71V280 executes a write cycle to evict a dirty line from the cache or to supply dirty data for a snoop hit.
HLDA	Bus Hold Acknowledge	I	HIGH	Connects to the HLDA output pin from the CPU, which is used to acknowledge a bus hold request from HOLD. Except when the IDT71V280 is performing a write back operation, HLDA will propagate through to CHLDA with a one cycle delay. When the IDT71V280 is performing a write back operation, it will block the propagation of HLDA until it has released control of the bus.
CHLDA	Bus Hold Acknowledge	O	HIGH	Typically reflects HLDA input delayed by one clock cycle. However, the IDT71V280 will force CHLDA LOW while it is performing a write back operation. Once the IDT71V280 has released SBOFF#, it will allow CHLDA to be asserted.
LOCK#	Lock	I/O	LOW	If LOCK# is sampled LOW at the beginning of a read cycle and the data in the cache is not dirty, the read cycle is treated as a non-cacheable read miss. If the cache contains dirty data at the address location requested by the locked read cycle, the IDT71V280 first evicts the dirty line, then the read cycle is treated as a non-cacheable read miss. If LOCK# is sampled LOW at the beginning of a write cycle, the IDT71V280 ignores its internal write back/write through flag, and treats the write cycle as write through. The IDT71V280 drives

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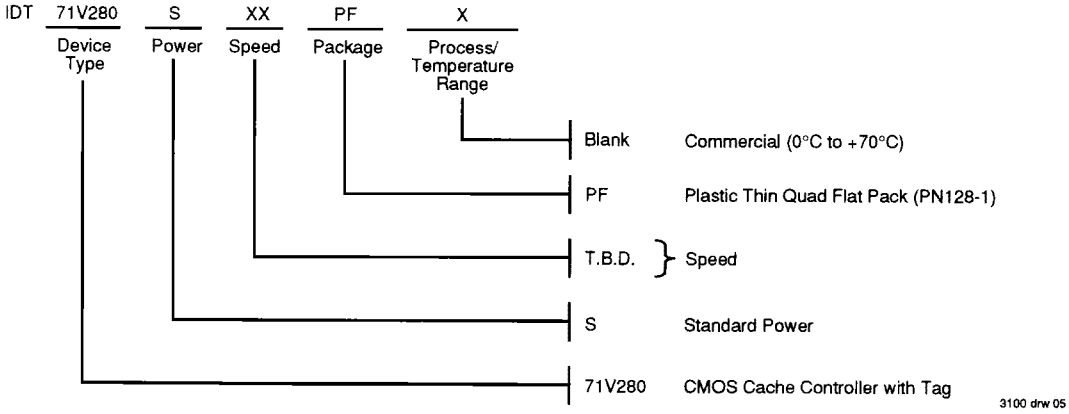
PIN DEFINITION (CONTINUED)

Symbol	Pin Function	I/O	Level	Description
				this pin HIGH, while CBOFF# is asserted, when it executes a write cycle to evict a dirty line from the cache or to supply dirty data for a snoop hit.
OEA#(0:1), OEB#(0:1)	Data RAM Output Enable	O	LOW	These pins are used to assert output enable of the data SRAMs, two for each bank of SRAMs.
WE7#- WE0#	Data RAM Write Enable	O	LOW	These pins are used to assert Write Enable of the data SRAMs, one for each byte.
CEA#(0:1), CEB#(0:1)	Data RAM Chip Enable	O	LOW	These pins are used to assert Chip Enable of the data SRAMs, one for each bank of SRAMs.
ADV#	Data RAM Adv	O	LOW	This pin is used with burst SRAMs to advance the internal address counter
AD3/4A(0:1), AD4/4B(0:1)	Data RAM Address	O	N/A	These pins are the least significant two address lines of the data SRAMs when asynchronous SRAMs are used. When one bank of SRAMs is used these pins are AD3 and AD4. If two banks of interleaved SRAM are used these pins are AD4A and AD4B; that is, the least significant address of the odd bank and the even bank.
ALE/ ADSC#	Address LE/ Controller ADS#	O	LOW	This pin is used to latch the CPU address into external latch(es) for the asynchronous data SRAMs, and is ADSC# when a burst SRAM implementation is used.
MODE (0:3)	Mode Select	I	N/A	These pins are used to select the mode in which the IDT71V280 operates and are not allowed to change once the IDT71V280 is powered up.
PWRDN#	Power Down	I	LOW	This pin is used to force the IDT71V280 into a Low Power Mode while retaining data. As long as this input is asserted the IDT71V280 will not initiate any new activity. After this input is negated, the IDT71V280 will respond normally within 1ms.
Vcc	Power	N/A	N/A	Power supply inputs for the IDT71V280.
GND	Ground	N/A	N/A	Ground pins of the IDT71V280.

3100 tbl 05

ORDERING INFORMATION



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