

# DRAM Dual-In-Line Memory Module (DIMM)

## 8, 16, and 32 Megabyte

- JEDEC—Standard 168—Lead Dual—In—Line Memory Module (DIMM)
- Single 5 V Power Supply, TTL-Compatible Inputs and Outputs
- Extended Data Out (EDO)
- $\overline{\text{RAS}}$ —Only Refresh,  $\overline{\text{CAS}}$  Before  $\overline{\text{RAS}}$  Refresh, Hidden Refresh
- 8MB/16MB: 1024 Cycle Refresh: 16 ms (Max)
- 32MB: 2048 Cycle Refresh: 32 ms (Max)
- Keys Prevent Accidental Insertion into 3.3 V Systems
- Serial Presence Detect (SPD) Provides Module Configuration Information

### PART NUMBERS (See Page 31 for Definitions)

Organization	60	70
1M x 72	MB721BT08TADG60	MB721BT08TADG70
2M x 72	MB722BT08TADG60	MB722BT08TADG70
4M x 72	MB724CT00TADG60	MB724CT00TADG70

### KEY TIMING PARAMETERS

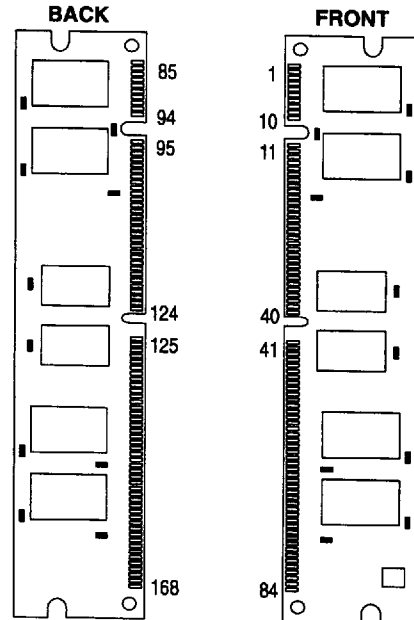
Speed	t <sub>RC</sub> (ns)	t <sub>RAC</sub> (ns)	t <sub>CAC</sub> (ns)	t <sub>AA</sub> (ns)	t <sub>EPC</sub> (ns)
60	104	60	17	30	25
70	124	70	20	35	30

### ADDITIONAL PARAMETERS

Configuration	Speed	Active Power Dissipation (mW) (Max)	Standby Power Dissipation	
			TTL	CMOS
8MB	60	4,895	66	33
	70	4,125		
16MB	60	4,961	132	66
	70	4,191		
32MB	60	10,890	198	99
	70	9,405		

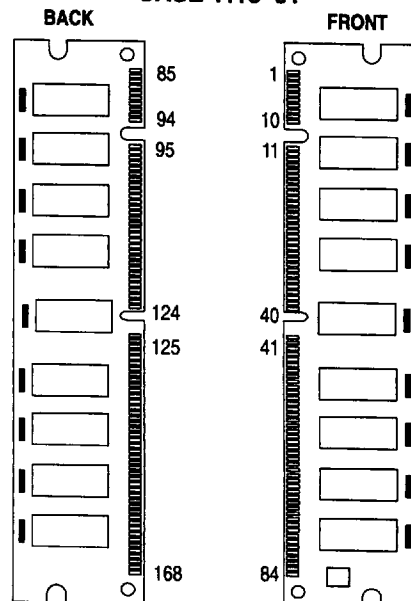
**1, 2, 4M x 72**  
5 V, EDO, Unbuffered

1M x 72 (8MB), 2M x 72 (16MB)  
168-LEAD DIMM  
CASE 1115A-01



BACK NOT POPULATED ON 1M x 72 (8MB)

4M x 72 (32MB)  
168-LEAD DIMM  
CASE 1115-01



**PIN ASSIGNMENTS**

Front Side						Back Side									
Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	V <sub>SS</sub>	22	CB1	43	V <sub>SS</sub>	64	V <sub>SS</sub>	85	V <sub>SS</sub>	106	CB5	127	V <sub>SS</sub>	148	V <sub>SS</sub>
2	DQ0	23	V <sub>SS</sub>	44	$\overline{G2}$	65	DQ21	86	DQ32	107	V <sub>SS</sub>	128	NC	149	DQ53
3	DQ1	24	NC	45	$\overline{RAS2}$	66	DQ22	87	DQ33	108	NC	129	$\overline{RAS3^*}$	150	DQ54
4	DQ2	25	NC	46	$\overline{CAS2}$	67	DQ23	88	DQ34	109	NC	130	$\overline{CAS6}$	151	DQ55
5	DQ3	26	V <sub>CC</sub>	47	$\overline{CAS3}$	68	V <sub>SS</sub>	89	DQ35	110	V <sub>CC</sub>	131	$\overline{CAS7}$	152	V <sub>SS</sub>
6	V <sub>CC</sub>	27	WE0	48	$\overline{WE2}$	69	DQ24	90	V <sub>CC</sub>	111	NC	132	NC	153	DQ56
7	DQ4	28	$\overline{CAS0}$	49	V <sub>CC</sub>	70	DQ25	91	DQ36	112	$\overline{CAS4}$	133	V <sub>CC</sub>	154	DQ57
8	DQ5	29	$\overline{CAS1}$	50	NC	71	DQ26	92	DQ37	113	$\overline{CAS5}$	134	NC	155	DQ58
9	DQ6	30	$\overline{RAS0}$	51	NC	72	DQ27	93	DQ38	114	$\overline{RAS1^*}$	135	NC	156	DQ59
10	DQ7	31	$\overline{G0}$	52	CB2	73	V <sub>CC</sub>	94	DQ39	115	NC	136	CB6	157	V <sub>CC</sub>
11	DQ8	32	V <sub>SS</sub>	53	CB3	74	DQ28	95	DC40	116	V <sub>SS</sub>	137	CB7	158	DQ60
12	V <sub>SS</sub>	33	A0	54	V <sub>SS</sub>	75	DQ29	96	V <sub>SS</sub>	117	A1	138	V <sub>SS</sub>	159	DQ61
13	DQ9	34	A2	55	DQ16	76	DQ30	97	DQ41	118	A3	139	DQ48	160	DQ62
14	DQ10	35	A4	56	DQ17	77	DQ31	98	DQ42	119	A5	140	DQ49	161	DQ63
15	DQ11	36	A6	57	DQ18	78	V <sub>SS</sub>	99	DQ43	120	A7	141	DQ50	162	V <sub>SS</sub>
16	DQ12	37	A8	58	DQ19	79	NC	100	DQ44	121	A9	142	DQ51	163	NC
17	DQ13	38	A10**	59	V <sub>CC</sub>	80	NC	101	DQ45	122	NC	143	V <sub>CC</sub>	164	NC
18	V <sub>CC</sub>	39	NC	60	DQ20	81	NC	102	V <sub>CC</sub>	123	NC	144	DQ52	165	SA0
19	DQ14	40	V <sub>CC</sub>	61	NC	82	SDA	103	DQ46	124	V <sub>CC</sub>	145	NC	166	SA1
20	DQ15	41	V <sub>CC</sub>	62	NC	83	SCL	104	DQ47	125	NC	146	NC	167	SA2
21	CB0	42	NC	63	NC	84	V <sub>CC</sub>	105	CB4	126	NC	147	NC	168	V <sub>CC</sub>

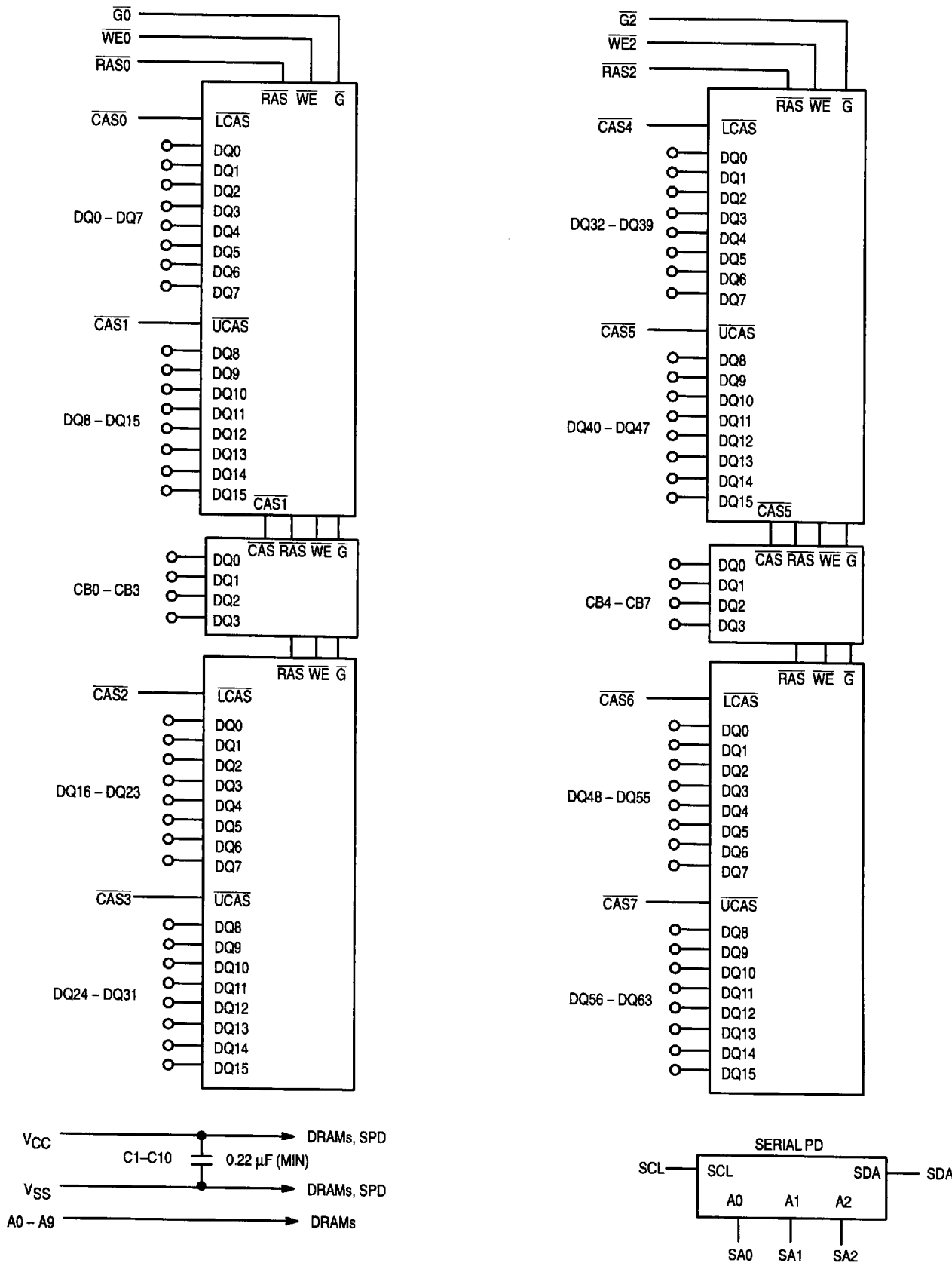
\* NC on the 8 MB and 32 MB.

\*\* NC on the 8 MB and 16 MB.

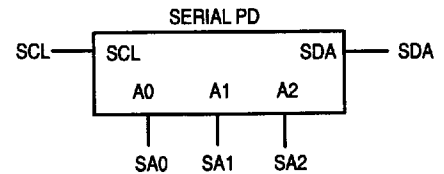
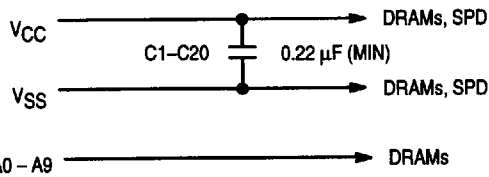
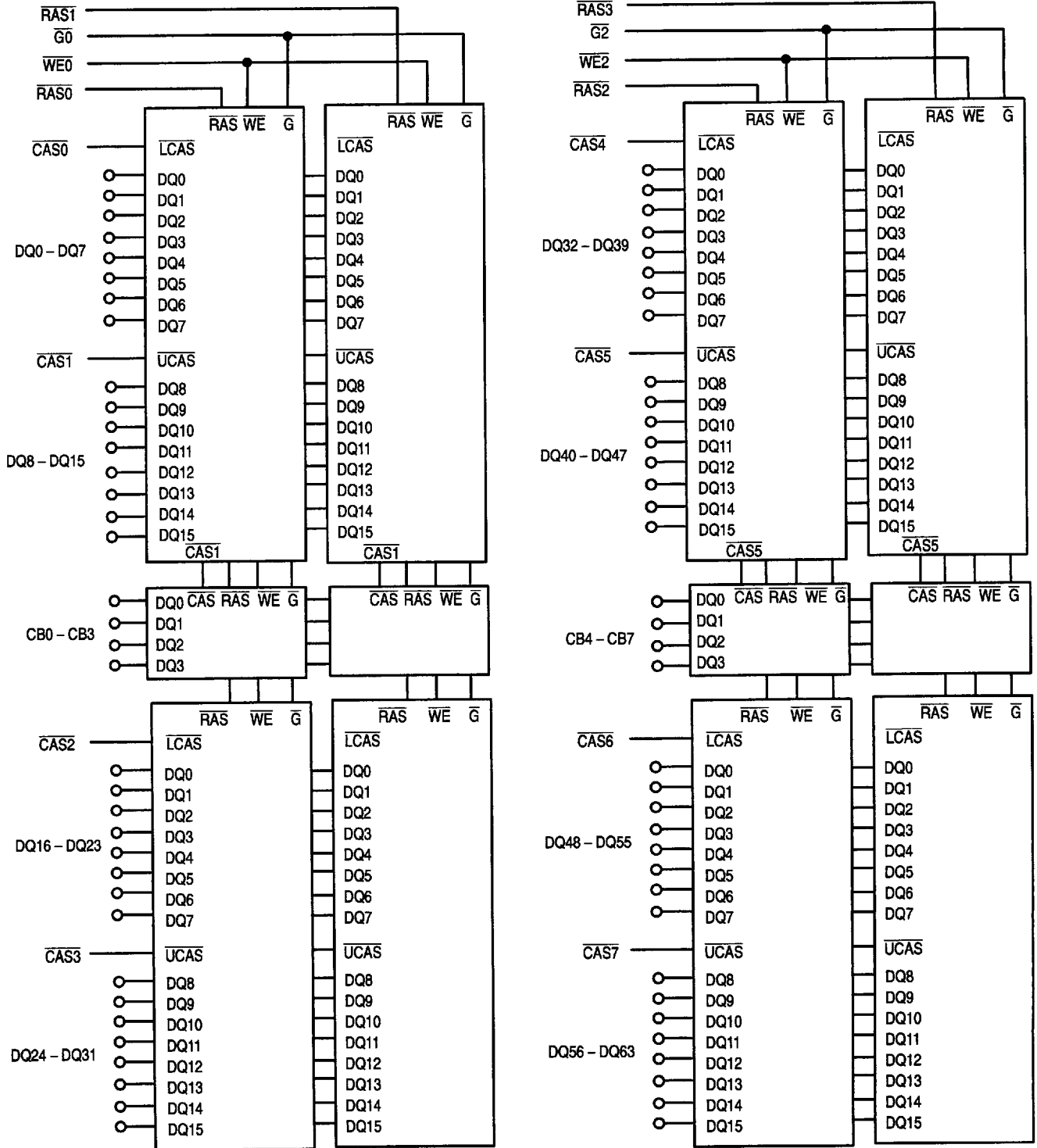
PIN NAMES	
A0 – A10	Address Inputs
DQ0 – DQ63	Data Input/Output
CB0 – CB7	Data Input/Output
$\overline{CAS0}$ – $\overline{CAS7}$	Column Address Strobe
$\overline{RAS0}$ – $\overline{RAS3}$	Row Address Strobe
$\overline{WE0}$ , $\overline{WE2}$	Write Enable
$\overline{G0}$ , $\overline{G2}$	Output Enable
SA0 – SA2	SPD Address
SCL	SPD Clock
SDA	SPD Data I/O
V <sub>CC</sub>	Power
V <sub>SS</sub>	Ground
NC	No Connection

All power supply and ground pins must be connected for proper operation of the device.

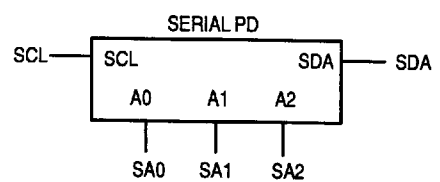
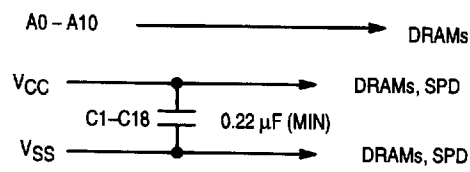
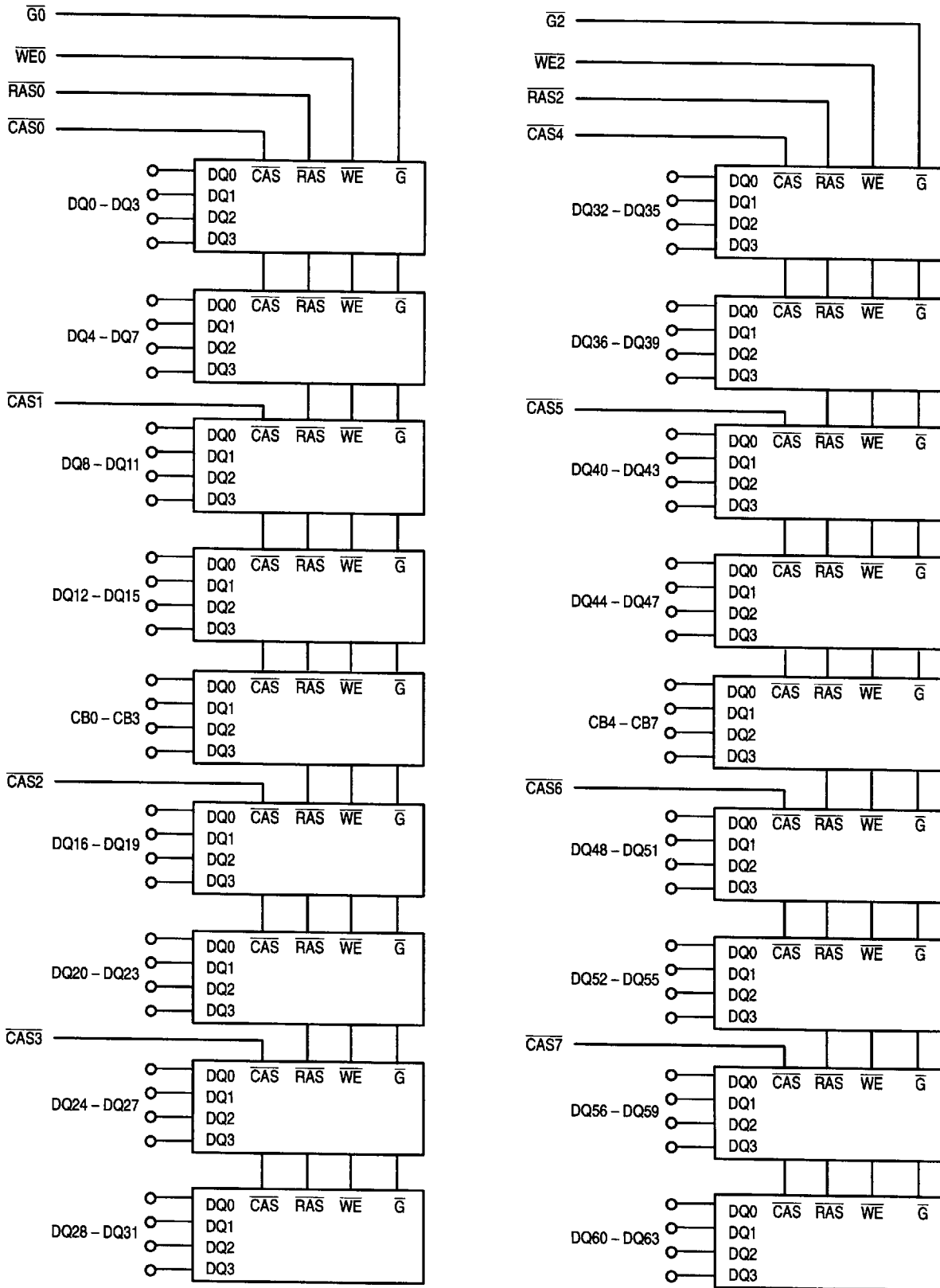
8MB BLOCK  
DIAGRAM



16MB BLOCK  
DIAGRAM



32MB BLOCK  
DIAGRAM



**ABSOLUTE MAXIMUM RATINGS** (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	$V_{CC}$	- 0.5 to + 7	V
Voltage Relative to $V_{SS}$ (For Any Pin Except $V_{CC}$ )	$V_{in}, V_{out}$	- 0.5 to $V_{CC} + 0.5$	V
SPD Pins	$V_{in}, V_{out}$	- 0.3 to 6.5	V
Data Output Current per DQ Pin	$I_{out}$	50	mA
Power Dissipation	$P_D$	6.4 12.8 16.2	W
		8MB	
		16MB	
		32MB	
Operating Temperature Range	$T_A$	0 to + 70	°C
Storage Temperature Range	$T_{stg}$	- 55 to + 150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

**DC OPERATING CONDITIONS AND CHARACTERISTICS**

( $V_{CC} = 5\text{ V} \pm 10\% \text{ V}$ ,  $T_A = 0$  to  $70^\circ\text{C}$ , Unless Otherwise Noted)

**RECOMMENDED OPERATING CONDITIONS** (All Voltages Referenced to  $V_{SS}$ )

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	$V_{CC}$	4.5	5	5.5	V
	$V_{SS}$	0	0	0	
Logic High Voltage, All Inputs	$V_{IH}$	2.4	—	$V_{CC} + 0.5$	V
Logic Low Voltage, All Inputs	$V_{IL}$	- 0.3*	—	0.8	V
SPD Pins	$V_{IL}$	- 0.3	—	$V_{CC} + 0.3$	V
SPD Pins	$V_{IH}$	$V_{CC} \times 0.7$	—	$V_{CC} + 0.5$	V
SPD ( $I_{VOL} = 2.1\text{ mA}$ )	$V_{OL}$	—	—	0.4	V
Input Leakage Current ( $V_{SS} \leq V_{in} \leq V_{CC}$ )	$I_{lkg(I)}$	- 180	—	180	$\mu\text{A}$
Output Leakage Current ( $\overline{\text{CAS}}$ at Logic 1, $V_{SS} \leq V_{out} \leq V_{CC}$ )	$I_{lkg(O)}$	- 20	—	20	$\mu\text{A}$
Output High Voltage ( $I_{OH} = - 2\text{ mA}$ )	$V_{OH}$	2.4	—	—	V
Output Low Voltage ( $I_{OL} = 2\text{ mA}$ )	$V_{OL}$	—	—	0.4	V

\* - 2.0 V at pulse widths  $\leq 20\text{ ns}$ .

**DC CHARACTERISTICS AND SUPPLY CURRENTS** (All Voltages Referenced to  $V_{SS}$ )

Characteristic	Symbol	8MB		16MB		32MB		Unit	Notes
		Min	Max	Min	Max	Min	Max		
$V_{CC}$ Power Supply Current ( $t_{RC} = t_{RC} \text{ Min}$ )	60 70 $I_{CC1}$	— —	890 750	— —	902 762	— —	1980 1710	mA	1, 2
$V_{CC}$ Power Supply Current (Standby) ( $\overline{RAS} = \overline{CAS} = V_{IH}$ )	$I_{CC2}$	—	12	—	24	—	36	mA	
$V_{CC}$ Power Supply Current ( $t_{RC} = t_{RC} \text{ Min}$ )	60 70 $I_{CC3}$	— —	890 750	— —	902 762	— —	1980 1710	mA	1, 2
$V_{CC}$ Power Supply Current ( $t_{EPC} = t_{EPC} \text{ Min}$ ) During EDO Cycle	60 70 $I_{CC4}$	— —	630 570	— —	642 582	— —	1260 1080	mA	1, 2
$V_{CC}$ Power Supply Current (Standby) ( $\overline{RAS} = \overline{CAS} = V_{CC} - 0.2 \text{ V}$ )	$I_{CC5}$	—	6	—	12	—	18	mA	
$V_{CC}$ Power Supply Current ( $t_{RC} = t_{RC} \text{ Min}$ ) During $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle	60 70 $I_{CC6}$	— —	890 750	— —	902 762	— —	1980 1710	mA	1

## NOTES:

- Current is a function of cycle rate and output loading; maximum current is measured at the fastest cycle rate with the output open.
- Column address can be changed once or less while  $\overline{RAS} = V_{IL}$  and  $\overline{CAS} = V_{IH}$ .

**CAPACITANCE** ( $f = 1.0 \text{ MHz}$ ,  $T_A = 25^\circ\text{C}$ ,  $V_{CC} = 5 \text{ V}$ , Periodically Sampled Rather Than 100% Tested)

Input Capacitance	Symbol	8MB Max	16MB Max	32MB Max	Unit
A0 – A10	$C_{in}$	40	70	100	pF
$\overline{WE}$ , $\overline{G}$	$C_{in}$	31	52	73	pF
$\overline{RAS}$	$C_{in}$	31	31	73	pF
$\overline{CAS}$	$C_{in}$	24	38	31	pF
SPD	$C_{in}$	18	18	18	pF
DQ0 – DQ63	$C_{out}$	17	24	17	pF

NOTE: Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation:  $C = I \Delta t / \Delta V$ .

## AC OPERATING CONDITIONS AND CHARACTERISTICS

 $(V_{CC} = 5 V \pm 10\%, T_A = 0 \text{ to } 70^\circ\text{C}, \text{ Unless Otherwise Noted})$ 

## ALL DEVICES: READ, WRITE, AND READ-WRITE CYCLES (See Notes 1, 2, 3, and 4)

Parameter	Symbol		60		70		Unit	Notes
	Std	Alt	Min	Max	Min	Max		
Random Read or Write Cycle Time	$t_{RELREL}$	$t_{RC}$	104	—	124	—	ns	5
Read-Write Cycle Time	$t_{RELREL}$	$t_{RWC}$	140	—	165	—	ns	5
Access Time from $\overline{RAS}$	$t_{RELQV}$	$t_{RAC}$	—	60	—	70	ns	6, 7, 8, 9
Access Time from $\overline{CAS}$	$t_{CELQV}$	$t_{CAC}$	—	17	—	20	ns	6, 8, 10
Access Time from Column Address	$t_{AVQV}$	$t_{AA}$	—	30	—	35	ns	6, 9, 11
Access Time from Precharge $\overline{CAS}$	$t_{CEHQV}$	$t_{CPA}$	—	35	—	40	ns	6
$\overline{CAS}$ to Output in Low-Z	$t_{CELQX}$	$t_{CLZ}$	0	—	0	—	ns	
Output Buffer and Turn-Off Delay	$t_{CEHQZ}$	$t_{OFF}$	0	15	0	20	ns	12, 13
Transition Time (Rise and Fall)	$t_T$	$t_T$	2	50	2	50	ns	
$\overline{RAS}$ Precharge Time	$t_{REHREL}$	$t_{RP}$	40	—	50	—	ns	
$\overline{RAS}$ Pulse Width	$t_{RELREH}$	$t_{RAS}$	60	10 k	70	10 k	ns	
$\overline{RAS}$ Hold Time	$t_{CELREH}$	$t_{RSH}$	15	—	20	—	ns	
$\overline{CAS}$ Hold Time	$t_{RELCEH}$	$t_{CSH}$	50	—	60	—	ns	
$\overline{CAS}$ Pulse Width	$t_{CELCEH}$	$t_{CAS}$	10	10 k	15	10 k	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	$t_{RELCEL}$	$t_{RCD}$	20	43	20	50	ns	8
$\overline{RAS}$ to Column Address Delay Time	$t_{RELAV}$	$t_{RAD}$	15	30	15	35	ns	9
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	$t_{CEHREL}$	$t_{CRP}$	5	—	5	—	ns	
$\overline{CAS}$ Precharge Time	$t_{CEHCEL}$	$t_{CP}$	10	—	12	—	ns	
Row Address Setup Time	$t_{AVREL}$	$t_{ASR}$	0	—	0	—	ns	
Row Address Hold Time	$t_{RELAX}$	$t_{RAH}$	10	—	10	—	ns	
Column Address Setup Time	$t_{AVCEL}$	$t_{ASC}$	0	—	0	—	ns	
Column Address Hold Time	$t_{CELAX}$	$t_{CAH}$	10	—	15	—	ns	
Column Address to $\overline{RAS}$ Lead Time	$t_{AVREH}$	$t_{RAL}$	30	—	35	—	ns	
Read Command Setup Time	$t_{WHCEL}$	$t_{RCS}$	0	—	0	—	ns	

## NOTES:

(continued)

- $V_{IH}$  (min) and  $V_{IL}$  (max) are reference levels for measuring timing of input signals. Transition times are measured between  $V_{IH}$  and  $V_{IL}$ .
- An initial pause of 200  $\mu\text{s}$  is required after power-up followed by 8  $\overline{RAS}$  cycles before proper device operation is guaranteed. If using the internal refresh counter, a minimum of 8  $\overline{CAS}$  before  $\overline{RAS}$  refresh cycles, instead of 8  $\overline{RAS}$  only refresh cycles are required.
- The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transition between  $V_{IH}$  and  $V_{IL}$  (or between  $V_{IL}$  and  $V_{IH}$ ) in a monotonic manner.
- AC measurements  $t_T = 5.0$  ns.
- The specification for  $t_{RC}$  (min),  $t_{RWC}$  (min), and  $t_{EPC}$  (min) is used only to indicate cycle time at which proper operation over the full temperature range ( $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$ ) is ensured.
- Measured with a current load equivalent to 2 TTL ( $-200 \mu\text{A}$ ,  $+4 \text{ mA}$ ) loads and 100 pF with the data output trip points set at  $V_{OH} = 2.0 \text{ V}$  and  $V_{OL} = 0.8 \text{ V}$ .
- Assumes that  $t_{RCD} \leq t_{RCD}$  (max).
- Operation within the  $t_{RCD}$  (max) limit ensures that  $t_{RAC}$  (max) can be met.  $t_{RCD}$  (max) is specified as a reference point only; if  $t_{RCD}$  is greater than the specified  $t_{RCD}$  (max) limit, then access time is controlled exclusively by  $t_{CAC}$ .
- Operation within the  $t_{RAD}$  (max) limit ensures that  $t_{RAC}$  (max) can be met.  $t_{RAD}$  (max) is specified as a reference point only; if  $t_{RAD}$  is greater than the specified  $t_{RAD}$  (max), then access time is controlled exclusively by  $t_{AA}$ .
- Assumes that  $t_{RCD} \geq t_{RCD}$  (max).
- Assumes that  $t_{RAD} \geq t_{RAD}$  (max).
- $t_{OFF}$  (max),  $t_{REZ}$  (max),  $t_{WEZ}$  (max), and  $t_{GZ}$  (max) define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
- If  $\overline{RAS}$  goes high before  $\overline{CAS}$  goes high, the open circuit condition is controlled by  $\overline{CAS}$  going high ( $t_{OFF}$ ). If  $\overline{CAS}$  goes high before  $\overline{RAS}$  goes high, the open circuit condition is controlled by  $\overline{RAS}$  going high ( $t_{REZ}$ ).

## ALL DEVICES: READ, WRITE, AND READ-WRITE CYCLES (continued)

Parameter	Symbol		60		70		Unit	Notes
	Std	Alt	Min	Max	Min	Max		
Read Command Hold Time Referenced to $\overline{\text{CAS}}$	$t_{\text{CEHWX}}$	$t_{\text{RCH}}$	0	—	0	—	ns	14
Read Command Hold Time Referenced to $\overline{\text{RAS}}$	$t_{\text{REHWX}}$	$t_{\text{RRH}}$	0	—	0	—	ns	14
Write Command Hold Time Referenced to $\overline{\text{CAS}}$	$t_{\text{CELWH}}$	$t_{\text{WCH}}$	10	—	15	—	ns	
Write Command Pulse Width	$t_{\text{WLWH}}$	$t_{\text{WP}}$	10	—	15	—	ns	
Write Command to $\overline{\text{RAS}}$ Lead Time	$t_{\text{WLREH}}$	$t_{\text{RWL}}$	15	—	20	—	ns	
Write Command to $\overline{\text{CAS}}$ Lead Time	$t_{\text{WLCEH}}$	$t_{\text{CWL}}$	10	—	15	—	ns	
Data In Setup Time	$t_{\text{DVCEL}}$	$t_{\text{DS}}$	0	—	0	—	ns	15
Data In Hold Time	$t_{\text{CELDX}}$	$t_{\text{DH}}$	10	—	15	—	ns	15
Refresh Period	8MB, 16MB 32MB	$t_{\text{RVRV}}$ $t_{\text{RFSH}}$	—	16 32	—	16 32	ms	
Write Command Setup Time	$t_{\text{WLCEL}}$	$t_{\text{WCS}}$	0	—	0	—	ns	16
$\overline{\text{CAS}}$ to Write Delay	$t_{\text{CELWL}}$	$t_{\text{CWD}}$	36	—	44	—	ns	16
$\overline{\text{RAS}}$ to Write Delay	$t_{\text{RELWL}}$	$t_{\text{RWD}}$	79	—	89	—	ns	16
Column Address to Write Delay	$t_{\text{AVWL}}$	$t_{\text{AWD}}$	49	—	59	—	ns	16
$\overline{\text{CAS}}$ Precharge to Write Delay	$t_{\text{CEHWL}}$	$t_{\text{CPWD}}$	54	—	64	—	ns	16
$\overline{\text{CAS}}$ Setup Time for $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh	$t_{\text{CELCEL}}$	$t_{\text{CSR}}$	5	—	5	—	ns	
$\overline{\text{CAS}}$ Hold Time for $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh	$t_{\text{RELCEH}}$	$t_{\text{CHR}}$	10	—	15	—	ns	
$\overline{\text{RAS}}$ Precharge to $\overline{\text{CAS}}$ Active Time	$t_{\text{REHCEL}}$	$t_{\text{RPC}}$	5	—	5	—	ns	
$\overline{\text{CAS}}$ Precharge Time for $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Counter Test	$t_{\text{CEHCEL}}$	$t_{\text{CPT}}$	20	—	25	—	ns	
$\overline{\text{G}}$ Access Time	$t_{\text{GLQV}}$	$t_{\text{GA}}$	—	15	—	20	ns	6
$\overline{\text{G}}$ to Data Delay	$t_{\text{GLHDX}}$	$t_{\text{GD}}$	15	—	20	—	ns	
Output Buffer Turn-Off Delay from $\overline{\text{G}}$	$t_{\text{GHQZ}}$	$t_{\text{GZ}}$	0	15	0	20	ns	12
$\overline{\text{G}}$ Command Hold Time	$t_{\text{WLGL}}$	$t_{\text{GH}}$	15	—	20	—	ns	
$\overline{\text{RAS}}$ Hold Time from $\overline{\text{CAS}}$ Precharge (EDO)	$t_{\text{CEHREH}}$	$t_{\text{RHCP}}$	35	—	40	—	ns	
$\overline{\text{RAS}}$ Pulse Width (EDO)	$t_{\text{RELREH}}$	$t_{\text{RASP}}$	60	100 k	70	100 k	ns	
$\overline{\text{RAS}}$ to Next $\overline{\text{CAS}}$ Delay (EDO)	$t_{\text{RELCEL}}$	$t_{\text{RNCD}}$	60	—	70	—	ns	
EDO Cycle Time	$t_{\text{CELCEL}}$	$t_{\text{EPC}}$	25	—	30	—	ns	
EDO Read-Write Cycle Time	$t_{\text{CELCEL}}$	$t_{\text{ERWC}}$	68	—	75	—	ns	
Output Data Hold Time	$t_{\text{CELQZ}}$	$t_{\text{COH}}$	5	—	5	—	ns	
Output Buffer Turn-Off Delay from $\overline{\text{RAS}}$	$t_{\text{REHQZ}}$	$t_{\text{REZ}}$	0	15	0	20	ns	12, 13
Output Buffer Turn-Off Delay from $\overline{\text{WE}}$	$t_{\text{WLQZ}}$	$t_{\text{WEZ}}$	0	15	0	20	ns	12
$\overline{\text{WE}}$ to Data Delay	$t_{\text{WLDV}}$	$t_{\text{WED}}$	15	—	20	—	ns	
$\overline{\text{G}}$ Precharge Time	$t_{\text{GHGL}}$	$t_{\text{GP}}$	10	—	12	—	ns	

## NOTES:

14. Either  $t_{\text{RRH}}$  or  $t_{\text{RCH}}$  must be satisfied for a read cycle.
15. These parameters are referenced to  $\overline{\text{UCAS}}$  or  $\overline{\text{LCAS}}$  leading edge in early write cycles and to  $\overline{\text{W}}$  leading edge in late write or read-write cycles.
16.  $t_{\text{WCS}}$ ,  $t_{\text{RWD}}$ ,  $t_{\text{CWD}}$ ,  $t_{\text{AWD}}$ , and  $t_{\text{CPWD}}$  are not restrictive operating parameters. They are included in the datasheet as electrical characteristics only; if  $t_{\text{WCS}} \geq t_{\text{WCS}}(\text{min})$ , the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if  $t_{\text{CWD}} \geq t_{\text{CWD}}(\text{min})$ ,  $t_{\text{RWD}} \geq t_{\text{RWD}}(\text{min})$ , and  $t_{\text{AWD}} \geq t_{\text{AWD}}(\text{min})$ ,  $t_{\text{CPWD}} \geq t_{\text{CPWD}}(\text{min})$ , (extended data out), the cycle is a read-write cycle and the data out will contain data read from the selected cell. If neither of these sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

**SERIAL PRESENCE DETECT DATA**

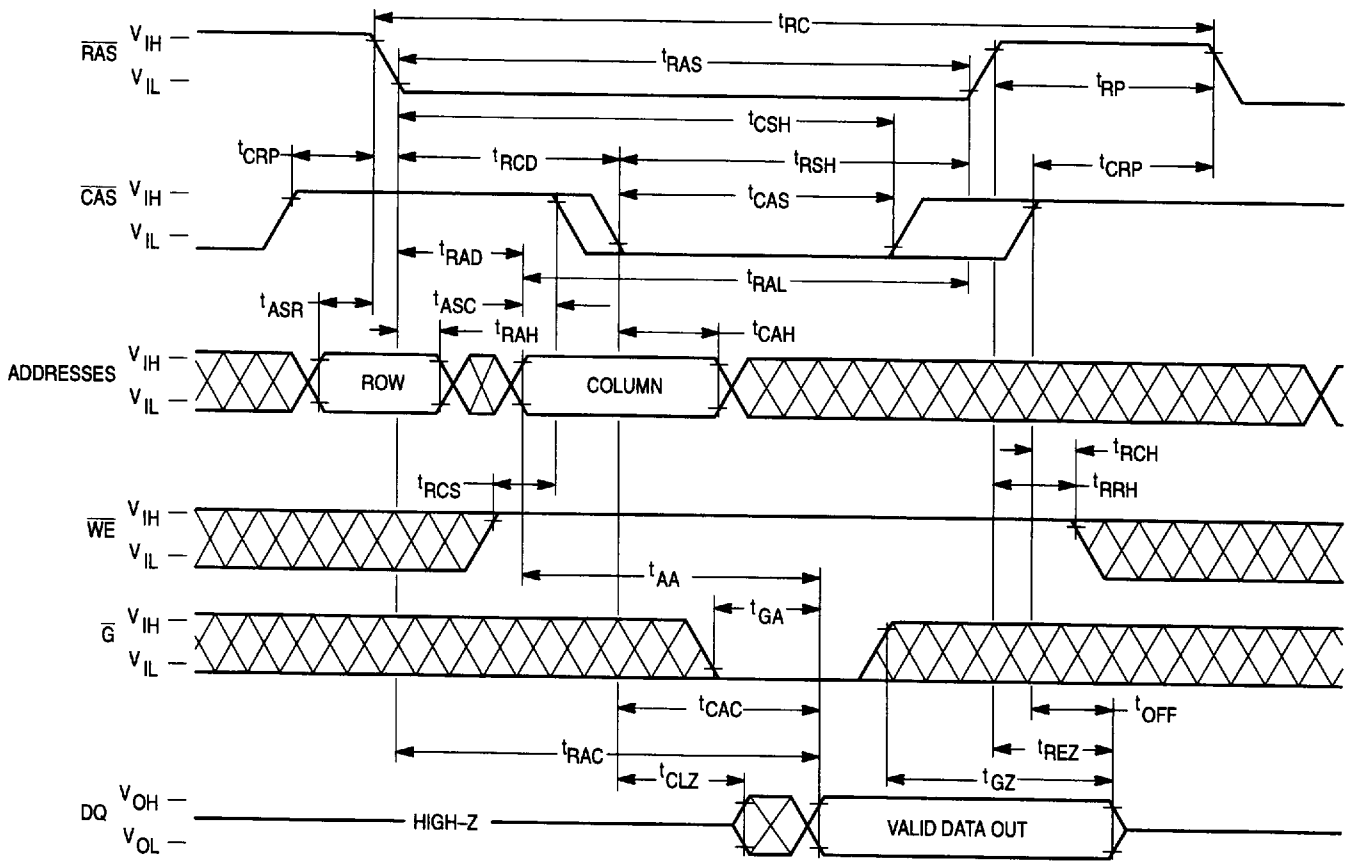
Field Description	Byte Number	Byte Value (Hex)	Byte Value Meaning	
<b>8MB</b>				
Number of Banks	5	01	1 bank	
Fundamental Memory Type	2	02	EDO	
Number of Rows	3	0A	10 rows	
Number of Columns	4	0A	10 columns	
Number of Banks	5	01	1 bank	
Module Data Width	6	48	72 bits wide	
Module Data Width (Continued)	7	00	None	
Supply Voltage	8	00	5 V (TTL)	
RAS Access Time	60/70	9	3C/46	60 ns/70 ns
CAS Access Time	60/70	10	11/14	17 ns/20 ns
Error Detection	11	02	ECC	
Refresh Rates	12	00	15.625 $\mu$ s	
Primary DRAM Organization	13	10	x16 DRAMs	

<b>16MB</b>				
SPD Size	0	80	128 bytes	
Total SPD Memory Size	1	08	256 bytes	
Fundamental Memory Type	2	02	EDO	
Number of Rows	3	0A	10 rows	
Number of Columns	4	0A	10 columns	
Number of Banks	5	02	2 banks	
Module Data Width	6	48	72 bits wide	
Module Data Width (Continued)	7	00	None	
Supply Voltage	8	00	5 V (TTL)	
RAS Access Time	60/70	9	3C/46	60 ns/70 ns
CAS Access Time	60/70	10	11/14	17 ns/20 ns
Error Detection	11	02	ECC	
Refresh Rates	12	00	15.625 $\mu$ s	
Primary DRAM Organization	13	10	x16 DRAMs	

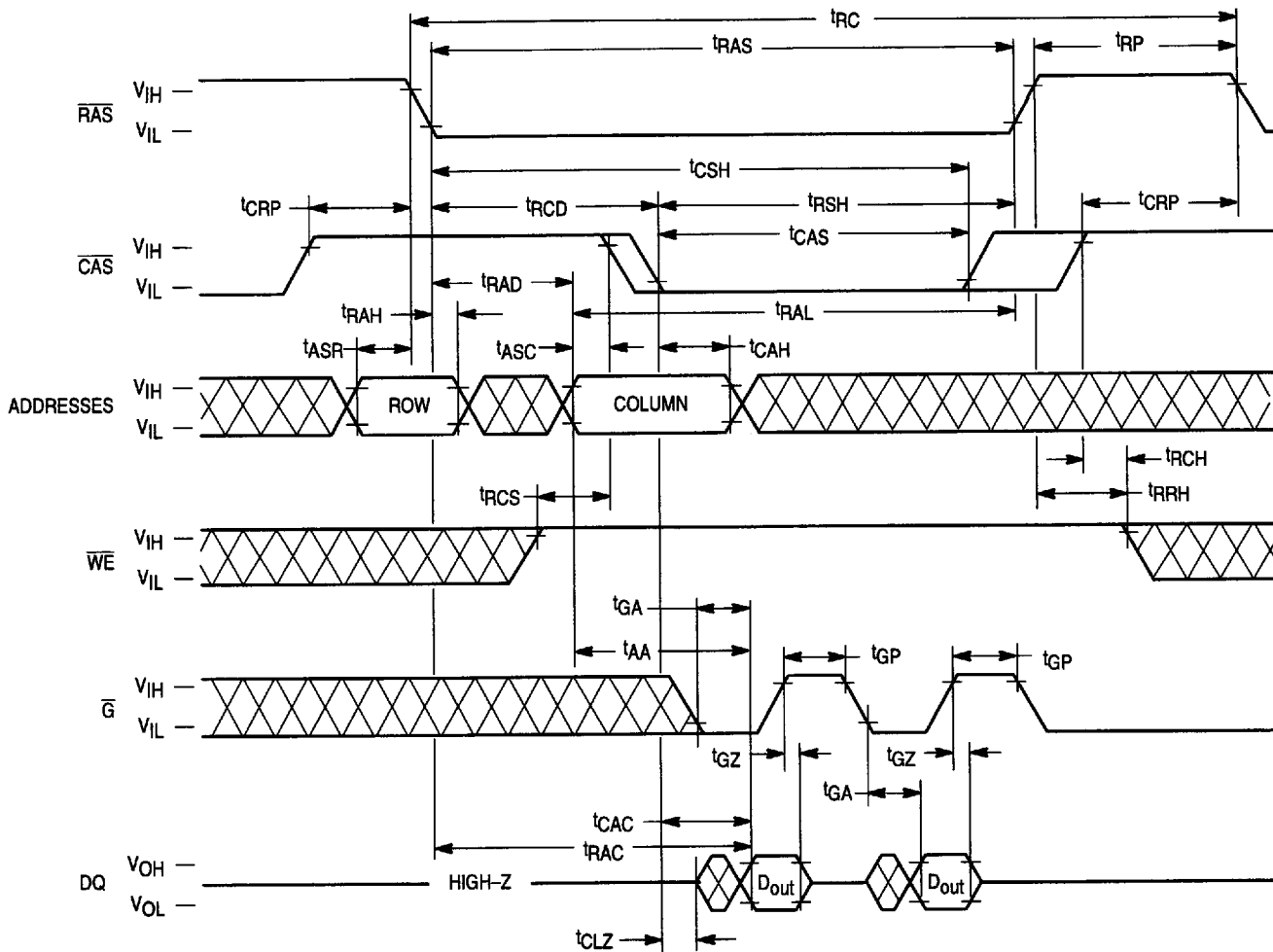
<b>32MB</b>				
SPD Size	0	80	128 bytes	
Total SPD Memory Size	1	08	256 bytes	
Fundamental Memory Type	2	02	EDO	
Number of Rows	3	0B	11 rows	
Number of Columns	4	0B	11 columns	
Number of Banks	5	01	1 bank	
Module Data Width	6	48	72 bits wide	
Module Data Width (Continued)	7	00	None	
Supply Voltage	8	00	5 V (TTL)	
RAS Access Time	60/70	9	3C/46	60 ns/70 ns
CAS Access Time	60/70	10	11/14	17 ns/20 ns
Error Detection	11	02	ECC	
Refresh Rates	12	00	15.625 $\mu$ s	
Primary DRAM Organization	13	04	x4 DRAMs	

**TIMING DIAGRAMS**

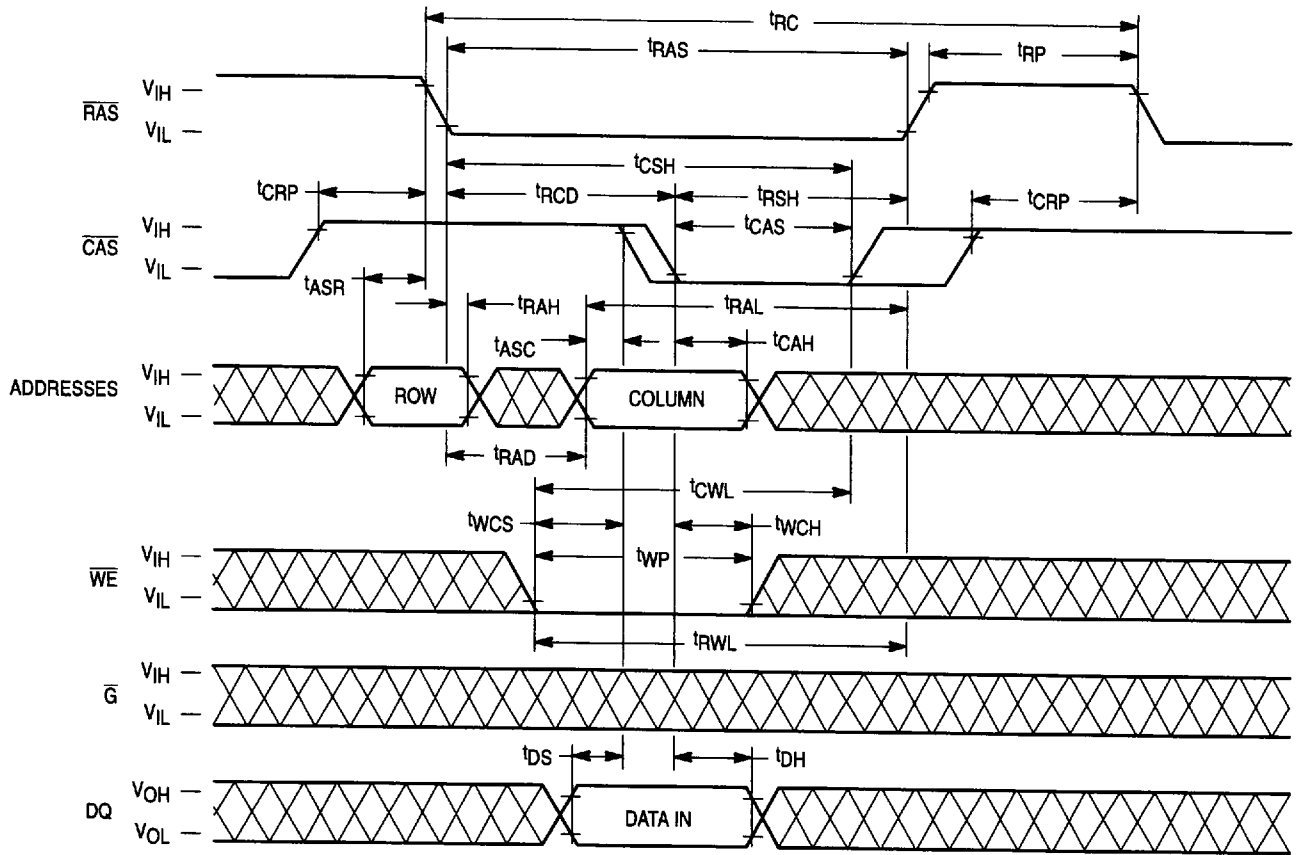
**READ CYCLE**



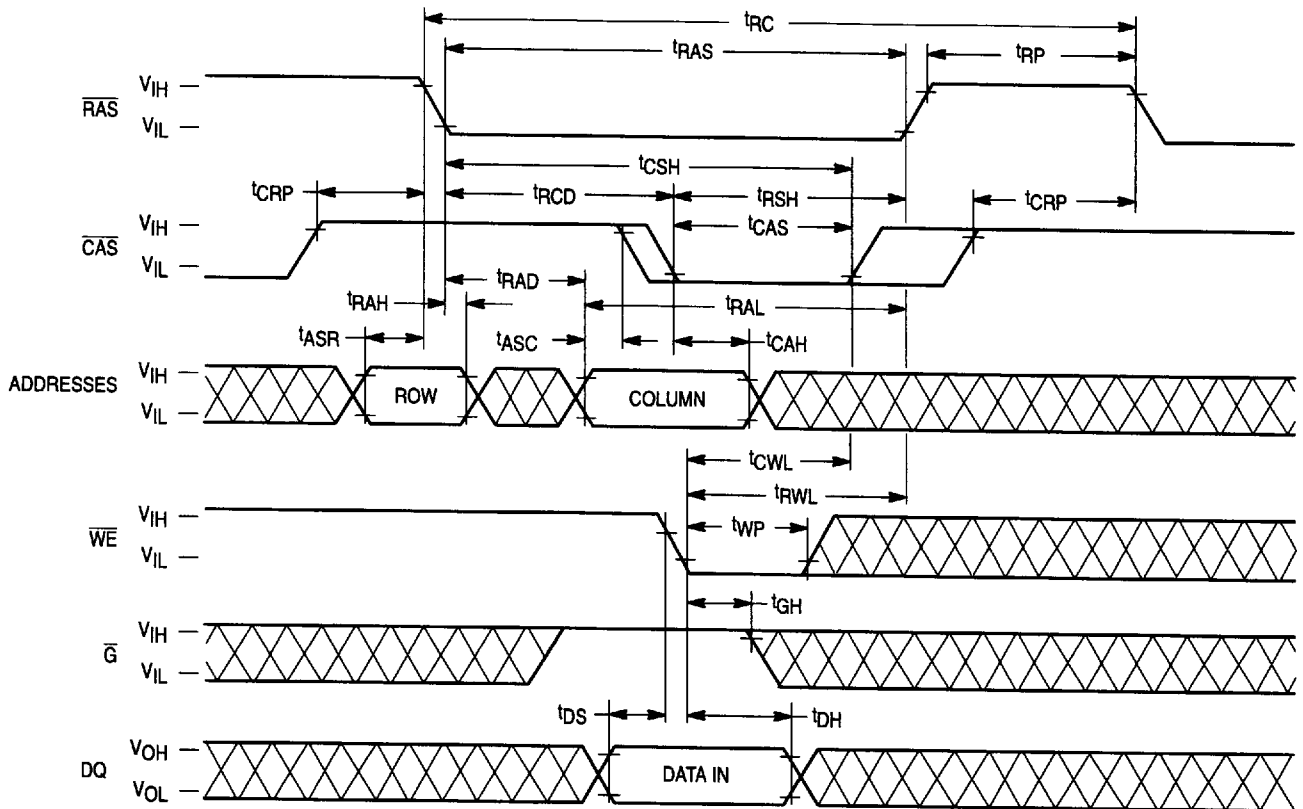
READ CYCLE ( $\bar{G}$  CONTROLLED READ)



**WRITE CYCLE (EARLY WRITE)**

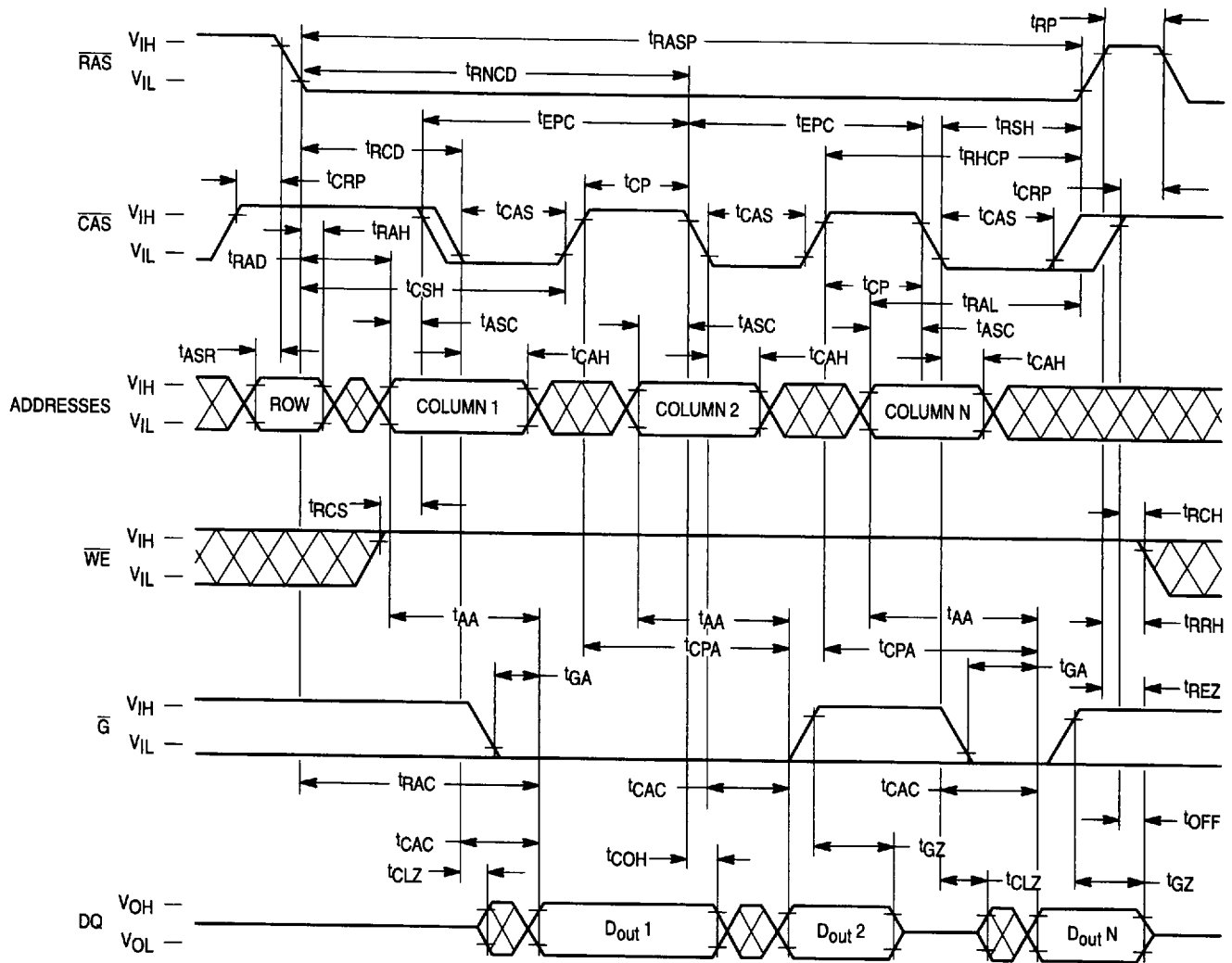


**WRITE CYCLE ( $\overline{G}$  CONTROLLED WRITE)**

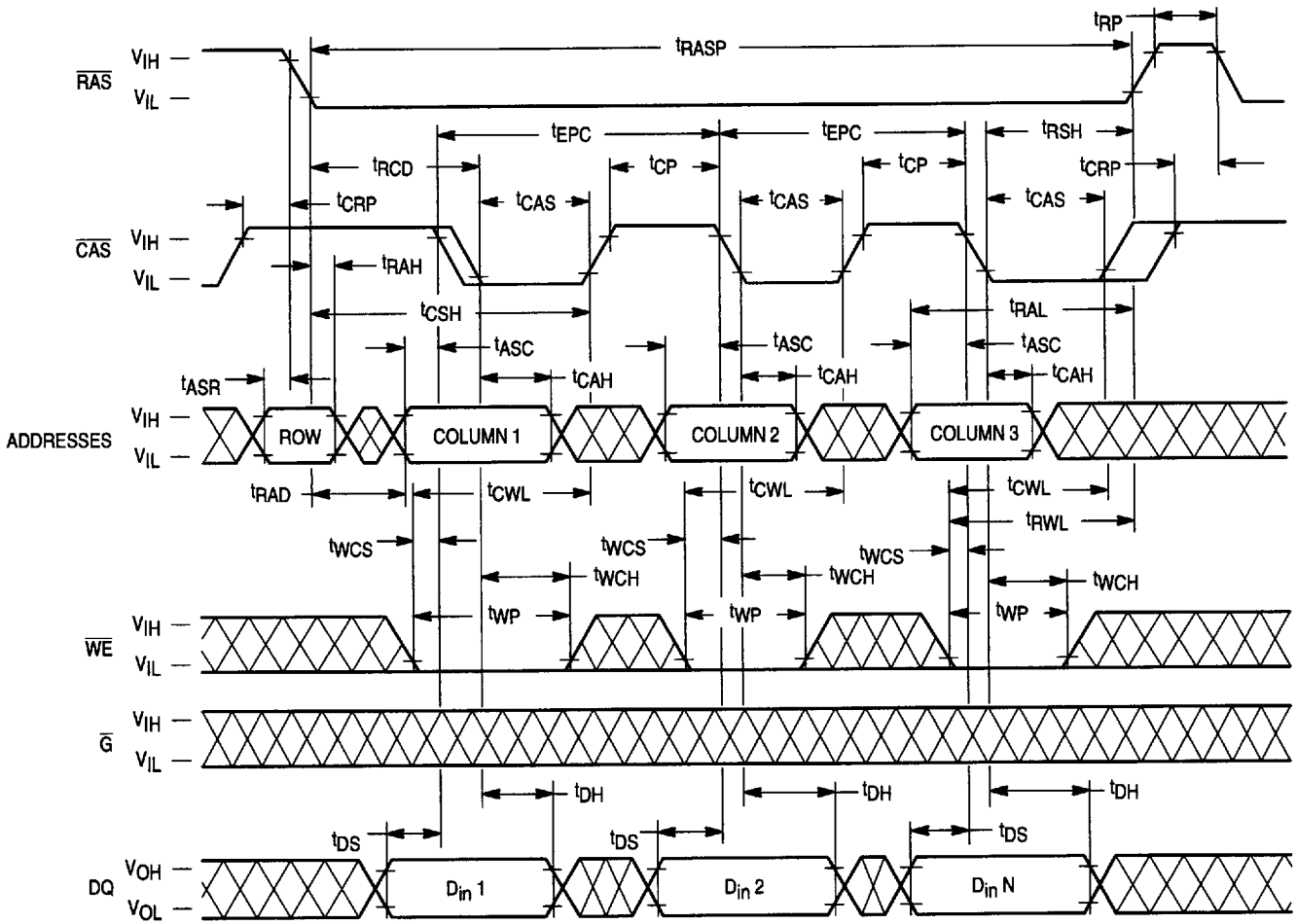




EXTENDED DATA OUT READ CYCLE



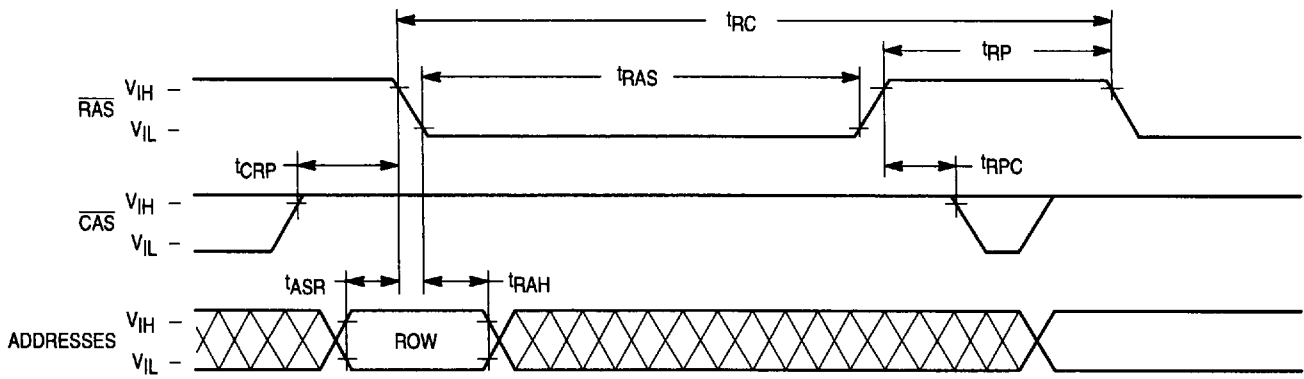
EXTENDED DATA OUT WRITE CYCLE (EARLY WRITE)





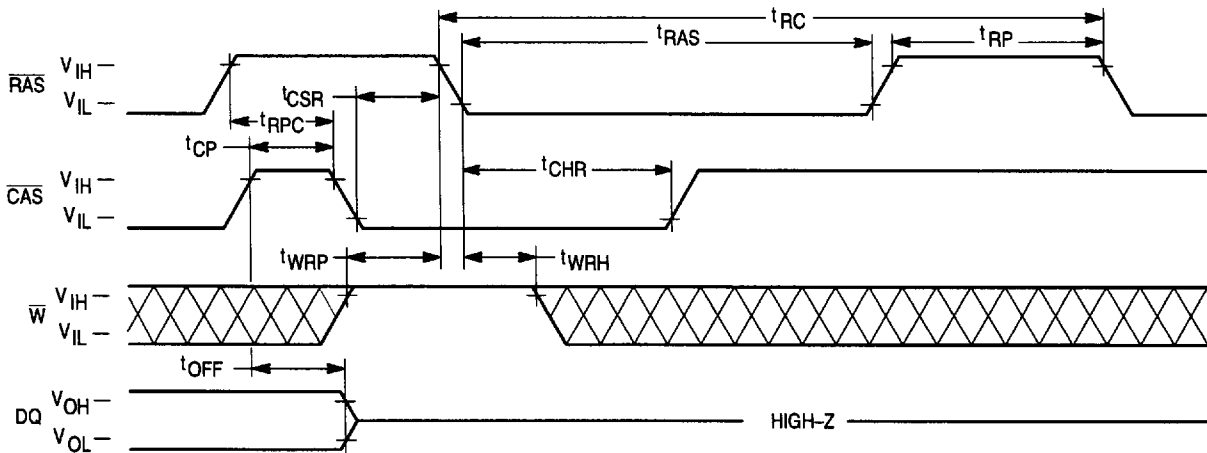


**RAS-ONLY REFRESH CYCLE**



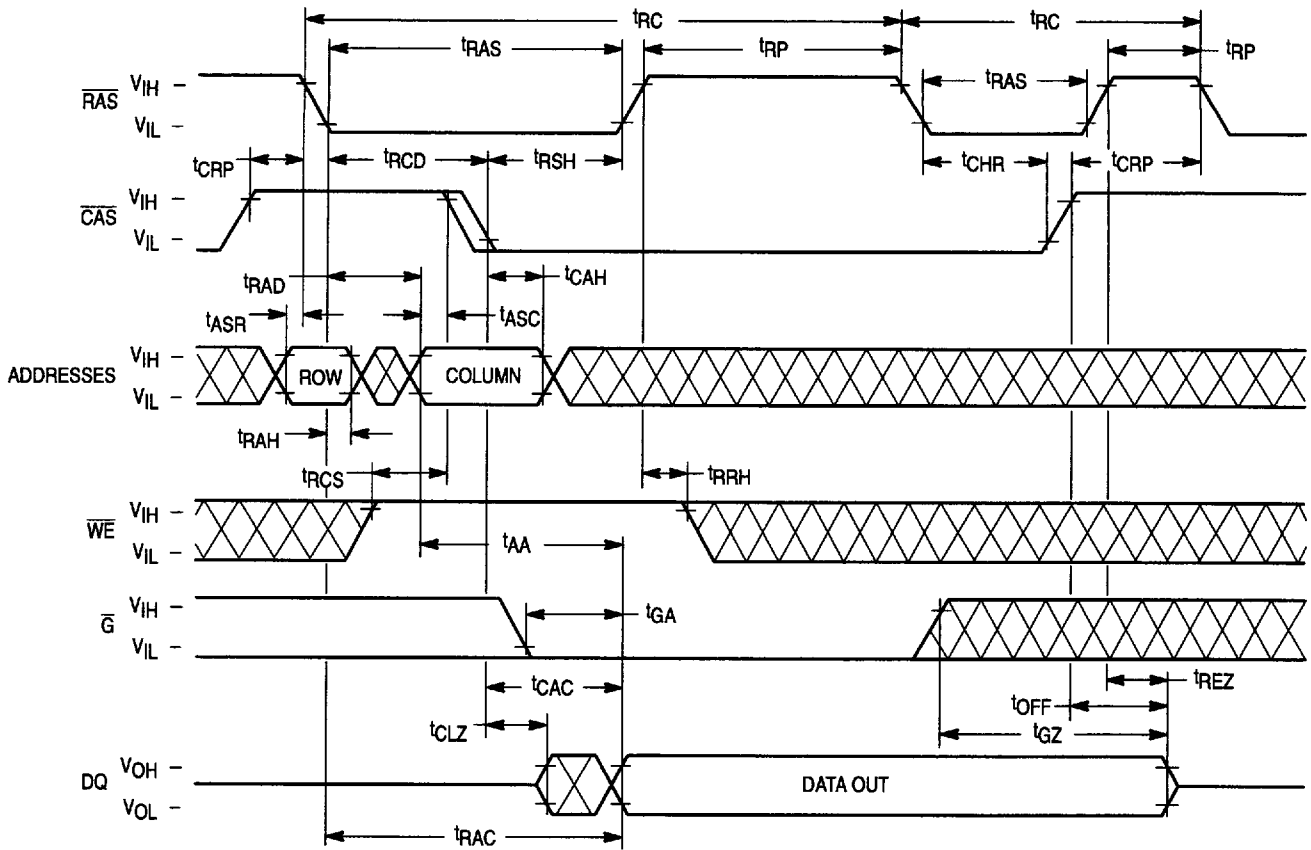
NOTE:  $\overline{WE}$ ,  $\overline{G}$  = H or L.  
DQ = Open.

**CAS BEFORE RAS REFRESH CYCLE**

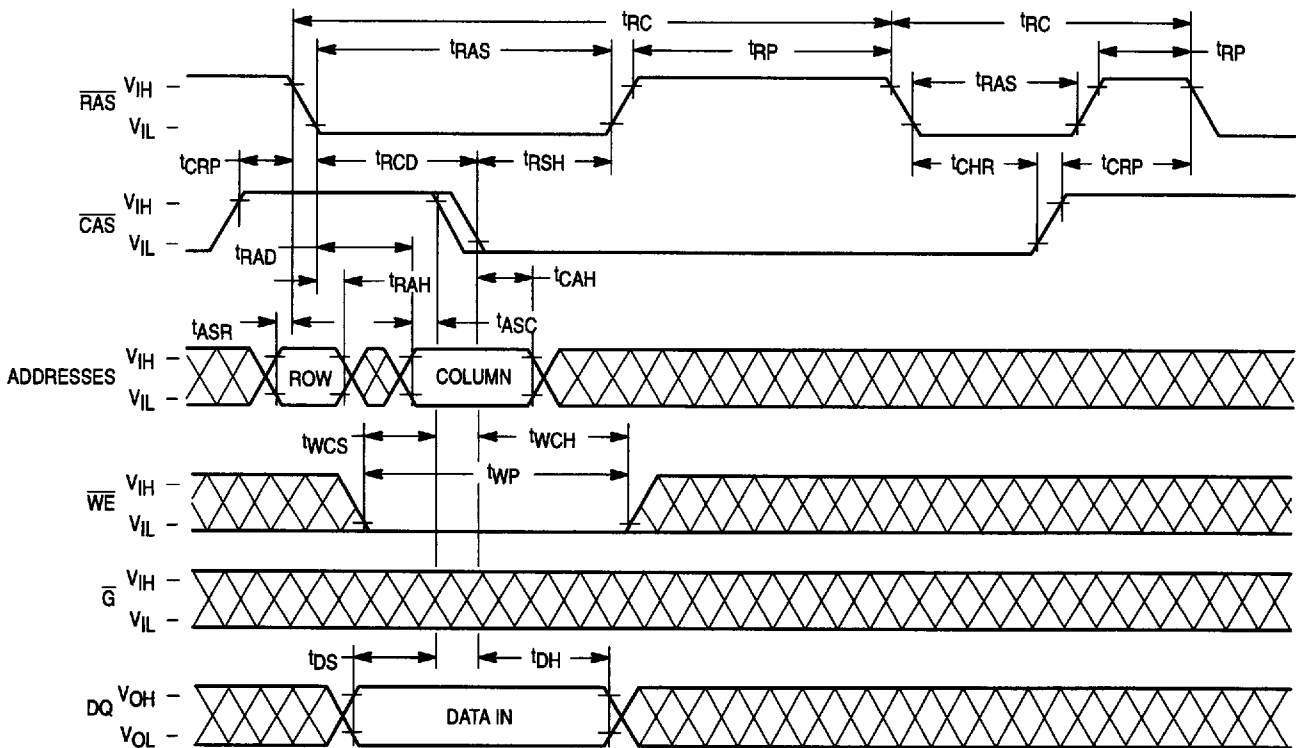


NOTE: Addresses = H or L.  
8MB, 16MB:  $\overline{W}$  = H or L.  
32MB:  $\overline{W}$  must be as shown to avoid switching into component test mode.

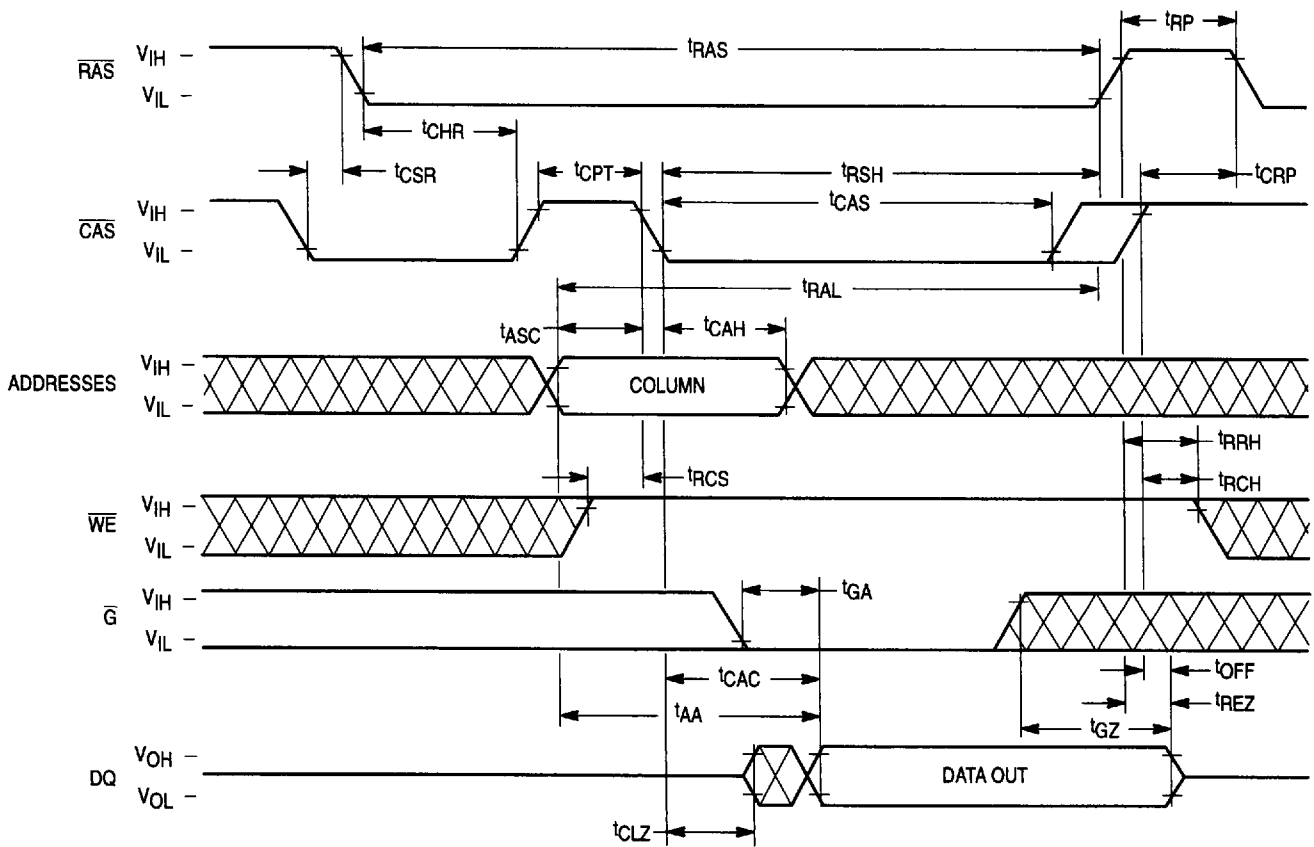
**HIDDEN REFRESH CYCLE (READ)**



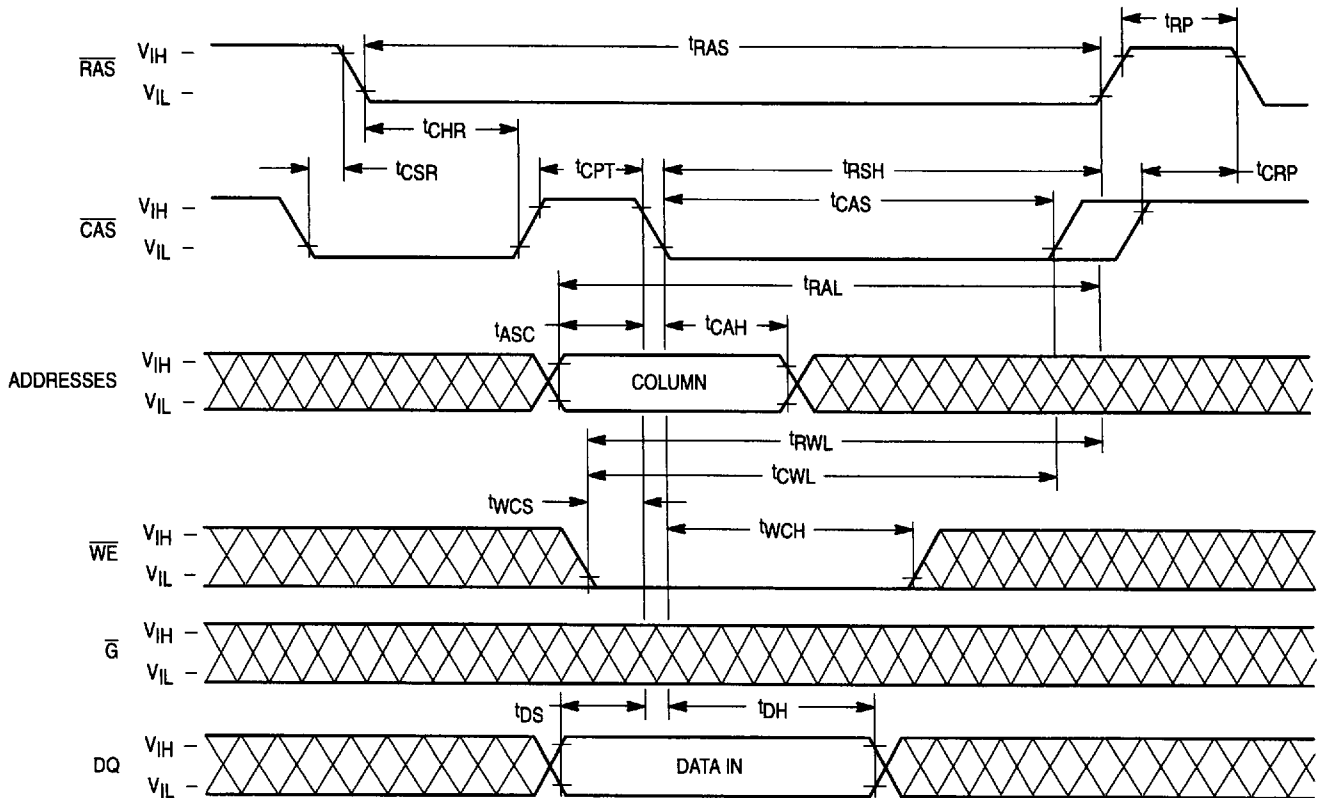
**HIDDEN REFRESH CYCLE (WRITE)**



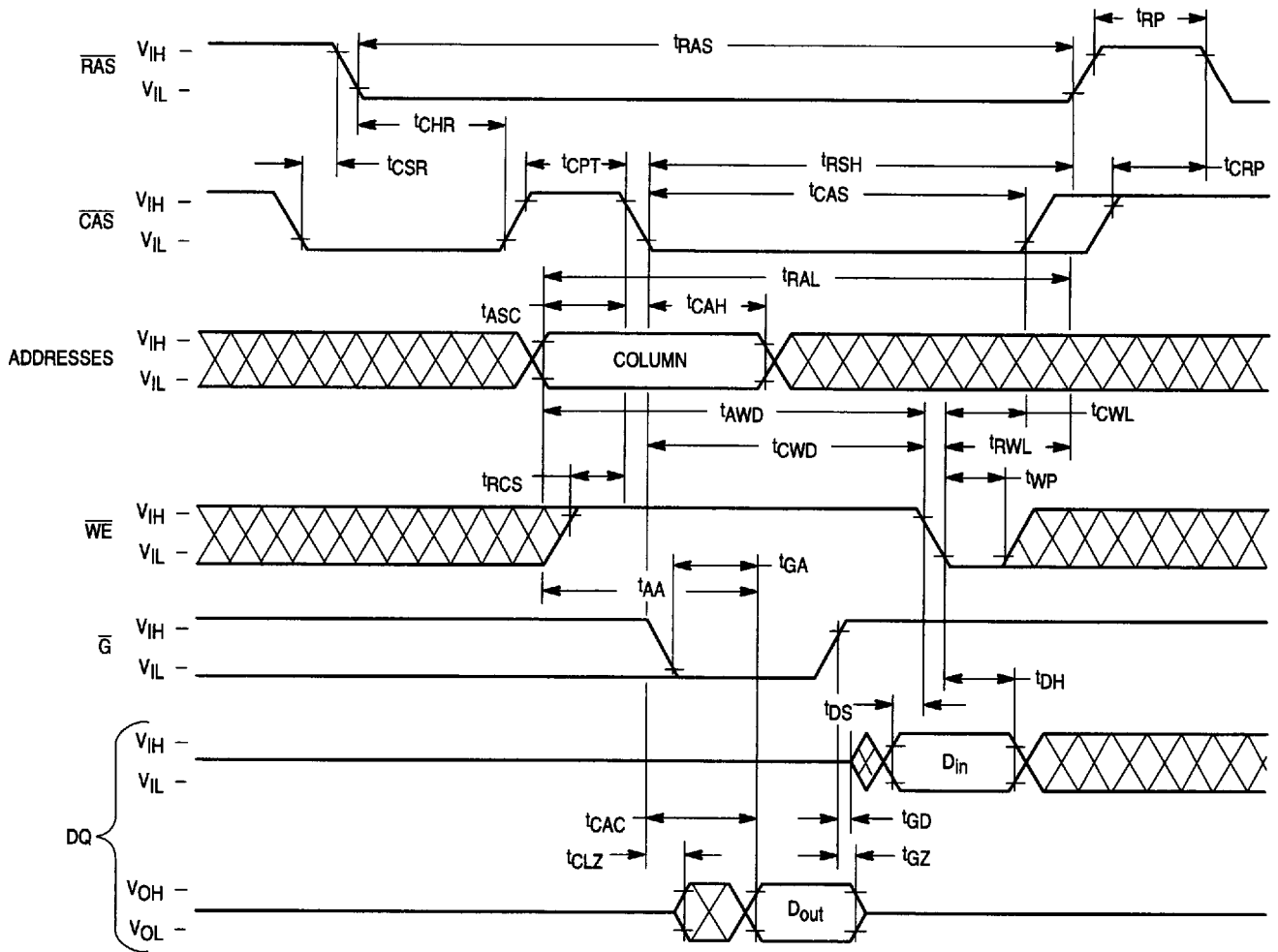
**CAS BEFORE RAS REFRESH COUNTER TEST READ CYCLE**



**CAS BEFORE RAS REFRESH COUNTER TEST WRITE CYCLE**



**CAS BEFORE RAS REFRESH COUNTER TEST READ-WRITE CYCLE**



## DEVICE INITIALIZATION

On power-up, an initial pause of 200  $\mu$ s is required for the internal substrate generator to establish the correct bias voltage. This must be followed by a minimum of eight active cycles of the row address strobe (clock) to initialize all dynamic nodes within the module. During an extended inactive state (greater than 16 ms for the 8MB and 16MB, 32 ms for the 32MB with the device powered up), a wake up sequence of eight active cycles is necessary to ensure proper operation.

## ADDRESSING THE RAM

The address pins on the device are time multiplexed at the beginning of a memory cycle by two clocks, row address strobe ( $\overline{\text{RAS}}$ ) and column address strobe ( $\overline{\text{CAS}}$ ), into two separate address fields. For the 8MB and 16MB modules a total of 20 address bits, 10 rows and 10 columns, will decode one of the word locations in the device. For the 32MB module 22 address bits, 11 rows and 11 columns, decode one of the word locations in the device.  $\overline{\text{RAS}}$  active transition is followed by  $\overline{\text{CAS}}$  active transition (active =  $V_{IL}$ ,  $t_{RCD}$  minimum) for all read or write cycles. The delay between  $\overline{\text{RAS}}$  and  $\overline{\text{CAS}}$  active transitions, referred to as the **multiplex window**, gives a system designer flexibility in setting up the external addresses into the RAM.

The external  $\overline{\text{CAS}}$  signal is ignored until an internal  $\overline{\text{RAS}}$  signal is available. This "gate" feature on the external  $\overline{\text{CAS}}$  clock enables the internal  $\overline{\text{CAS}}$  line as soon as the row address hold time ( $t_{RAH}$ ) specification is met (and defines  $t_{RCD}$  minimum). The multiplex window can be used to absorb skew delays in switching the address bus from row to column addresses and in generating the  $\overline{\text{CAS}}$  clock.

There are three other variations in addressing the module:  **$\overline{\text{RAS}}$ -only refresh cycle**,  **$\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  refresh cycle**, and **page mode**. All three are discussed in separate sections that follow.

## READ CYCLE

The DRAM may be read with four different cycles: "normal" random read cycle, extended data out read cycle, read-write cycle, and extended data out read-write cycle. The normal read cycle is outlined here, while the other cycles are discussed in separate sections.

The normal read cycle begins as described in **ADDRESSING THE RAM**, with  $\overline{\text{RAS}}$  and  $\overline{\text{CAS}}$  active transitions latching the desired bit location. The write ( $\overline{W}$ ) input level must be high ( $V_{IH}$ ),  $t_{RCS}$  (minimum) before the  $\overline{\text{CAS}}$  or active transition, to enable read mode.

Both the  $\overline{\text{RAS}}$  and  $\overline{\text{CAS}}$  clocks trigger a sequence of events that are controlled by several delayed internal clocks. The internal clocks are linked in such a manner that the read access time of the device is independent of the address multiplex window.

Both  $\overline{\text{CAS}}$  and output enable ( $\overline{G}$ ) control read access time:  $\overline{\text{CAS}}$  must be active before or at  $t_{RCD}$  maximum and  $\overline{G}$  must be active  $t_{RAC}-t_{GA}$  (both minimum) after  $\overline{\text{RAS}}$  active transition to guarantee valid data out (Q) at  $t_{RAC}$ . If the  $t_{RCD}$  maximum is exceeded and/or  $\overline{G}$  active transition does not occur in time, read access time is determined by either the  $\overline{\text{CAS}}$  or  $\overline{G}$  clock active transition ( $t_{CAC}$  or  $t_{GA}$ ).

## WRITE CYCLE

The user can write to the DRAM with any of four cycles: early write, late write, extended data out early write, and extended data out read-write. Early and late write modes are

discussed here, while extended data out write operation is covered in a separate section.

A write cycle begins as described in **ADDRESSING THE RAM**. Write mode is enabled by the transition of  $\overline{W}$  to active ( $V_{IL}$ ). Early and late write modes are distinguished by the active transition of  $\overline{W}$ , with respect to  $\overline{\text{CAS}}$ . Minimum active time  $t_{RAS}$  and  $t_{CAS}$ , and precharge time  $t_{RP}$ , apply to write mode, as in the read mode.

An early write cycle is characterized by  $\overline{W}$  active transition at minimum time  $t_{WCS}$  before  $\overline{\text{CAS}}$  active transition. Column address setup and hold times ( $t_{ASC}$ ,  $t_{CAH}$ ) and data in (D) setup and hold times ( $t_{DS}$ ,  $t_{DH}$ ) are referenced to  $\overline{\text{CAS}}$  in an early write cycle.  $\overline{\text{RAS}}$  and  $\overline{\text{CAS}}$  clocks must stay active for  $t_{RWL}$  and  $t_{CWL}$ , respectively, after the start of the early write operation to complete the cycle.

A late-write cycle (referred to as  $\overline{G}$ -controlled write) occurs when  $\overline{W}$  active transition is made after  $\overline{\text{CAS}}$  active transition.  $\overline{W}$  active transition could be delayed for almost 10  $\mu$ s after  $\overline{\text{CAS}}$  active transition, ( $t_{RCD} + t_{CWD} + t_{RWL} + 2t_{\tau}$ )  $\leq t_{RAS}$ , if other timing minimums ( $t_{RCD}$ ,  $t_{RWL}$ , and  $t_{\tau}$ ) are maintained. D timing parameters are referenced to  $\overline{W}$  active transition in a late write cycle. Output buffers are enabled by  $\overline{\text{CAS}}$  active transition. Outputs are switched off by  $\overline{G}$  inactive transition, which is required to write to the device.  $\overline{\text{RAS}}$  and  $\overline{\text{CAS}}$  must remain active for  $t_{RWL}$  and  $t_{CWL}$ , respectively, after  $\overline{W}$  active transition to complete the write cycle.  $\overline{G}$  devices must remain inactive for  $t_{GH}$  after  $\overline{W}$  active transition to complete the write cycle.

## READ-WRITE CYCLE

A read-write cycle performs a read and then a write at the same address, during the same cycle. This cycle is basically a late write cycle, as discussed in the **WRITE CYCLE** section, except  $\overline{W}$  must remain high for  $t_{CWD}$  and/or  $t_{AWD}$  minimum, to guarantee valid Q before writing the bit.

## EDO MODE CYCLES

EDO mode allows fast successive data operations at all column locations on a selected row. Read access time in page mode ( $t_{CAC}$ ) is typically half the regular  $\overline{\text{RAS}}$  clock access time,  $t_{RAC}$ . EDO mode operation consists of keeping  $\overline{\text{RAS}}$  active while toggling  $\overline{\text{CAS}}$  between  $V_{IH}$  and  $V_{IL}$ . The row is latched by  $\overline{\text{RAS}}$  active transition, while each  $\overline{\text{CAS}}$  active transition allows selection of a new column location on the row.

An EDO mode cycle is initiated by a normal read, write, or read-write cycle, as described in prior sections. Once the timing requirements for the first cycle are met,  $\overline{\text{CAS}}$  transitions to inactive for minimum  $t_{CP}$ , while  $\overline{\text{RAS}}$  remains low ( $V_{IL}$ ). The second  $\overline{\text{CAS}}$  active transition while  $\overline{\text{RAS}}$  is low initiates the first EDO mode cycle ( $t_{EPC}$  or  $t_{ERWC}$ ). Either a read, write, or read-write operation can be performed in an EDO mode cycle, subject to the same conditions as in normal operation (previously described). These operations can be intermixed in consecutive EDO mode cycles and performed in any order. The maximum number of consecutive EDO mode cycles is limited by  $t_{RASp}$ . EDO mode operation is ended when  $\overline{\text{RAS}}$  transitions to inactive, coincident with or following  $\overline{\text{CAS}}$  inactive transition.

## REFRESH CYCLES

The dynamic RAM design is based on capacitor charge storage for each bit in the array. This charge will tend to degrade with time and temperature. Each bit must be periodically **refreshed** (recharged) to maintain the correct bit state. Bits require refresh every  $t_{RFSH}$ .

This is accomplished by cycling through the row addresses in sequence within the specified refresh time. All the bits on a row are refreshed simultaneously when the row is addressed. Distributed refresh implies a row refresh every 15.6  $\mu$ s. Burst refresh, a refresh of all rows consecutively, must be performed every  $t_{REFSH}$ .

A normal read, write, or read-write operation to the RAM will refresh all the bits associated with the particular row decodes. Three other methods of refresh, **RAS-only refresh**, **CAS before RAS refresh**, and **hidden refresh** are available on this device for greater system flexibility.

**RAS-Only Refresh**

RAS-only refresh consists of  $\overline{RAS}$  transition to active, latching the row address to be refreshed, while  $\overline{CAS}$  remains high ( $V_{IH}$ ) throughout the cycle. An external counter should be employed to ensure that all rows are refreshed within the specified limit.

**CAS Before RAS Refresh**

CAS before RAS refresh is enabled by bringing  $\overline{CAS}$  active before  $\overline{RAS}$ . This clock order activates an internal refresh counter that generates the row address to be refreshed. External address lines are ignored during the automatic refresh cycle. The output buffer remains at the same state it was in during the previous cycle (hidden refresh).  $\overline{W}$  must be inactive for time  $t_{WRP}$  before and time  $t_{WRH}$  after  $\overline{RAS}$  active transition to prevent switching the device into a test mode cycle.

**Hidden Refresh**

Hidden refresh allows refresh cycles to occur while maintaining valid data at the output pin. Holding  $\overline{CAS}$  active at the end of a read or write cycle while  $\overline{RAS}$  cycles inactive for  $t_{RP}$

and back to active starts the hidden refresh. This is essentially the execution of a CAS before RAS refresh from a cycle in progress (see Figure 1).  $\overline{W}$  is subject to the same conditions with respect to  $\overline{RAS}$  active transition (to prevent test mode entry) as in  $\overline{CAS}$  before  $\overline{RAS}$  refresh.

**CAS BEFORE RAS REFRESH COUNTER TEST**

The internal refresh counter of this device can be tested with a **CAS before RAS refresh counter test**. This test is performed with a read-write operation. During the test, the internal refresh counter generates the row address, while the external address supplies the column address. The entire array is refreshed after completing one cycle for each column as indicated by the check data written in each row. See **CAS before RAS refresh counter test cycle timing diagram**.

The test can be performed after a minimum of eight **CAS before RAS** initialization cycles. Test procedure:

1. Write 0s into all memory cells with normal write mode.
2. Select a column address, read 0 out and write 1 into the cell by performing the **CAS before RAS refresh counter test, read-write cycle**. Repeat this operation for every column.
3. Read the 1s that were written in step two in normal read mode.
4. Using the same starting column address as in step two, read 1 out and write 0 into the cell by performing the **CAS before RAS refresh counter test, read-write cycle**. Repeat this operation for every column.
5. Read 0s which were written in step four in normal read mode.
6. Repeat steps one through five using complement data.

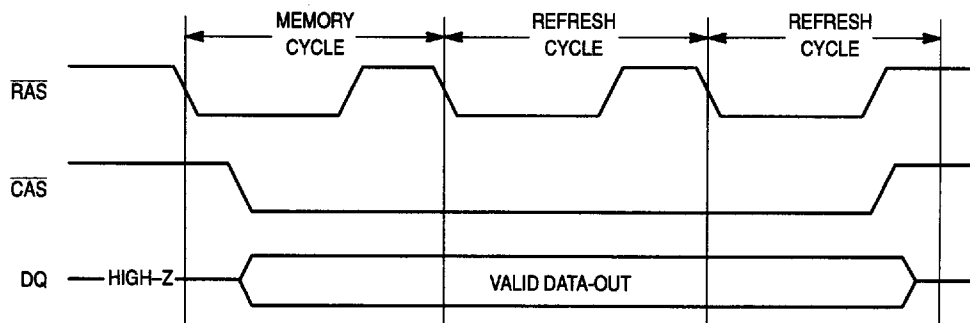


Figure 1. Hidden Refresh Cycle

**PRESENCE DETECT OPERATION**

**LEXICON**

This lexicon will describe some terms used in this serial interface description.

**MASTER:** The device that initiates the serial transmission is designated as master. In general, it is the device generating the clock. The SPD device can never function as a master.

**SLAVE:** The SPD device always operates as a slave.

**TRANSMITTER:** The device with its SDA pin in output is a data transmitter. In the case of multiple devices in output, the device sending a low level will win due to the Open-Drain connection.

**RECEIVER:** A device that has been properly selected by a chip address followed by a write bit is a receiver, and will shift data present on the SDA pin in internal registers.

**MSB:** The Most Significant Bit is the first bit transmitted and received.

**START CONDITION:** The start condition is defined as a 1 to 0 transition of SDA when SCL is high. The first byte of data following a start condition includes the chip address followed by the Read/Write bit. All devices connected on the same bus receive this data to check if they are addressed.

**STOP CONDITION:** The stop condition is defined as a 0 to 1 transition of SDA when SCL is high. In this circuit, the stop condition is never mandatory. An EEPROM programming can be initiated by the STOP or also by any following START condition.

A STOP after a serial read sequence will put the device in standby state.

**CHIP ADDRESS:** The first byte transmitted after a START contains the chip address followed by the Read/Write bit. The 7-bit chip address is formed of 4 fixed bits followed by 3 chip select bits.

Fixed bits are 1010 for this device. The 3 chip select bits must correspond to the 3 SA0–2 inputs for proper chip selection.

**READ/WRITE BIT:** The 8th bit transmitted by the master after the 7-bit chip address will indicate the direction of transfer for the next bytes (until a new start or stop). If low, the following bytes are transmitted by the master. If high, the following bytes are transmitted by the SPD device.

**BYTE ADDRESS:** The first byte of data received by the memory after the chip address, will be latched in the byte address register and is used to select one of the 256 EEPROM bytes.

**ACKNOWLEDGE BIT:** This bit is sent by the selected receiver on the data line after a byte reception. Due to the open drain structure, a valid acknowledge bit corresponds to a low level. While operating as a transmitter, sending a sequence of data bits, this device will check the acknowledge bit generated by the master. The absence of this bit will stop the transmission of data.

**PROTOCOL**

At the protocol level, the transmission of data is defined in the form of sequences of Start (STA), Stop (STO) conditions, and bytes followed by acknowledge bits.

**Standby State**

When no serial transmission and no programming are made, the SPD is in standby. A STOP condition following a read sequence or a write byte address sequence (without data write), will put the SPD in standby. A new START condition will wake up the SPD, to get the chip address. If the chip address is not valid, the SPD will return to standby.

The power consumption is minimum in standby.

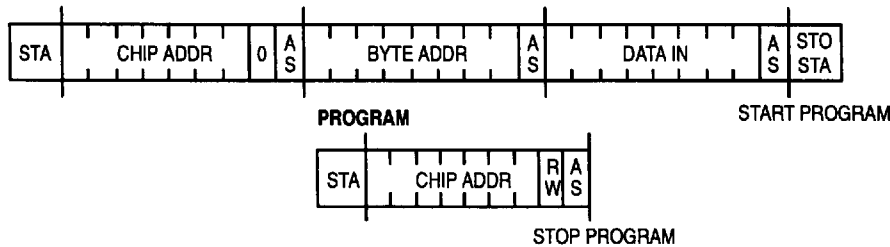
**Write Sequence**

The serial write to the memory includes a serial transmission of the byte address and the data to be written. When this is completed by a stop, the programming sequence is initiated.

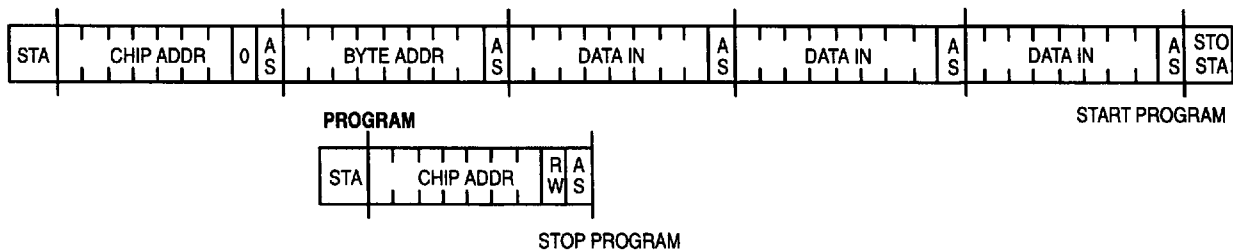
During the write cycle, the SPD inputs and the SDA pin are disabled for the time  $t_{WFR}$  and the SPD will not respond to any requests from the master.

It is possible to program simultaneously up to 8 bytes, provided the 5 most significant bits of their addresses are identical. The byte address is incremented after each new data byte shifted in.

**WRITE ONE BYTE**



**WRITE UP TO 8 BYTES**



STA: Start Condition  
STO: Stop Condition

R/W Bit: 1 = Read/0 = Write  
INC: Increment Byte Address

AS: Slave Acknowledge (SPD)  
AM: Master Acknowledge

**Figure 2. SPD Write Protocol**

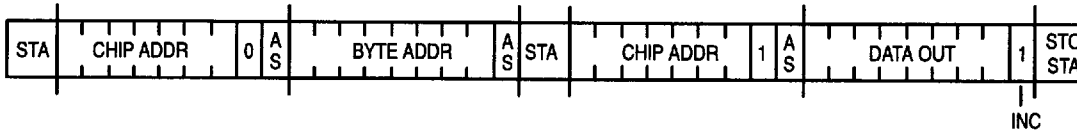
**Read Sequence**

Reading data from the memory is made in two steps. First the byte address must be loaded in the byte address register. Then data can be read out of the memory. The first step is only required to define the byte address. If this address was predefined from a previous read, this step can be skipped.

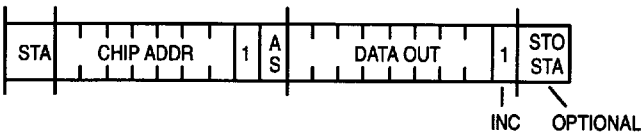
The byte address is automatically incremented after each data byte transmitted.

This is also valid after the last byte of a transmission. Therefore, the next read sequence without any byte address specified will transmit data of the next byte. A read sequence will transmit data bytes of successive addresses until the absence of the acknowledge bit from the master. In this case, the SDA output driver will switch off and the circuit will go to standby.

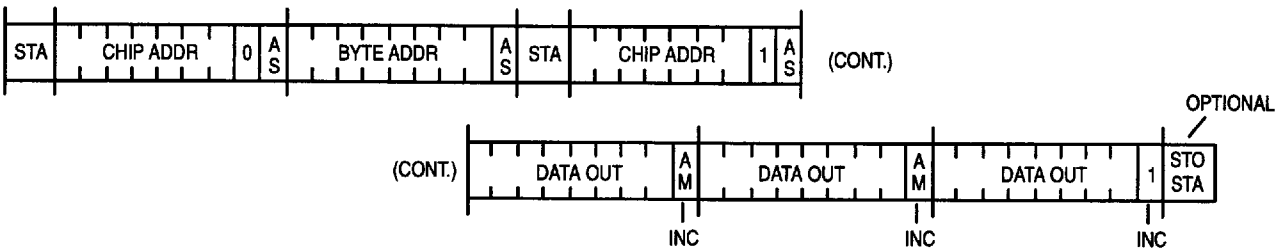
**READ ONE BYTE (INCREMENT WRITE BYTE ADDRESS)**



**READ ONE MORE BYTE (BYTE ADDRESS DEFINED)**



**READ MANY BYTES**



STA: Start Condition  
STO: Stop Condition

R/W Bit: 1 = Read/0 = Write  
INC: Increment Byte Address

AS: Slave Acknowledge (SPD)  
AM: Master Acknowledge

**Figure 3. SPD Read Protocol**

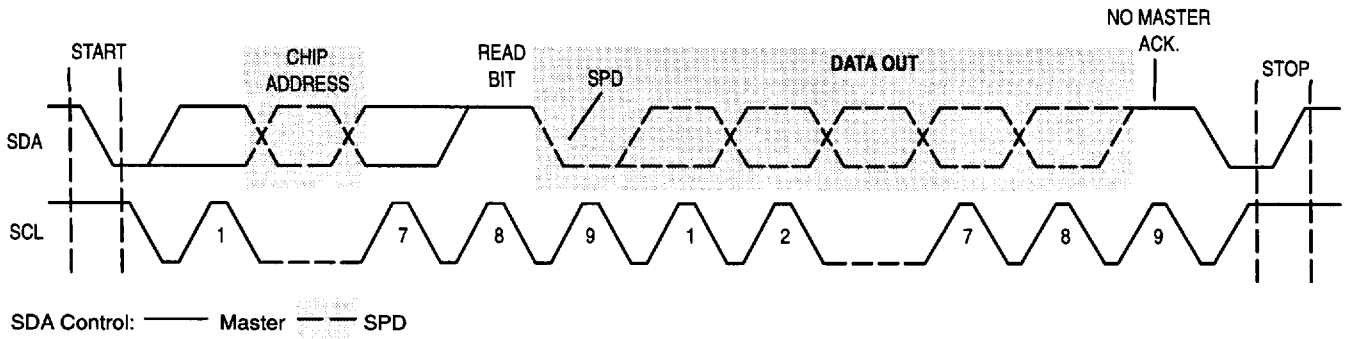


Figure 4. SPD Read Detail

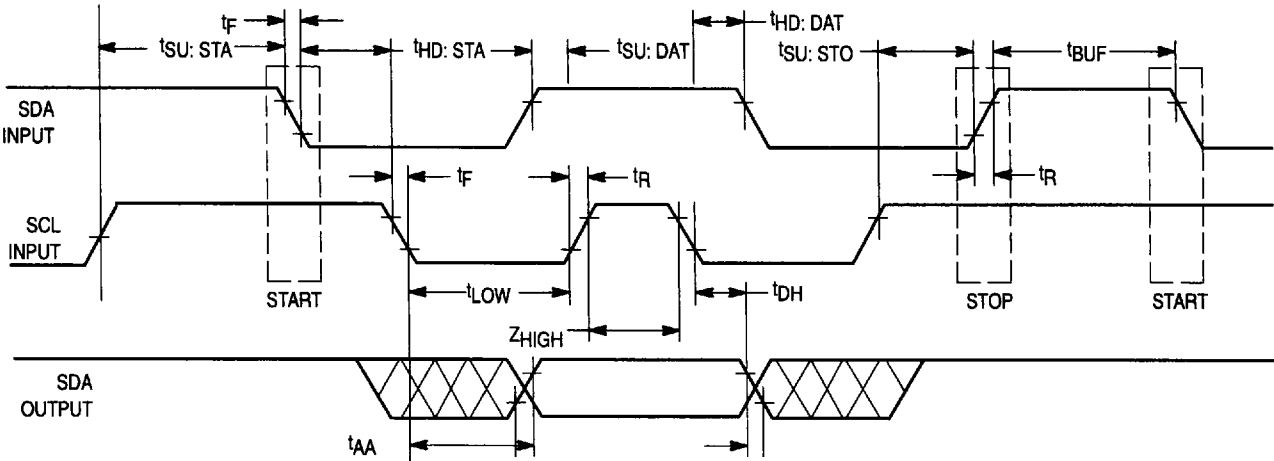


Figure 5. SPD Timings

## PRESENCE DETECT READ AND WRITE CYCLE

Parameter	Symbol	Min	Max	Unit
SCL Clock Frequency	F <sub>SCL</sub>		100	kHz
Noise Suppression Time Constant at SCL, SDA Inputs	T <sub>I</sub>		100	ns
SCL Low to SDA Data Out Valid	t <sub>AA</sub>	0.1	4.5	μs
Time Bus Must be Free Before a New Transmission Can Start	t <sub>BUF</sub>	4.7		μs
Start Condition Hold Time	t <sub>HD:STA</sub>	4.0		μs
Clock Low Period	t <sub>LOW</sub>	4.7		μs
Clock High Period	t <sub>HIGH</sub>	4.0		μs
Start Condition Setup Time (for a Repeated Start Condition)	t <sub>SU:STA</sub>	4.7		μs
Data In Hold Time	t <sub>HD:DAT</sub>	0		μs
Data In Setup time	t <sub>SU:STA</sub>	250		ns
SDA and SCL Rise Time	t <sub>R</sub>		1	μs
SDA and SCL Fall Time	t <sub>F</sub>		300	ns
Stop Condition Setup Time	t <sub>SU:STO</sub>	4.7		μs
Data Out Hold Time	t <sub>DH</sub>	100		ns
Write Cycle Time	t <sub>WR</sub> *		10	ms

\* The write cycle time (t<sub>WR</sub>) is the time from a valid stop condition of a write sequence to the end of the internal erase/program cycle.

**Signal Levels**

During a transmission, SDA line transitions must occur when SCL is low. A negative transition of SDA with SCL high is recognized as a START condition, the positive transition as a STOP condition.

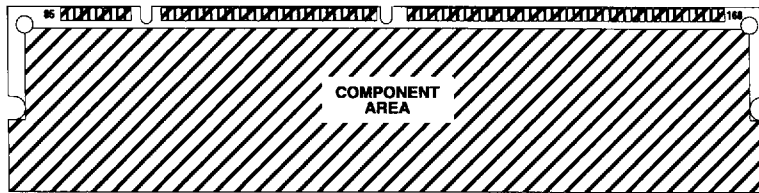
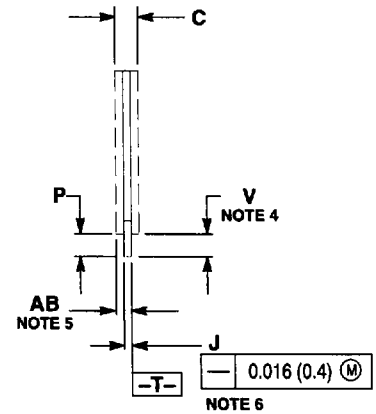
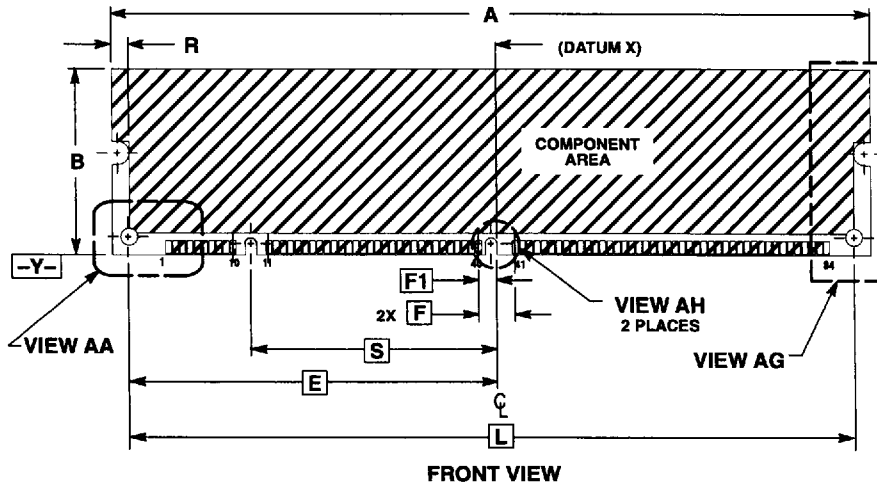
The acknowledge bit is provided by the device receiving

data. Therefore, during this time the data transmitter must leave the SDA line at high impedance.

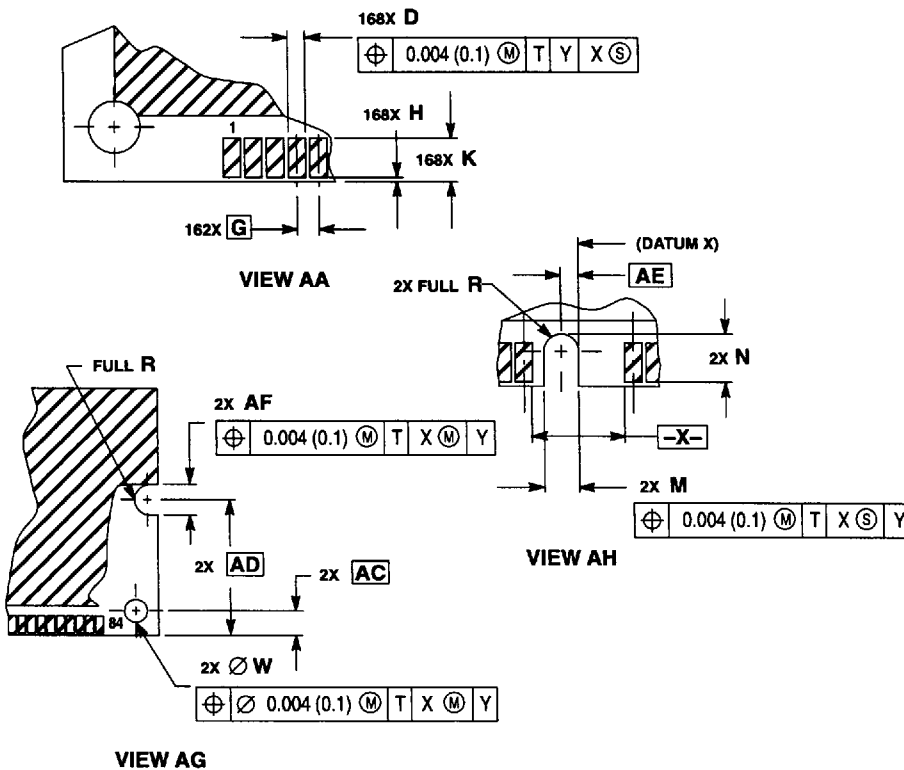
This memory has an open drain SDA output, so an external pull-up resistor to V<sub>CC</sub> should be included on the SDA line.

PACKAGE DIMENSIONS

168-LEAD DIMM  
CASE 1115A-01



BACK VIEW

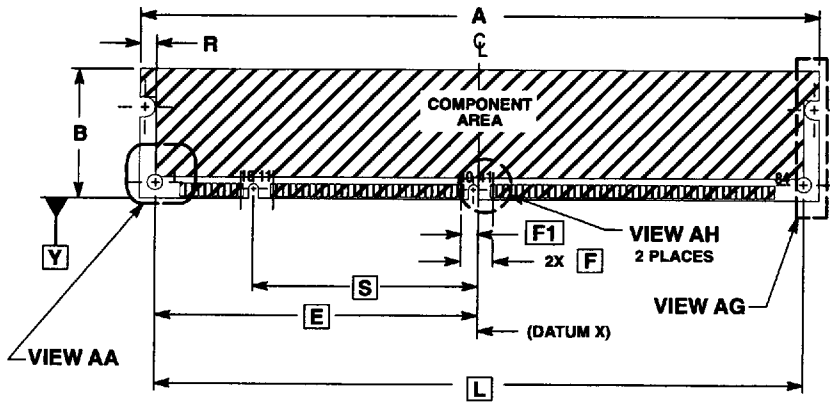


NOTES:

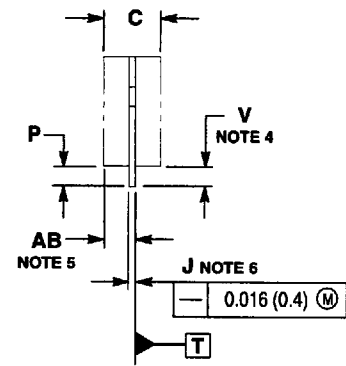
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. CARD THICKNESS APPLIES ACROSS TABS AND INCLUDES PLATING AND/OR METALLIZATION.
4. DIMENSIONS C AND V DEFINE A DOUBLE-SIDED MODULE.
5. DIMENSION AB DEFINES OPTIONAL SINGLE-SIDED MODULE.
6. STRAIGHTNESS CALLOUT APPLIES TO TAB AREA ONLY.
7. R DIMENSION DEFINES SLOT END AND EDGE OF COMPONENT AREA.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	5.245	5.255	133.22	133.48
B	1.245	1.255	31.62	31.88
C	—	0.157	—	4.00
D	0.037	0.041	0.95	1.05
E	2.507 BSC	—	63.675 BSC	—
F	0.250 BSC	—	6.35 BSC	—
F1	0.125 BSC	—	3.175 BSC	—
G	0.050 BSC	—	1.27 BSC	—
H	—	0.010	—	0.25
J	0.046	0.054	1.17	1.37
K	0.100	—	2.54	—
L	5.014 BSC	—	127.35 BSC	—
M	0.075	0.083	1.90	2.10
N	0.118	0.128	3.00	3.25
P	0.158	—	4.00	—
R	0.118	—	3.00	—
S	1.700 BSC	—	43.18 BSC	—
V	0.158	—	4.00	—
W	0.114	0.122	2.90	3.10
AB	—	0.106	—	2.70
AC	0.118 BSC	—	3.00 BSC	—
AD	0.700 BSC	—	17.78 BSC	—
AE	0.039 BSC	—	1.00 BSC	—
AF	0.154	0.161	3.90	4.10

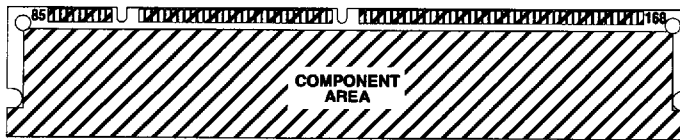
168-LEAD DIMM  
CASE 1115-01



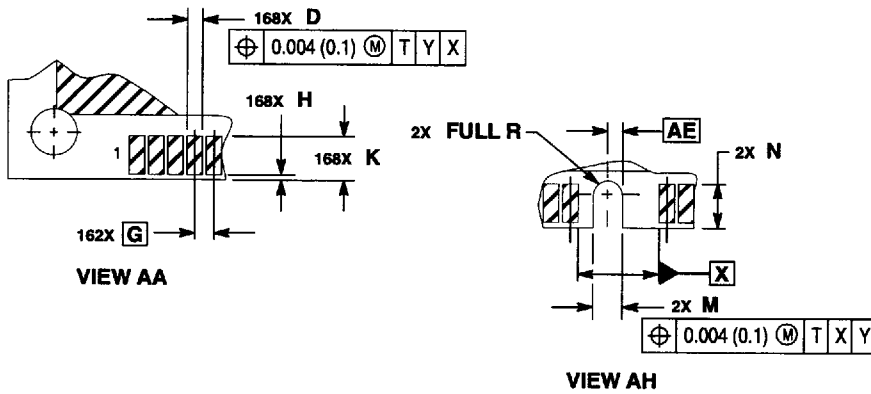
FRONT VIEW



SIDE VIEW

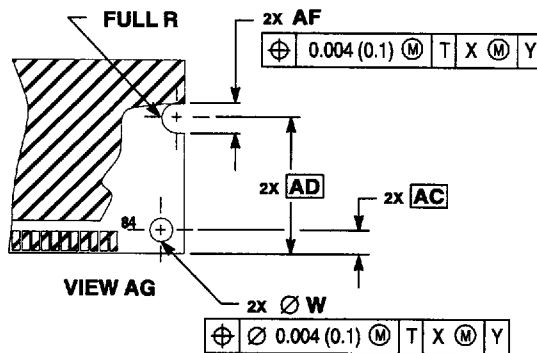


BACK VIEW



VIEW AA

VIEW AH



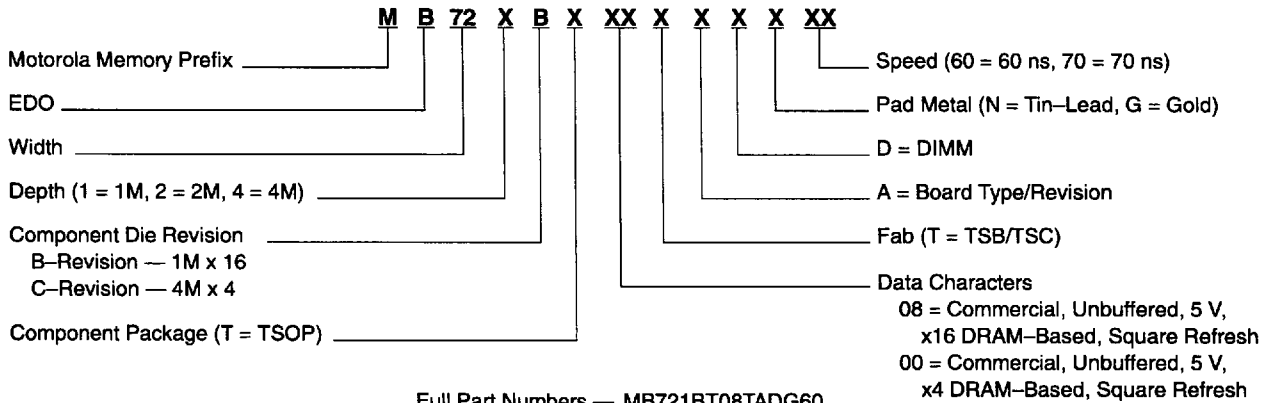
VIEW AG

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCH.
3. CARD THICKNESS APPLIES ACROSS TABS AND INCLUDES PLATING AND/OR METALLIZATION.
4. DIMENSIONS C AND V DEFINE A DOUBLE-SIDED MODULE.
5. DIMENSION AB DEFINES OPTIONAL SINGLE-SIDED MODULE.
6. STRAIGHTNESS CALLOUT APPLIES TO TAB AREA ONLY.
7. R DIMENSION DEFINES SLOT END AND EDGE OF COMPONENT AREA.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	5.245	5.255	133.22	133.48
B	0.995	1.005	25.27	25.53
C	—	0.354	—	9.00
D	0.037	0.041	0.95	1.05
E	2.507 BSC		63.675 BSC	
F	0.250 BSC		6.35 BSC	
F1	0.125 BSC		3.175 BSC	
G	0.050 BSC		1.27 BSC	
H	—	0.010	—	0.25
J	0.046	0.054	1.17	1.37
K	0.100	—	2.54	—
L	5.014 BSC		127.35 BSC	
M	0.075	0.083	1.90	2.10
N	0.118	0.128	3.00	3.25
P	0.158	—	4.00	—
R	0.118	—	3.00	—
S	1.700 BSC		43.18 BSC	
V	0.158	—	4.00	—
W	0.114	0.122	2.90	3.10
AB	—	0.205	—	5.20
AC	0.118 BSC		3.00 BSC	
AD	0.700 BSC		17.78 BSC	
AE	0.039 BSC		1.00 BSC	
AF	0.154	0.161	3.90	4.10


**ORDERING INFORMATION**  
(Order by Full Part Number)



Full Part Numbers — MB721BT08TADG60  
MB721BT08TADG70

MB722BT08TADG60  
MB722BT08TADG70

MB724CT00TADG60  
MB724CT00TADG70

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