DPV64X16A

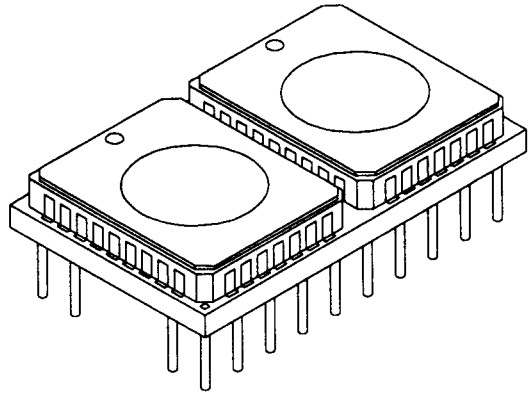
64K X 16 UVEPROM PGA MODULE

PRELIMINARY

DESCRIPTION:

The DPV64X16A is a 40-pin Pin Grid Array (PGA) consisting of two 64K X 8 UVEPROM devices in ceramic LCC packages surface mounted on a co-fired ceramic substrate with matched thermal coefficients. The LCCs are mounted in a pattern resulting in the smallest possible module outline.

The pins have been arranged around a central 0.3" gap which can accommodate a heat rail, if desired. In this central gap is a cavity containing two 0.1µf decoupling capacitors.

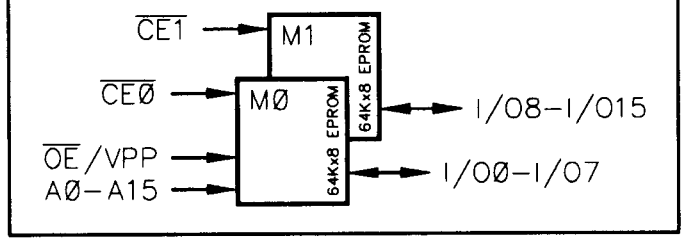


FEATURES:

- Organizations Available:
  128K X 8 or 64K X 16
- Access Times:
  55*, 70, 90, 120, 150, 170, 200, 250ns
- Fully Static Operation - No clock or refresh required
- Programming Voltage 12.5 Vdc
- Simple Programming Requirements
- Three-State Outputs
- High Speed Programming Algorithm (1.0ms Pulses Typ.)
- Common Data Inputs and Outputs
- TTL-compatible Inputs and Outputs
- 40-Pin PGA (Pin Grid Array) Package

* Commercial only.

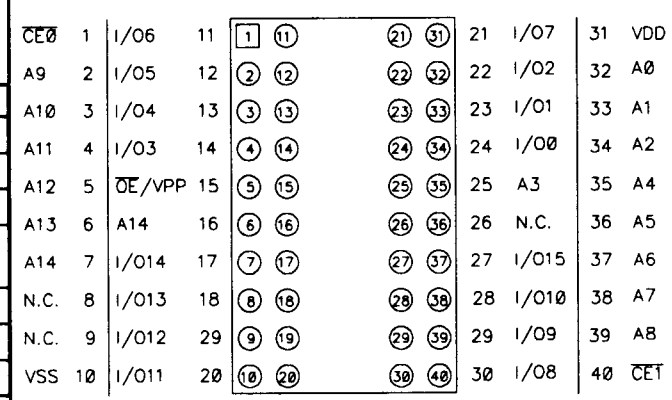
FUNCTIONAL BLOCK DIAGRAM



PIN NAMES	
A0 - A15	Address Inputs
I/O0 - I/O15	Data In/Out
$\overline{CE0}$, $\overline{CE1}$	Chip Enables
$\overline{OE}$ / V_{PP}	Output Enable / Programming Voltage
V_{DD}	Power (+5V)
V_{SS}	Ground
N.C.	No Connect

PIN-OUT DIAGRAM

(TOP VIEW)



$\overline{CE0}$	1	I/O6	11	1	21	I/O7	31	VDD
A9	2	I/O5	12	2	22	I/O2	32	AØ
A10	3	I/O4	13	3	23	I/O1	33	A1
A11	4	I/O3	14	4	24	I/OØ	34	A2
A12	5	$\overline{OE}$/VPP	15	5	25	A3	35	A4
A13	6	A14	16	6	26	N.C.	36	A5
A14	7	I/O14	17	7	27	I/O15	37	A6
N.C.	8	I/O13	18	8	28	I/O10	38	A7
N.C.	9	I/O12	29	9	29	I/O9	39	A8
VSS	10	I/O11	20	10	30	I/O8	40	$\overline{CE1}$

FOR FURTHER INFORMATION
SEE CHAPTER 10
FOR COMPLETE DATA SHEET