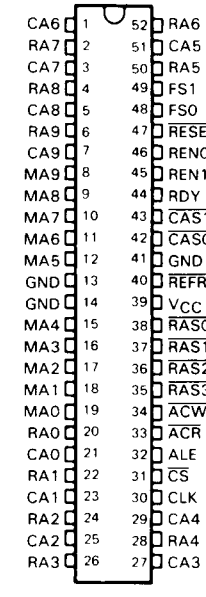
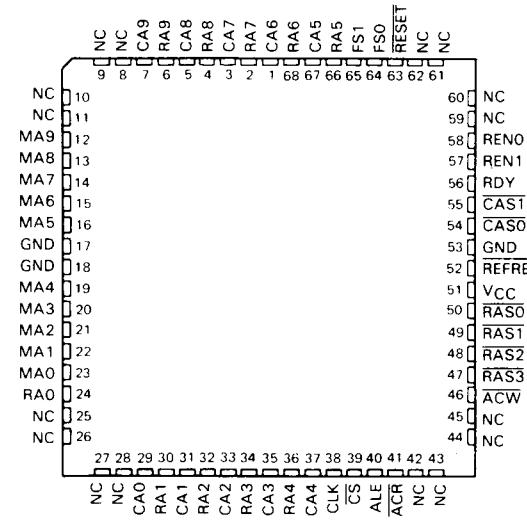
D3132, SEPTEMBER 1988 - REVISED MAY 1989

- Inputs are TTL- and CMOS-Voltage Compatible
- Controls Operation of 64K, 256K, and 1M Dynamic RAMs
- Creates Static RAM Appearance
- One Package Contains Address Multiplexer, Refresh Control, and Timing Control
- Directly Addresses and Drives Up to 4 Banks of Memory
- Operates from Microprocessor Clock
  - No Crystals, Delay Lines, or RC Networks
  - Eliminates Arbitration Delays
- Refresh May Be Internally or Externally Initiated
- Versatile
  - Strap-Selected Refresh Rate
  - Synchronous, Predictable Refresh
  - Selection of Distributed, Transparent, and Cycle-Steal Refresh Modes
  - Interfaces Easily to Popular Microprocessors
  - Asynchronous $\overline{\text{RESET}}$
  - Choice of CLK Polarity on Refresh/Access Arbitration
- High-Performance Si-Gate CMOS Technology
- Strap-Selected Refresh Frequencies for Microprocessor/Memory Speed Matching
- Ability to Synchronize or Interleave Controller with the Microprocessor System (Including Multiple Controllers)
- 3-State Outputs Allow Multiport Memory Configuration
- Performance Range:
  100 ns ALE low to $\overline{\text{CAS}}$ low
- Functionally Compatible with TMS4500A/B and with THCT4502B
- Available in Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

JD OR N PACKAGE
(TOP VIEW)



FK OR FN PACKAGE
(TOP VIEW)



NC – No internal connection

description

The 'ACT4503 is a monolithic DRAM system controller providing address multiplexing, timing, control, and refresh/access arbitration functions to simplify the interface of dynamic RAMs to microprocessor systems.

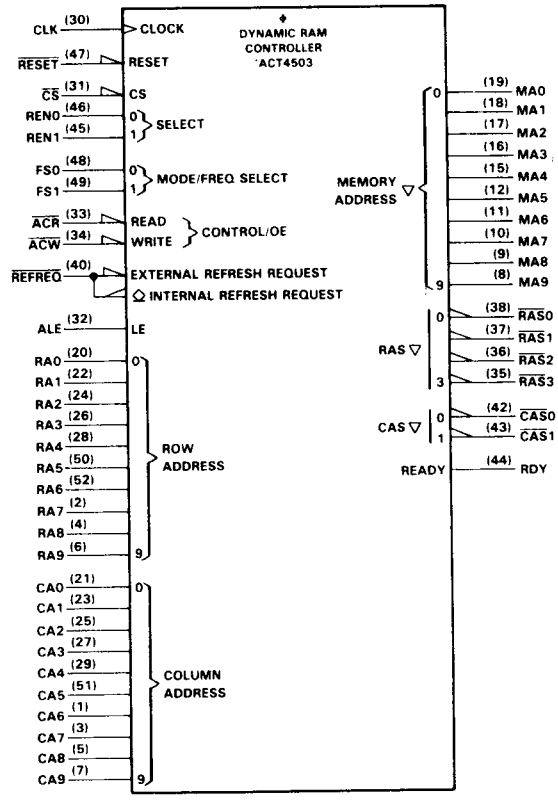
The controller contains an 20-bit multiplexer that generates the address lines for the memory device from the 20 system address bits and provides the strobe signals required by the memory to decode the address. A 10-bit refresh counter generates up to 1024 row addresses required to refresh.

A refresh timer is provided to generate the necessary timing to refresh the dynamic memories and ensure data retention.

for complete data sheet

The complete version of this data sheet and application information can be found in the *Cache Memory Management Data Book*, Literature #SCAD002. To obtain a copy of this data book, contact your local TI sales representative or call the TI Customer Response Center at 1-800-223-3200.

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std. 91-1984.
Pin numbers shown are for JD and N packages.