



MT43C8128/9

7-46-23-37

# TRIPLE PORT DRAM

# 128K x 8 DRAM WITH DUAL 256 x 8 SAMS

## FEATURES

- Three asynchronous, independent, data access ports
- Fast access times - 80ns random, 25ns serial
- Operation and control compatible with 1 Meg VRAMS
- High performance CMOS silicon gate process
- Low power: 15mW standby; 450mW active, typical
- 512-cycle refresh within 8ms
- Refresh modes: RAS-ONLY, CAS-BEFORE-RAS, and HIDDEN
- FAST PAGE MODE access cycles
- Two bidirectional Serial Access Memories (SAMs)
- Fully static SAMs and Mask Register, no refresh required
- 2048-bit Transfer Mask Register
- SERIAL MASK DATA INPUT mode

## SPECIAL FUNCTIONS

- MASKED WRITE (Write-Per-Bit)
- PERSISTENT MASKED WRITE
- SPLIT READ AND WRITE TRANSFERS
- BLOCK WRITE
- BIT MASKED TRANSFERS

## OPTIONS

- Timing (DRAM, SAMs)
  - 80ns, 25ns - 8
  - 100ns, 30ns -10
  - 120ns, 35ns -12
- Packages
  - Plastic LCC (750 mil) EJ
- Functionality
  - QSF output (indicates SAM half accessed) 43C8128
  - SSF input (Split SAM special function, stop count) 43C8129

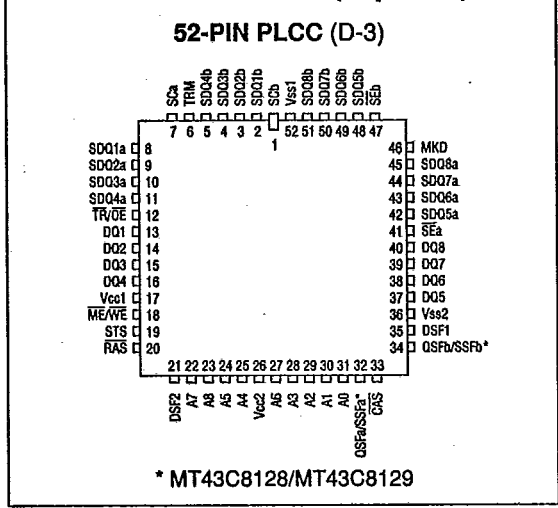
## MARKING

## GENERAL DESCRIPTION

The MT43C8128/9 are high speed, triple port CMOS dynamic random access memories (TPDRAM) containing 1,048,576 bits. Data may be accessed by an 8 bit wide DRAM port or by either of two independently-clocked 256 x 8-bit serial access memory (SAM) ports. Data may be transferred bidirectionally between the DRAM and the SAMs.

The DRAM portion of the TPDRAM is functionally identical to the MT4C4256 (256K x 4) DRAM. Sixteen 256-bit data registers make up the serial access memory portions of the TPDRAM. Data I/O and internal data transfer are accomplished using five separate bidirectional data paths; the 8-bit random access I/O port, a pair of internal 2048 bit wide paths between the DRAM and the SAMs, and the pair

## PIN ASSIGNMENT (Top View)



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of 8-bit serial I/O ports for the SAMs. The rest of the circuitry consists of the control, timing, and address decoding logic.

All three ports may be operated asynchronously and independently of the others except when data is being internally transferred between the DRAM and either SAM.

Each of the 2048 bits involved in an internal transfer may be individually masked by performing a BIT MASKED TRANSFER operation. The 256 x 8-bit, Bit Mask Data Register can be parallel loaded from the DRAM or, either SAM, or it may be serial loaded through the MKD serial input.

As with all DRAMs, the TPDRAM must be refreshed to maintain data. The refresh cycles must be timed so that all 512 combinations of RAS addresses are executed at least every 8ms (regardless of sequence). Micron recommends evenly spaced refresh cycles for maximum data integrity. An internal transfer between the DRAM and either SAM counts as a refresh cycle. The SAM portions of the TPDRAM are fully static and do not require any refresh.

The operation and control of the MT43C8128/9 are compatible with the operation of the MT42C8128 (128K x 8 Video RAM). However, the MT43C8128/9 offer an additional SAM and special features that may be used to enhance system performance.

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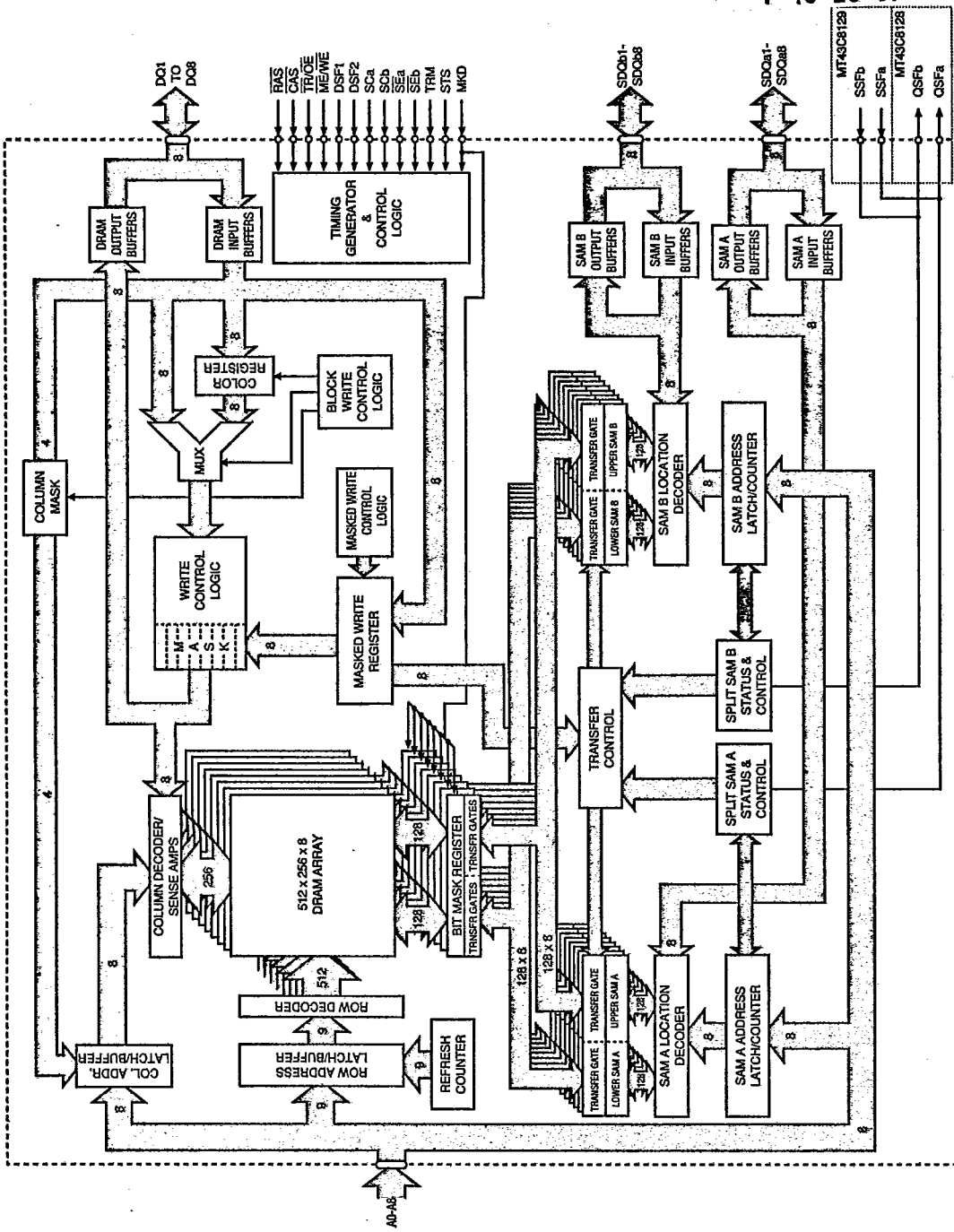


Figure 1  
MT43C8128/9 BLOCK DIAGRAM

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## PIN DESCRIPTIONS

PLCC PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
7	SCa	Input	Serial Clock, SAMA: Clock input to the serial address counter for the SAMA registers and strobe for SAMA control and data inputs.
1	SCb	Input	Serial Clock, SAMb: Clock input to the serial address counter for the SAMb registers and strobe for SAMb control and data inputs.
12	TR/OE	Input	Transfer Enable: Enables an internal TRANSFER operation at the falling edge of $\overline{RAS}$ , or Output Enable: Enables the DRAM output buffers when taken LOW after $\overline{RAS}$ goes LOW ( $\overline{CAS}$ must also be LOW), otherwise the output buffers are in a high impedance state.
18	$\overline{ME/WE}$	Input	Mask Enable: If $\overline{ME/WE}$ is LOW at the falling edge of $\overline{RAS}$ , a MASKED WRITE cycle is performed, or Write Enable: $\overline{ME/WE}$ is also used to select a READ ( $\overline{ME/WE} = H$ ) or WRITE ( $\overline{ME/WE} = L$ ) cycle when accessing the DRAM. This includes a READ TRANSFER ( $\overline{ME/WE} = H$ ) or WRITE TRANSFER ( $\overline{ME/WE} = L$ ).
41	$\overline{SEa}$	Input	Serial Port Enable SAMA: $\overline{SEa}$ enables Port A serial I/O buffers and allows a serial READ or WRITE operation to occur; otherwise, the output buffers are in a High-Z state. $\overline{SEa}$ is also used during a TRANSFER operation to indicate whether a WRITE TRANSFER or a SERIAL INPUT MODE ENABLE (PSEUDO WRITE TRANSFER) cycle is performed.
47	$\overline{SEb}$	Input	Serial Port Enable, SAMb: $\overline{SEb}$ enables Port B serial I/O buffers and allows a serial READ or WRITE operation to occur; otherwise, the output buffers are in a High-Z state. $\overline{SEb}$ is also used during a TRANSFER operation to indicate whether a WRITE TRANSFER or a SERIAL-INPUT-MODE ENABLE (PSEUDO WRITE TRANSFER) cycle is performed.
35	DSF1	Input	Special Function (Control) 1: DSF1 is used to indicate which special functions are used on a particular access or transfer cycle. See the Functional Truth Table for a detailed description.
21	DSF2	Input	Special Function (Control) 2: DSF2 is used to indicate which special functions are used on a particular access or transfer cycle. See the Functional Truth Table for a detailed description.
20	$\overline{RAS}$	Input	Row Address Strobe: $\overline{RAS}$ is used to clock in the 9 row-address bits and as a strobe for control and data inputs.
33	$\overline{CAS}$	Input	Column Address Strobe: $\overline{CAS}$ is used to clock in the 8 column-address bits, enable the DRAM output buffers (along with TR/OE), and as a strobe for control and data inputs.

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## PIN DESCRIPTIONS (Continued)

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PLCC PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
31, 30, 29, 28 25, 24, 27, 22 23	A0 - A8	Input	Address Inputs: For DRAM operation, these inputs are multiplexed and clocked by $\overline{RAS}$ and $\overline{CAS}$ to select one 8-bit word out of the 128K available. During TRANSFER operations, A0 to A8 indicate the DRAM row being accessed (when $\overline{RAS}$ goes LOW) and A0-A7 indicate the SAM start address (when $\overline{CAS}$ goes LOW). A7, A8 = "don't care" for the start address when doing SPLIT TRANSFER.
19	STS	Input	SAM Transfer Select: The state of STS at $\overline{RAS}$ time determines which SAM is involved in a transfer (SAMA=LOW, SAMb=HIGH).
46	MKD	Input	Mask Data Input: MKD is used during BIT MASK REGISTER LOAD cycles to enable or disable the serial mask input mode (SMI). If SMI is enabled (MKD=HIGH at $\overline{RAS}$ ), then MKD is used as mask data input and is clocked by SCb into the mask data register.
6	TRM	Input	Transfer Mask Select: TRM is used to select between NORMAL TRANSFER cycles and BIT MASKED TRANSFER or BIT MASK REGISTER LOAD cycles.
13, 14, 15, 16 37, 38, 39, 40	DQ1 - DQ8	Input/ Output	DRAM Data I/O: Data inputs and outputs for the DRAM memory array; inputs for the MASK and COLOR REGISTER load cycles; address mask inputs for BLOCK WRITE cycles.
8, 9, 10, 11 42, 43, 44, 45	SDQa1-SDQa8	Input/ Output	Serial Data I/O, SAMA: Input, Output, or High-Z.
2, 3, 4, 5 48, 49, 50, 51	SDQb1-SDQb8	Input/ Output	Serial Data I/O, SAMb: Input, Output, or High-Z.
32	QSFa/SSFa	Output	Split SAM Status, SAMA (MT43C8128): QSFa indicates which half of SAMA is being accessed (Lower = LOW, Upper = HIGH).
		Input	Split SAM Special Function, SAMA (MT43C8129): SSFa=HIGH stops access to current half of SAM and will load the Tap address of the next half into the address pointer. SSFa is synchronized with SCa.
34	QSFb/SSFb	Output	Split SAM Status, SAMb (MT43C8128): QSFb indicates which half of SAMb is being accessed (Lower = LOW, Upper = HIGH).
		Input	Split SAM Special Function, SAMb (MT43C8129): SSFb=HIGH stops access to current half of SAM and will load the Tap address of the next half into the address pointer. SSFb is synchronized with SCb.
17, 26	Vcc	Supply	Power Supply: +5V $\pm$ 10%
52, 36	Vss	Supply	Ground

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## FUNCTIONAL DESCRIPTION

The MT43C8128/9 may be divided into four functional blocks (see Figure 1): the DRAM and its special functions, the Bit Mask Register (BMR), the two Serial Access Memories (SAMs), and the DRAM/SAM/BMR transfer circuitry. All the operations described below are also shown in the AC Timing Diagrams section of this data sheet and are summarized in the Functional Truth Table.

**Note:** For dual function pins, the function that is not being discussed will be surrounded by parentheses. For example, when discussing transfer operations the  $\overline{TR}/\overline{OE}$  pin will be shown as  $\overline{TR}/(\overline{OE})$ .

## DRAM OPERATION

This section describes the operation of the random access port and the special functions associated with the DRAM.

## DRAM REFRESH (ROR, CBR, and HR)

Like any DRAM-based memory, the MT43C8128/9 TPD RAM must be refreshed to retain data. All 512 row-address combinations must be accessed within 8ms. The MT43C8128/9 supports  $\overline{CAS}$ -BEFORE- $\overline{RAS}$ ,  $\overline{RAS}$ -ONLY and HIDDEN types of refresh cycles.

For the  $\overline{CAS}$ -BEFORE- $\overline{RAS}$  REFRESH cycle, the row addresses are generated and stored in an internal address counter. The user need not supply any address data and simply must perform 512  $\overline{CAS}$ -BEFORE- $\overline{RAS}$  cycles within the 8ms time period.

For  $\overline{RAS}$ -ONLY REFRESH cycles, the refresh address must be generated externally and applied to the A0-A8 inputs. The DQ pins remain in a High-Z state for both the  $\overline{RAS}$  ONLY and  $\overline{CAS}$ -BEFORE- $\overline{RAS}$  cycles.

HIDDEN REFRESH (HR) cycles are performed by toggling  $\overline{RAS}$  (while keeping  $\overline{CAS}$  LOW) after a READ or WRITE cycle. This performs  $\overline{CAS}$ -BEFORE- $\overline{RAS}$  cycles but does not disturb the DQ lines.

Any DRAM READ, WRITE, or TRANSFER cycle also refreshes the DRAM row that is being accessed. The SAM and Bit Mask Register portions of the MT43C8128/9 are fully static and do not require any refreshing.

## DRAM READ AND WRITE CYCLES (RW)

The DRAM portion of the TPD RAM is nearly identical to standard 128K x 8 DRAMs. However, because several of the DRAM control pins are used for additional functions on this device, several conditions that were undefined or "don't care" states for the DRAM are specified for the TPD RAM. These conditions are highlighted in the following discussion. In addition, the TPD RAM has several special functions that may be used when writing to the DRAM.

The 17 address bits used to select an 8-bit word from the 131,072 available are latched into the chip using the A0-A8,  $\overline{RAS}$ , and  $\overline{CAS}$  inputs. First, the 9 row-address bits are setup on the address inputs and clocked into the part when  $\overline{RAS}$  transitions from HIGH to LOW. Next, the 8 column-address bits (A0 - A7) are setup on the address inputs and clocked in when  $\overline{CAS}$  goes from HIGH to LOW.

For single port DRAMs, the  $\overline{OE}$  pin is a "don't care" when  $\overline{RAS}$  goes LOW. For the TPD RAM,  $\overline{TR}/\overline{OE}$  is used when  $\overline{RAS}$  goes LOW, to select between DRAM and TRANSFER cycles.  $\overline{TR}/\overline{OE}$  must be HIGH at the  $\overline{RAS}$  HIGH-to-LOW transition for all DRAM operations.

If  $\overline{ME}/\overline{WE}$  is HIGH when  $\overline{CAS}$  goes LOW, a DRAM READ operation is performed and the data from the memory cells selected will appear at the DQ1-DQ8 port. The  $\overline{TR}/\overline{OE}$  input must transition from HIGH-to-LOW sometime after  $\overline{RAS}$  falls to enable the DRAM output port.

For single port DRAMs,  $\overline{WE}$  is a "don't care" when  $\overline{RAS}$  goes LOW. For the TPD RAM,  $\overline{ME}/\overline{WE}$  is used, when  $\overline{RAS}$  goes LOW, to select between a MASKED WRITE cycle or a normal WRITE cycle. If  $\overline{ME}/\overline{WE}$  is LOW at the  $\overline{RAS}$  HIGH-to-LOW transition, a MASKED WRITE operation is selected. For any TPD RAM non-masked access cycle (READ or WRITE),  $\overline{ME}/\overline{WE}$  must be HIGH at the  $\overline{RAS}$  HIGH to LOW transition. If  $\overline{ME}/\overline{WE}$  is LOW when  $\overline{CAS}$  goes LOW, a DRAM WRITE operation is performed and the data present on the DQ1-DQ8 data port will be written into the selected memory cells.

The TPD RAM can perform all the normal DRAM cycles: READ, EARLY-WRITE, LATE-WRITE, READ-MODIFY-WRITE, FAST-PAGE-MODE READ, FAST-PAGE-MODE WRITE, and FAST-PAGE-MODE READ-MODIFY-WRITE. Refer to the AC timing parameters and diagrams in the data sheet for more details on these operations.

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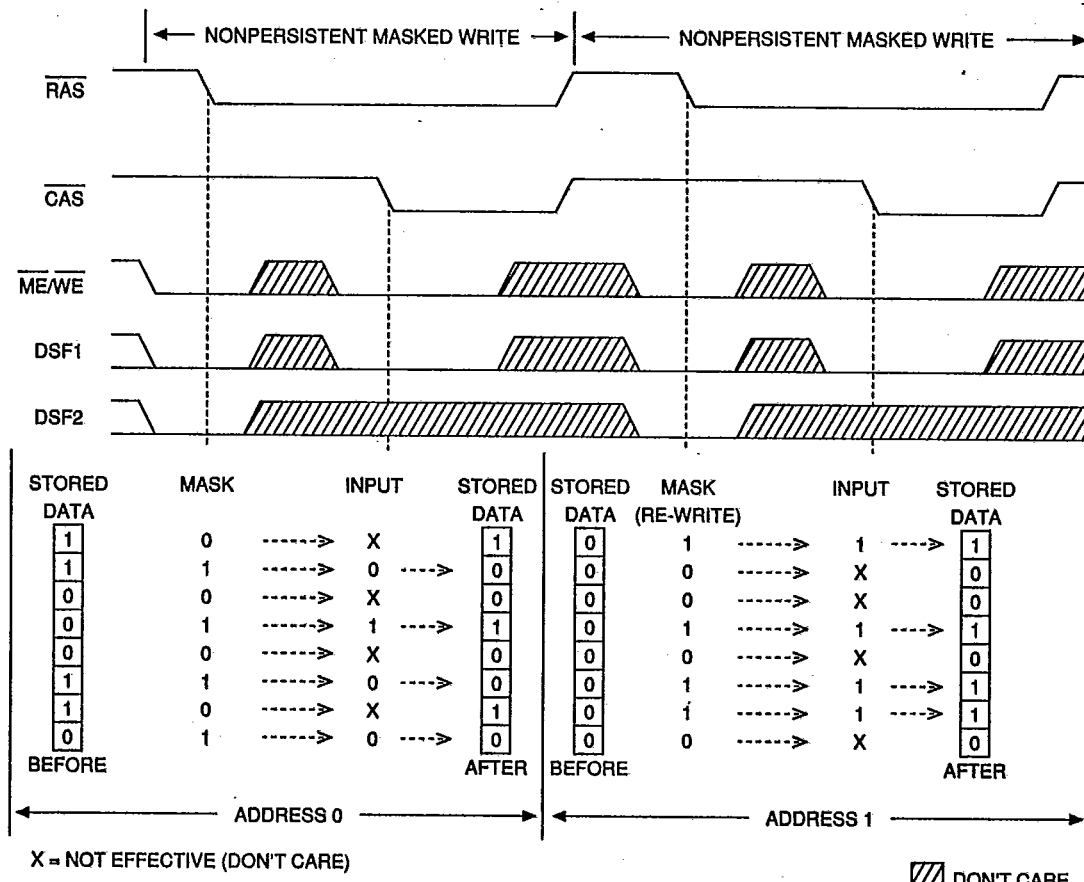


Figure 2  
NONPERSISTENT MASKED WRITE EXAMPLE

**NONPERSISTENT MASKED WRITE (RWNM)**

The MASKED WRITE feature eliminates the need to do a READ-MODIFY-WRITE cycle when changing only certain bits within an 8-bit word. The MT43C8128/9 supports two types of MASKED WRITE cycles, NONPERSISTENT MASKED WRITE and PERSISTENT MASKED WRITE.

If  $\overline{ME}/\overline{WE}$ , DSF1 and DSF2 are LOW at the  $\overline{RAS}$  HIGH-to-LOW transition, the data (mask data) present on the DQ1-DQ8 inputs will be written into the mask data register. The mask data acts as an individual write enable for each of the eight DQ1-DQ8 pins. If a LOW (logic 0) is written to a mask data register bit, the input port for that bit is disabled during the subsequent WRITE operation and no new data will be written to that DRAM cell location. A HIGH (logic 1) on a mask data register bit enables the input port and

allows normal WRITE operations to proceed. This convention is used for all masks on the MT43C8128/9. Note that  $\overline{CAS}$  is still HIGH. When  $\overline{CAS}$  goes LOW, the bits present on the DQ1-DQ8 inputs will be either written to the DRAM (if the mask data bit was HIGH) or ignored (if the mask data bit was LOW). The DRAM contents that correspond to the masked bits will not be changed during the WRITE cycle. When using NONPERSISTENT MASKED WRITE, the data present on the DQ inputs is loaded into the mask data register at every falling edge of  $\overline{RAS}$ . FAST PAGE MODE may be used in tandem with NONPERSISTENT MASKED WRITE to write several column locations using the same mask during one  $\overline{RAS}$  cycle. An example of NONPERSISTENT MASKED WRITE cycle is shown in Figure 2.



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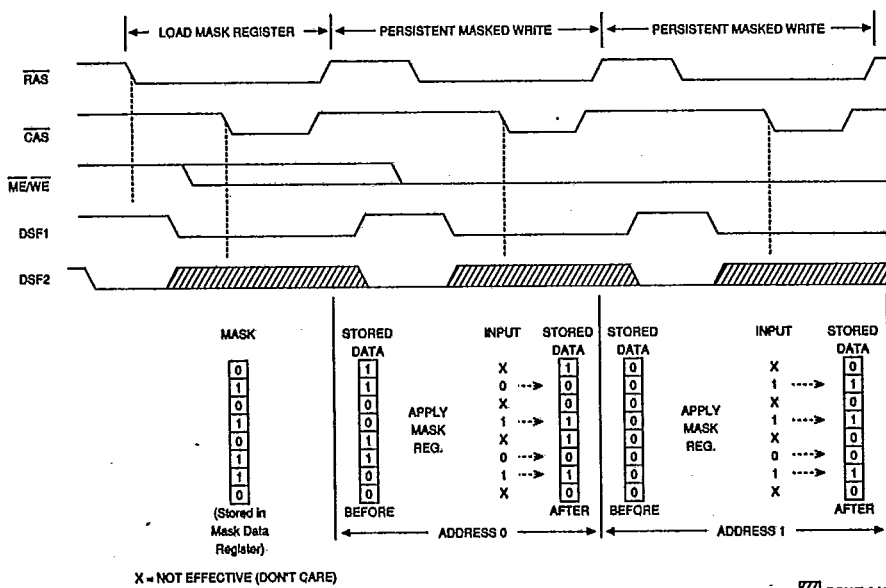


Figure 3  
PERSISTENT MASKED WRITE EXAMPLE

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**PERSISTENT MASKED WRITE (RWOM)**

The PERSISTENT MASKED WRITE feature eliminates the need to rewrite the mask data before each MASKED WRITE cycle if the same mask data is being used repeatedly. To initiate a PERSISTENT MASKED WRITE, a LOAD MASK REGISTER cycle is performed by taking  $\overline{ME}/\overline{WE}$  and DSF1 HIGH, and DSF2 LOW when  $\overline{RAS}$  goes LOW. The mask data is loaded into the internal register when  $\overline{CAS}$  goes LOW, provided DSF1 is LOW (see the LOAD MASK REGISTER description).

Mask data may also be loaded into the mask register by simply performing a NONPERSISTENT MASKED WRITE before the PERSISTENT MASKED WRITE cycles.

PERSISTENT MASKED WRITE cycles may then be performed by taking  $\overline{ME}/\overline{WE}$  and DSF2 LOW and DSF1 HIGH when  $\overline{RAS}$  goes LOW. The contents of the mask data register will then be used as the mask data for the DRAM inputs. Unlike the NONPERSISTENT MASKED WRITE cycle, the data present at the DQ inputs is not loaded into the mask register when  $\overline{RAS}$  falls. Another PERSISTENT MASKED WRITE cycle may be performed without reloading the register. Figure 3 shows the LOAD MASK REGISTER and PERSISTENT MASKED WRITE cycle operations. The LOAD MASK REGISTER and PERSISTENT MASKED WRITE cycles allow systems that cannot output data at  $\overline{RAS}$  time to perform MASKED WRITE cycles. PERSISTENT MASKED WRITE can also operate in FAST PAGE MODE.

**BLOCK WRITE (BW)**

If DSF1 is HIGH when  $\overline{CAS}$  goes LOW, the MT43C8128/9 will perform a BLOCK WRITE cycle ( $\overline{WE}$  = "don't care") instead of a normal WRITE cycle. In BLOCK WRITE cycles, the contents of the color register (instead of the DQ inputs) are directly written to four adjacent column locations (see Figure 4). A total of 32 bits will be written simultaneously, improving the normal DRAM fill rate by four times. The color register must be loaded prior to beginning BLOCK WRITE cycles (see LOAD COLOR REGISTER).

The row is addressed as in a normal DRAM WRITE cycle. However, when  $\overline{CAS}$  goes LOW, only the A2-A7 inputs are used. A2-A7 specify the "block" (out of the 64 possible) of four adjacent column locations that will be accessed. When  $\overline{CAS}$  goes LOW, the DQ inputs are then used to determine which combination of the four column locations will be changed. DQ1 acts as a write enable for column location A0=0, A1=0; DQ2 controls column location A0=1, A1=0; DQ3 controls A0=0, A1=1; and DQ4 controls A0=1, A1=1. The write enable controls are active HIGH; a logic 1 enables and a logic 0 disables the WRITE function.



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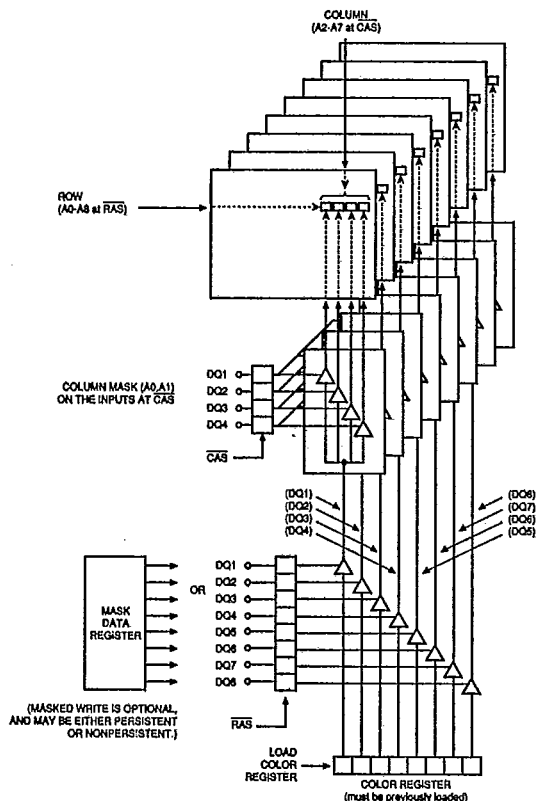


Figure 4  
BLOCK WRITE EXAMPLE

The contents of the color register will then be written to the column locations enabled. Each DQ location of the color register is written to the four column locations (or any of the four that are enabled) in the corresponding DQ bit plane. The DQ mask is not used in this mode.

**Note:** When performing a BLOCK WRITE,  $\overline{WE}$  is a "don't care". This means LATE-WRITES in the BW mode are not allowed.

**NONPERSISTENT MASKED BLOCK WRITE (BWNM)**

The MASKED WRITE functions can also be used during BLOCK WRITE cycles. NONPERSISTENT MASKED BLOCK WRITE operates exactly like the normal NONPERSISTENT MASKED WRITE except the mask is now applied to four column locations instead of just one column location.

Like NONPERSISTENT MASKED WRITE, the combination of  $\overline{ME}/(\overline{WE})$  LOW and DSF1 LOW when RAS goes LOW, initiates a NONPERSISTENT MASK cycle. The DSF

pin must be driven HIGH, when  $\overline{CAS}$  goes LOW, to perform a NONPERSISTENT MASKED BLOCK WRITE. By using both the column mask input and the MASKED WRITE function, any combination of the four bit planes may be masked and any combination of the eight column locations may be masked.

**PERSISTENT MASKED BLOCK WRITE (BWOM)**

This cycle is also performed exactly like the normal PERSISTENT MASKED WRITE except that DSF1 is HIGH when CAS goes LOW to indicate the BLOCK WRITE function. Both the mask data register and the color register must be loaded with the appropriate data prior to starting a PERSISTENT MASKED BLOCK WRITE.

**DRAM REGISTER OPERATIONS**

The MT43C8128/9 contains two 8-bit registers that are used as data registers for special functions. This section describes how to load these registers.

**LOAD MASK REGISTER (LMR)**

The LOAD MASK REGISTER operation and timing are identical to a normal WRITE cycle except that DSF1 is HIGH when RAS goes LOW. As shown in the Truth Table, the combination of  $\overline{TR}/(\overline{OE})$ ,  $\overline{ME}/(\overline{WE})$ , and DSF1 being HIGH when RAS goes LOW indicates the cycle is a REGISTER load cycle. DSF1 is used when  $\overline{CAS}$  goes LOW to select the register to be loaded, and must be LOW for a LOAD MASK REGISTER cycle. The data present on the DQ lines will then be written to the mask data register.

**Note:** For a normal DRAM WRITE cycle, the mask data register is disabled but not modified. The contents of mask data register will not be changed unless a NONPERSISTENT MASKED WRITE cycle or a LOAD MASK REGISTER cycle is performed.

The row address supplied will be refreshed, but it is not necessary to provide any particular row address. The column address inputs are ignored during a LOAD MASK REGISTER cycle.

The mask data register contents are used during PERSISTENT MASKED WRITE and PERSISTENT MASKED BLOCK WRITE cycles to selectively enable writes to the eight DQ planes.

**LOAD COLOR REGISTER (LCR)**

A LOAD COLOR REGISTER cycle is identical to the LOAD MASK REGISTER cycle except DSF1 is HIGH when  $\overline{CAS}$  goes LOW. The contents of the color register are retained until changed by another LOAD COLOR REGISTER cycle (or the part loses power) and are used as data inputs during BLOCK WRITE cycles.

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## TRANSFER OPERATIONS

This section describes transfer operations between the DRAM and either SAM. The direction of the transfer is specified with respect to the DRAM portion of the device. A write is referenced to the DRAM array and a read is referenced from the array.

**Note:** *The three ports of the TPDRAM are independent and asynchronous to one another. Any or all of the ports may be accessed simultaneously at the maximum allowable frequencies. The only time the ports are synchronized is during transfers to or from the DRAM and SAM portions of the device. A transfer involving a SAM does not affect access from the other SAM port. Both SAMs may be accessed during a DRAM/BMR transfer operation or any other DRAM access cycle other than a SAM transfer.*

TRANSFER operations are initiated when  $\overline{TR}/(\overline{OE})$  is LOW at the falling edge of  $\overline{RAS}$ . The state of STS when  $\overline{RAS}$  goes LOW indicates which SAM the TRANSFER will address. The state of  $(\overline{ME})/\overline{WE}$  when  $\overline{RAS}$  goes LOW indicates the direction of the TRANSFER. At the same time, DSF1 is used to select between normal TRANSFER cycles and SPLIT TRANSFER cycles and DSF2 is used to select between normal TRANSFER cycles and MASKED TRANSFER cycles. A TRANSFER cycle can be performed without dropping  $\overline{CAS}$ . In this case, the previously loaded Tap address will be used.

The MT43C8128/9 include a feature called BIT MASKED TRANSFER, which uses a third, 2048-bit data register to individually mask every bit involved in a TRANSFER operation. The BIT MASKED TRANSFER may be applied to either READ or WRITE TRANSFERS. The TRM pin is used to select between NORMAL and BIT MASKED TRANSFER (or BIT MASK REGISTER LOAD) cycles. The type of transfer operation is always selected on the falling edge of  $\overline{RAS}$ .

## NORMAL TRANSFERS

The MT43C8128/9 support all of the popular transfer cycles available on the 1 Meg video RAMs. Each of these is described in the following section.

### READ TRANSFER (RT)

A READ TRANSFER cycle is selected if  $\overline{ME}/(\overline{WE})$  is HIGH, and DSF1 and  $\overline{TR}/(\overline{OE})$  are LOW when  $\overline{RAS}$  goes LOW. When  $\overline{RAS}$  goes LOW, the READ TRANSFER is to SAMa if STS = LOW, or to SAMb if STS = HIGH. The row address bits indicate the eight 256-bit DRAM rows that are to be transferred to the eight SAM data registers. The column address bits indicate the start address (or Tap point)

of the next serial output cycle from the designated SAM data registers. QSF indicates the SAM half being accessed: LOW if the lower half; HIGH if the upper. Performing a READ TRANSFER cycle sets the direction of the selected SAMs I/O buffers to the output mode.

To complete a REAL-TIME READ-TRANSFER,  $\overline{TR}/(\overline{OE})$  is taken HIGH while  $\overline{RAS}$  and  $\overline{CAS}$  are LOW. In order to synchronize the REAL-TIME READ-TRANSFER to the serial clock, the rising edge of  $\overline{TR}/(\overline{OE})$  must occur between the rising edges of successive clocks on the SC input (refer to the AC timing diagrams). A "regular" READ TRANSFER is not synchronized with the SC pin of the addressed SAM. This type of RT is performed when  $\overline{TR}/(\overline{OE})$  is taken HIGH "early," without regard to the falling edge of  $\overline{CAS}$ . The transfer will be completed internally by the device. The first serial clock must meet the tRSD, tCSD and tASD delays. (see READ TRANSFER AC timing diagram). The 2048 bits of DRAM data are then written into the SAM data registers, and the selected SAM's Tap address that was stored in the internal, 8-bit Tap address register is loaded into the address counter. If  $\overline{SE}$  for the SAM selected ( $\overline{SEa}$  for SAMa) is LOW, the first bits of the new row data will appear at the serial outputs with the next SC clock pulse.  $\overline{SE}$  enables the serial outputs, and may be either HIGH or LOW during this operation.

### SPLIT READ TRANSFER (SRT)

The SPLIT READ TRANSFER cycle eliminates the critical transfer timing required to maintain a continuous serial output data stream (the "full" READ TRANSFER cycle has to occur immediately after the final bit of "old data," and before the first bit of "new data" is clocked out of the SAM port).

When using the SPLIT TRANSFER mode, the SAM is divided into an upper half and a lower half. While data is being serially read from one half of the SAM, new DRAM data may be transferred to the other half. The transfer can occur at any time while the other half is sending data and need not be synchronized with the SC clock.

The  $\overline{TR}/(\overline{OE})$  timing is relaxed for SRT cycles. The rising edge of  $\overline{TR}/(\overline{OE})$  is not used to complete the TRANSFER cycle and therefore is independent of the rising edges of  $\overline{RAS}$  and  $\overline{CAS}$ . The transfer timing is generated internally for SPLIT TRANSFER cycles.

SPLIT TRANSFERS do not change the SAM I/O direction. A normal (nonsplit) READ TRANSFER cycle must precede any sequence of SRT cycles to put the SAM I/O in the output mode and provide the initial SAM Tap address (which half). Then an SRT may be initiated by taking DSF1 HIGH and selecting the desired SAM (using STS) when  $\overline{RAS}$  goes LOW during the TRANSFER cycle. As in nonsplit transfers, the row address is used to specify the DRAM row to be transferred. When an SRT cycle is initiated, the half of

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the SAM not actively being accessed will be the half that receives the transfer. When  $\overline{CAS}$  falls, address pins A0-A6 determine the Tap address for the SAM-half selected; A7 = "don't care." If  $\overline{CAS}$  does not fall, the previously loaded Tap address will be reused and the TRANSFER will be to the idle half.

Figure 5 shows a typical SRT initiation sequence. The normal READ TRANSFER is first performed, followed by an SRT of the same row to the upper half of the SAM. The purpose of the SRT from the same row is to initiate the split SAM operating mode and load the Tap address for the upper half of the SAM. For the MT43C8128, serial access continues and when the SAM address counter reaches 127 ("A7"=1, A0-A6=0), the QSF output for that SAM goes HIGH and the Tap address for the upper half is automatically loaded. Since the serial access has now switched to the upper half of the SAM, new data may now be transferred to the lower half. This sequence of waiting for the state of QSF to change and then transferring new data to the SAM half that is not being accessed may now be repeated. For ex-

ample, the next step in Figure 5 would be to wait until QSF went LOW (indicating that row-1 data is shifting out the lower SAM) and then transferring the upper half of row 1 to the upper SAM.  $\overline{CAS}$  is used to load the Tap address. If  $\overline{CAS}$  does not fall, the last Tap address load for the addressed SAM will be reused.

The split SAM operation is slightly different for the MT43C8129. Instead of having a QSF, this device has a Split SAM Special Function (SSF) input. With this input the serial access may be switched at will from one half of the SAM to the other. In other words, the address count may be stopped on the current half and the Tap address of the next half may be loaded, without waiting for the maximum address count of the current half (127; lower, 255; upper). If no SSF pulse is applied, the Tap address of the next half will be automatically loaded when the maximum count of the current SAM-half is reached. QSF = 0 when the Lower SAM (bits 0-255) is being accessed. QSF = 1 when the Upper SAM (bits 256-511) is being accessed.

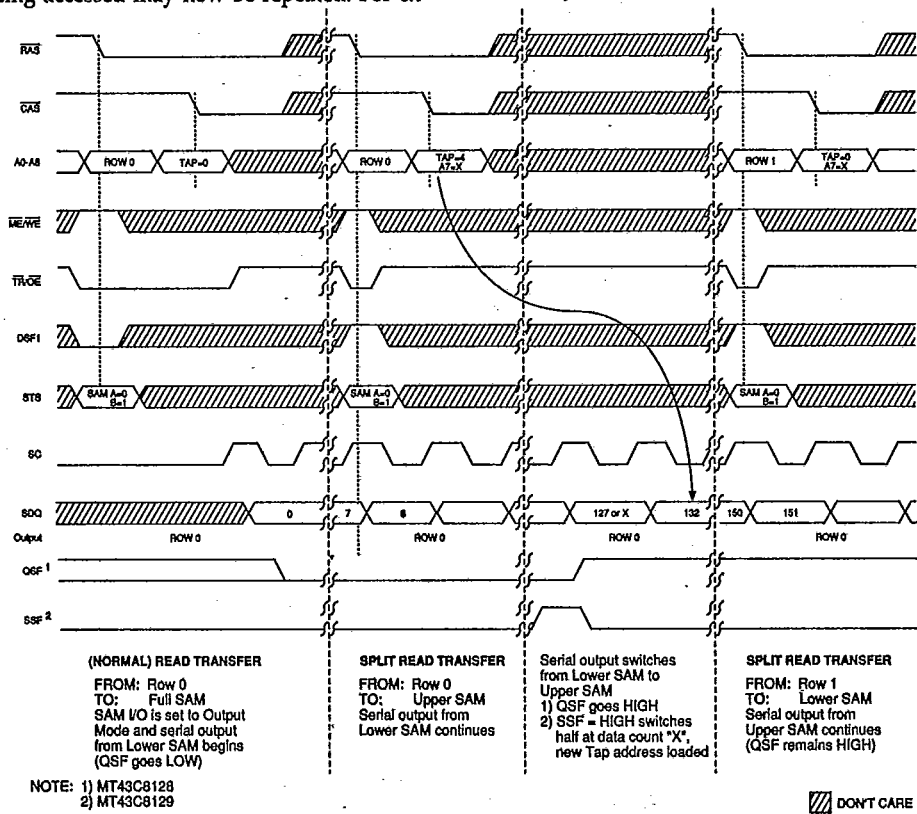


Figure 5  
TYPICAL SPLIT READ TRANSFER INITIATION SEQUENCE

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**WRITE TRANSFER (WT)**

The operation of the WRITE TRANSFER is identical to the READ TRANSFER described previously, except (ME)/WE and SE must be LOW when RAS goes LOW. The DSF2 input is used to select between the WT and DQ MASKED WRITE TRANSFER cycles, and must be LOW for the WT cycle. The STS pin is also taken LOW or HIGH to select SAMa or SAMb, respectively, when RAS goes LOW. The row address indicates the DRAM row to which the SAM data register will be written, and the Tap address indicates the starting address of the next SERIAL INPUT cycle for the SAM data registers. QSF indicates the SAM half being accessed; LOW if the lower half, HIGH if the upper. Performing a WT sets the direction of the SAM I/O buffers to the input mode.

**PSEUDO WRITE TRANSFER (PWT)**

The PSEUDO WRITE TRANSFER cycle can be used to change the direction of a SAM port from output to input without disturbing the DRAM data in the selected row. A PSEUDO WRITE TRANSFER cycle is a WRITE TRANSFER cycle with the SE of the appropriate SAM held HIGH instead of LOW. The addressed row will be refreshed. A DQ MASKED WRITE TRANSFER (with all bits masked) is an alternate method for changing the direction of the SAM port without disturbing the addressed row data.

**DQ MASKED WRITE TRANSFER (DMWT)**

The data being transferred from either SAM to the DRAM may be masked by performing a DQ MASKED WRITE TRANSFER cycle. The transfer of data may be selectively enabled for each of the eight DQ planes (see Figure 6). The DMWT cycle is identical to the WRITE TRANSFER cycle except DSF2 is HIGH and mask data must be on the DQ inputs at the falling edge of RAS.

The complete SAM register will be transferred to the selected row in each DQ plane if the mask data input is HIGH, and the SAM register will not be transferred if the mask data input for that DQ plane is LOW. DRAM data is not disturbed in masked DQ planes.

**SPLIT WRITE TRANSFER (SWT)**

The SPLIT WRITE TRANSFER feature makes it possible to input and transfer uninterrupted bit streams. Figure 7 shows a typical initiation sequence for SWT cycles.

Like the SRT, the SPLIT WRITE TRANSFER cycle does not change the state of the SAM I/O buffers. A normal, DQ MASKED or PSEUDO WRITE TRANSFER cycle is required to set the Tap address and set the SAM I/O direction to input mode.

After the WT, a SWT is performed to enter the split SAM operating mode. This sets the Tap for the next half of the SAM. The addressed half of the SAM is immediately trans-

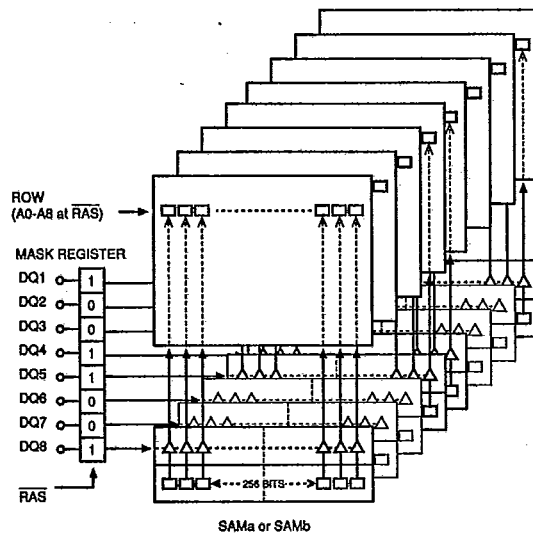


Figure 6  
DQ MASKED WRITE TRANSFER

ferred to the first destination row. This half of the SAM may not yet contain valid data. However, another SWT to the same row will normally occur after this is loaded, so the initial invalid data will be overwritten. Another approach would be to initiate an SWT addressed to any DRAM row, but mask (disable) all eight of the DQ planes. This method can be used to initiate the SWT sequence without disturbing any DRAM data.

Write mask data must be supplied to the DQ inputs during every SWT cycle at RAS time. The mask data acts as an individual write enable for each of the eight DRAM DQ planes. For example, the DQ1 MASKED WRITE bit enables or disables the transfer of the SAMSDQ1 register to the DQ1 plane of the DRAM row selected (see the DQ MASKED WRITE TRANSFER description). As in all other MASKED WRITE operations, a HIGH enables the WRITE TRANSFER and a LOW disables the WRITE TRANSFER. As with SPLIT READ TRANSFER, the half of the SAM not receiving data will be the half transferred and the Tap address (A0-A6) for the other half is loaded when CAS falls (A7 is a "don't care"). If CAS does not fall, the previously loaded Tap address, A0-A6, will be reused. The TRANSFER will be to the idle half. When the serial clock crosses the half-SAM boundary, the new Tap address for that half is automatically loaded.

The QSFa and QSFb outputs (MT43C8128) indicate which half of SAMa or SAMb, respectively, is currently accepting data. After QSF goes HIGH, indicating that serial input has now switched to the upper SAM, the contents of the lower

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half of the SAM may be transferred to any DRAM row. The cycle of checking for a change in QSF and then transferring the half of the SAM just filled may now be repeated. The next step on Figure 7 is to wait for QSF to go LOW and then SWT the contents of the upper half of the SAM to row 0. If the terminal count of the SAM half is reached before an SWT is performed for the next half, the access will be repeated from the same half and previously loaded address (access will not move to the next half).

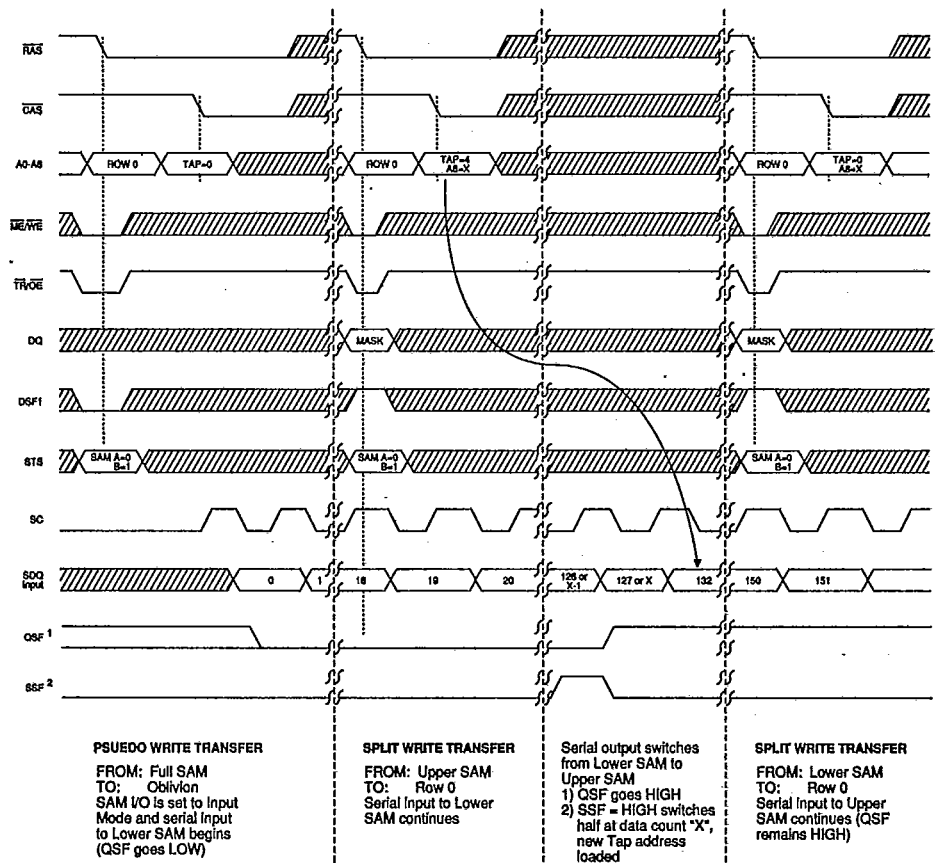
When operating the MT43C8129 in the SWT mode, the address pointer may be changed, at will, to the new Tap address of the next half when the final desired input data is clocked-in. When the final data is input, the SSF input is taken HIGH at the corresponding rising edge of SC. The next SC rising edge will input data into the Tap location of the next half of the SAM. If SSF is not applied, the Tap

address will be automatically loaded when the maximum Tap address count is reached for the current half (127 or 255). If SSF is HIGH at SC, before an SWT is performed for the next half, the access will jump to the old Tap address of the same half. Access will not proceed to the next half. If terminal count is reached before an SWT, the access will proceed as it does for the MT43C4257.

SERIAL INPUT and SERIAL OUTPUT

The control inputs for SERIAL INPUT and SERIAL OUTPUT are SCa,b and SEa,b. The rising edge of SC increments the serial address counter and provides access to the next SAM location. SE enables or disables the serial input/output buffers.

Serial output of the SAM contents will start at the serial start address that was loaded during the DRAM-TO-SAM



NOTE: 1) MT43C8128  
2) MT43C8129

DONT CARE

Figure 7  
TYPICAL SPLIT WRITE TRANSFER INITIATION SEQUENCE

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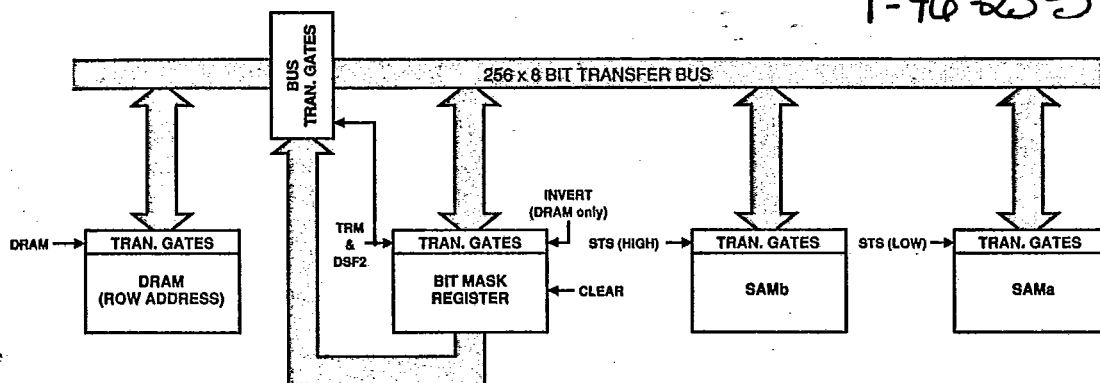


Figure 8  
BIT MASKED TRANSFER BLOCK DIAGRAM

TRANSFER cycle. The SC input increments the address counter and presents the contents of the next SAM location to the 8-bit port.  $\overline{SE}$  is used as an output enable during the SAM output operation. The serial address is automatically incremented with every SC LOW-to-HIGH transition, regardless of whether  $\overline{SE}$  is HIGH or LOW. For the MT43C8128, the address progresses through the SAM and will wrap around (after count 127 or 255) to the Tap address of the next half, for split modes. Address count will wrap around (after count 255) to Tap address 0 if in the "full" SAM modes. For the MT43C8129, the address count will wrap as it does for the MT43C8128 or it may be triggered, at will, to the next half by the SSF input (split SAM modes). If SSF is HIGH at a LOW-to-HIGH transition of SC, the Tap address of the next half will be loaded into the address pointer. The following LOW-to-HIGH transition of SC will clock data from the Tap address of the new half.

SC is also used to clock-in data when the device is in the serial input mode. As in the serial output operation, the contents of the serial address register (loaded when the serial input mode was enabled) will determine the serial address of the first 8-bit word written.  $\overline{SE}$  acts as a WRITE ENABLE for serial input data and must be LOW for valid serial input. If  $\overline{SE}$  = HIGH, the data inputs are disabled and the SAM contents will not be modified. The serial address counter is incremented with every LOW-to-HIGH transition of SC, regardless of the logic level on the  $\overline{SE}$  input.

### BIT MASKED TRANSFERS

This section describes transfers between the DRAM and either of the two SAMs using the BIT MASKED TRANSFER capability. Before performing these BIT MASKED TRANSFERS, the bit mask register must first be loaded with the

mask data. See the next section, BIT MASK REGISTER OPERATIONS, for instructions on how to load the Bit Mask Register (BMR).

The BMR is a 2048-bit register that individually controls each of the 2048 transfer gates on the internal 256 x 8 transfer bus (see Figure 8). These bus transfer gates reside between the DRAM array and the three data registers and are set to the "pass-thru" mode for nonmasked transfers. For BIT MASKED TRANSFERS, the data in the BMR is coupled to the control inputs of the bus transfer gates. A logic "1" in the BMR will select the pass-thru (unmasked) mode for the corresponding SAM data bit, while a logic "0" will select the masked mode for that bit.

BIT MASKED TRANSFERS may be incorporated when doing READ, WRITE, SPLIT READ and SPLIT WRITE TRANSFERS. The timing and control required for any particular BIT MASKED TRANSFER cycle is identical to the corresponding normal TRANSFER cycle, except that TRM and DSF2 are HIGH instead of LOW. BIT MASKED TRANSFERS between the DRAM and either of the two SAM registers are possible. Figure 9 illustrates the BIT MASKED TRANSFER functions.

### BIT MASKED READ TRANSFER (BMRT)

BIT MASKED READ TRANSFER can be used to transfer any combination of the 2048 bits contained in any DRAM row address to either of the two SAMs. The logic conditions and timing for the BMRT function are identical to the normal READ TRANSFER function except to select the BIT MASKED feature, TRM and DSF2 are HIGH. If a bit in the BMR is a logic "1", the bus connection between the corresponding DRAM bit and the selected SAM bit is enabled and the data at the destination (one of the SAMs for BMRT) will be changed to the source data (the DRAM row for BMRT).

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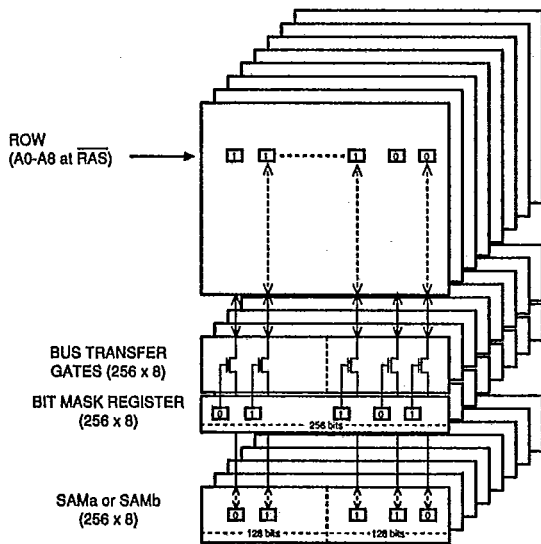


Figure 9

**BIT MASK TRANSFER BLOCK DIAGRAM****BIT MASKED SPLIT READ TRANSFER (BMSRT)**

The BIT MASKED SPLIT READ TRANSFER operation is identical to the normal SPLIT READ TRANSFER except that the bit mask (stored in the bit mask register) is applied to the transfer data by taking TRM and DSF2 HIGH when  $\overline{RAS}$  falls. The remaining control timing is identical to the requirements for a normal SPLIT READ TRANSFER.

**BIT MASKED WRITE TRANSFER (BMWT)**

Like WRITE TRANSFER, the BIT MASKED WRITE TRANSFER function may be used to transfer data to any DRAM row address from either of the two SAM registers. In this case, the SAM data will be masked by the contents of the bit mask register before the data is written to the DRAM.

**BIT MASKED SPLIT WRITE TRANSFER (BMSWT)**

Like the other BIT MASKED TRANSFER cycles, the BMSWT is nearly identical to the SPLIT WRITE TRANSFER, except TRM and DSF2 are HIGH when  $\overline{RAS}$  falls. Two masks are applied during a BMSWT operation. Each of the individual bits are masked by the bit mask register and each of the DQ planes are masked by the DQ inputs at  $\overline{RAS}$  time. If a DQ input is LOW at  $\overline{RAS}$  time, none of the 128 SAM bits for that DQ plane will be transferred to the DRAM row-half selected. If a DQ input is HIGH, the 128 SAM bits for that row-half will be masked by the corresponding 128 mask

register bits when written to the selected DRAM row-half. The remaining control timing is identical to the requirements for a normal SPLIT WRITE TRANSFER.

**BIT MASK REGISTER OPERATIONS**

This section describes how to transfer data to or from the Bit Mask Register (BMR) and how to clear the BMR's contents. Data may also be inverted when being transferred between the BMR and DRAM.

**BMR READ TRANSFER (BMR-RT)**

Any DRAM row may be transferred to the bit mask register by using the BMR READ TRANSFER function. When  $\overline{RAS}$  falls, TR/(OE) is LOW to select a transfer cycle. TRM is HIGH to indicate that the BMR is involved in the TRANSFER cycle, and DSF2 is LOW to indicate that the data is to be transferred to the BMR (as opposed to using the contents of the BMR as bit mask data). The remainder of the timing and control required is identical to a normal READ TRANSFER cycle. No Tap address is loaded in this TRANSFER.

Note that the SAM transfer select (STS) pin is used to select whether non-inverted (STS=LOW) or inverted (STS=HIGH) data is transferred to the bit mask register. For all transfers to or from the bit mask register, the state of the MKD pin when  $\overline{RAS}$  falls selects whether the Serial Mask Input (SMI) feature is enabled (see the Functional Truth Table). SMI is a special serial input mode that allows mask information to be clocked into the BMR at the same address location as the data clocked into SAMb (see the SMI mode description). MKD is LOW when  $\overline{RAS}$  falls to disable SMI or HIGH to enable SMI. After the transfer is completed the MKD pin then acts either as a mask data input to the BMR (SMI enabled) or is "don't care" (SMI disabled). The MKD input is tied to the 8 bit-planes, the data on the MKD pin is written to each bit-plane simultaneously.

**BMR INVERTED READ TRANSFER (BMR-IRT)**

If the STS pin is HIGH at  $\overline{RAS}$  time the DRAM data will be inverted before being written to the BMR. All 2048 bits involved in the transfer will be complemented. The functionality and logic levels for the other control inputs are identical to the BMR READ TRANSFER cycle. Note that MKD is still used to enable or disable the SMI mode. There is no added cycle time delay for either the BMR INVERTED READ or BMR INVERTED WRITE TRANSFER cycles.

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**BMR WRITE TRANSFER (BMR-WT)**

The contents of the BMR may also be transferred to any DRAM row by using the BMR WRITE TRANSFER cycle.  $(\overline{ME})/\overline{WE}$  and DSF2 are LOW and TRM is HIGH when  $\overline{RAS}$  falls, to select a write transfer from the BMR. The DQ inputs are used to input a DQ bit-plane mask when  $\overline{RAS}$  falls. This allows each of the four DQ planes to be write enabled or disabled during the BMR-WT. The MKD input is used to enable or disable the SMI mode. STS must be LOW at  $\overline{RAS}$  time to transfer non-inverted BMR data to the DRAM row selected.

**BMR INVERTED WRITE TRANSFER (BMR-IWT)**

As with the BMR INVERTED READ TRANSFER, the 2048 bits involved in the transfer may be inverted while being transferred. Taking STS HIGH at  $\overline{RAS}$  time will cause the BMR data to be inverted before it is stored in the selected DRAM row. The other control and DQ (mask) inputs are the same as the BMR-WT.

**SAM-TO-BMR TRANSFER (SAM-BMR)**

The contents of either SAM may be transferred to the BMR in the same manner that a DRAM row is transferred. In this case, DSF1 is HIGH to indicate that the SAM is the source of the data instead of the DRAM.  $(\overline{ME})/\overline{WE}$  is used to indicate the direction of the transfer and must be LOW, when  $\overline{RAS}$  falls, for a SAM-TO-BMR TRANSFER. STS is no longer used to select between normal and inverted data, it now indicates which SAM is involved in the transfer. Since a SAM-TO-BMR TRANSFER "reads" data from the SAM, the SAM will be placed into input mode by this transfer cycle. The MKD input is still used to determine if the SMI mode will be enabled after the transfer is completed. Since no DRAM access is involved, it is not necessary to provide any particular ROW address at  $\overline{RAS}$  time. However, whichever ROW address is present at  $\overline{RAS}$  time will be used as the address for a  $\overline{RAS}$ -ONLY REFRESH. Since a SAM is involved in the transfer, a new SAM starting Address (or Tap) will be loaded at  $\overline{CAS}$  time. This address will be loaded into the serial address counter of the SAM selected by STS at  $\overline{RAS}$  time.

**Note:** Any SAM/BMR TRANSFER will take the device out of the split SAM mode, if it was in that mode before the transfer.

**BMR-TO-SAM TRANSFER (BMR-SAM)**

The contents of the BMR may also be transferred to one of the SAM registers. The  $(\overline{ME})/\overline{WE}$  input is used to indicate the direction of the transfer and must be HIGH for a BMR-TO-SAM TRANSFER. STS is LOW to select SAMa or HIGH to select SAMb as the destination for the BMR data. The

remaining inputs and functionality are identical to the SAM-TO-BMR TRANSFER. Since a BMR-TO-SAM TRANSFER writes new data to the selected SAM register, the I/O for the SAM involved will be placed in the output mode and a new Tap address will be loaded when  $\overline{CAS}$  falls.

**CLEAR BIT MASK REGISTER (CLR-BMR)**

The entire contents of the BMR can be cleared (set all bit LOW) within a single transfer cycle by performing a CLEAR BMR cycle. Unlike the other cycles that access the BMR, TRM is LOW at  $\overline{RAS}$  time for the CLEAR BIT MASK REGISTER function.  $\overline{TR}/(\overline{OE})$  is LOW to indicate that the cycle is a transfer cycle (although there is really no data transfer involved). The CLR-BMR function is selected when  $\overline{ME}/(\overline{WE})$ , DSF1 and DSF2 are HIGH when  $\overline{RAS}$  falls.

When the BMR is cleared, all data will be masked when a BIT MASKED TRANSFER cycle is performed.

The BMR INVERTED WRITE and BMR WRITE TRANSFERS can be used with the CLR-BMR function to set or clear, respectively, any DRAM row. The CLR-BMR function is used to clear the BMR then the BMR TRANSFERS are performed to the addressed DRAM row.

The CLEAR BIT MASK REGISTER function is useful when using the SERIAL MASK INPUT mode. It is automatically performed (when in the SMI mode) when data is transferred from SAMb to the DRAM (see SERIAL MASK INPUT section).

**SERIAL MASK INPUT (SMI)**

Whenever the BMR is accessed, the MKD input is sensed and latched into the BMR control logic. If the MKD pin is LOW at  $\overline{RAS}$  time the Serial Mask Input (SMI) mode is disabled and the BMR may only be loaded via internal transfer cycles. If MKD is HIGH when  $\overline{RAS}$  falls, during a BMR access, then the BMR control logic enables the SMI mode and the BMR may be serially loaded via the MKD input.

When SMI is enabled, the MKD input is coupled to all eight of the bit mask register's DQ planes (see Figure 10). The SCb clock input and SAMb's address counter are used to input data to SAMb and the BMR. SEb will enable (LOW) or disable (HIGH) input data to SAMb and the BMR, the address count will increment regardless of the state of SEb.

The most common application of the SMI mode is to automatically load a transfer mask with the new data written to SAMb. To initialize the sequence, the BMR is cleared (CLR-BMR) with MKD=HIGH at  $\overline{RAS}$  time to enable the SMI mode. Then SAMb is prepared to accept input data by performing PSEUDO WRITE TRANSFER. The SAM starting address loaded will also apply to the BMR. For every address location that to which data is written in SAMb, the corresponding address location in the BMR will be written to the value present on MKD (all eight planes of the BMR will be written). After the input of data to SAMb

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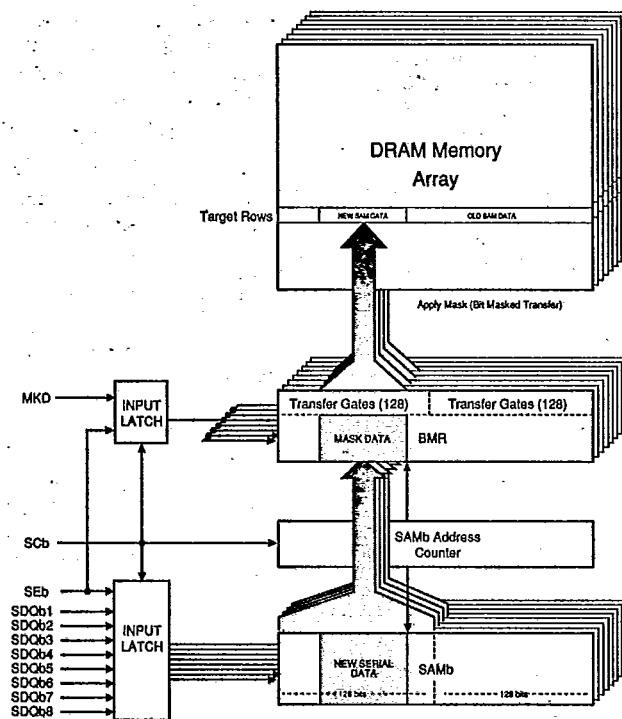


Figure 10  
SERIAL-MASK-INPUT MODE BLOCK DIAGRAM

is complete, a BIT MASKED WRITE TRANSFER may be done and only the unmasked data from SAMb will be transferred to the DRAM. The BMR will be cleared automatically after a BIT MASKED WRITE TRANSFER from SAMb, if the device is in the SMI mode. A BMSWT from SAMb will clear on half of the BMR. This allows a new mask to be loaded during the next fill of SAMb, without performing a CLR-BMR cycle. If data is to be masked during the BMWT, then MKD is held LOW when the corresponding SAMb data is written. If the data is to be written (unmasked) to the DRAM during the BMWT, then MKD is held HIGH when the corresponding SAMb location is written. The function of the MKD pin is dependent on the I/O direction of SAMb. MKD is an input only, if SMI is enabled and SAMb is in input mode. If SMI is enabled and SAMb is in output mode, the MKD input is a "don't care," no new data may be written to the BMR via MKD. MKD is also "don't care" if the SMI mode is disabled. Note that the mask data loaded via SAMb may also be applied to a SAMa TRANSFER cycle, if the mask hasn't been cleared by a SAMb TRANSFER or a CLR-BMR cycle. The BMR will not be cleared after a TRANSFER involving SAMa.

#### POWER UP INITIALIZATION

When Vcc is initially supplied or when refresh is interrupted for more than 8ms the device must be initialized.

After Vcc is at specified operating conditions, for 100µs (minimum), eight RAS cycles must be executed to initialize the dynamic memory array. When the device is initialized the DRAM I/O pins (DQs) are in a High-Z state, regardless of the state of (TR)/OE. The DRAM array will contain random data.

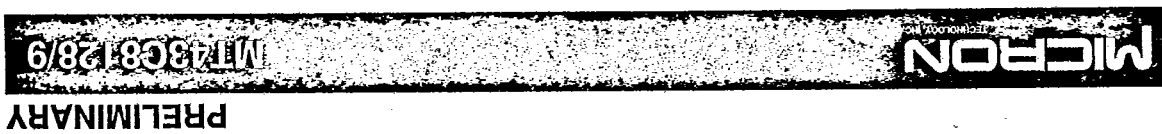
The SAM portion of the device is completely static and does not require an initialization cycle. Both SAM ports will power up in the serial input mode (WRITE TRANSFERS) and the SAM I/O pins (SDQ's) are in a High-Z state, regardless of the state of SE ab. Also, SPLIT TRANSFER and SMI modes are disabled. Both QSF (MT43C8128) outputs are in the High-Z state. Both SAMs as well as bit mask, color, and DRAM mask registers all contain random data after power-up.

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TRUTH TABLE 1

CODE	FUNCTION	RAS FALLING EDGE										CAS FALL		A0 - A8 <sup>2</sup>		DQ1 - DQ8 <sup>3</sup>		REGISTERS	
		CAS TR / OE	ME / WE <sup>0</sup>	DSF1	DSF2	SEa	SEb	TRIM	MKD	STS	DSF1	RAS	CAS AB-X	RAS	CAS <sup>4</sup>	RAS	CAS <sup>4</sup>	MASK	COLOR
<b>DRAM OPERATIONS</b>																			
CBR	CAS-BEFORE-RAS REFRESH	0	1 <sup>1</sup>	1 <sup>1</sup>	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
ROR	RAS ONLY REFRESH	1	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
ROW	NORMAL DRAM READ OR WRITE	1	1	0	0 <sup>1</sup>	X	X	X	X	X	X	X	X	X	X	X	X	X	X
RWNM	NONPERSISTENT (LOAD AND USE) MASKED WRITE TO DRAM	1	1	0	0 <sup>1</sup>	X	X	X	X	X	X	X	X	X	X	X	X	X	X
RWOM	PERSISTENT (USE REGISTER) MASKED WRITE TO DRAM	1	1	0	0 <sup>1</sup>	X	X	X	X	X	X	X	X	X	X	X	X	X	X
BW	BLOCK WRITE TO DRAM (NO DATA MASK)	1	1	0	0 <sup>1</sup>	X	X	X	X	X	X	X	X	X	X	X	X	X	X
BWNM	NONPERSISTENT (LOAD & USE) MASKED BLOCK WRITE TO DRAM	1	1	0	0 <sup>1</sup>	X	X	X	X	X	X	X	X	X	X	X	X	X	X
BWOM	PERSISTENT (USE MASK REGISTER) MASKED BLOCK WRITE TO DRAM	1	1	0	0 <sup>1</sup>	X	X	X	X	X	X	X	X	X	X	X	X	X	X
<b>REGISTER OPERATIONS</b>																			
LMR	LOAD MASK REGISTER	1	1	1	1	0 <sup>1</sup>	X	X	X	X	X	X	X	X	X <sup>2</sup>	X	X	WRITE MASK	LOAD
LCR	LOAD COLOR REGISTER	1	1	1	1	0 <sup>1</sup>	X	X	X	X	X	X	X	X	X <sup>2</sup>	X	X	COLOR DATA	LOAD
<b>TRANSFER OPERATIONS</b>																			
RT	READ TRANSFER (DRAM-TO-SAM TRANSFER)	1	0	1	0	0	X	0	X	0	X	0-SAMa 1-SAMb	X	ROW	TAP <sup>3</sup>	X	X	X	X
SRT <sup>3</sup>	SPLIT READ TRANSFER (SPLIT DRAM-TO-SAM TRANSFER)	1	0	1	1	0	X	0	X	0	X	0-SAMa 1-SAMb	X	ROW	TAP <sup>3</sup>	X	X	X	X
WT	WRITE TRANSFER (SAM-TO-DRAM TRANSFER)	1	0	0	0	0	0	0	0	0	X	0-SAMa 1-SAMb	X	ROW	TAP <sup>3</sup>	X	X	X	X
PWT	PSEUDO WRITE TRANSFER (SERIAL INPUT MODE ENABLE)	1	0	0	0	0	1	0	X	0	X	0-SAMa 1-SAMb	X	X <sup>2</sup>	TAP <sup>3</sup>	X	X	X	X
SWT <sup>3</sup>	SPLIT WRITE TRANSFER (SPLIT SAM-TO-DRAM TRANSFER WITH MASK)	1	0	0	1	0	X	0	X	0	X	0-SAMa 1-SAMb	X	ROW	TAP <sup>3</sup>	DQ MASK	DQ MASK	LOAD & USE	LOAD & USE
DMWT	DQ MASKED WRITE TRANSFER	1	0	0	0	1	X	0	X	0	X	0-SAMa 1-SAMb	X	ROW	TAP <sup>3</sup>	DQ MASK	DQ MASK	LOAD & USE	LOAD & USE



PRELIMINARY

(T-46-23-37)

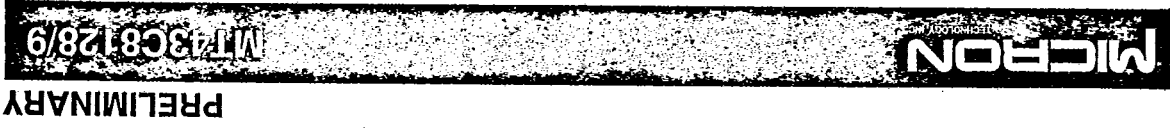
TRUTH TABLE 1

CODE	FUNCTION	RAS FALLING EDGE										CAS FALL		A0 - A8 <sup>2</sup>		DQ1 - DQ8 <sup>3</sup>		REGISTERS	
		CAS TR/DE	ME/WE <sup>1</sup>	DSF1	DSF2	SE2	SE1	TRM	MKD	STS	DSF1	DSF2	RAS	CAS AB-X	RAS	CAS	RAS	CAS	MASK
<b>BIT MASK REGISTER OPERATIONS</b>																			
BMR-RT	BMR READ TRANSFER (DRAM-BMR TRANSFER)	1	0	1	0	0	X	1	0 <sup>17</sup>	0	X	ROW	X	X	X	X	X	X	X
BMR-IRT	BMR READ TRANSFER (DRAM-INVERT-BMR TRANSFER)	1	0	1	0	0	X	1	0 <sup>17</sup>	1	X	ROW	X	X	X	X	X	X	X
BMR-WT	BMR WRITE TRANSFER (BMR-DRAM TRANSFER)	1	0	0	0	0	X	1	0 <sup>17</sup>	0	X	ROW	X	DQ MASK	X	X	X	X	X
BMR-IWT	BMR WRITE TRANSFER (BMR-INVERT-DRAM TRANSFER)	1	0	0	0	0	X	1	0 <sup>17</sup>	1	X	ROW	X	DQ MASK	X	X	X	X	X
SAM-BMR	SAM-BMR TRANSFER	1	0	0	1	0	X	1	0 <sup>17</sup>	0-SAMB 1-SAMB	X	X <sup>6</sup>	TAP <sup>8</sup>	X	X	X	X	X	X
BMR-SAM	BMR-SAM TRANSFER	1	0	1	1	0	X	1	0 <sup>17</sup>	0-SAMB 1-SAMB	X	X <sup>6</sup>	TAP <sup>8</sup>	X	X	X	X	X	X
CLR-BMR	CLEAR BIT MASK REGISTER (SETS BMR TO ALL "0s")	1	0	1	1	1	X	0	0 <sup>17</sup>	X	X <sup>6</sup>	X	X	X	X	X	X	X	X
<b>BIT MASKED TRANSFER OPERATIONS</b>																			
BMR-T	BIT MASKED READ TRANSFER (BMR-DRAM-SAM TRANSFER)	1	0	1	0	1	X	1	X	0-SAMB 1-SAMB	X	ROW	TAP <sup>8</sup>	X	X	X	X	X	X
BMR-TT	BIT MASKED SPLIT READ TRANSFER (BMR SPLIT DRAM-SAM TRANSFER)	1	0	1	1	1	X	1	X	0-SAMB 1-SAMB	X	ROW	TAP <sup>8</sup>	X	X	X	X	X	X
BMR-TT	BIT MASKED WRITE TRANSFER (BMR SAM-DRAM TRANSFER)	1	0	0	0	1	X	1	X <sup>6</sup>	0-SAMB 1-SAMB	X	ROW	TAP <sup>8</sup>	X	X	X	X	X	X
BMR-TT	BIT MASKED SPLIT WRITE TRANSFER (BMR SPLIT SAM-DRAM TRANSFER)	1	0	0	1	1	X	1	X <sup>6</sup>	0-SAMB 1-SAMB	X	ROW	TAP <sup>8</sup>	X	DQ MASK	X	LOAD & USE	X	X

NOTES: 1. 0 = LOW (V<sub>L</sub>), 1 = HIGH (V<sub>H</sub>), X = "don't care", - = "not applicable"

- These columns show what must be present on the A0-A8 inputs when RAS falls and A0-A7 when CAS falls.
- These columns show what must be present on the DQ1-DQ8 inputs when RAS falls and when CAS falls.
- On WRITE cycles (except BLOCK WRITE), the input data is latched at the falling edge of CAS or ME/WE, whichever is later. Similarly, on READ cycles, the output data is enabled on the falling edge of CAS or TR/DE, whichever is later.
- The ROW that is addressed will be refreshed, but no particular ROW address is required.
- Tap Address; this is the SAM location that the first SC cycle will access. For SPLIT TRANSFERS the half receiving the transfer is determined by the MSB of the internal address counter. The SAM half not currently being accessed will be the half receiving the transfer. Column address A7 is a "don't care" for SPLIT TRANSFERS.
- The Serial Mask Input mode (SMI) is enabled ("1") or disabled ("0") when the BMR is accessed (see BMR OPERATIONS). If SMI is enabled (MKD = "1"), mask data is serially clocked into the BMR with SCb and the BMR is automatically cleared after a BIT MASKED WRITE or BIT MASKED SPLIT WRITE TRANSFER cycle from SAMb. For BIT MASKED READ TRANSFERS to any SAM and BIT MASKED WRITE TRANSFERS from SAMa, the BMR is not cleared automatically.
- If the SMI mode is enabled, mask data is clocked into the BMR with SCb. A HIGH will allow data from the SAM address location to be written to the DRAM, a LOW will mask data to the DRAM during a BIT MASKED WRITE or BIT MASKED SPLIT WRITE TRANSFER.
- SPLIT TRANSFERS do not change SAM I/O direction.
- SAM I/O direction is a function of the state of ME/WE at RAS time. If ME/WE is LOW, then the selected SAM is an input; if ME/WE is HIGH then the SAM is an output.
- The MT43C8128/9 operates properly if this state is "X", but to allow for future functional enhancements it is recommended that they are driven as shown in the Truth Table.

MULTIPOINT DRAM





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**ABSOLUTE MAXIMUM RATINGS\***

Voltage on Vcc supply relative to Vss .....-1.0V to +7.0V  
 Operating Temperature, Ta(Ambient) .....0°C to +70°C  
 Storage Temperature (Ceramic) .....-65°C to +150°C  
 Storage Temperature (Plastic) .....-55°C to +150°C  
 Power Dissipation ..... 1W  
 Short Circuit Output Current .....50mA

\*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**RECOMMENDED DC OPERATING CONDITIONS**

(0°C ≤ T<sub>A</sub> ≤ 70°C)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V <sub>CC</sub>	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	V <sub>IH</sub>	2.4	V <sub>CC</sub> +1	V	1
Input Low (Logic 0) Voltage, All Inputs	V <sub>IL</sub>	-1.0	0.8	V	1

**DC ELECTRICAL CHARACTERISTICS**

(Notes 3, 4, 5) (0°C ≤ T<sub>A</sub> ≤ 70°C; V<sub>CC</sub> = 5.0V ± 10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
INPUT LEAKAGE CURRENT (any input (0V ≤ V <sub>IN</sub> ≤ V <sub>CC</sub> , all other pins not under test = 0V).	I <sub>L</sub>	-10	10	μA	
OUTPUT LEAKAGE CURRENT (Dout is disabled, 0V ≤ V <sub>OUT</sub> ≤ V <sub>CC</sub> ).	I <sub>OZ</sub>	-10	10	μA	
OUTPUT LEVELS					
Output High Voltage (I <sub>OUT</sub> = -2.5mA)	V <sub>OH</sub>	2.4		V	
Output Low Voltage (I <sub>OUT</sub> = 2.5mA)	V <sub>OL</sub>		0.4	V	1

**CAPACITANCE**

(T<sub>A</sub> = 25°C; V<sub>CC</sub> = 5.0V; f = 1MHz)

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A <sub>0</sub> -A <sub>8</sub> , TRM, MKD	C <sub>I1</sub>		5	pF	2
Input Capacitance: RAS, CAS, ME/WE, TR/OE, SCA,b, SEa,b, DSF1,2, STS SSFa,b	C <sub>I2</sub>		7	pF	2
Input/Output Capacitance: DQ, SDQa,b	C <sub>I/O</sub>		9	pF	2
Output Capacitance: QSFa,b	C <sub>O</sub>		9	pF	2

MULTIPORT DRAM

MICRON

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**CURRENT DRAIN, SAMA and SAMb IN STANDBY**  
 ( $0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$ ;  $V_{CC} = 5.0\text{V} \pm 10\%$ )

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PARAMETER/CONDITION	SYMBOL	MAX			UNITS	NOTES
		-8	-10	-12		
OPERATING CURRENT ( $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ = Cycling; $t_{RC} = t_{RC}(\text{MIN})$ )	lcc1	100	90	80	mA	3, 4
OPERATING CURRENT: FAST PAGE MODE ( $\overline{\text{RAS}} = V_{IL}$ , $\overline{\text{CAS}}$ = Cycling; $t_{PC} = t_{PC}(\text{MIN})$ )	lcc2	90	80	70	mA	3, 4
STANDBY CURRENT: TTL INPUT LEVELS Power supply standby current ( $\overline{\text{RAS}} = \overline{\text{CAS}} = V_{IH}$ , after 8 $\overline{\text{RAS}}$ cycles min)	lcc3	7	7	7	mA	
STANDBY CURRENT: CMOS INPUT LEVELS Power supply standby current ( $\overline{\text{RAS}} = \overline{\text{CAS}} = V_{CC} - 0.2\text{V}$ , after 8 $\overline{\text{RAS}}$ cycles min). All other inputs at $V_{CC} - 0.2\text{V}$ or $V_{SS} + 0.2\text{V}$	lcc4	1	1	1	mA	
REFRESH CURRENT: $\overline{\text{RAS}}$ -ONLY ( $\overline{\text{RAS}}$ = Cycling; $\overline{\text{CAS}} = V_{IH}$ )	lcc5	100	90	80	mA	3
REFRESH CURRENT: $\overline{\text{CAS}}$ -BEFORE- $\overline{\text{RAS}}$ ( $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ = Cycling)	lcc6	90	80	70	mA	3, 5
TRANSFER CURRENT: SAM/DRAM DATA TRANSFER	lcc7	110	100	90	mA	3

**CURRENT DRAIN, SAMA and SAMb ACTIVE**

 (Notes 3, 4) ( $0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$ ;  $V_{CC} = 5.0\text{V} \pm 10\%$ )

PARAMETER/CONDITION	SYMBOL	MAX			UNITS	NOTES
		-8	-10	-12		
OPERATING CURRENT ( $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ = Cycling; $t_{RC} = t_{RC}(\text{MIN})$ )	lcc8	180	170	160	mA	
OPERATING CURRENT: FAST PAGE MODE ( $\overline{\text{RAS}} = V_{IL}$ , $\overline{\text{CAS}}$ = Cycling; $t_{PC} = t_{PC}(\text{MIN})$ )	lcc9	160	150	140	mA	
STANDBY CURRENT: TTL INPUT LEVELS Power supply standby current ( $\overline{\text{RAS}} = \overline{\text{CAS}} = V_{IH}$ , after 8 $\overline{\text{RAS}}$ cycles min)	lcc10	85	85	85	mA	
STANDBY CURRENT: CMOS INPUT LEVELS Power supply standby current ( $\overline{\text{RAS}} = \overline{\text{CAS}} = V_{CC} - 0.2\text{V}$ , after 8 $\overline{\text{RAS}}$ cycles min). All other inputs at $V_{CC} - 0.2\text{V}$ or $V_{SS} + 0.2\text{V}$	lcc11	75	75	75	mA	
REFRESH CURRENT: $\overline{\text{RAS}}$ -ONLY ( $\overline{\text{RAS}}$ = Cycling; $\overline{\text{CAS}} = V_{IH}$ )	lcc12	180	170	160	mA	
REFRESH CURRENT: $\overline{\text{CAS}}$ -BEFORE- $\overline{\text{RAS}}$ ( $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ = Cycling)	lcc13	170	160	150	mA	5
TRANSFER CURRENT: SAM/DRAM DATA TRANSFER	lcc14	180	170	160	mA	



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DRAM TIMING PARAMETERS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T<sub>A</sub> ≤ +70°C; V<sub>CC</sub> = 5.0V ± 10%)

A.C. CHARACTERISTICS		-8		-10		-12		UNITS	NOTES
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX		
Random READ or WRITE cycle time	t <sub>RC</sub>	150		180		210		ns	
READ-MODIFY-WRITE cycle time	t <sub>RWC</sub>	205		235		280		ns	
FAST-PAGE-MODE READ or WRITE cycle time	t <sub>PC</sub>	45		55		65		ns	
FAST-PAGE-MODE READ-MODIFY-WRITE cycle time	t <sub>PRWC</sub>	100		110		140		ns	
Access time from RAS	t <sub>RAC</sub>		80		100		120	ns	14, 17
Access time from CAS	t <sub>CAC</sub>		20		25		30	ns	15
Access time from (TR)/OE	t <sub>OE</sub>		20		25		30	ns	
Access time from column address	t <sub>AA</sub>		40		50		60	ns	
Access time from CAS precharge	t <sub>CPA</sub>		45		55		65	ns	
RAS pulse width	t <sub>RAS</sub>	80	10,000	100	10,000	120	10,000	ns	
RAS pulse width (FAST PAGE MODE)	t <sub>RASP</sub>	80	100,000	100	100,000	120	100,000	ns	
RAS hold time	t <sub>RSH</sub>	20		25		30		ns	
RAS precharge time	t <sub>RP</sub>	60		70		80		ns	
CAS pulse width	t <sub>CAS</sub>	20	10,000	25	10,000	30	10,000	ns	
CAS hold time	t <sub>CSH</sub>	80		100		120		ns	
CAS precharge time	t <sub>CPN</sub>	15		15		20		ns	16
CAS precharge time (FAST PAGE MODE)	t <sub>CP</sub>	10		10		15		ns	
RAS to CAS delay time	t <sub>RCD</sub>	20	60	20	75	25	90	ns	17
CAS to RAS precharge time	t <sub>CRP</sub>	5		5		10		ns	
Row address setup time	t <sub>ASR</sub>	0		0		0		ns	
Row address hold time	t <sub>RAH</sub>	12		15		15		ns	
RAS to column address delay time	t <sub>RAD</sub>	17	40	20	50	25	60	ns	18
Column address setup time	t <sub>ASC</sub>	0		0		0		ns	
Column address hold time	t <sub>CAH</sub>	15		20		25		ns	
Column address hold time (referenced to RAS)	t <sub>AR</sub>	60		70		85		ns	
Column address to RAS lead time	t <sub>RAL</sub>	40		50		60		ns	
Read command setup time	t <sub>RCS</sub>	0		0		0		ns	
Read command hold time (referenced to CAS)	t <sub>RCH</sub>	0		0		0		ns	19
Read command hold time (referenced to RAS)	t <sub>RRH</sub>	0		0		0		ns	19
CAS to output in Low-Z	t <sub>CLZ</sub>	0		0		0		ns	
Output buffer turn-off delay	t <sub>OFF</sub>	0	20	0	20	0	30	ns	20
Output Disable	t <sub>OD</sub>	0	20	0	20	0	30	ns	
Output Disable hold time from start of write	t <sub>OEH</sub>		15		15		20	ns	
Output Enable to RAS delay	t <sub>ORD</sub>		0		0		0	ns	

MULTIPORT DRAM

PRELIMINARY

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## DRAM TIMING PARAMETERS (Continued)

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) ( $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ ;  $V_{CC} = 5.0\text{V} \pm 10\%$ )

A.C. CHARACTERISTICS		-8		-10		-12		UNITS	NOTES
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX		
Write command setup time	$t^{\text{WCS}}$	0		0		0		ns	21
Write command hold time	$t^{\text{WCH}}$	15		20		25		ns	
Write command hold time (referenced to RAS)	$t^{\text{WCR}}$	60		75		85		ns	
Write command pulse width	$t^{\text{WP}}$	15		15		20		ns	
Write command to RAS lead time	$t^{\text{RWL}}$	20		20		25		ns	
Write command to CAS lead time	$t^{\text{CWL}}$	20		20		25		ns	
Data-in setup time	$t^{\text{DS}}$	0		0		0		ns	22
Data-in hold time	$t^{\text{DH}}$	20		20		25		ns	22
Data-in hold time (referenced to RAS)	$t^{\text{DHR}}$	60		70		90		ns	
RAS to WE delay time	$t^{\text{RWD}}$	110		130		160		ns	21
Column address to WE delay time	$t^{\text{AWD}}$	70		80		100		ns	21
CAS to WE delay time	$t^{\text{CWD}}$	50		60		70		ns	21
Transition time (rise or fall)	$t^{\text{T}}$	3	50	3	50	3	50	ns	9, 10
Refresh period (512 cycles)	$t^{\text{REF}}$		8		8		8	ms	
RAS to CAS precharge time	$t^{\text{RPC}}$	0		0		0		ns	
CAS setup time (CAS-BEFORE-RAS refresh)	$t^{\text{CSR}}$	10		10		10		ns	5
CAS hold time (CAS-BEFORE-RAS refresh)	$t^{\text{CHR}}$	30		30		30		ns	5
ME/WE to RAS setup time	$t^{\text{WSR}}$	0		0		0		ns	
ME/WE to RAS hold time	$t^{\text{RWH}}$	12		15		15		ns	
Mask data to RAS setup time	$t^{\text{MS}}$	0		0		0		ns	
Mask data to RAS hold time	$t^{\text{MH}}$	12		15		15		ns	

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**TRANSFER AND MODE CONTROL TIMING PARAMETERS**  
**ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS**  
 (Notes 6, 7, 8, 9, 10) ( $0^{\circ}C \leq T_A \leq +70^{\circ}C$ ;  $V_{CC} = 5.0V \pm 10\%$ )

A.C. CHARACTERISTICS		-8		-10		-12		UNITS	NOTES
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX		
TRANSFER command to RAS <sup>1</sup> setup time	<sup>t</sup> TL <sub>S</sub>	0		0		0		ns	25
TRANSFER command to RAS <sup>1</sup> hold time	<sup>t</sup> TL <sub>H</sub>	12	10,000	15	10,000	15	10,000	ns	25
TRANSFER command to RAS <sup>1</sup> hold time (REAL-TIME READ TRANSFER only)	<sup>t</sup> R <sub>T</sub> H	70	10,000	80	10,000	90	10,000	ns	25
TRANSFER command to CAS <sup>1</sup> hold time (REAL-TIME READ TRANSFER only)	<sup>t</sup> C <sub>T</sub> H	20		25		30		ns	25
TRANSFER command to column address hold time (For REAL-TIME READ TRANSFER only)	<sup>t</sup> A <sub>T</sub> H	25		30		35		ns	25
TRANSFER command to SC lead time	<sup>t</sup> S <sub>L</sub>	5		5		5		ns	25
TRANSFER command to RAS HIGH lead time	<sup>t</sup> TR <sub>L</sub>	0		0		0		ns	25
TRANSFER command to RAS <sup>1</sup> delay time	<sup>t</sup> TR <sub>D</sub>	15		15		15		ns	25
TRANSFER command to CAS HIGH lead time	<sup>t</sup> T <sub>C</sub> L	0		0		0		ns	25
TRANSFER command to CAS <sup>1</sup> delay time	<sup>t</sup> T <sub>C</sub> D	15		15		15		ns	25
First SC edge to TRANSFER command delay time	<sup>t</sup> T <sub>S</sub> D	10		10		10		ns	25
RAS to first SC edge delay time	<sup>t</sup> R <sub>S</sub> D	80		95		105		ns	
CAS to first SC edge delay time	<sup>t</sup> C <sub>S</sub> D	25		30		35		ns	
Column address to first SC edge delay time	<sup>t</sup> A <sub>S</sub> D	50		60		65		ns	
Serial output buffer turn-off delay from RAS <sup>1</sup>	<sup>t</sup> S <sub>D</sub> Z	10	35	10	40	10	45	ns	
SC to RAS <sup>1</sup> setup time	<sup>t</sup> S <sub>R</sub> S	30		30		40		ns	
RAS to SC delay time	<sup>t</sup> S <sub>R</sub> D	20		25		30		ns	
Serial data input to SE <sup>1</sup> delay time	<sup>t</sup> S <sub>Z</sub> E	0		0		0		ns	
RAS to SD buffer turn-on time	<sup>t</sup> S <sub>R</sub> O	10		15		15		ns	
Serial data input delay from RAS <sup>1</sup>	<sup>t</sup> S <sub>D</sub> D	45		50		55		ns	
Serial data input to RAS <sup>1</sup> delay time	<sup>t</sup> S <sub>Z</sub> S	0		0		0		ns	
Serial Input Mode enable (SE) to RAS <sup>1</sup> setup time	<sup>t</sup> E <sub>S</sub> R	0		0		0		ns	
Serial Input Mode enable (SE) to RAS <sup>1</sup> hold time	<sup>t</sup> R <sub>E</sub> H	12		15		15		ns	
NONTRANSFER command to RAS <sup>1</sup> setup time	<sup>t</sup> Y <sub>S</sub>	0		0		0		ns	26
NONTRANSFER command to RAS <sup>1</sup> hold time	<sup>t</sup> Y <sub>H</sub>	12		15		15		ns	26
DSF, TRM, STS, MKD to RAS <sup>1</sup> setup time	<sup>t</sup> F <sub>S</sub> R	0		0		0		ns	
DSF, TRM, STS, MKD to RAS <sup>1</sup> hold time	<sup>t</sup> R <sub>F</sub> H	12		15		15		ns	
DSF to RAS <sup>1</sup> hold time	<sup>t</sup> F <sub>H</sub> R	60		65		70		ns	
DSF to CAS <sup>1</sup> setup time	<sup>t</sup> F <sub>S</sub> C	0		0		0		ns	
DSF to CAS <sup>1</sup> hold time	<sup>t</sup> C <sub>F</sub> H	15		20		20		ns	
SC to QSF delay time	<sup>t</sup> S <sub>Q</sub> D		35		40		45	ns	
RAS to QSF delay time	<sup>t</sup> R <sub>Q</sub> D		65		85		105	ns	
CAS to QSF delay time	<sup>t</sup> C <sub>Q</sub> D		35		40		45	ns	
TR/OE to QSF delay time	<sup>t</sup> T <sub>Q</sub> D		25		30		35	ns	
SPLIT TRANSFER setup time	<sup>t</sup> S <sub>T</sub> S	30		35		40		ns	
SPLIT TRANSFER hold time	<sup>t</sup> S <sub>T</sub> H	30		35		40		ns	
Split SAM setup time to RAS <sup>1</sup> from last SC	<sup>t</sup> S <sub>C</sub> R	30		35		40		ns	29
Split SAM hold time to RAS <sup>1</sup> from first SC	<sup>t</sup> S <sub>C</sub> R	30		35		40		ns	29

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## SAM TIMING PARAMETERS

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes 6, 7, 8, 9, 10) ( $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ ;  $V_{CC} = 5.0\text{V} \pm 10\%$ )

A.C. CHARACTERISTICS		-8		-10		-12		UNITS	NOTES
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX		
Serial clock cycle time	$t_{SC}$	25		30		35		ns	
Access time from SC	$t_{SAC}$		25		30		35	ns	24
SC precharge time (SC LOW time)	$t_{SP}$	10		10		12		ns	
SC pulse width (SC HIGH time)	$t_{SAS}$	5		10		12		ns	
Access time from $\overline{SE}$	$t_{SEA}$		15		20		30	ns	24
$\overline{SE}$ precharge time	$t_{SEP}$	10		15		15		ns	
$\overline{SE}$ pulse width	$t_{SE}$	10		15		15		ns	
Serial data out hold time after SC HIGH	$t_{SOH}$	5		5		5		ns	24
Serial output buffer turn-off delay from $\overline{SE}$	$t_{SEZ}$	0	12	0	15	0	25	ns	24
Serial data in setup time	$t_{SDS}$	0		0		0		ns	24
Serial data in hold time	$t_{SDH}$	10		15		20		ns	24
SERIAL INPUT (Write) Enable setup time	$t_{SWS}$	0		0		0		ns	
SERIAL INPUT (Write) Enable hold time	$t_{SWH}$	15		15		25		ns	
SERIAL INPUT (Write) Disable setup time	$t_{SWIS}$	0		0		0		ns	
SERIAL INPUT (Write) Disable hold time	$t_{SWIH}$	15		15		25		ns	
SSF to SC setup time	$t_{SFS}$	0		0		0		ns	29
SSF to SC hold time	$t_{SFH}$	15		20		20		ns	29
SSF LOW to SC HIGH delay	$t_{SFD}$	0		0		0		ns	29

MULTIPORT DRAM

MICRON  
TECHNOLOGY

MT43C8128/9

T-46-23-37

## NOTES

1. All voltages referenced to Vss.
2. This parameter is sampled. Capacitance is calculated from the equation  $C = \frac{I \Delta t}{\Delta V}$  with  $\Delta V = 3V$  and  $V_{CC} = 5V$ .
3. Icc is dependent on cycle rates.
4. Icc is dependent on output loading. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ( $0^{\circ}C \leq T_A \leq 70^{\circ}C$ ) is assured.
7. An initial pause of 100 $\mu$ s is required after power-up followed by any 8  $\overline{RAS}$  cycles before proper device operation is assured. The 8  $\overline{RAS}$  cycle wake-up should be repeated any time the 8ms refresh requirement is exceeded.
8. AC characteristics assume  $t_T = 5ns$ .
9.  $V_{IH}$  MIN and  $V_{IL}$  MAX are reference levels for measuring timing of input signals. Transition times are measured between  $V_{IH}$  and  $V_{IL}$  (or between  $V_{IL}$  and  $V_{IH}$ ).
10. In addition to meeting the transition rate specification, all input signals must transit between  $V_{IH}$  and  $V_{IL}$  (or between  $V_{IL}$  and  $V_{IH}$ ) in a monotonic manner.
11. If  $\overline{CAS} = V_{IH}$ , DRAM data outputs (DQ1-DQ8) is high impedance.
12. If  $\overline{CAS} = V_{IL}$ , DRAM data outputs (DQ1-DQ8) may contain data from the last valid READ cycle.
13. DRAM output timing measured with a load equivalent to 1 TTL gate and 50pF. Output reference levels:  $V_{OH} = 2.0V$ ;  $V_{OL} = 0.8V$ .
14. Assumes that  $t_{RCD} < t_{RCD} (MAX)$ . If  $t_{RCD}$  is greater than the maximum recommended value shown in this table,  $t_{RAC}$  will increase by the amount that  $t_{RCD}$  exceeds the value shown.
15. Assumes that  $t_{RCD} \geq t_{RCD} (MAX)$ .
16. If  $\overline{CAS}$  is LOW at the falling edge of  $\overline{RAS}$ , DQ will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer,  $\overline{CAS}$  must be pulsed HIGH for  $t_{CPN}$ .
17. Operation within the  $t_{RCD} (MAX)$  limit ensures that  $t_{RAC} (MAX)$  can be met.  $t_{RCD} (MAX)$  is specified as a reference point only; if  $t_{RCD}$  is greater than the specified  $t_{RCD} (MAX)$  limit, then access time is controlled exclusively by  $t_{CAC}$ .
18. Operation within the  $t_{RAD} (MAX)$  limit ensures that  $t_{RCD} (MAX)$  can be met.  $t_{RAD} (MAX)$  is specified as a reference point only; if  $t_{RAD}$  is greater than the specified  $t_{RAD} (MAX)$  limit, then access time is controlled exclusively by  $t_{AA}$ .
19. Either  $t_{RCH}$  or  $t_{RRH}$  must be satisfied for a READ cycle.
20.  $t_{OFF} (MAX)$  defines the time at which the output achieves the open circuit condition and is not referenced to  $V_{OH}$  or  $V_{OL}$ .
21.  $t_{WCS}$ ,  $t_{RWD}$ ,  $t_{AWD}$  and  $t_{CWD}$  are restrictive operating parameters in LATE-WRITE, READ-WRITE and READ-MODIFY-WRITE cycles only. If  $t_{WCS} \geq t_{WCS} (MIN)$ , the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle, regardless of  $\overline{TR}/\overline{OE}$ . If  $t_{WCS} \leq t_{WCS} (MIN)$ , the cycle is a LATE-WRITE and  $\overline{TR}/\overline{OE}$  must control the output buffers during the write to avoid data contention. If  $t_{RWD} \geq t_{RWD} (MIN)$ ,  $t_{AWD} \geq t_{AWD} (MIN)$  and  $t_{CWD} \geq t_{CWD} (MIN)$ , the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met, the state of the output buffers (at access time and until  $\overline{CAS}$  goes back to  $V_{IH}$ ) is indeterminate but the WRITE will be valid, if  $t_{OD}$  and  $t_{OEH}$  are met. See the LATE-WRITE AC Timing diagram.
22. These parameters are referenced to  $\overline{CAS}$  leading edge in early WRITE cycles and  $\overline{ME}/\overline{WE}$  leading edge in late WRITE or READ-WRITE cycles.
23. During a READ cycle, if  $\overline{TR}/\overline{OE}$  is LOW then taken HIGH, DQ goes open. The DQs will go open with  $\overline{OE}$  or  $\overline{CAS}$ , whichever goes HIGH first.
24. SAM output timing is measured with a load equivalent to 1 TTL gate and 30pF. Output reference levels:  $V_{OH} = 2.0V$ ;  $V_{OL} = 0.8V$ .
25. TRANSFER command means that  $\overline{TR}/\overline{OE}$  is LOW when  $\overline{RAS}$  goes LOW.
26. NON-TRANSFER command means that  $\overline{TR}/\overline{OE}$  is HIGH when  $\overline{RAS}$  goes LOW.
27. LATE-WRITE and READ-MODIFY-WRITE cycles must have  $t_{OD}$  and  $t_{OEH}$  met ( $\overline{OE}$  HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide previously read data if  $\overline{CAS}$  remains LOW and  $\overline{OE}$  is taken LOW after  $t_{OEH}$  is met. If  $\overline{CAS}$  goes HIGH prior to  $\overline{OE}$  going back LOW, the DQs will remain open.
28. Applies to the MT43C8128 only.
29. Applies to the MT43C8129 only.

MULTI-PORT DRAM

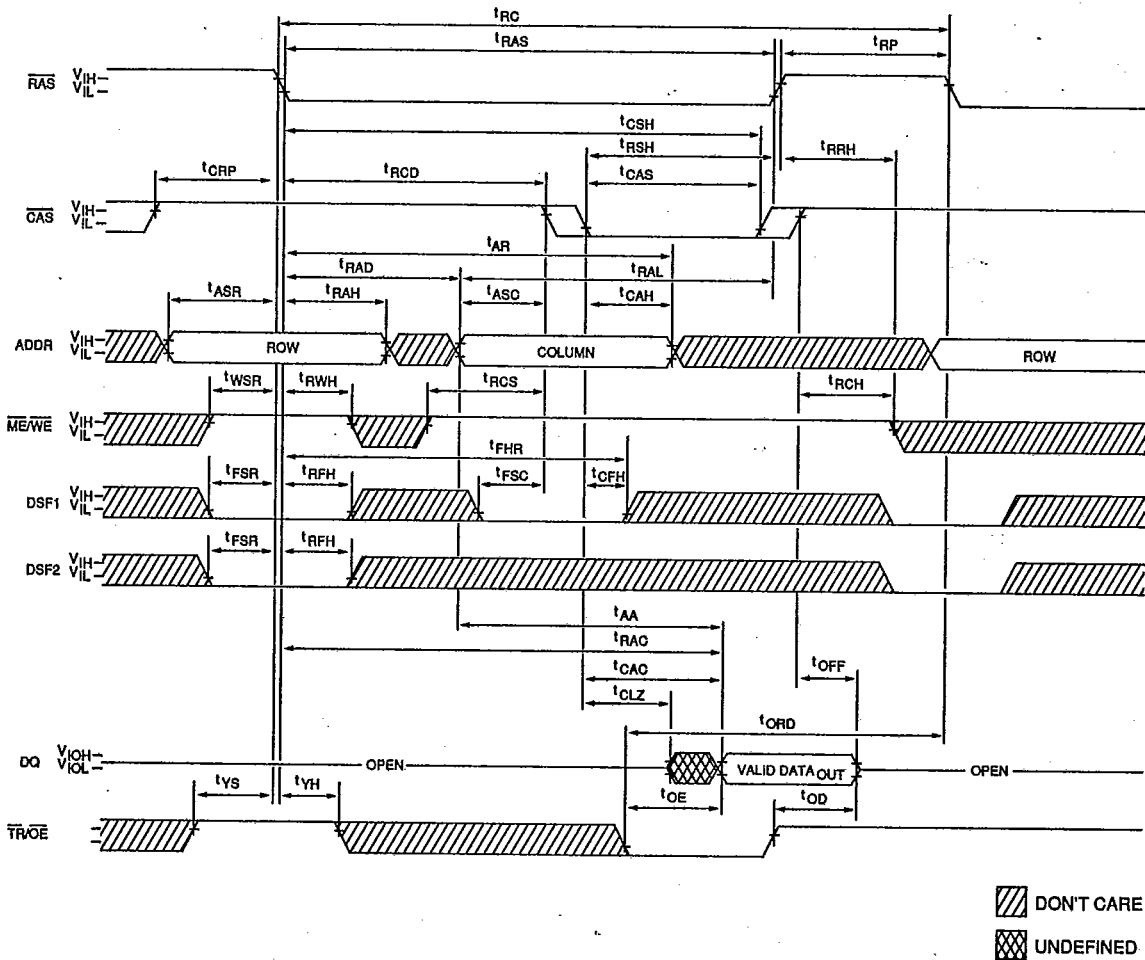


MT43C8128/9

T-46-23-37-

DRAM READ CYCLE

MULTIPORT DRAM





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MT43C8128/9

## WRITE CYCLE FUNCTION TABLE 1

T-46-23-37

LOGIC STATES <sup>2</sup>						FUNCTION	CODE
RAS Falling Edge			CAS Falling Edge				
A ME/WE	B DSF1	C DQ (Input)	D ME/WE	E DSF1	F DQ (Input)		
1	0	X	0/1 <sup>5</sup>	0	DRAM	Normal DRAM WRITE	RW
0	0	Write Mask	0/1 <sup>5</sup>	0	DRAM (Masked)	NONPERSISTENT (Load and Use) MASKED WRITE to DRAM	RWNM
0	1	X	0/1 <sup>5</sup>	0	DRAM (Masked)	PERSISTENT (Use Register) MASKED WRITE to DRAM	RWOM
1	0	X	X <sup>3</sup>	1	Column Mask	BLOCK WRITE to DRAM (No Data Mask)	BW
0	0	Write Mask	X <sup>3</sup>	1	Column Mask	NONPERSISTENT (Load and Use) MASKED BLOCK WRITE to DRAM	BWNM
0	1	X	X <sup>3</sup>	1	Column Mask	PERSISTENT (Use Register) MASKED BLOCK WRITE to DRAM	BWOM
1	1	X	X <sup>4</sup>	0	Write Mask	LOAD MASK REGISTER	LMR
1	1	X	X <sup>4</sup>	1	Color Data	LOAD COLOR REGISTER	LCR

MULTIPORT DRAM

- NOTE:**
1. Refer to this function table to determine the logic states of "A", "B", "C", "D", "E" and "F" for the WRITE cycle timing diagrams on the following pages.
  2. TRM, MKD and STS are "don't care" for all WRITE cycles.
  3. WE is a "don't care" for BLOCK WRITE cycles. It occurs on the falling edge of CAS.
  4. Register load cycles can be either EARLY or LATE-WRITE cycles.
  5. If ME/WE is LOW, an EARLY-WRITE is performed; if it is HIGH, a LATE-WRITE is performed if ME/WE falls after CAS.

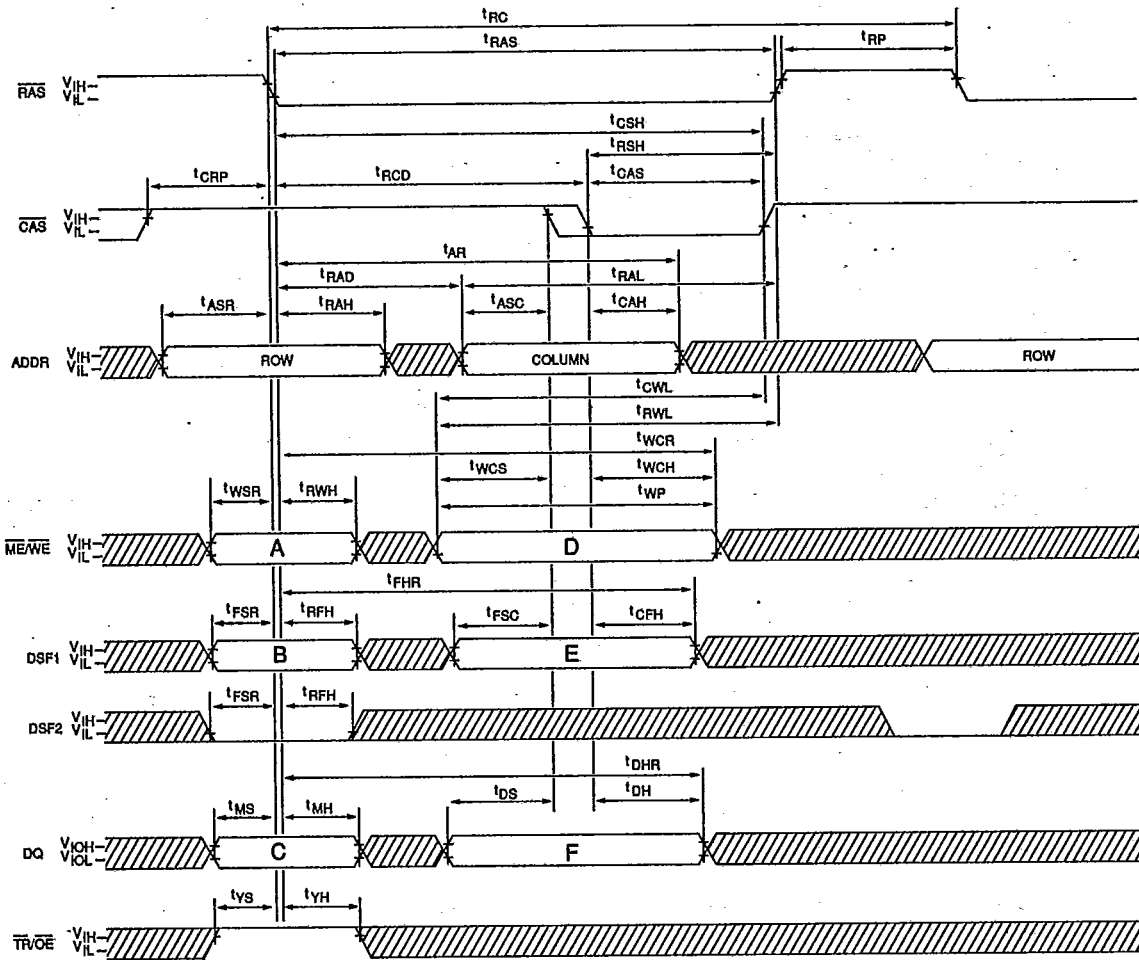


MT43C8128/9

T-46-23-37

DRAM EARLY-WRITE CYCLE

MULTI-PORT DRAM



DON'T CARE  
 UNDEFINED

**NOTE:** The logic states of "A", "B", "C", "D", "E" and "F" determine the type of WRITE operation performed. See the WRITE Cycle Function Table for a detailed description.

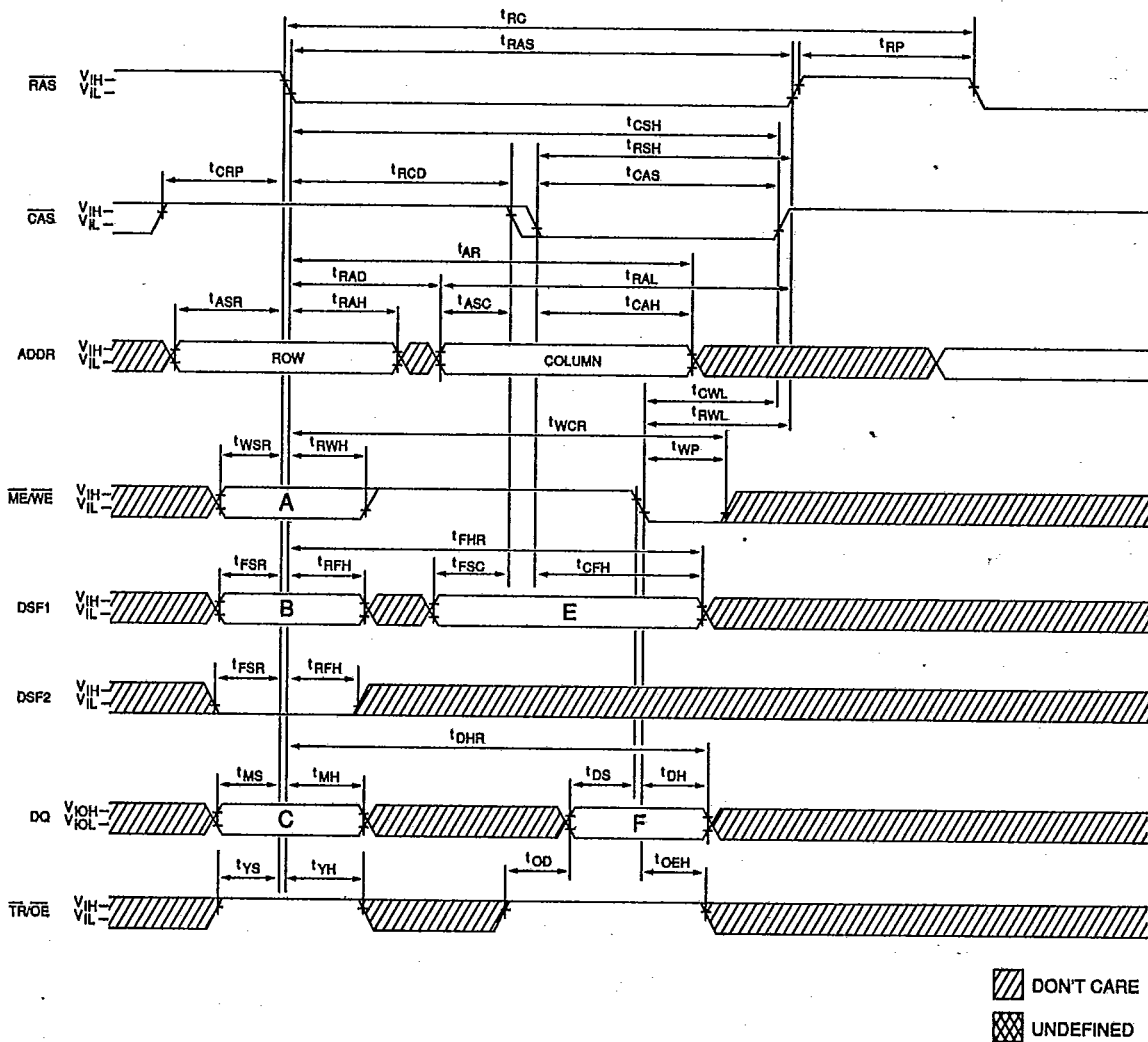


MT4308128/9

T-46-23-37-

DRAM LATE-WRITE CYCLE

MULTIPORT DRAM



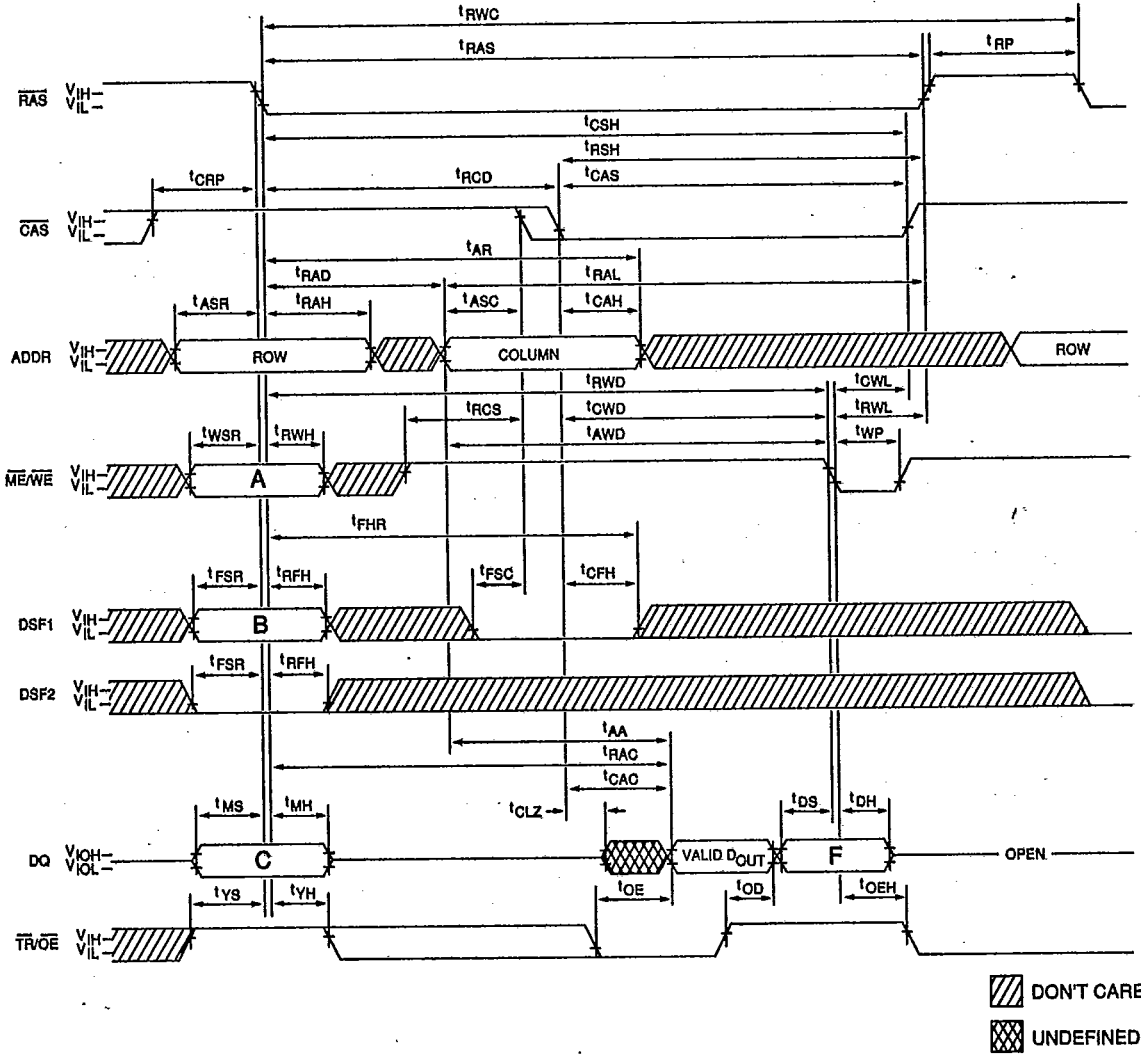
- NOTE:**
1. The logic states of "A", "B", "C", "E", and "F" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.
  2. LATE-WRITE cycles are not valid for BLOCK WRITES. (ME)/WE = "don't care" at the falling edge of CAS.

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MT43C8128/9

T-4623-37-

DRAM READ-WRITE CYCLE  
(READ-MODIFY-WRITE CYCLE)



MULTIPORT DRAM

**NOTE:** The logic states of "A", "B", "C", and "F" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

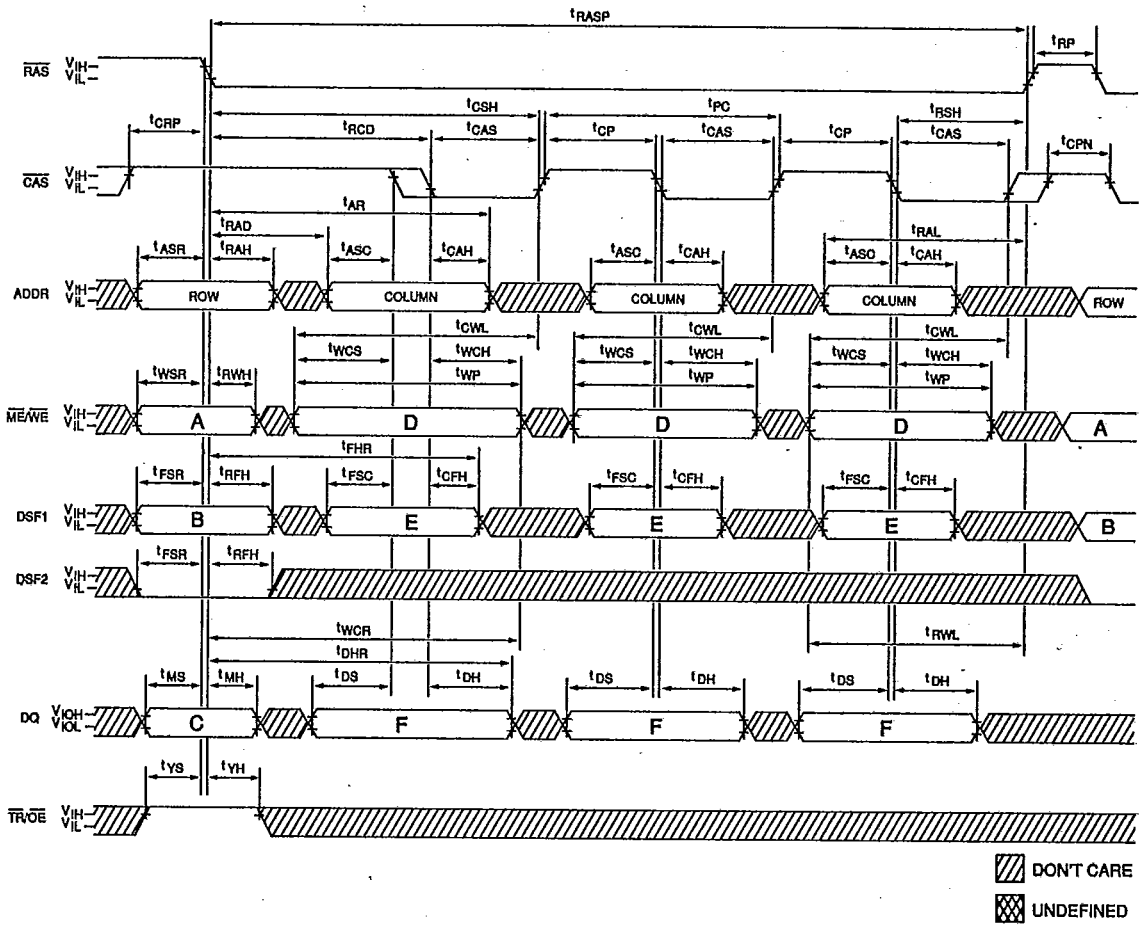


MT43C8128/9

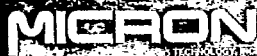
T-46-23-37

DRAM FAST-PAGE-MODE EARLY-WRITE CYCLE 1,2

MULTIPORT DRAM



- NOTE:**
1. READ cycles or READ-MODIFY-WRITE cycles can be mixed with WRITE cycles while in FAST PAGE MODE.
  2. The logic states of "A", "B", "C", "D", "E", and "F" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

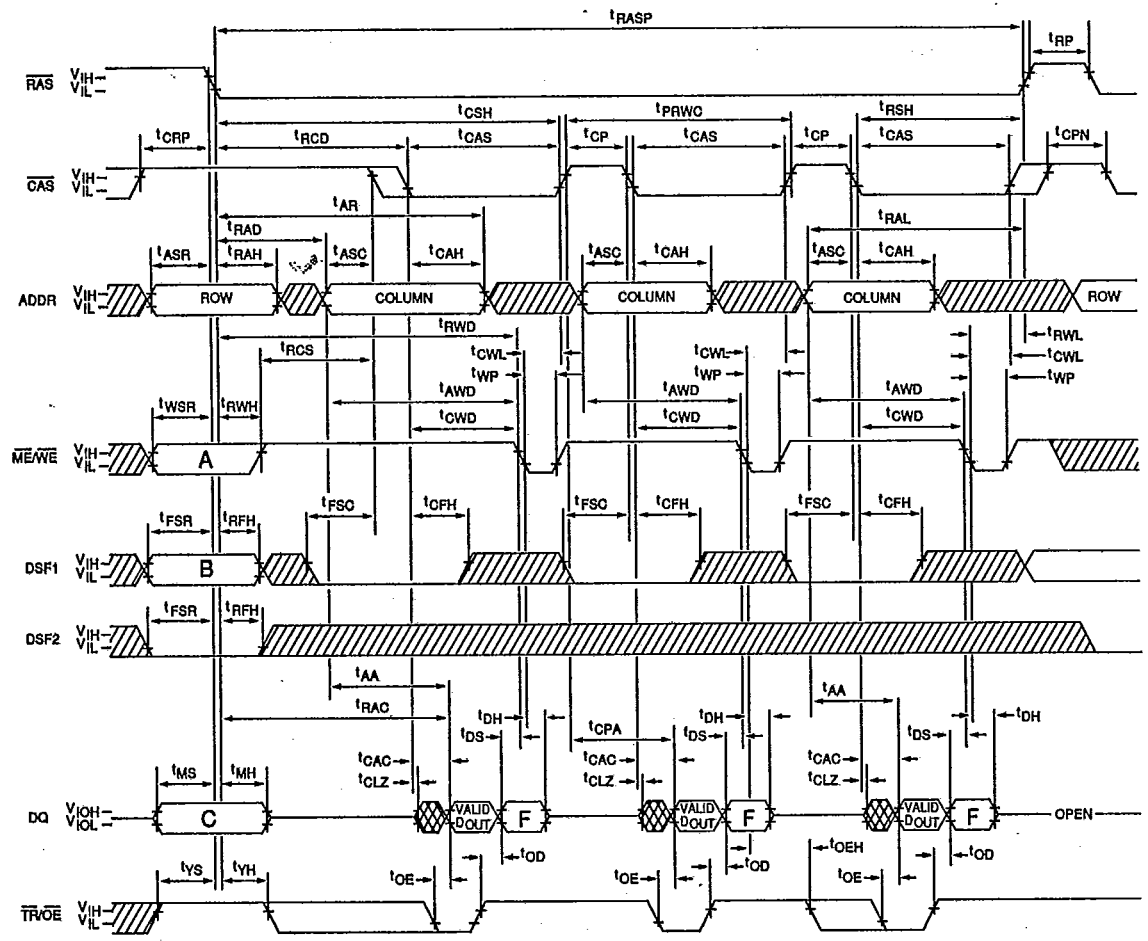


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DRAM FAST-PAGE-MODE READ-WRITE CYCLE (READ-MODIFY-WRITE or LATE-WRITE CYCLES)

MULTI-PORT DRAM



DON'T CARE  
 UNDEFINED

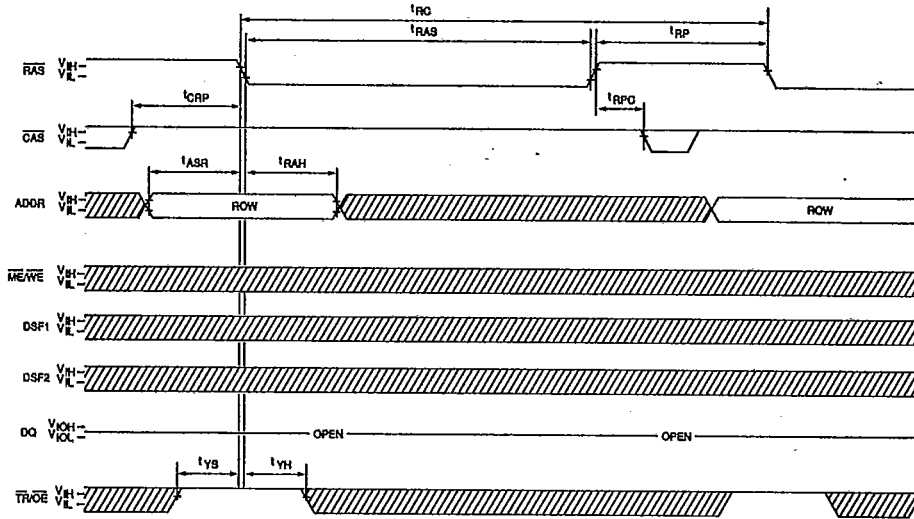
- NOTE:**
1. READ or WRITE cycles can be mixed with READ-MODIFY-WRITE cycles while in FAST PAGE MODE. Use the Write Function Table to determine the proper DSF1 state for the desired WRITE operation.
  - 2: The logic states of "A", "B", "C", and "F" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.



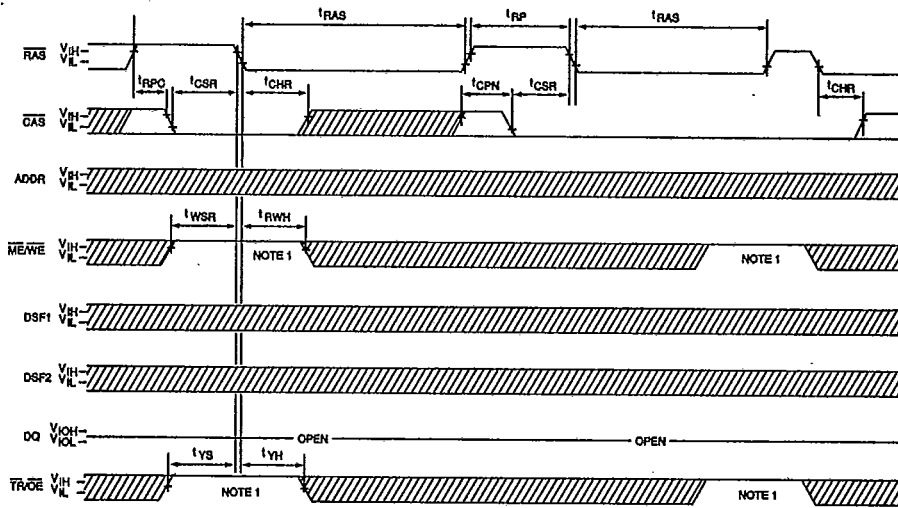
MT43C8128/9

T-46-23-37

DRAM RAS-ONLY REFRESH CYCLE  
(ADDR = A0-A8)



CAS-BEFORE-RAS REFRESH CYCLE



 DONT CARE  
 UNDEFINED

NOTE: 1. The MT43C8128/9 operates with this state as "don't care", but to allow for future functional enhancements it is recommended that they be driven as illustrated for system upgradability.

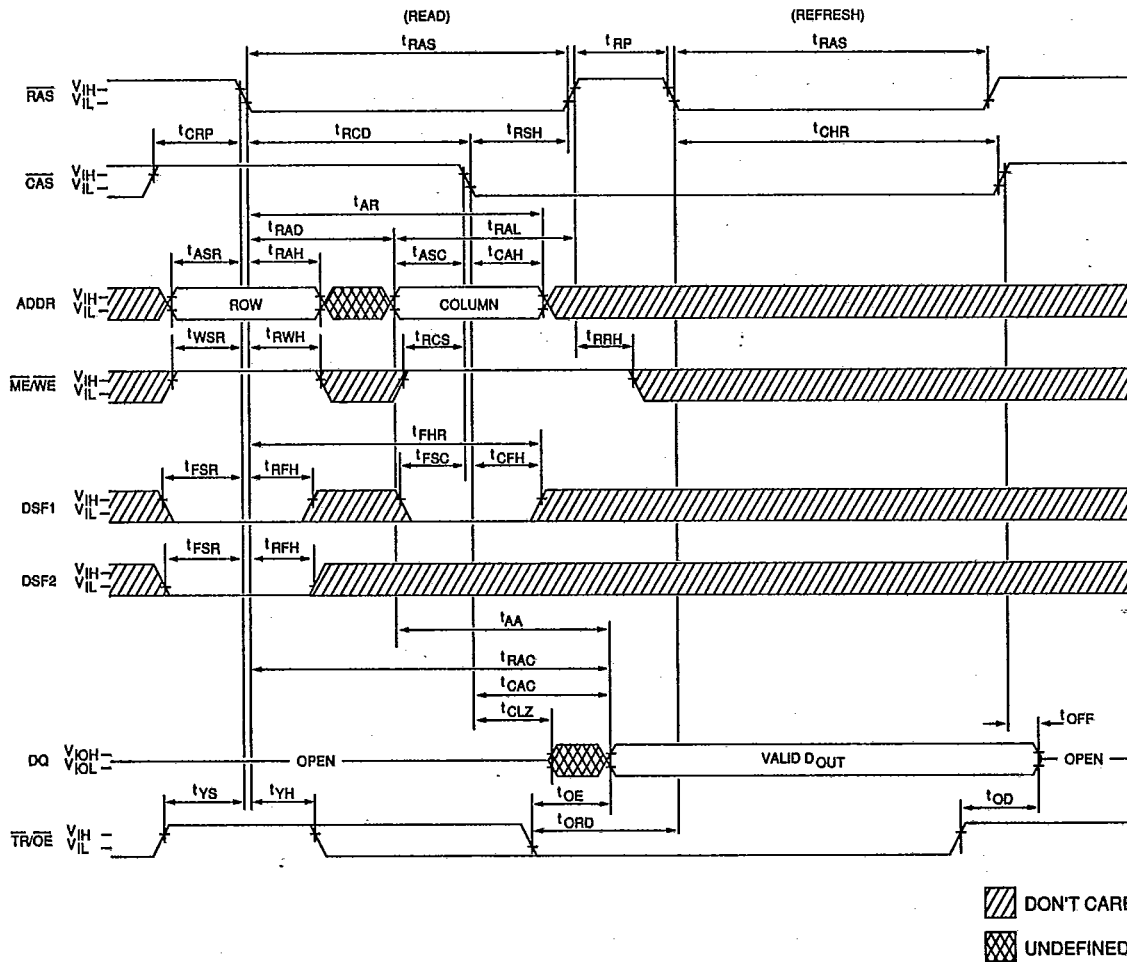
MULTIPORT DRAM



MT43C812819

T-46-23-37

DRAM HIDDEN-REFRESH CYCLE



MULTI-PORT DRAM

**NOTE:** A HIDDEN REFRESH may also be performed after a WRITE or TRANSFER cycle. In the WRITE case,  $\overline{ME/WE}$  = LOW (when  $\overline{CAS}$  goes LOW) and  $\overline{TR/OE}$  = HIGH. In the TRANSFER case,  $\overline{TR/OE}$  = LOW (when  $\overline{RAS}$  goes LOW) and the DQ pins stay High-Z during the refresh period, regardless of  $\overline{TR/OE}$ .

PRELIMINARY



MT43C8128/9

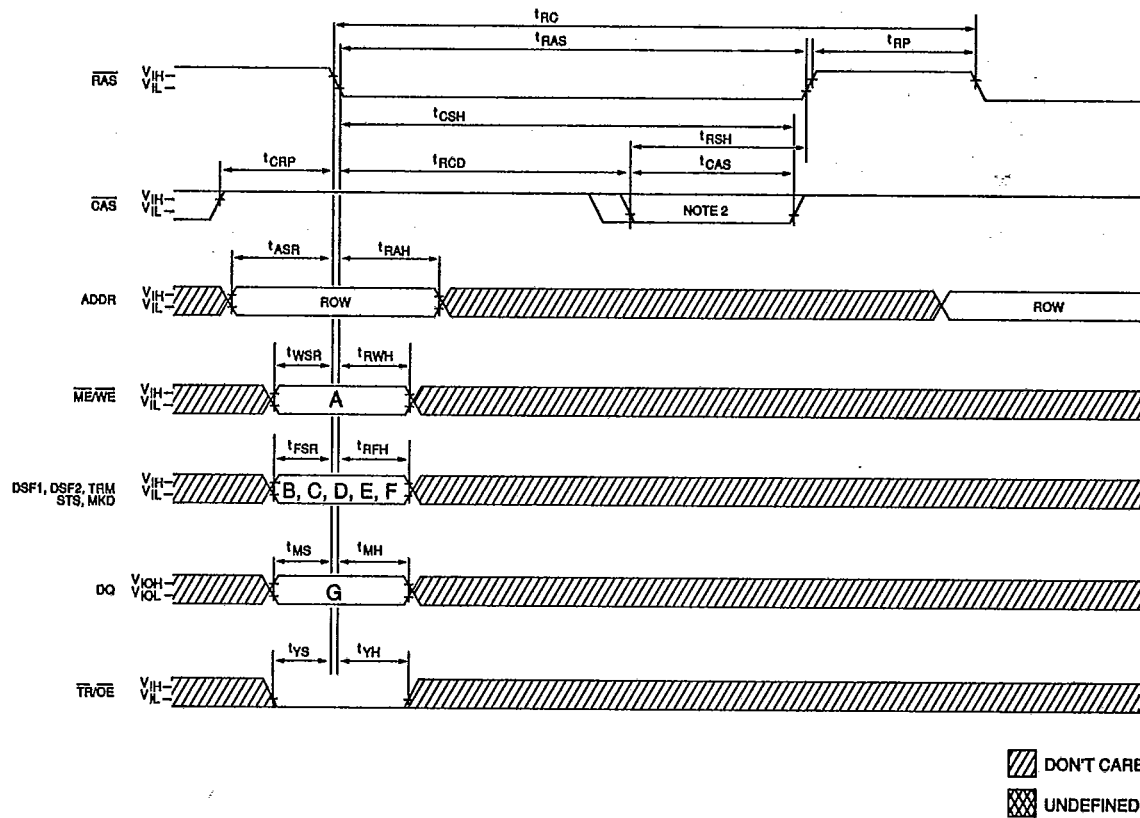
T-46-23-37

DRAM/BMR TRANSFER CYCLE FUNCTION TABLE

LOGIC STATES							FUNCTION	CODE
RAS Falling Edge								
A ME/WE	B DSF1	C DSF2	D TRM	E STS	F MKD	G DQ (Input)		
1	0	0	1	0	X'	X	BMR READ TRANSFER (DRAM→BMR TRANSFER)	BMR-RT
1	0	0	1	1	X'	X	BMR READ TRANSFER (DRAM→Invert→BMR TRANSFER)	BMR-IRT
0	0	0	1	0	X'	MASK	BMR WRITE TRANSFER (BMR→DRAM TRANSFER)	BMR-WT
0	0	0	1	1	X'	MASK	BMR WRITE TRANSFER (BMR→Invert→DRAM TRANSFER)	BMR-IWT
1	1	1	0	X	X'	X	CLEAR BMR (CLR-BMR)	CLR-BMR

MULTIPORT DRAM

DRAM/BMR TRANSFERS



**NOTE:** 1. Serial Mask Input mode is enabled if MKD = HIGH; disabled if MKD = LOW.  
 2. It is not necessary to drop CAS during a DRAM/BMR TRANSFER.

PRELIMINARY

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MT43C8128/9

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READ TRANSFER CYCLE FUNCTION TABLE<sup>1</sup>

LOGIC STATES <sup>2</sup>					FUNCTION	CODE
RAS Falling Edge						
A DSF1	B DSF2	C TRM	D STS	E MKD		
0	0	0	0/1 <sup>2</sup>	X	READ TRANSFER (DRAM→SAM)	RW
1	0	0	0/1 <sup>2</sup>	X	SPLIT READ TRANSFER (DRAM→SAM)	SRT
0	1	1	0/1 <sup>2</sup>	X	BIT MASKED READ TRANSFER	BMRT
1	1	1	0/1 <sup>2</sup>	X	BIT MASKED SPLIT READ TRANSFER	BMSRT
1	0	1	0/1 <sup>2</sup>	0/1 <sup>3</sup>	BMR→SAM TRANSFER	BMR-SAM

MULTIPORT DRAM

- NOTE:**
1. Refer to this function table to determine the logic states of "A", "B", "C", "D" and "E" for READ TRANSFER cycle timing diagrams on the following pages.
  2. The state of STS at the falling edge of RAS determines the SAM involved in the transfer. When STS = LOW the transfer is to SAMa; when STS = HIGH the transfer is to SAMb.
  3. Serial Mask Input mode is enabled if MKD = HIGH; disabled if MKD = LOW.

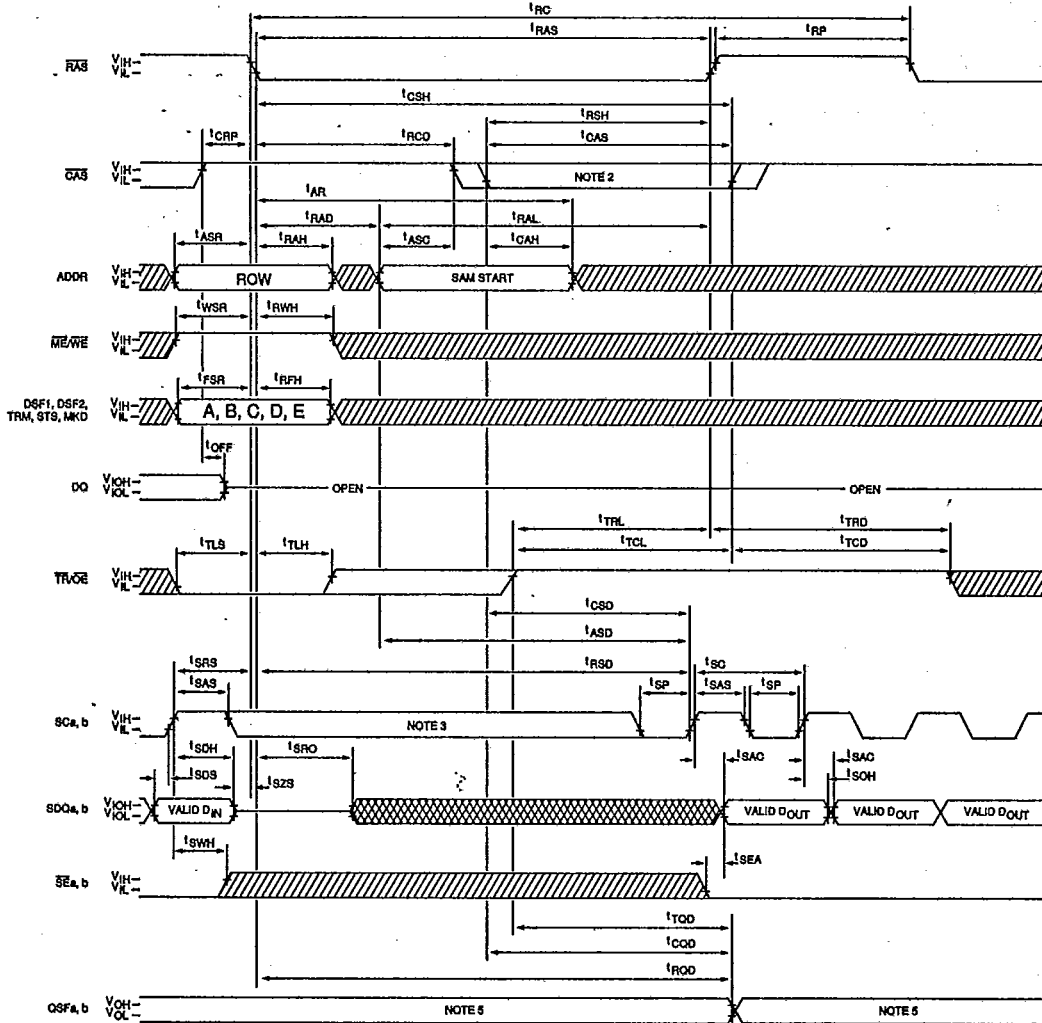


MT43C8128/9

T-46-23-37

READ TRANSFER<sup>1,4</sup>  
(DRAM-TO-SAM TRANSFER)  
(When part was previously in the SERIAL INPUT mode)

MULTIPORT DRAM



▨ DON'T CARE  
▩ UNDEFINED

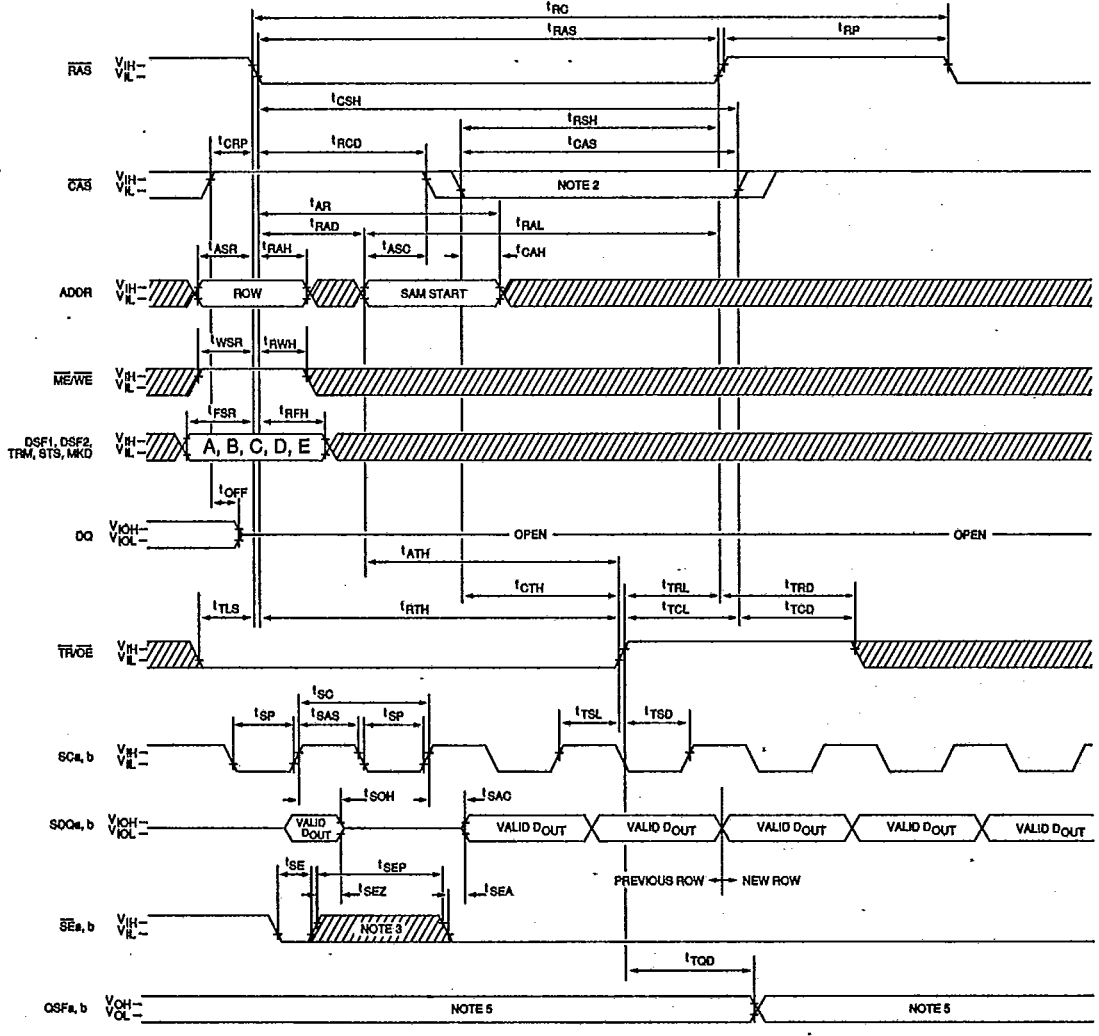
- NOTE:**
1. SSF = "Don't Care"
  2.  $\overline{CAS}$  is used to load the Tap address. If  $\overline{CAS}$  does not fall, the last Tap address loaded for the addressed SAM will be reused.
  3. There must be no rising edges on the SC input during this time period.
  4. The logic states of "A", "B", "C", and "D" determine the type of TRANSFER operation performed. See the Read Transfer Cycle Function Table.
  5. QSF = 0 when the Lower SAM (bits 0-127) is being accessed.  
QSF = 1 when the Upper SAM (bits 128-255) is being accessed.



MT43C8128/9

T-46-23-37-

**REAL-TIME READ TRANSFER<sup>1,4</sup>**  
**(DRAM-TO-SAM TRANSFER)**  
 (When part was previously in the SERIAL OUTPUT mode)



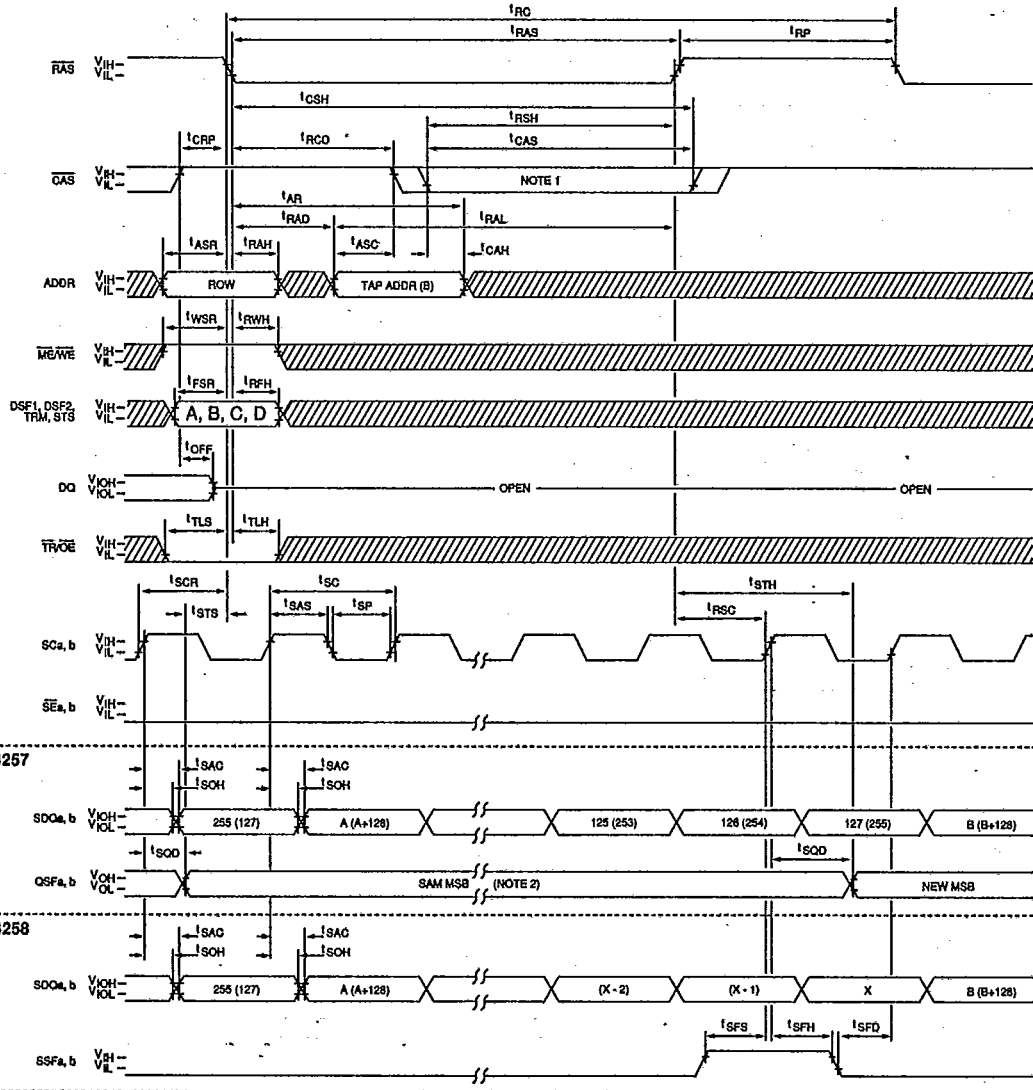
MULTIPORT DRAM

- NOTE:**
1. SSF = "Don't Care"
  2.  $\overline{\text{CAS}}$  is used to load the Tap address. If  $\overline{\text{CAS}}$  does not fall, the last Tap address loaded for the addressed
  3. The  $\overline{\text{SE}}$  pulse is shown to illustrate the serial output enable and disable timing. It is not required.
  4. The logic states of "A", "B", "C", and "D" determine the type of TRANSFER operation performed. See the Read Transfer Cycle Function Table.
  5. QSF = 0 when the Lower SAM (bits 0-127) is being accessed.  
 QSF = 1 when the Upper SAM (bits 128-255) is being accessed.



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**SPLIT READ TRANSFER<sup>3</sup>**  
**(SPLIT DRAM-TO-SAM TRANSFER)**



MULTIPORT DRAM

- NOTE:**
1.  $\overline{\text{CAS}}$  is used to load the Tap address. If  $\overline{\text{CAS}}$  does not fall, the last Tap address loaded for the addressed SAM will be reused for the idle half.
  2.  $\text{QSF} = 0$  when the Lower SAM (bits 0-127) is being accessed.  
 $\text{QSF} = 1$  when the Upper SAM (bits 128-255) is being accessed.
  3. The logic states of "A", "B", "C", and "D" determine the type of TRANSFER operation performed. See the Read Transfer Cycle Function Table.

▨ DON'T CARE  
▩ UNDEFINED

MICRON

MT43C8128/9

T-46-23-37

WRITE TRANSFER CYCLE FUNCTION TABLE<sup>1</sup>

LOGIC STATES								FUNCTION	CODE
RAS Falling Edge							SC		
A DSF1	B DSF2	C DQ	D TRM	E STS	F SE	G MKD	H MKD		
0	0	X	0	0/1 <sup>2</sup>	0	X	-	WRITE TRANSFER (SAM→DRAM)	WT
0	0	X	0	0/1 <sup>2</sup>	1	X	-	PSEUDO WRITE TRANSFER	PWT
1	0	mask	0	0/1 <sup>2</sup>	X	X	-	SPLIT WRITE TRANSFER (SAM→DRAM)	SWT
0	1	mask	0	0/1 <sup>2</sup>	X	X	-	DQ MASKED WRITE TRANSFER (SAM→DRAM)	DMWT
0	1	X	1	0/1 <sup>2</sup>	X	X	0/1 <sup>4</sup>	BIT MASKED WRITE TRANSFER (SAM→DRAM)	BMWT
1	1	mask	1	0/1 <sup>2</sup>	X	X	0/1 <sup>4</sup>	BIT MASKED SPLIT WRITE TRANSFER (SAM→DRAM)	BMSWT
1	0	X	1	0/1 <sup>2</sup>	X	0/1 <sup>3</sup>	-	SAM-BMR TRANSFER	SAM-BMR

MULTIPORT DRAM

- NOTE:**
1. Refer to this function table to determine the logic states of "A", "B", "C", "D", "E", "F", "G", and "H" for WRITE TRANSFER cycle timing diagrams on the following pages.
  2. The state of STS at the falling edge of RAS determines the SAM involved in the transfer. When STS = LOW the transfer is to SAMa; when SAM = HIGH the transfer is to SAMb.
  3. Serial Mask Input (SMI) mode is enabled if MKD = HIGH and disabled if MKD = LOW.
  4. When in the SMI mode (see BMR transfer waveforms) MKD is the SMI data input. MKD data is clocked into all bit planes of the bit mask register with SCb. A logic "1" on MKD will allow data to pass through all the mask; a logic "0" will mask the corresponding location of the SAM during a BIT MASKED TRANSFER. BIT MASKED TRANSFERS to or from SAMa must not take place while mask data is being serially input via SCb and MKD.



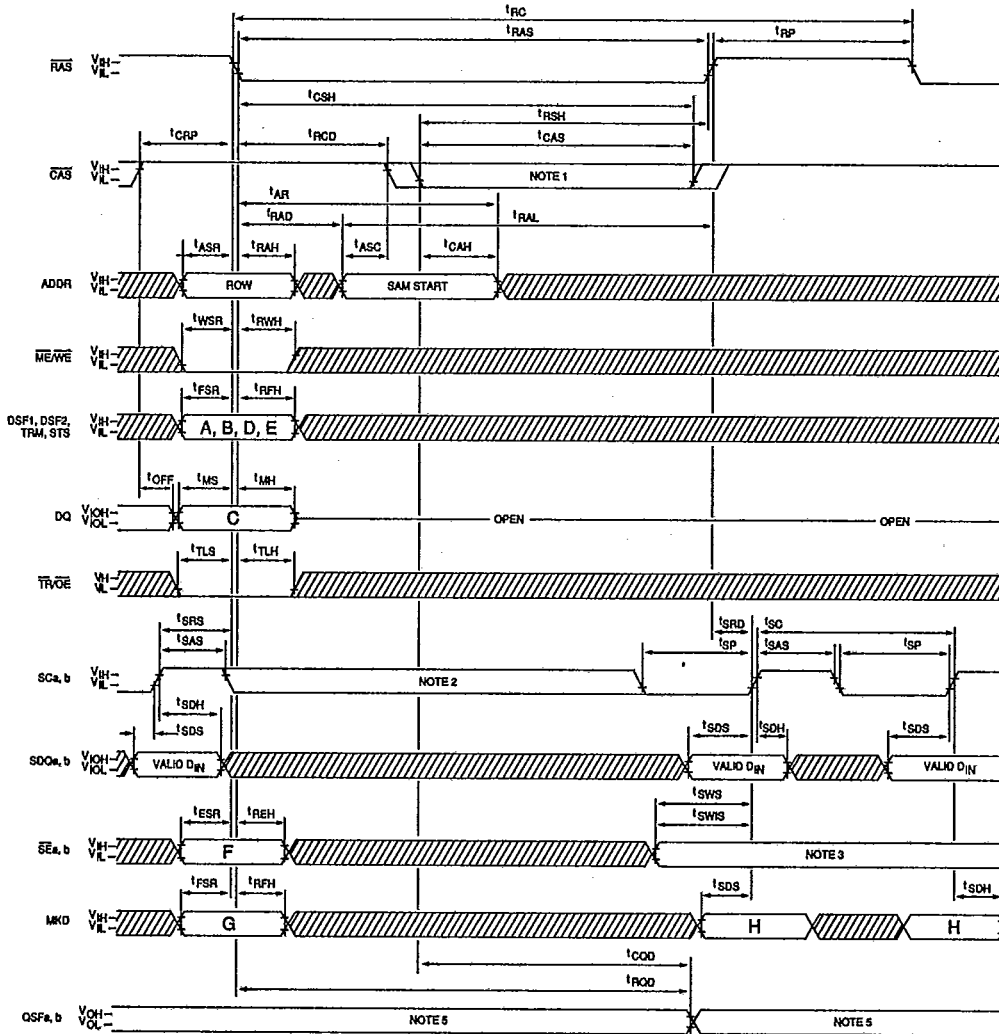


MT43C8128/9

T-46-23-37

**WRITE TRANSFER<sup>4</sup>**

(When part was previously in the SERIAL INPUT mode)



MULTIPORT DRAM

- NOTE:**
1.  $\overline{CAS}$  is used to load the Tap address. If  $\overline{CAS}$  does not fall, the last Tap address loaded for the addressed SAM will be reused.
  2.  $\overline{SE}$  must be LOW to input new serial data, but the serial address register is incremented by SC regardless of  $\overline{SE}$ .
  3. There must be no rising edges on the SC input during this time period.
  4. The logic states of "A", "B", "C", "D", "E", "F", "G" and "H" determine the type of TRANSFER operation performed. See the Write Transfer Cycle Function Table.
  5. QSF = 0 when the Lower SAM (bits 0-127) is being accessed.  
QSF = 1 when the Upper SAM (bits 128-255) is being accessed. SSFa,b = "don't care" (MT43C8129).

DONT CARE  
 UNDEFINED

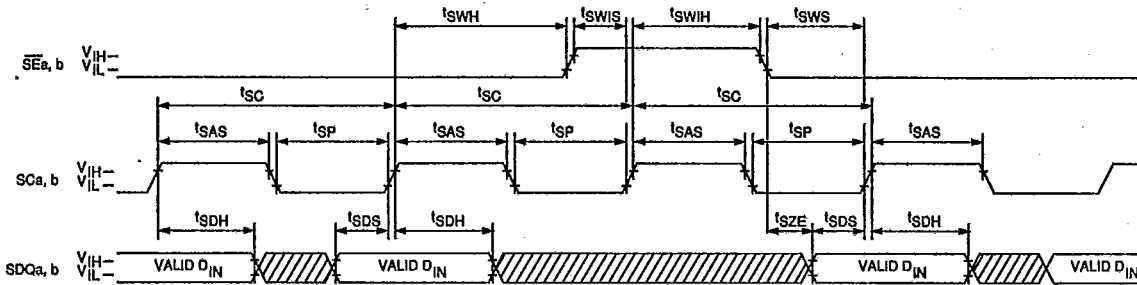




MT43C8128/9

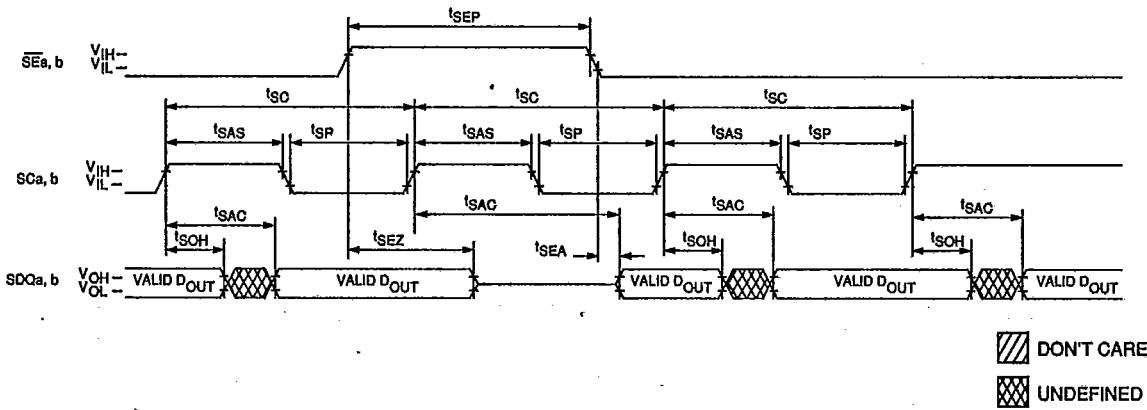
T-46-23-37-

SAMa or SAMb SERIAL INPUT



MULTI-PORT DRAM

SAMa or SAMb SERIAL OUTPUT



NOTE : SEa, SCa and SDQa are used when accessing SAMa and SEb; SCb and SDQb are used when access in SAMb.