HD66753

(132 x 168-dot Graphics LCD Controller/Driver with
Bit-operation Functions)

HITACHI

Rev 0.1
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Description

The HD66753, dot-matrix graphics LCD controller and driver LSI, displays 132-by-168-dot graphics for four monochrome grayscales. When 12-by-13-dot size fonts are used, up to 13 lines x 11 characters (143 characters) can be simultaneously displayed. Since the HD66753 incorporates bit-operation functions and a 16-bit high-speed bus interface, it enables efficient data transfer and high-speed rewriting of data in the graphics RAM.

The HD66753 has various functions for reducing the power consumption of an LCD system, such as low-voltage operation of 1.7 V/min., a step-up circuit to generate a maximum of seven-times the LCD drive voltage from the input-supplied voltage, and voltage followers to decrease the direct current flow in the LCD drive bleeder-resistors. Combining these hardware functions with software functions, such as a partial display with low-duty drive and standby and sleep modes, allows precise power control. The HD66753 is suitable for any mid-sized or small portable battery-driven product requiring long-term driving capabilities, such as digital cellular phones supporting a WWW browser.

Features

- 132 × 168-dot graphics display LCD controller/driver for four monochrome grayscales
- 16-/8-bit high-speed bus interface
- Clock-synchronized serial interface (transfer rate: 10 MHz max.)
- I2C bus interface (transfer rate: 1.3 MHz max.)
- Bit-operation functions for graphics processing:
  - — Write-data mask function in bit units
  - — Bit rotation function
  - — Bit logic-operation function
- Low-power operation supports:
  - — Vcc = 1.7 to 3.6 V (low voltage)
  - — V_{LPS} = 5 to 17.5 V (liquid crystal drive voltage)
  - — Internal three-, five-, six-, or seven-times step-up circuit for liquid crystal drive voltage to be selected by software
  - — 128-step contrast adjuster and voltage followers to decrease direct current flow in the LCD drive bleeder-resistors

— Power-save functions such as the standby mode and sleep mode
— Programmable drive duty ratios and bias values displayed on LCD

- Internal LCD-drive-voltage regulator circuits
- 168-segment × 132-common liquid crystal display driver
- n-raster-row AC liquid-crystal drive (C-pattern waveform drive)
- Duty ratio and drive bias (selectable by program)
- Window cursor display supported by hardware
- Black-and-white reversed display
- Internal oscillation and hardware reset
- Shift change of segment and common driver

Table 1 Progammable Display Sizes and Duty Ratios

			Graphics Display				
Duty Ratio	**Optimum Drive Bias**	**Bit-map Display Area**	**12 x 13-dot Font Width**	**12 x 14-dot Font Width**	**16 x 16-dot Font Width**	**16 x 17-dot Font Width**	**8 x 10-dot Font Width**
1/96	1/10	96 x 168 dots	13 lines x 8 characters	12 lines x 8 characters	10 lines x 6 characters	9 lines x 6 characters	16 lines x 12 characters
1/104	1/11	104 x 168 dots	13 lines x 8 characters	12 lines x 8 characters	10 lines x 6 characters	9 lines x 6 characters	16 lines x 13 characters
1/112	1/11	112 x 168 dots	13 lines x 9 characters	12 lines x 9 characters	10 lines x 7 characters	9 lines x 7 characters	16 lines x 14 characters
1/120	1/11	120 x 168 dots	13 lines x 10 characters	12 lines x 10 characters	10 lines x 7 characters	9 lines x 7 characters	16 lines x 15 characters
1/128	1/11	128 x 168 dots	13 lines x 10 characters	12 lines x 10 characters	10 lines x 8 characters	9 lines x 8 characters	16 lines x 16 characters
1/132	1/11	132 x 168 dots	13 lines x 10 characters	12 lines x 11 characters	10 lines x 8 characters	9 lines x 8 characters	16 lines x 16 characters

Note: When 12 x 13-dot fonts are used for display, the spaces between characters on the last line are not displayed.

<Target values>

Total Current Consumption Characteristics (Vcc = 3 V, TYP Conditions, LCD Drive Power Current Included)

Character Display Dot Size	Duty Ratio	R-C Oscillation Frequency	Frame Frequency	Total Power Consumption: Normal Display Operation: Internal Logic	LCD Power	Total*	Sleep Mode	Standby Mode
96 x 168 dots	1/96	100 kHz	69 Hz	(60 µA)	(20 µA)	Five-times (160 µA)	(12 µA)	0.1 µA
104 x 168 dots	1/104	100 kHz	69 Hz	(60 µA)	(20 µA)	Five-times (160 µA)	(12 µA)	
112 x 168 dots	1/112	100 kHz	69 Hz	(70 µA)	(25 µA)	Six-times (220 µA)	(12 µA)	
120 x 168 dots	1/120	100 kHz	69 Hz	(70 µA)	(25 µA)	Six-times (220 µA)	(12 µA)	
128 x 168 dots	1/128	100 kHz	71 Hz	(80 µA)	(25 µA)	Six-times (230 µA)	(12 µA)	
132 x 168 dots	1/132	100 kHz	69 Hz	(80 µA)	(25 µA)	Six-times (230 µA)	(12 µA)	

Note: When a three-, five-, six-, or seven-times step-up is used:
the total current consumption = internal logic current + LCD power current x 3 (three-times step-up),
the total current consumption = internal logic current + LCD power current x 5 (five-times step-up),
the total current consumption = internal logic current + LCD power current x 6 (six-times step-up), and
the total current consumption = internal logic current + LCD power current x 7 (seven-times step-up)

Type Name

Types	External Dimensions	MPU Interface	COM Driver Arrangement	Display
HD66753TB0	Bending TCP	or 16-bit8-bit parallel or clock-synchronized serial interface	Both sides of COM (Output from left and right sides of the chip)	Four monochrome grayscales
HCD66753BP	Au-bump chip			
HWD66753BP	Au-bump wafer			
HD66753WTB0	Bending TCP	8-bit or 16-bit parallel, clock-synchronized serial, or I2C bus interface		
HCD66753WBP	Au-bump chip			
HWD66753WBP	Au-bump wafer			

LCD Family Comparison

Items	HD66724	HD66725	HD66726
Character display sizes	12 characters x 3 lines	16 characters x 3 lines	16 characters x 5 lines
Graphic display sizes	72 x 26 dots	96 x 26 dots	96 x 42 dots
Grayscale display	—	—	—
Multiplexing icons	144	192	192
Annunciator	1/2 duty: 144	1/2 duty: 192	1/2 duty: 192
Key scan control	8 x 4	8 x 4	8 x 4
LED control ports	—	—	—
General output ports	3	3	3
Operating power voltages	1.8 V to 5.5 V	1.8 V to 5.5 V	1.8 V to 5.5 V
Liquid crystal drive voltages	3 V to 6.5 V	3 V to 6.5 V	4.5 V to 11 V
Serial bus	Clock-synchronized serial	Clock-synchronized serial	Clock-synchronized serial
Parallel bus	4 bits, 8 bits	4 bits, 8 bits	4 bits, 8 bits
Liquid crystal drive duty ratios	1/2, 10, 18, 26	1/2, 10, 18, 26	1/2, 10, 18, 26, 34, 42
Liquid crystal drive biases	1/4 to 1/6.5	1/4 to 1/6.5	1/2 to 1/8
Liquid crystal drive waveforms	B	B	B
Liquid crystal voltage step-up	Single, two-, or three-times	Single, two-, or three-times	Single, two-, three-, or four-times
Bleeder-resistor for liquid crystal drive	Incorporated (external)	Incorporated (external)	Incorporated (external)
Liquid crystal drive operational amplifier	Incorporated	Incorporated	Incorporated
Liquid crystal contrast adjuster	Incorporated (32 steps)	Incorporated (32 steps)	Incorporated (32 steps)
Horizontal smooth scroll	3-dot unit	3-dot unit	—
Vertical smooth scroll	Line unit	Line unit	Line unit
Double-height display	Yes	Yes	Yes
DDRAM	80 x 8	80 x 8	80 x 8
CGROM	20,736	20,736	20,736
CGRAM	384 x 8	384 x 8	480 x 8
SEGRAM	72 x 8	96 x 8	96 x 8
No. of CGROM fonts	240 + 192	240 + 192	240 + 192
No. of CGRAM fonts	64	64	64
Font sizes	6 x 8	6 x 8	6 x 8
Bit map areas	72 x 26	96 x 26	96 x 42
R-C oscillation resistor/ oscillation frequency	External resistor, incorporated (32 kHz)	External resistor, incorporated (32 kHz)	External resistor (50 kHz)
Reset function	External	External	External
Low power control	Partial display off, Oscillation off, Liquid crystal power off, Key wake-up interrupt	Partial display off, Oscillation off, Liquid crystal power off, Key wake-up interrupt	Partial display off, Oscillation off, Liquid crystal power off, Key wake-up interrupt
SEG/COM direction switching	SEG, COM	SEG, COM	SEG, COM
QFP package	—	—	—
TQFP package	—	—	—
TCP package	TCP-146	TCP-170	TCP-188
Bare chip	—	—	Yes
Bumped chip	Yes	Yes	Yes
Chip sizes	10.34 x 2.51	10.97 x 2.51	13.13 x 2.51
Pad intervals	80 µm	80 µm	100 µm

LCD Family Comparison (cont)

Items	HD66728	HD66729	HD66740
Character display sizes	16 characters x 10 lines	—	—
Graphic display sizes	112 x 80 dots	105 x 68 dots	112 x 80 dots
Grayscale display	—	—	—
Multiplexing icons	—	—	—
Annunciator	—	—	—
Key scan control	8 x 4	—	—
LED control ports	—	—	—
General output ports	3	—	—
Operating power voltages	1.8 V to 5.5 V	1.8 V to 5.5 V	1.8 V to 3.6 V
Liquid crystal drive voltages	4.5 V to 15 V	4.0 V to 13 V	4.5 V to 15 V
Serial bus	Clock-synchronized serial	Clock-synchronized serial	Clock-synchronized serial
Parallel bus	4 bits, 8 bits	4 bits, 8 bits	4 bits, 8 bits
Liquid crystal drive duty ratios	1/8, 16, 24, 32, 40, 48, 56, 64, 72, 80	1/8, 16, 24, 32, 40, 48, 56, 64, 68	1/8, 16, 24, 32, 40, 48, 56, 64, 72, 80
Liquid crystal drive biases	1/4 to 1/10	1/4 to 1/9	1/4 to 1/10
Liquid crystal drive waveforms	B, C	B, C	B, C
Liquid crystal voltage step-up	Three-, four-, or five-times	Two-, three-, four-, or five-times	Three-, four-, or five-times
Bleeder-resistor for liquid crystal drive	Incorporated (external)	Incorporated (external)	Incorporated (external)
Liquid crystal drive operational amplifier	Incorporated	Incorporated	Incorporated
Liquid crystal contrast adjuster	Incorporated (64 steps)	Incorporated (64 steps)	Incorporated (64 steps)
Horizontal smooth scroll	—	—	—
Vertical smooth scroll	Line unit	Line unit	Line unit
Double-height display	Yes	Yes	Yes
DDRAM	160 x 8	—	—
CGROM	20,736	—	—
CGRAM	1,120 x 8	1,050 x 8	1,120 x 8
SEGRAM	—	—	—
No. of CGROM fonts	240 + 192	—	—
No. of CGRAM fonts	64	—	—
Font sizes	6 x 8	—	—
Bit map areas	112 x 80	105 x 68	112 x 80
R-C oscillation resistor/ oscillation frequency	External resistor (70–90 kHz)	External resistor (75 kHz)	External resistor (70–90 kHz)
Reset function	External	External	External
Low power control	Partial display off, Oscillation off, Liquid crystal power off, Key wake-up interrupt	Partial display off, Oscillation off, Liquid crystal power off	Partial display off, Oscillation off, Liquid crystal power off
SEG/COM direction switching	SEG, COM	SEG, COM	SEG, COM
QFP package	—	—	—
TQFP package	—	—	—
TCP package	TCP-241	TCP-213	TCP-236
Bare chip	—	—	—
Bumped chip	Yes	Yes	Yes
Chip sizes	13.67 x 2.78	12.23 x 2.52	9.40 x 2.18
Pad intervals	70 µm	70 µm	50 µm

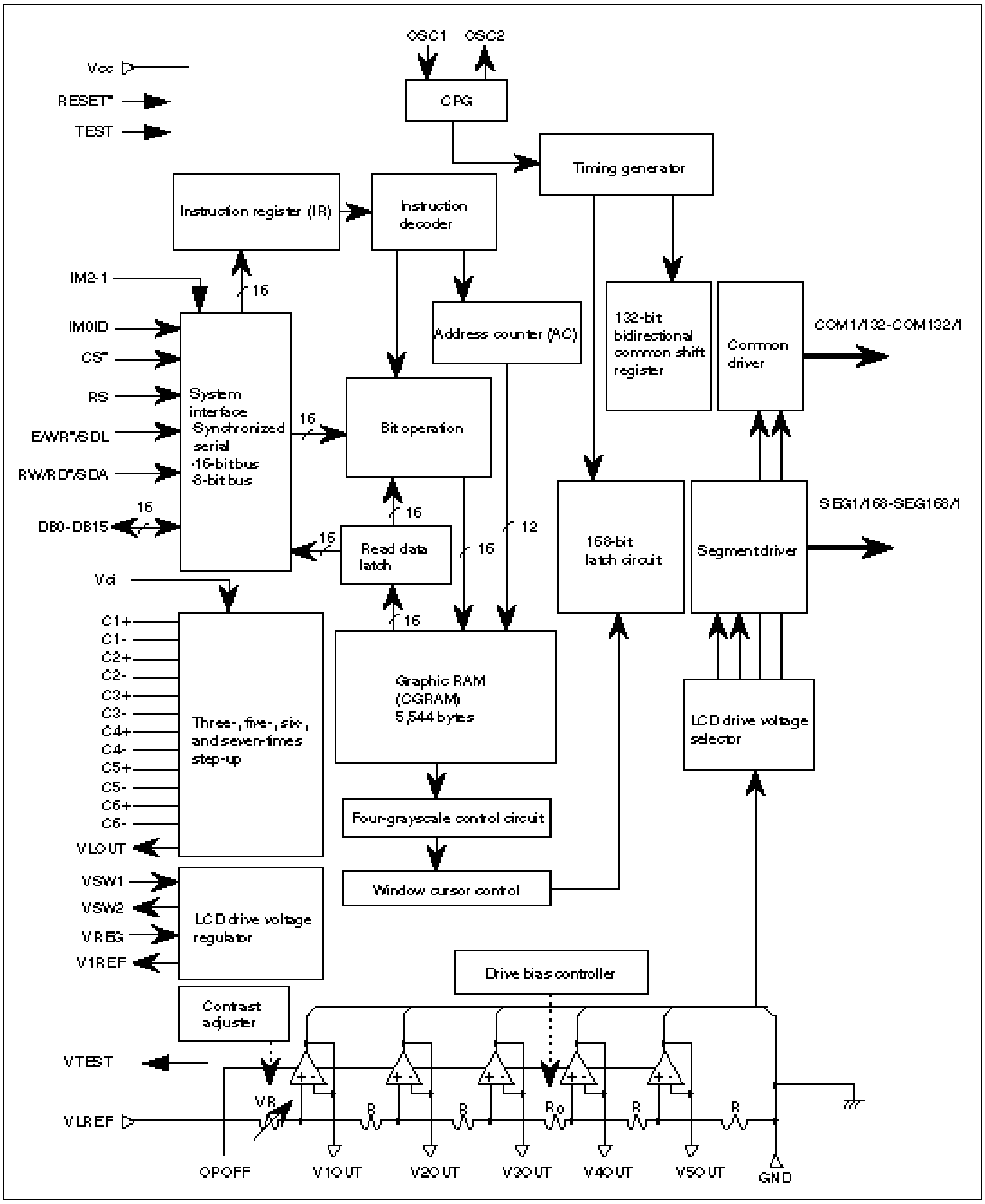
LCD Family Comparison (cont)

Items	HD66741	HD66751S	HD66750S
Character display sizes	—	—	—
Graphic display sizes	128 x 80 dots	128 x 128 dots	128 x 128 dots
Grayscale display	—	Four monochrome grayscales (5 levels)	Four monochrome grayscales (5 levels)
Multiplexing icons	—	—	—
Annunciator	—	—	—
Key scan control	—	—	—
LED control ports	—	—	—
General output ports	3	—	—
Operating power voltages	1.8 V to 5.5 V	1.7 V to 3.6 V	1.7 V to 3.6 V
Liquid crystal drive voltages	4.5 V to 15 V	5.0 V to 16.5V	5.0 V to 16.5V
Serial bus	Clock-synchronized serial	—	Clock-synchronized serial
Parallel bus	4 bits, 8 bits	8 bits, 16 bits	8 bits, 16 bits
Liquid crystal drive duty ratios	1/8, 16, 24, 32, 40, 48, 56, 64, 72, 80	1/16, 24, 72, 80, 88, 96, 104, 112, 120, 128	1/16, 24, 72, 80, 88, 96, 104, 112, 120, 128
Liquid crystal drive biases	1/4 to 1/10	1/4 to 1/11	1/4 to 1/11
Liquid crystal drive waveforms	B, C	B, C	B, C
Liquid crystal voltage step-up	Three-, four-, or five-times	Two-, five-, six-, or seven-times	Two-, five-, six-, or seven-times
Bleeder-resistor for liquid crystal drive	Incorporated (external)	Incorporated (external)	Incorporated (external)
Liquid crystal drive operational amplifier	Incorporated	Incorporated	Incorporated
Liquid crystal contrast adjuster	Incorporated (64 steps)	Incorporated (64 steps)	Incorporated (64 steps)
Horizontal smooth scroll	—	—	—
Vertical smooth scroll	Line unit	Line unit	Line unit
Double-height display	Yes	Yes	Yes
DDRAM	—	—	—
CGROM	—	—	—
CGRAM	1,280 x 8	4,096 x 8	4,096 x 8
SEGRAM	—	—	—
No. of CGROM fonts	—	—	—
No. of CGRAM fonts	—	—	—
Font sizes	—	—	—
Bit map areas	128 x 80	128 x 128	128 x 128
R-C oscillation resistor/ oscillation frequency	External resistor (70–90 kHz)	External resistor (70 kHz)	External resistor (70 kHz)
Reset function	External	External	External
Low power control	Partial display off, Oscillation off, Liquid crystal power off	Partial display off, Oscillation off, Liquid crystal power off	Partial display off, Oscillation off, Liquid crystal power off
SEG/COM direction switching	SEG, COM	SEG, COM	SEG, COM
QFP package	—	—	—
TQFP package	—	—	—
TCP package	TCP-254	TCP-308	TCP-308
Bare chip	—	—	—
Bumped chip	Yes	Yes	Yes
Chip sizes	14.30 x 2.78	8.42 x 3.18	8.44 x 2.95
Pad intervals	70 µm	50 µm	50 µm

LCD Family Comparison (cont)

Items	HD66752	HD66753
Character display sizes	—	—
Graphic display sizes	168 x 132 dots	168 x 132 dots
Grayscale display	Four monochrome grayscales (7 levels)	Four monochrome grayscales (7 levels)
Multiplexing icons	—	—
Annunciator	—	—
Key scan control	—	—
LED control ports	—	—
General output ports	—	—
Operating power voltages	2.0 V to 3.6 V	1.7 V to 3.6 V
Liquid crystal drive voltages	5.0 V to 15.5V	5 V to 16.5V
Serial bus	—	Clock-synchronized serial
Parallel bus	8 bits, 16 bits	8 bits, 16 bits
Liquid crystal drive duty ratios	1/80, 88, 96, 104, 112, 120, 128, 132	1/80, 88, 96, 104, 112, 120, 128, 132
Liquid crystal drive biases	1/4 to 1/11	1/4 to 1/11
Liquid crystal drive waveforms	B, C	B, C
Liquid crystal voltage step-up	Two-, five-, six-, or seven-times	Two-, five-, six-, or seven-times
Bleeder-resistor for liquid crystal drive	Incorporated (external)	Incorporated (external)
Liquid crystal drive operational amplifier	Incorporated	Incorporated
Liquid crystal contrast adjuster	Incorporated (128 steps)	Incorporated (128 steps)
Horizontal smooth scroll	—	—
Vertical smooth scroll	Line unit	Line unit
Double-height display	Yes	Yes
DDRAM	—	—
CGROM	—	—
CGRAM	5,544 x 8	5,544 x 8
SEGRAM	—	—
No. of CGROM fonts	—	—
No. of CGRAM fonts	—	—
Font sizes	—	—
Bit map areas	168 x 132, 132 x 168	168 x 132, 132 x 168
R-C oscillation resistor/ oscillation frequency	External resistor (70 kHz)	External resistor (70 kHz)
Reset function	External	External
Low power control	2-screen division partial drive, Partial display off, Oscillation off, Liquid crystal power off	2-screen division partial drive, Partial display off, Oscillation off, Liquid crystal power off
SEG/COM direction switching	SEG, COM	SEG, COM
QFP package	—	—
TQFP package	—	—
TCP package	—	TCP-352
Bare chip	—	—
Bumped chip	Yes	Yes
Chip sizes	12.68 x 4.31	15.90 x 2.02
Pad intervals	60 µm	50 µm

HD66753 Block Diagram



■C

Chip size: 15.90 mm x 2.02 mm
Chip thickness: 400 µm (typ.)
Pad coordinates: pad centers
Coordinate origin: chip center

Au bump size:

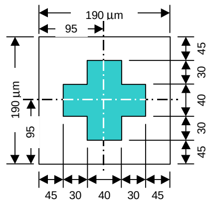
(1) 80 µm x 80 µm (min 100-µm pitch)
Dummy1, Dummy2 to GNDDUM2, Dummy8,
GNDDUM3, DB15 to V4OUT, V5OUT,
Dummy9, Dummy10 to Dummy19, Dummy20

(2) 45 µm x 80 µm (min 60-µm pitch)
COM1/132 to COM14/119,
COM17/116 to COM30/103

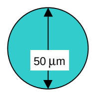
(3) 35 µm x 80 µm (min 50-µm pitch)
SEG1/168 to SEG168/1,
COM15/118, COM16/117,
COM65/68 to COM112/21,
COM31/102 to COM132/1

Au bump pitch: see the pad coordinates
Height of the Au bump: 15 µm (typ.)
Numbers in the figure correspond to pad no.

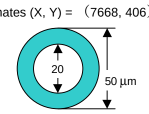
Alignment mark
(1) Alignment: two points
Coordinates (X, Y) = (±7642, 613)



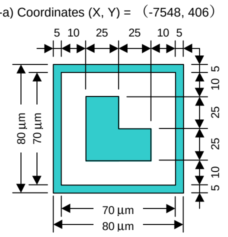
(2-a) Coordinates (X, Y) = (-7668, 406)



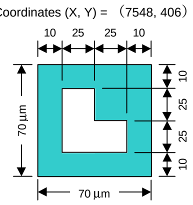
(2-b) Coordinates (X, Y) = (7668, 406)



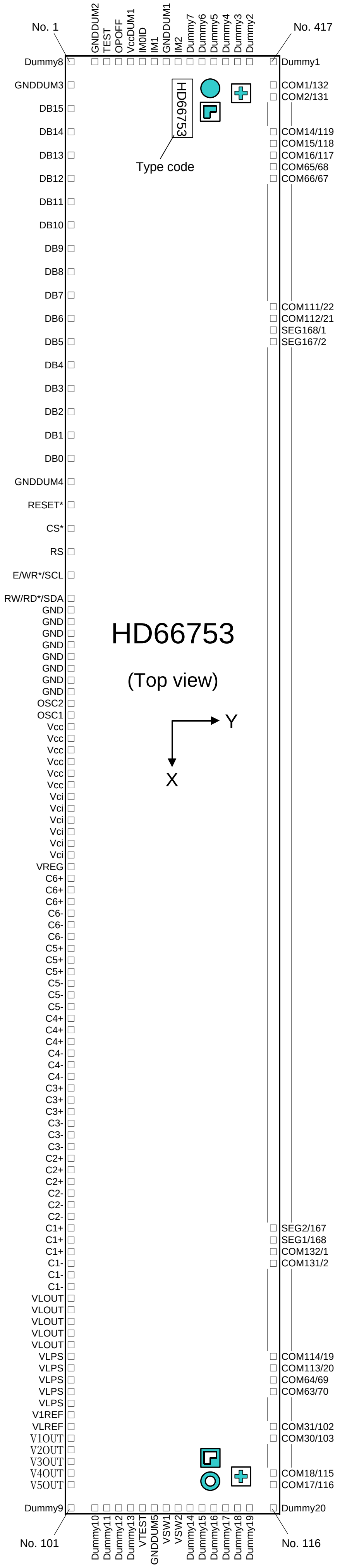
(3-a) Coordinates (X, Y) = (-7548, 406)



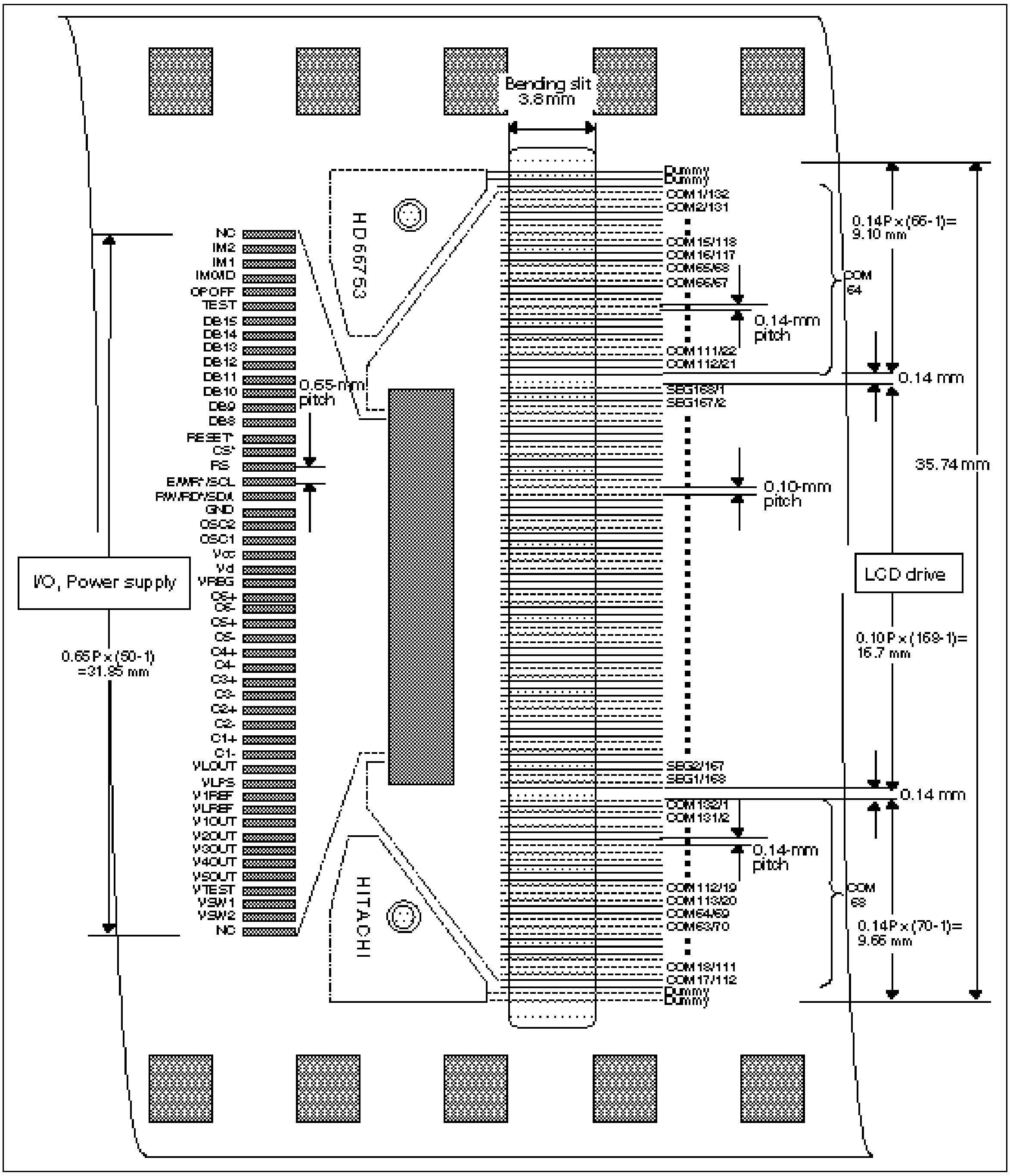
(3-b) Coordinates (X, Y) = (7548, 406)



Update history
Rev 0.0: newly created
Rev 0.1: pad coordinate no. updated,
type code added
Rev 0.2: pin name modified in Au bump
size (3)



TCP External Dimensions (HD66753TB0L/R)



HD66753 Pad Coordinates

No.	Pad Name	X	Y
1	Dummy8	-7788	-848
2	GNDDUM3	-7610	-848
3	DB15	-7395	-848
4	DB14	-7071	-848
5	DB13	-6747	-848
6	DB12	-6423	-848
7	DB11	-6099	-848
8	DB10	-5775	-848
9	DB9	-5451	-848
10	DB8	-5126	-848
11	DB7	-4802	-848
12	DB6	-4478	-848
13	DB5	-4154	-848
14	DB4	-3830	-848
15	DB3	-3506	-848
16	DB2	-3181	-848
17	DB1	-2857	-848
18	DB0	-2533	-848
19	GNDDUM4	-2319	-848
20	RESET*	-2105	-848
21	CS*	-1781	-848
22	RS	-1456	-848
23	E/WR*/SCL	-1132	-848
24	RW/RD*/SDA	-808	-848
25	GND	-594	-848
26	GND	-494	-848
27	GND	-394	-848
28	GND	-294	-848
29	GND	-193	-848
30	GND	-93	-848
31	GND	7	-848
32	GND	107	-848
33	OSC2	358	-848
34	OSC1	682	-848
35	Vcc	932	-848
36	Vcc	1032	-848
37	Vcc	1132	-848
38	Vcc	1233	-848
39	Vcc	1333	-848
40	Vcc	1433	-848
41	Vci	1576	-848
42	Vci	1676	-848
43	Vci	1776	-848
44	Vci	1876	-848
45	Vci	1976	-848
46	Vci	2076	-848
47	VREG	2176	-848
48	C6+	2319	-848
49	C6+	2419	-848
50	C6+	2519	-848
51	C6-	2619	-848
52	C6-	2719	-848
53	C6-	2819	-848
54	C5+	2920	-848
55	C5+	3020	-848
56	C5+	3120	-848
57	C5-	3220	-848
58	C5-	3320	-848
59	C5-	3420	-848
60	C4+	3520	-848
61	C4+	3620	-848
62	C4+	3720	-848
63	C4-	3820	-848
64	C4-	3921	-848
65	C4-	4021	-848
66	C3+	4121	-848
67	C3+	4221	-848
68	C3+	4321	-848
69	C3-	4421	-848
70	C3-	4521	-848
71	C3-	4621	-848
72	C2+	4721	-848
73	C2+	4821	-848
74	C2+	4922	-848

HD66753 Pad Coordinates (cont)

No.	Pad Name	X	Y
75	C2-	5022	-848
76	C2-	5122	-848
77	C2-	5222	-848
78	C1+	5322	-848
79	C1+	5422	-848
80	C1+	5522	-848
81	C1-	5622	-848
82	C1-	5722	-848
83	C1-	5823	-848
84	VLOUT	5965	-848
85	VLOUT	6065	-848
86	VLOUT	6166	-848
87	VLOUT	6266	-848
88	VLOUT	6366	-848
89	VLPS	6466	-848
90	VLPS	6566	-848
91	VLPS	6666	-848
92	VLPS	6766	-848
93	VLPS	6866	-848
94	V1REF	7009	-848
95	VLREF	7109	-848
96	V1OUT	7209	-848
97	V2OUT	7309	-848
98	V3OUT	7409	-848
99	V4OUT	7510	-848
100	V5OUT	7610	-848
101	Dummy9	7788	-848
102	Dummy10	7788	-635
103	Dummy11	7788	-535
104	Dummy12	7788	-435
105	Dummy13	7788	-335
106	VTEST	7788	-235
107	GNDDUM5	7788	-135
108	VSW1	7788	-34
109	VSW2	7788	66
110	Dummy14	7788	166
111	Dummy15	7788	266

No.	Pad Name	X	Y
112	Dummy16	7788	366
113	Dummy17	7788	466
114	Dummy18	7788	566
115	Dummy19	7788	666
116	Dummy20	7788	880
117	COM17/116	7628	880
118	COM18/115	7568	880
119	COM19/114	7508	880
120	COM20/113	7448	880
121	COM21/112	7388	880
122	COM22/111	7328	880
123	COM23/110	7268	880
124	COM24/109	7207	880
125	COM25/108	7147	880
126	COM26/107	7087	880
127	COM27/106	7027	880
128	COM28/105	6967	880
129	COM29/104	6907	880
130	COM30/103	6847	880
131	COM31/102	6792	880
132	COM32/101	6742	880
133	COM33/100	6691	880
134	COM34/99	6641	880
135	COM35/98	6591	880
136	COM36/97	6541	880
137	COM37/96	6491	880
138	COM38/95	6441	880
139	COM39/94	6391	880
140	COM40/93	6341	880
141	COM41/92	6290	880
142	COM42/91	6240	880
143	COM43/90	6190	880
144	COM44/89	6140	880
145	COM45/88	6090	880
146	COM46/87	6040	880
147	COM47/86	5990	880
148	COM48/85	5940	880

HD66753 Pad Coordinates (cont)

No.	Pad Name	X	Y
149	COM49/84	5889	880
150	COM50/83	5839	880
151	COM51/82	5789	880
152	COM52/81	5739	880
153	COM53/80	5689	880
154	COM54/79	5639	880
155	COM55/78	5589	880
156	COM56/77	5539	880
157	COM57/76	5488	880
158	COM58/75	5438	880
159	COM59/74	5388	880
160	COM60/73	5338	880
161	COM61/72	5288	880
162	COM62/71	5238	880
163	COM63/70	5188	880
164	COM64/69	5138	880
165	COM113/20	5087	880
166	COM114/19	5037	880
167	COM115/18	4987	880
168	COM116/17	4937	880
169	COM117/16	4887	880
170	COM118/15	4837	880
171	COM119/14	4787	880
172	COM120/13	4737	880
173	COM121/12	4686	880
174	COM122/11	4636	880
175	COM123/10	4586	880
176	COM124/9	4536	880
177	COM125/8	4486	880
178	COM126/7	4436	880
179	COM127/6	4386	880
180	COM128/5	4336	880
181	COM129/4	4285	880
182	COM130/3	4235	880
183	COM131/2	4185	880
184	COM132/1	4135	880
185	SEG1/168	4085	880
186	SEG2/167	4035	880
187	SEG3/166	3985	880
188	SEG4/165	3935	880
189	SEG5/164	3885	880
190	SEG6/163	3834	880
191	SEG7/162	3784	880
192	SEG8/161	3734	880
193	SEG9/160	3684	880
194	SEG10/159	3634	880
195	SEG11/158	3584	880
196	SEG12/157	3534	880
197	SEG13/156	3484	880
198	SEG14/155	3433	880
199	SEG15/154	3383	880
200	SEG16/153	3333	880
201	SEG17/152	3283	880
202	SEG18/151	3233	880
203	SEG19/150	3183	880
204	SEG20/149	3133	880
205	SEG21/148	3083	880
206	SEG22/147	3032	880
207	SEG23/146	2982	880
208	SEG24/145	2932	880
209	SEG25/144	2882	880
210	SEG26/143	2832	880
211	SEG27/142	2782	880
212	SEG28/141	2732	880
213	SEG29/140	2682	880
214	SEG30/139	2631	880
215	SEG31/138	2581	880
216	SEG32/137	2531	880
217	SEG33/136	2481	880
218	SEG34/135	2431	880
219	SEG35/134	2381	880
220	SEG36/133	2331	880
221	SEG37/132	2281	880
222	SEG38/131	2230	880

HD66753 Pad Coordinates (cont)

No.	Pad Name	X	Y	No.	Pad Name	X	Y
223	SEG39/130	2180	880	260	SEG76/93	326	880
224	SEG40/129	2130	880	261	SEG77/92	276	880
225	SEG41/128	2080	880	262	SEG78/91	226	880
226	SEG42/127	2030	880	263	SEG79/90	175	880
227	SEG43/126	1980	880	264	SEG80/89	125	880
228	SEG44/125	1930	880	265	SEG81/88	75	880
229	SEG45/124	1880	880	266	SEG82/87	25	880
230	SEG46/123	1829	880	267	SEG83/86	-25	880
231	SEG47/122	1779	880	268	SEG84/85	-75	880
232	SEG48/121	1729	880	269	SEG85/84	-125	880
233	SEG49/120	1679	880	270	SEG86/83	-175	880
234	SEG50/119	1629	880	271	SEG87/82	-226	880
235	SEG51/118	1579	880	272	SEG88/81	-276	880
236	SEG52/117	1529	880	273	SEG89/80	-326	880
237	SEG53/116	1479	880	274	SEG90/79	-376	880
238	SEG54/115	1428	880	275	SEG91/78	-426	880
239	SEG55/114	1378	880	276	SEG92/77	-476	880
240	SEG56/113	1328	880	277	SEG93/76	-526	880
241	SEG57/112	1278	880	278	SEG94/75	-576	880
242	SEG58/111	1228	880	279	SEG95/74	-627	880
243	SEG59/110	1178	880	280	SEG96/73	-677	880
244	SEG60/109	1128	880	281	SEG97/72	-727	880
245	SEG61/108	1078	880	282	SEG98/71	-777	880
246	SEG62/107	1028	880	283	SEG99/70	-827	880
247	SEG63/106	977	880	284	SEG100/69	-877	880
248	SEG64/105	927	880	285	SEG101/68	-927	880
249	SEG65/104	877	880	286	SEG102/67	-977	880
250	SEG66/103	827	880	287	SEG103/66	-1028	880
251	SEG67/102	777	880	288	SEG104/65	-1078	880
252	SEG68/101	727	880	289	SEG105/64	-1128	880
253	SEG69/100	677	880	290	SEG106/63	-1178	880
254	SEG70/99	627	880	291	SEG107/62	-1228	880
255	SEG71/98	576	880	292	SEG108/61	-1278	880
256	SEG72/97	526	880	293	SEG109/60	-1328	880
257	SEG73/96	476	880	294	SEG110/59	-1378	880
258	SEG74/95	426	880	295	SEG111/58	-1428	880
259	SEG75/94	376	880	296	SEG112/57	-1479	880

HD66753 Pad Coordinates (cont)

No.	Pad Name	X	Y
297	SEG113/56	-1529	880
298	SEG114/55	-1579	880
299	SEG115/54	-1629	880
300	SEG116/53	-1679	880
301	SEG117/52	-1729	880
302	SEG118/51	-1779	880
303	SEG119/50	-1829	880
304	SEG120/49	-1880	880
305	SEG121/48	-1930	880
306	SEG122/47	-1980	880
307	SEG123/46	-2030	880
308	SEG124/45	-2080	880
309	SEG125/44	-2130	880
310	SEG126/43	-2180	880
311	SEG127/42	-2230	880
312	SEG128/41	-2281	880
313	SEG129/40	-2331	880
314	SEG130/39	-2381	880
315	SEG131/38	-2431	880
316	SEG132/37	-2481	880
317	SEG133/36	-2531	880
318	SEG134/35	-2581	880
319	SEG135/34	-2631	880
320	SEG136/33	-2682	880
321	SEG137/32	-2732	880
322	SEG138/31	-2782	880
323	SEG139/30	-2832	880
324	SEG140/29	-2882	880
325	SEG141/28	-2932	880
326	SEG142/27	-2982	880
327	SEG143/26	-3032	880
328	SEG144/25	-3083	880
329	SEG145/24	-3133	880
330	SEG146/23	-3183	880
331	SEG147/22	-3233	880
332	SEG148/21	-3283	880
333	SEG149/20	-3333	880

No.	Pad Name	X	Y
334	SEG150/19	-3383	880
335	SEG151/18	-3433	880
336	SEG152/17	-3484	880
337	SEG153/16	-3534	880
338	SEG154/15	-3584	880
339	SEG155/14	-3634	880
340	SEG156/13	-3684	880
341	SEG157/12	-3734	880
342	SEG158/11	-3784	880
343	SEG159/10	-3834	880
344	SEG160/9	-3885	880
345	SEG161/8	-3935	880
346	SEG162/7	-3985	880
347	SEG163/6	-4035	880
348	SEG164/5	-4085	880
349	SEG165/4	-4135	880
350	SEG166/3	-4185	880
351	SEG167/2	-4235	880
352	SEG168/1	-4285	880
353	COM112/21	-4336	880
354	COM111/22	-4386	880
355	COM110/23	-4436	880
356	COM109/24	-4486	880
357	COM108/25	-4536	880
358	COM107/26	-4586	880
359	COM106/27	-4636	880
360	COM105/28	-4686	880
361	COM104/29	-4737	880
362	COM103/30	-4787	880
363	COM102/31	-4837	880
364	COM101/32	-4887	880
365	COM100/33	-4937	880
366	COM99/34	-4987	880
367	COM98/35	-5037	880
368	COM97/36	-5087	880
369	COM96/37	-5138	880
370	COM95/38	-5188	880

HD66753 Pad Coordinates (cont)

No.	Pad Name	X	Y
371	COM94/39	-5238	880
372	COM93/40	-5288	880
373	COM92/41	-5338	880
374	COM91/42	-5388	880
375	COM90/43	-5438	880
376	COM89/44	-5488	880
377	COM88/45	-5539	880
378	COM87/46	-5589	880
379	COM86/47	-5639	880
380	COM85/48	-5689	880
381	COM84/49	-5739	880
382	COM83/50	-5789	880
383	COM82/51	-5839	880
384	COM81/52	-5889	880
385	COM80/53	-5940	880
386	COM79/54	-5990	880
387	COM78/55	-6040	880
388	COM77/56	-6090	880
389	COM76/57	-6140	880
390	COM75/58	-6190	880
391	COM74/59	-6240	880
392	COM73/60	-6290	880
393	COM72/61	-6341	880
394	COM71/62	-6391	880
395	COM70/63	-6441	880
396	COM69/64	-6491	880
397	COM68/65	-6541	880
398	COM67/66	-6591	880
399	COM66/67	-6641	880
400	COM65/68	-6691	880
401	COM16/117	-6742	880
402	COM15/118	-6792	880
403	COM14/119	-6847	880
404	COM13/120	-6907	880
405	COM12/121	-6967	880
406	COM11/122	-7027	880
407	COM10/123	-7087	880
408	COM9/124	-7147	880
409	COM8/125	-7207	880
410	COM7/126	-7268	880
411	COM6/127	-7328	880
412	COM5/128	-7388	880
413	COM4/129	-7448	880
414	COM3/130	-7508	880
415	COM2/131	-7568	880
416	COM1/132	-7628	880
417	Dummy1	-7788	880
418	Dummy2	-7788	666
419	Dummy3	-7788	566
420	Dummy4	-7788	466
421	Dummy5	-7788	366
422	Dummy6	-7788	266
423	Dummy7	-7788	166
424	IM2	-7788	66
425	GNDDUM1	-7788	-34
426	IM1	-7788	-135
427	IM0ID	-7788	-235
428	VccDUM1	-7788	-335
429	OPOFF	-7788	-435
430	TEST	-7788	-535
431	GNDDUM2	-7788	-635

Alignment Mark	X	Y
Cross	-7642	613
	7642	613
Circle (positive)	-7668	406
Circle (negative)	7668	406
L type (positive)	-7548	406
L type (negative)	7548	406

Pin Functions

Table 2 Pin Functional Description

<table>
<tr><th>Signals</th><th>Number of Pins</th><th>I/O</th><th>Connected to</th><th>Functions</th></tr>
<tr><td>IM2, IM1, IM0/ID</td><td>3</td><td>I</td><td>GND or V_{CC}</td><td>Selects the MPU interface mode:
<table>
<tr><th>IM2</th><th>IM1</th><th>IM0</th><th>MPU interface mode</th></tr>
<tr><td>GND</td><td>GND</td><td>GND</td><td>68-system 16-bit bus interface</td></tr>
<tr><td>GND</td><td>GND</td><td>Vcc</td><td>68-system 8-bit bus interface</td></tr>
<tr><td>GND</td><td>Vcc</td><td>GND</td><td>80-system 16-bit bus interface</td></tr>
<tr><td>GND</td><td>Vcc</td><td>Vcc</td><td>80-system 8-bit bus interface</td></tr>
<tr><td>Vcc</td><td>GND</td><td>ID</td><td>Clock-synchronized serial interface</td></tr>
<tr><td>Vcc</td><td>Vcc</td><td>ID</td><td>I2C bus interface</td></tr>
</table>
When a serial interface is selected, the IM0 pin is used for setting the device code ID.</td></tr>
<tr><td>CS*</td><td>1</td><td>I</td><td>MPU</td><td>Selects the HD66753:
Low: HD66753 is selected and can be accessed
High: HD66753 is not selected and cannot be accessed
Must be fixed at GND level when not in use.</td></tr>
<tr><td>RS</td><td>1</td><td>I</td><td>MPU</td><td>Selects the register.
Low: Index/status High: Control
Must be fixed at Vcc or GND level for a clock-synchronized interface.</td></tr>
<tr><td>E/WR*/SCL</td><td>1</td><td>I</td><td>MPU</td><td>For a 68-system bus interface, serves as an enable signal to activate data read/write operation.
For an 80-system bus interface, serves as a write strobe signal and writes data at the low level.
For a clock-synchronized interface, serves as a synchronized clock signal.</td></tr>
<tr><td>RW/RD*/SDA</td><td>1</td><td>I/O</td><td>MPU</td><td>For a 68-system bus interface, serves as a signal to select data read/write operation.
Low: Write High: Read
For an 80-system bus interface, serves as a read strobe signal and reads data at the low level.
For a clock-synchronized interface, serves as a bidirectional serial transfer data to receive and send the data.</td></tr>
<tr><td>DB0–DB15</td><td>16</td><td>I/O</td><td>MPU</td><td>Serves as a 16-bit bidirectional data bus.
For an 8-bit bus interface, data transfer uses DB15-DB8; fix unused DB7-DB0 to the Vcc or GND level.
For a clock-synchronized interface, fix DB15-DB0 to the Vcc or GND level.</td></tr>
</table>

Table 2 Pin Functional Description (cont)

Signals	Number of Pins	I/O	Connected to	Functions
COM1/132 – COM132/1	132	O	LCD	Output signals for common drive: All the unused pins output unselected waveforms. In the display-off period (D = 0), sleep mode (SLP = 1), or standby mode (STB = 1), all pins output GND level. The CMS bit can change the shift direction of the common signal. For example, if CMS = 0, COM1/132 is COM1, and COM132/1 is COM132. If CMS = 1, COM1/132 is COM132, and COM132/1 is COM1.
SEG1/168 – SEG168/1	168	O	LCD	Output signals for segment drive. In the display-off period (D = 0), sleep mode (SLP = 1), or standby mode (STB = 1), all pins output GND level. The SGS bit can change the shift direction of the segment signal. For example, if SGS = 0, SEG1/168 is SEG1. If SGS = 1, SEG1/168 is SEG168.
V1OUT–V5OUT	5	I or O	Open or external bleeder-resistor	Used for output from the internal operational amplifiers when they are used (OPOFF = GND); attach a capacitor to stabilize the output. When the amplifiers are not used (OPOFF = V_{CC}), V1 to V5 voltages can be supplied to these pins externally.
V_{LPS}	1	—	Power supply	Power supply for LCD drive. V_{LPS} = 19.5 V max.
V_{CC}, GND	2	—	Power supply	V_{CC}: +1.7 V to + 3.6 V; GND (logic): 0 V
OSC1, OSC2	2	I or O	Oscillation-resistor or clock	For R-C oscillation using an external resistor, connect an external resistor. For external clock supply, input clock pulses to OSC1.
Vci	1	I	Power supply	Inputs a reference voltage and supplies power to the step-up circuit; generates the liquid crystal display drive voltage from the operating voltage. The step-up output voltage must not be larger than the absolute maximum ratings. Must be left disconnected when the step-up circuit is not used.
VLOUT	1	O	V_{LPS} pin/step-up capacitance	Potential difference between Vci and GND is two- to seven-times-stepped up and then output. Magnitude of step-up is selected by instruction.
C1+, C1–	2	—	Step-up capacitance	External capacitance should be connected here when using the five-times or more step-up.
C2+, C2–	2	—	Step-up capacitance	External capacitance should be connected here for step-up.
C3+, C3–	2	—	Step-up capacitance	External capacitance should be connected here for step-up.
C4+, C4–	2	—	Step-up capacitance	External capacitance should be connected here when using the five-times or more step-up.
C5+, C5–	2	—	Step-up capacitance	External capacitance should be connected here for step-up.
C6+, C6–	2	—	Step-up capacitance	External capacitance should be connected here for step-up.

Table 2 Pin Functional Description (cont)

Signals	Number of Pins	I/O	Connected to	Functions
RESET*	1	I	MPU or external R-C circuit	Reset pin. Initializes the LSI when low. Must be reset after power-on.
OPOFF	1	I	V_{CC} or GND	Turns the internal operational amplifier off when OPOFF = V_{CC}, and turns it on when OPOFF = GND. If the amplifier is turned off (OPOFF = V_{CC}), V1 to V5 must be supplied to the V1OUT to V5OUT pins.
VSW1	1	I	GND	Test pin. Must be fixed at GND level.
VSW2	1	—	—	Test pin. Must be left disconnected.
VREG	1	I	Input pin	Input pin for the reference voltage of the LCD-drive-voltage regulator circuit. Connect Vci or external power supply.
V1REF	1	O	Output pin	Output pin for the LCD-drive-voltage regulator circuit. Must be left disconnected when not in use.
VLREF	1	I	Input pin	Connected to the top electrode of the internal bleeder-resistor. Use this pin to supply the LCD voltage externally.
VccDUM	1	O	Input pins	Outputs the internal V_{CC} level; shorting this pin sets the adjacent input pin to the V_{CC} level.
GNDDUM	3	O	Input pins	Outputs the internal GND level; shorting this pin sets the adjacent input pin to the GND level.
Dummy	4	—	—	Dummy pad. Must be left disconnected.
TEST	1	I	GND	Test pin. Must be fixed at GND level.
VTEST	1	—	—	Test pin. Must be left disconnected.

Block Function Description

System Interface

The HD66753 has five high-speed system interfaces: an 80-system 16-bit/8-bit bus, a 68-system 16-bit/8-bit bus, and a clock-synchronized serial interface. The interface mode is selected by the IM2-0 pins.

The HD66753 has three 16-bit registers: an index register (IR), a write data register (WDR), and a read data register (RDR). The IR stores index information from the control registers and the CGRAM. The WDR temporarily stores data to be written into control registers and the CGRAM, and the RDR temporarily stores data read from the CGRAM. Data written into the CGRAM from the MPU is first written into the WDR and then is automatically written into the CGRAM by internal operation. Data is read through the RDR when reading from the CGRAM, and the first read data is invalid and the second and the following data are normal (for the serial interface, the 5-byte data is invalid). When a logic operation is performed inside of the HD66753 by using the display data set in the CGRAM and the data written from the MPU, the data read through the RDR is used. Accordingly, the MPU does not need to read data twice nor to fetch the read data into the MPU. This enables high-speed processing.

Execution time for instruction excluding oscillation start is 0 clock cycle and instructions can be written in succession.

Table 3 Register Selection

R/W Bits	RS Bits	Operations
0	0	Writes indexes into IR
1	0	Status read
0	1	Writes into control registers and CGRAM through WDR
1	1	Reads from CGRAM through RDR

Bit Operation

The HD66753 supports the following functions: a bit rotation function that writes the data written from the MPU into the CGRAM by moving the display position in bit units, a write data mask function that selects and writes data into the CGRAM in bit units, and a logic operation function that performs logic operations on the display data set in the CGRAM and writes into the CGRAM. With the 16-bit bus interface, these functions can greatly reduce the processing loads of the MPU graphics software and can rewrite the display data in the CGRAM at high speed. For details, see the Graphics Operation Function section.

Address Counter (AC)

The address counter (AC) assigns addresses to the CGRAM. When an address set instruction is written into the IR, the address information is sent from the IR to the AC.

After writing into the CGRAM, the AC is automatically incremented by 1 (or decremented by 1). After reading from the data, the RDM bit automatically updates or does not update the AC.

Graphic RAM (CGRAM)

The graphic RAM (CGRAM) stores bit-pattern data of 168 x 132 dots. It has two bits/pixel and 4,096-byte capacity.

Grayscale Control Circuit

The grayscale control circuit performs four-grayscale control with the frame rate control (FRC) method for four-monochrome grayscale display. For details, see the Four Grayscale Display Function section.

Timing Generator

The timing generator generates timing signals for the operation of internal circuits such as the CGRAM. The RAM read timing for display and internal operation timing by MPU access are generated separately to avoid interference with one another.

Oscillation Circuit (OSC)

The HD66753 can provide R-C oscillation simply through the addition of an external oscillation-resistor between the OSC1 and OSC2 pins. The appropriate oscillation frequency for operating voltage, display size, and frame frequency can be obtained by adjusting the external-resistor value. Clock pulses can also be supplied externally. Since R-C oscillation stops during the standby mode, current consumption can be reduced. For details, see the Oscillation Circuit section.

Liquid Crystal Display Driver Circuit

The liquid crystal display driver circuit consists of 132 common signal drivers (COM1 to COM132) and 168 segment signal drivers (SEG1 to SEG168). When the number of lines are selected by a program, the required common signal drivers automatically output drive waveforms, while the other common signal drivers continue to output unselected waveforms.

Display pattern data is latched when 168-bit data has arrived. The latched data then enables the segment signal drivers to generate drive waveform outputs. The shift direction of 168-bit data can be changed by the SGS bit. The shift direction for the common driver can also be changed by the CMS bit by selecting an appropriate direction for the device mounting configuration.

When multiplexing drive is not used, or during the standby or sleep mode, all the above common and segment signal drivers output the GND level, halting the display.

Step-up Circuit (DC-DC Converter)

The step-up generates three-, five-, six-, or seven-times voltage input to the Vci pin. With this, both the internal logic units and LCD drivers can be controlled with a single power supply. Step-up output level from three-times to seven-times step-up can be selected by software. For details, see the Liquid Crystal Display Voltage Generator section.

V-Pin Voltage Follower

A voltage follower for each voltage level (V1 to V5) reduces current consumption by the LCD drive power supply circuit. No external resistors are required because of the internal bleeder-resistor, which generates different levels of LCD drive voltage. This internal bleeder-resistor can be software-specified from 1/4 bias to 1/11 bias, according to the liquid crystal display drive duty value. The voltage followers can be turned off while multiplexing drive is not being used. For details, see the Power Supply for Liquid Crystal Display Drive section.

Contrast Adjuster

The contrast adjuster can be used to adjust LCD contrast in 128 steps by varying the LCD drive voltage by software. This can be used to select an appropriate LCD brightness or to compensate for temperature.

LCD-Drive Power-Supply Regulator Circuit

The LCD-drive power-supply regulator circuit generates an LCD-drive voltage from the reference voltage that does not depend on the LCD load current. Change of the LCD-drive voltage is controlled for the LCD load current. For details, see the Liquid Crystal Display Voltage Generator section.

CGRAM Address Map

Table 4 Relationships between the CGRAM Address and the Display Screen Position

Segment Driver		SEG1/168	SEG2/167	SEG3/166	SEG4/165	SEG5/164	SEG6/163	SEG7/162	SEG8/161	SEG9/160 --- SEG16/153	SEG17/152 --- SEG24/145	------	SEG161/8 -- SEG168/1
Bit	SGS="0"	D0 D1	D2 D3	D4 D5	D6 D7	D8 D9	D10 D11	D12 D13	D14 D15	D0 D1 --- D15	D0 D1 --- D15	------	D0 D1 -- D15
	SGS="1"	D15 D14	D13 D12	D11 D10	D9 D8	D7 D6	D5 D4	D3 D2	D1 D0	D15 D14 --- D0	D15 D14 --- D0	--------	D15 D14 -- D0
COM1		Address:'0000'H								'0001'H	'0002'H	--------	'0014'H
COM2		Address:'0020'H								'0021'H	'0022'H	--------	'0034'H
COM3		Address:'0040'H								'0041'H	'0042'H	--------	'0054'H
COM4		Address:'0060'H								'0061'H	'0062'H	--------	'0074'H
COM5		Address:'0080'H								'0081'H	'0082'H	--------	'0094'H
COM6		Address:'00A0'H								'00A1'H	'00A2'H	--------	'00B4'H
COM7		Address:'00C0'H								'00C1'H	'00C2'H	--------	'00D4'H
COM8		Address:'00E0'H								'00E1'H	'00E2'H	--------	'00F4'H
COM9		Address:'0100'H								'0101'H	'0102'H	--------	'0114'H
COM10		Address:'0120'H								'0121'H	'0122'H	--------	'0134'H
COM11		Address:'0140'H								'0141'H	'0142'H	--------	'0154'H
COM12		Address:'0160'H								'0161'H	'0162'H	--------	'0174'H
COM13		Address:'0180'H								'0181'H	'0182'H	--------	'0194'H
COM14		Address:'01A0'H								'01A1'H	'01A2'H	--------	'01B4'H
COM15		Address:'01C0'H								'01C1'H	'01C2'H	--------	'01D4'H
COM16		Address:'01E0'H								'01E1'H	'01E2'H	--------	'01F4'H
COM17		Address:'0200'H								'0201'H	'0202'H	--------	'0214'H
COM18		Address:'0220'H								'0221'H	'0222'H	--------	'0234'H
COM19		Address:'0240'H								'0241'H	'0242'H	--------	'0254'H
COM20		Address:'0260'H								'0261'H	'0262'H	--------	'0274'H
⋮		⋮								⋮	⋮	--------	⋮
COM125		Address:'0F80'H								'0F81'H	'0F82'H	--------	'0F94'H
COM126		Address:'0FA0'H								'0FA1'H	'0FA2'H	--------	'0FB4'H
COM127		Address:'0FC0'H								'0FC1'H	'0FC2'H	--------	'0FD4'H
COM128		Address:'0FE0'H								'0FE1'H	'0FE2'H	--------	'0FF4'H
COM129		Address:'1000'H								'1001'H	'1002'H	--------	'1014'H
COM130		Address:'1020'H								'1021'H	'1022'H	--------	'1034'H
COM131		Address:'1040'H								'1041'H	'1042'H	--------	'1054'H
COM132		Address:'1060'H								'1061'H	'1062'H	--------	'1074'H

Table 5 Relationships between the CGRAM Data and the Display Contents

Upper Bit	Lower Bit	LCD
0	0	Non-selection display (unlit)
0	1	1/4-, 1/3- or 2/4-level grayscale display (selected by the GSL1-0 bits)
1	0	1/4-, 2/3-, or 3/4-level grayscale display (selected by the GSH1-0 bits)
1	1	Selection display (lit)

Note: Upper bits: DB15, DB13, DB11, DB9, DB7, DB5, DB3, DB1
Lower bits: DB14, DB12, DB10, DB8, DB6, DB4, DB2, DB0

Instructions

Outline

The HD66753 uses the 16-bit bus architecture. Before the internal operation of the HD66753 starts, control information is temporarily stored in the registers described below to allow high-speed interfacing with a high-performance microcomputer. The internal operation of the HD66753 is determined by signals sent from the microcomputer. These signals, which include the register selection signal (RS), the read/write signal (R/W), and the data bus signals (DB15 to DB0), make up the HD66753 instructions. There are seven categories of instructions that:

- Specify the index
- Read the status
- Control the display
- Control power management
- Process the graphics data
- Set internal CGRAM addresses
- Transfer data to and from the internal CGRAM

Normally, instructions that write data are used the most. However, an auto-update of internal CGRAM addresses after each data write can lighten the microcomputer program load.

Because instructions are executed in 0 cycles, they can be written in succession.

Instruction Descriptions

Index (IR)

The index instruction specifies the RAM control and control register indexes (R00 to R12). It sets the register number in the range of 00000 to 10010 in binary form.

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	-	-	-	-	-	-	-	-	-	-	-	ID4	ID3	ID2	ID1	ID0

Figure 1 Index Instruction

Status Read (SR)

The status read instruction reads the internal status of the HD66753.

L7–0: Indicate the driving raster-row position where the liquid crystal display is being driven.

C6–0: Read the contrast setting values (CT6–0).

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	L7	L6	L5	L4	L3	L2	L1	L0	0	C6	C5	C4	C3	C2	C1	C0

Figure 2 Status Read Instruction

Start Oscillation (R00)

The start oscillation instruction restarts the oscillator from the halt state in the standby mode. After issuing this instruction, wait at least 10 ms for oscillation to stabilize before issuing the next instruction. (See the Standby Mode section.)

If this register is read forcibly as R/W = 1, 0753H is read.

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	1
1	1	0	0	0	0	0	1	1	1	0	1	0	1	0	0	0	0

Figure 3 Start Oscillation Instruction

Driver Output Control (R01)

CMS: Selects the output shift direction of a common driver. When CMS = 0, COM1/132 shifts to COM1, and COM132/1 to COM132. When CMS = 1, COM1/132 shifts to COM132, and COM132/1 to COM1.

SGS: Selects the output shift direction of a segment driver. When SGS = 0, SEG1/168 shifts to SEG1, and SEG168/1 to SEG168. When SGS = 1, SEG1/168 shifts to SEG128, and SEG168/1 to SEG1.

NL4-0: Specify the LCD drive duty ratio. The duty ratio can be adjusted for every eight raster-rows. CGRAM address mapping does not depend on the setting value of the drive duty ratio.

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	-	-	-	-	-	-	CMS	SGS	-	-	-	NL4	NL3	NL2	NL1	NL0

Figure 4 Driver Output Control Instruction

Table 6 NL Bits and Drive Duty

NL4	NL3	NL2	NL1	NL0	Display Size	LCD Drive Duty	Common Driver Used
0	0	0	0	0	168 x 8 dots	1/8 Duty	COM1–COM8
0	0	0	0	1	168 x 16 dots	1/16 Duty	COM1–COM16
0	0	0	1	0	168 x 24 dots	1/24 Duty	COM1–COM24
0	0	0	1	1	168 x 32 dots	1/32 Duty	COM1–COM32
0	0	1	0	0	168 x 40 dots	1/40 Duty	COM1–COM40
0	0	1	0	1	168 x 48 dots	1/48 Duty	COM1–COM48
0	0	1	1	0	168 x 56 dots	1/56 Duty	COM1–COM56
0	0	1	1	1	168 x 64 dots	1/64 Duty	COM1–COM64
0	1	0	0	0	168 x 72 dots	1/72 Duty	COM1–COM72
0	1	0	0	1	168 x 80 dots	1/80 Duty	COM1–COM80
0	1	0	1	0	168 x 88 dots	1/88 Duty	COM1–COM88
0	1	0	1	1	168 x 96 dots	1/96 Duty	COM1–COM96
0	1	1	0	0	168 x 104 dots	1/104 Duty	COM1–COM104
0	1	1	0	1	168 x 112 dots	1/112 Duty	COM1–COM112
0	1	1	1	0	168 x 120 dots	1/120 Duty	COM1–COM120
0	1	1	1	1	168 x 128 dots	1/128 Duty	COM1–COM128
1	1	1	1	1	168 x 132 dots	1/132 Duty	COM1–COM132

LCD-Driving-Waveform Control (R02)

B/C: When B/C = 0, a B-pattern waveform is generated and alternates in every frame for LCD drive. When B/C = 1, a C-pattern waveform is generated and alternates in each raster-row specified by bits EOR and NW4–NW0 in the LCD-driving-waveform control register. For details, see the n-raster-row Reversed AC Drive section.

EOR: When the C-pattern waveform is set (B/C = 1) and EOR = 1, the odd/even frame-select signals and the n-raster-row reversed signals are EORed for alternating drive. EOR is used when the LCD is not alternated by combining the set values of the LCD drive duty ratio and the n raster-row. For details, see the n-raster-row Reversed AC Drive section.

NW4–0: Specify the number of raster-rows n that will alternate at the C-pattern waveform setting (B/C = 1). NW4–NW0 alternate for every set value + 1 raster-row, and the first to the 32nd raster-rows can be selected.

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	-	-	-	-	-	-	-	-	-	B/C	EOR	NW4	NW3	NW2	NW1	NW0

Figure 5 LCD-Driving-Waveform Control Instruction

Power Control (R03)

BS2–0: The LCD drive bias value is set within the range of a 1/4 to 1/11 bias. The LCD drive bias value can be selected according to its drive duty ratio and voltage. For details, see the Liquid Crystal Display Drive Bias Selector section.

BT1-0: The output factor of VLOUT between two-times, three-times, four-times, five-times, six-times, and seven-times step-up is switched. The LCD drive voltage level can be selected according to its drive duty ratio and bias. Lower amplification of the step-up circuit consumes less current.

PS1-0: Using the internal or external power supply is selected as the reference voltage for the LCD drive voltage generator.

DC1-0: The operating frequency in the step-up circuit is selected. When the step-up operating frequency is high, the driving ability of the step-up circuit and the display quality become high, but the current consumption is increased. Adjust the frequency considering the display quality and the current consumption.

AP1-0: The amount of fixed current from the fixed current source in the operational amplifier for V pins (V1 to V5) is adjusted. When the amount of fixed current is large, the LCD driving ability and the display quality become high, but the current consumption is increased. Adjust the fixed current considering the display quality and the current consumption.

During no display, when AP1–0 = 00, the current consumption can be reduced by ending the operational amplifier and step-up circuit operation.

Table 7 BS Bits and LCD Drive Bias Value

BS2	BS1	BS0	LCD Drive Bias Value
0	0	0	1/11 bias drive
0	0	1	1/10 bias drive
0	1	0	1/9 bias drive
0	1	1	1/8 bias drive
1	0	0	1/7 bias drive
1	0	1	1/6 bias drive
1	1	0	1/5 bias drive
1	1	1	1/4 bias drive

Table 8 BT Bits and Output Level

BT1	BT0	VLOUT Output Level
0	0	Three-times step-up
0	1	Five-times step-up
1	0	Six-times step-up
1	1	Seven-times step-up

Table 9 DC Bits and Operating Clock Frequency

DC1	DC0	Operating Clock Frequency in the Step-up Circuit
0	0	32-divided clock
0	1	16-divided clock
1	0	8-divided clock
1	1	Setting inhibited

Table 10 AP Bits and Amount of Fixed Current

AP1	AP0	Amount of Fixed Current in the Operational Amplifier
0	0	Operational amplifier and booster do not operate.
0	1	Small
1	0	Middle
1	1	Large

Table 11 PS Bits and Reference Power Supply

PS1	PS0	Switching the Reference Power Supply for the LCD Voltage Generator			
		VREG Pin	**V1REF Pin**	**VLREF Pin**	**VLREF Regulator**
0	0	Input	Output from regulator	Input (internal short between V1REF and VLREF)	Used
0	1	Input	Output from regulator	Input	Used
1	0	Open	Open	Input (from external power supply)	Halt
1	1	Setting inhibited			

SLP: When SLP = 1, the HD66753 enters the sleep mode, where the internal display operations are halted except for the R-C oscillator, thus reducing current consumption. For details, see the Sleep Mode section. Only the following instructions can be executed during the sleep mode.

Power control (BS2–0, BT1–0, DC1–0, AP1–0, SLP, and STB bits)

During the sleep mode, the other CGRAM data and instructions cannot be updated although they are retained.

STB: When STB = 1, the HD66753 enters the standby mode, where display operation completely stops, halting all the internal operations including the internal R-C oscillator. Further, no external clock pulses are supplied. For details, see the Standby Mode section.

Only the following instructions can be executed during the standby mode.

a. Standby mode cancel (STB = 0)
b. Start oscillation
c. Power control (BS2–0, BT1–0, DC1–0, AP1–0, SLP, and STB bits)

During the standby mode, the CGRAM data and instructions may be lost. To prevent this, they must be set again after the standby mode is canceled.

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	-	-	-	BS2	BS1	BS0	BT1	BT0	PS1	PS0	DC1	DC0	AP1	AP0	SLP	STB

Figure 6 Power Control Instruction

Contrast Control (R04)

CT6–0: These bits control the LCD drive voltage (potential difference between V1 and GND) to adjust 128-step contrast. For details, see the Contrast Adjuster section.

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	-	-	-	-	-	VR2	VR1	VR0	-	CT6	CT5	CT4	CT3	CT2	CT1	CT0

Figure 7 Contrast Control Instruction

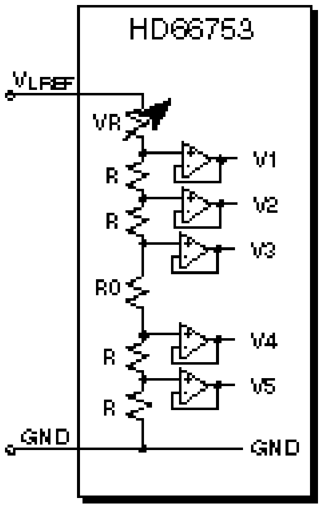


Figure 8 Contrast Adjuster

Table 12 CT Bits and Variable Resistor Value of Contrast Adjuster

CT Set Value							Variable
CT6	**CT5**	**CT4**	**CT3**	**CT2**	**CT1**	**CT0**	**Resistor (VR)**
0	0	0	0	0	0	0	6.40 x R
0	0	0	0	0	0	1	6.35 x R
0	0	0	0	0	1	0	6.30 x R
0	0	0	0	0	1	1	6.25 x R
0	0	0	0	1	0	0	6.20 x R
			•				•
			•				•
1	1	1	1	1	0	0	1.20 x R
1	1	1	1	1	0	1	0.15 x R
1	1	1	1	1	1	0	0.10 x R
1	1	1	1	1	1	1	0.05 x R

VR2–0: These bits adjust the output voltage (V1REF) for the LCD-drive reference voltage generator within the 2.8- to 6.5-times ranges of Vreg (Vci or VREG pin input voltage).

Table 13 VR Bits and V1REF Voltages

VR2	VR1	VR0	V1REF Voltage Setting
0	0	0	Vreg x 2.8
0	0	1	Vreg x 3.5
0	1	0	Vreg x 4.0
0	1	1	Vreg x 4.5
1	0	0	Vreg x 5.0
1	0	1	Vreg x 5.5
1	1	0	Vreg x 6.0
1	1	1	Vreg x 6.5

Entry Mode (R05)

Rotation (R06)

The write data sent from the microcomputer is modified in the HD66753 and written to the CGRAM. The display data in the CGRAM can be quickly rewritten to reduce the load of the microcomputer software processing. For details, see the Graphics Operation Function section.

I/D: When I/D = 1, the address counter (AC) is automatically incremented by 1 after the data is written to the CGRAM. When I/D = 0, the AC is automatically decremented by 1 after the data is written to the CGRAM.

AM1–0: Set the automatic update method of the AC after the data is written to the CGRAM. When AM1–0 = 00, the data is continuously written in parallel. When AM1–0 = 01, the data is continuously written vertically. When AM1–0 = 10, the data is continuously written vertically with two-word width (32-bit length).

LG1–0: Write again the data read from the CGRAM and the data written from the microcomputer to the CGRAM by a logical operation. When LG1–0 = 00, replace (no logical operation) is done. ORed when LG1–0 = 01, ANDed when LG1–0 = 10, and EORed when LG1–0 = 11.

RT2–0: Write the data sent from the microcomputer to the CGRAM by rotating in a bit unit. RT3–0 specify rotation. For example, when RT2–0 = 001, the data is rotated in the upper side by two bits. When RT2–0 = 111, the data is rotated in the upper side by 14 bits. The upper bit overflown in the most significant bit (MSB) side is rotated in the least significant bit (LSB) side.

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	-	-	-	-	-	-	-	-	-	-	-	I/D	AM1	AM0	LG1	LG0
0	1	-	-	-	-	-	-	-	-	-	-	-	-	-	RT2	RT1	RT0

Figure 9 Entry Mode and Rotation Instructions

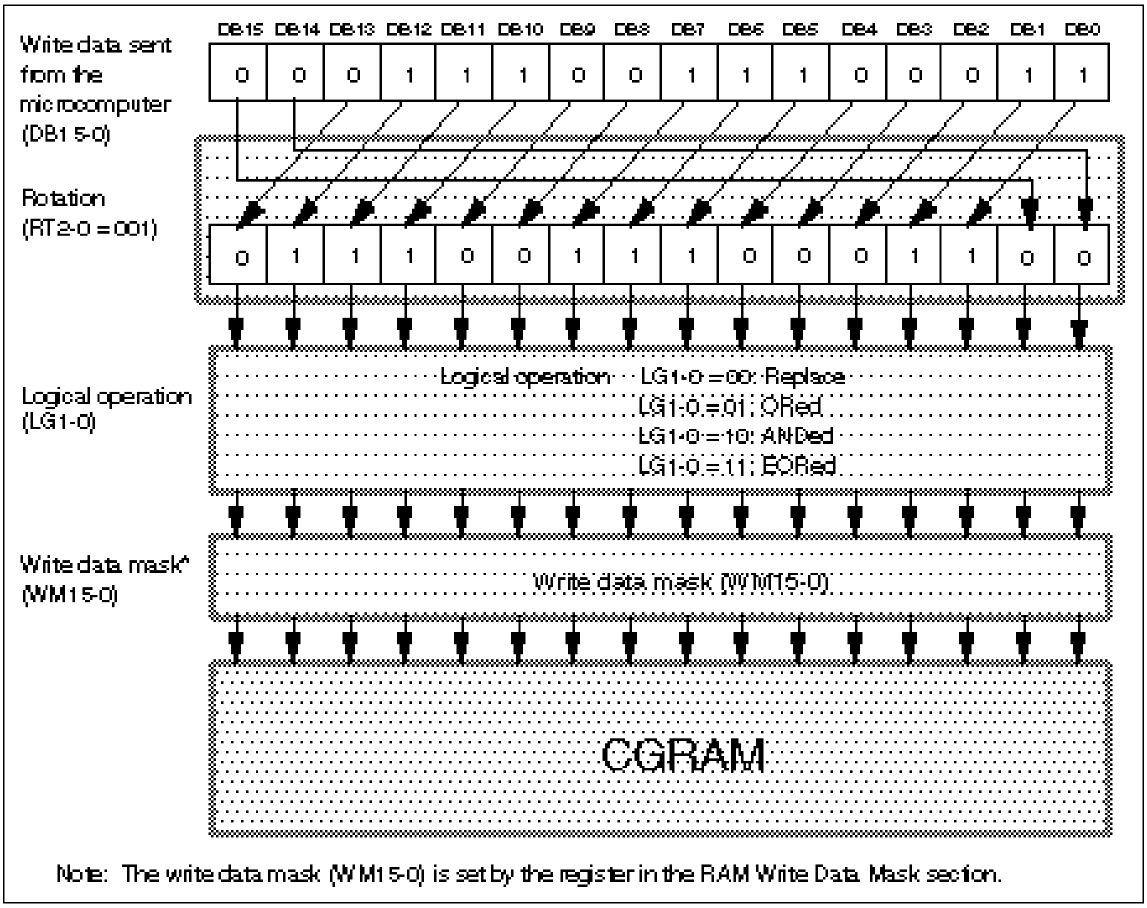


Figure 10 Logical Operation and Rotation for the CGRAM

Display Control (R07)

SPT: When SPT = 01, the 2-division LCD drive is performed. For details, see the Division Screen Drive section.

GSH1-0: When GS = 0, the grayscale level at a brightly-colored display (when DB = 10) is selected. For details, see the 4-Grayscale Display Function section.

GSL1-0: The grayscale level at a weakly-colored display (when DB = 01) is selected.

Table 14 GSH Bits and Output Level

GSH1	GSH0	Grayscale Output Level (DB = 10)
0	0	3/4 level grayscale control
0	1	2/3 level grayscale control
1	0	2/4 level grayscale control
1	1	Lit (No grayscale control)

Table 15 GSL Bits and Output Level

GSL1	GSL0	Grayscale Output Level (DB = 01)
0	0	1/4 level grayscale control
0	1	1/3 level grayscale control
1	0	2/4 level grayscale control
1	1	Lit (No grayscale control)

REV: Displays all character and graphics display sections with black-and-white reversal when REV = 1. For details, see the Reversed Display Function section.

D: Display is on when D = 1 and off when D = 0. When off, the display data remains in the CGRAM, and can be displayed instantly by setting D = 1. When D is 0, the display is off with the SEG1 to SEG168 outputs and COM1 to COM132 outputs set to the GND level. Because of this, the HD66753 can control the charging current for the LCD with AC driving.

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	-	-	-	-	-	-	-	SPT	-	-	GSH1	GSH0	GSL1	GSL0	REV	D

Figure 11 Display Control Instruction

Cursor Control (R08)

C: When C = 1, the window cursor display is started. The display mode is selected by the CM1–0 bits, and the display area is specified in a dot unit by the horizontal cursor position register (HS6–0 and HE6–0 bits) and vertical cursor position register (VS6–0 and VE6–0 bits). For details, see the Window Cursor Display section.

CM1–0: The display mode of the window cursor is selected. These bits can display a white-blink cursor, black-blink cursor, black-and-white reversed cursor, and black-and-white-reversed blink cursor.

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	-	-	-	-	-	-	-	-	-	-	-	-	-	C	CM1	CM0

Figure 12 Cursor Control Instruction

Table 16 CM Bits and Window Cursor Display Mode

CM1	CM0	Window Cursor Display Mode
0	0	White-blink cursor (alternately blinking between the normal display and an all-white display (all unlit))
0	1	Black-blink cursor (alternately blinking between the normal display and an all-black display (all lit))
1	0	Black-and-white reversed cursor (black-and-white-reversed normal display (no blinking))
1	1	Black-and-white-reversed blink cursor (alternately blinking the black-and-white-reversed normal display)

Horizontal Cursor Position (R0B)

Vertical Cursor Position (R0C)

HS7-0: Specify the start position for horizontally displaying the window cursor in a dot unit. The cursor is displayed from the 'set value + 1' dot. Ensure that HS7–0 ≤ HE7–0.

HE7-0: Specify the end position for horizontally displaying the window cursor in a dot unit. The cursor is displayed to the 'set value + 1' dot. Ensure that HS7–0 ≤ HE7–0.

VS7-0: Specify the start position for vertically displaying the window cursor in a dot unit. The cursor is displayed from the 'set value + 1' dot. Ensure that VS7–0 ≤ VE7–0.

VE7-0: Specify the end position for vertically displaying the window cursor in a dot unit. The cursor is displayed to the 'set value + 1' dot. Ensure that VS7–0 ≤ VE7–0.

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	HE7	HE6	HE5	HE4	HE3	HE2	HE1	HE0	HS7	HS6	HS5	HS4	HS3	HS2	HS1	HS0
0	1	VE7	VE6	VE5	VE4	VE3	VE2	VE1	VE0	VS7	VS6	VS5	VS4	VS3	VS2	VS1	VS0

Figure 13 Horizontal Cursor Position and Vertical Cursor Position Instructions

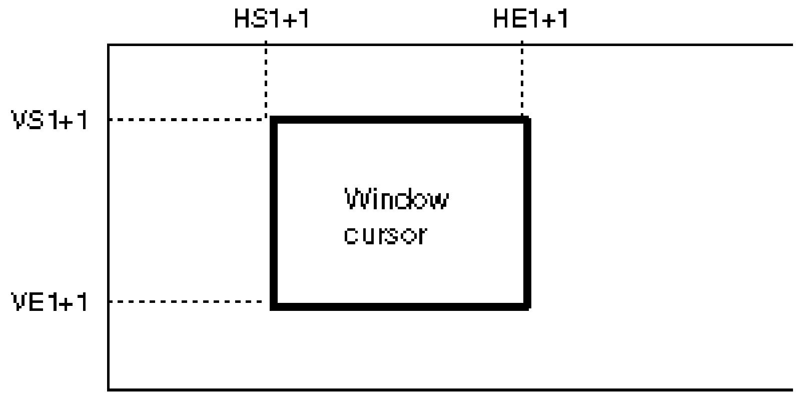


Figure 14 Window Cursor Position

1st Screen Driving Position (R0D)

2nd Screen Driving Position (R0E)

SS17-10: Specify the driving start position for the first screen in a line unit. The LCD driving starts from the 'set value + 1' common driver.

SE17-10: Specify the driving end position for the first screen in a line unit. The LCD driving is performed to the 'set value + 1' common driver. For instance, when SS17-10 = 07H and SE17-10 = 10H are set, the LCD driving is performed from COM8 to COM17, and non-selection driving is performed for COM1 to COM7, COM18, and others. Ensure that SS17–10 ≤ SE17–10 ≤ 83H. For details, see the Screen Division Driving Function section.

SS27-20: Specify the driving start position for the second screen in a line unit. The LCD driving starts from the 'set value + 1' common driver. The second screen is driven when SPT = 1.

SE27-20: Specify the driving end position for the second screen in a line unit. The LCD driving is performed to the 'set value + 1' common driver. For instance, when SPT = 1, SS27-20 = 20H, and SE27-20 = 5FH are set, the LCD driving is performed from COM33 to COM96 and the non-selected driving is performed from COM1 to COM7 and COM18 and followings. Ensure that SS17–10 ≤ SE17–10 < SS27–20 ≤ SE27–20 ≤ 83H. For details, see the Screen Division Driving Function section.

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	SE17	SE16	SE15	SE14	SE13	SE12	SE11	SE10	SS17	SS16	SS15	SS14	SS13	SS12	SS11	SS10
0	1	SE27	SE26	SE25	SE24	SE23	SE22	SE21	SE20	SS27	SS26	SS25	SS24	SS23	SS22	SS21	SS20

Figure 15 1st Screen Driving Position and 2nd Screen Driving Position

RAM Write Data Mask (R10)

WM15-0: In writing to the CGRAM, these bits mask writing in a bit unit. When WM15 = 1, this bit masks the write data of DB15 and does not write to the CGRAM. Similarly, the WM14–0 bits mask the write data of DB14–0 in a bit unit. However, when AM = 10, the write data is masked with the set values of WM15–0 for the odd-times CGRAM write. It is also masked automatically with the reversed set values of WM15–0 for the even-times CGRAM write. For details, see the Graphics Operation Function section.

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	WM 15	WM 14	WM 13	WM 12	WM 11	WM 10	WM 9	WM 8	WM 7	WM 6	WM 5	WM 4	WM 3	WM 2	WM 1	WM 0

Figure 16   RAM Write Data Mask Instruction

RAM Address Set (R11)

AD12-0: Initially set CGRAM addresses to the address counter (AC). Once the CGRAM data is written, the AC is automatically updated according to the AM1–0 and I/D bit settings. This allows consecutive accesses without resetting addresses. Once the CGRAM data is read, the AC is not automatically updated. CGRAM address setting is not allowed in the sleep mode or standby mode.

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	-	-	-	AD 12	AD 11	AD 10	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0

Figure 17 RAM Address Set Instruction

Table 17 AD Bits and CGRAM Settings

AD12–AD0	CGRAM Setting
"0000"H–"0014"H	Bitmap data for COM1
"0020"H–"0034"H	Bitmap data for COM2
"0040"H–"0054"H	Bitmap data for COM3
"0060"H–"0074"H	Bitmap data for COM4
"0080"H–"0094"H	Bitmap data for COM5
"00A0"H–"00B4"H	Bitmap data for COM6
:	:
"0FC0"H–"0FD4"H	Bitmap data for COM127
"0FE0"H–"0FF4"H	Bitmap data for COM128
"1000"H–"1014"H	Bitmap data for COM129
"1020"H–"1034"H	Bitmap data for COM130
"1040"H–"1054"H	Bitmap data for COM131
"1060"H–"1074"H	Bitmap data for COM132

Write Data to CGRAM (R12)

WD15-0 : Write 16-bit data to the CGRAM. After a write, the address is automatically updated according to the AM1–0 and I/D bit settings. During the sleep and standby modes, the CGRAM cannot be accessed.

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	WD 15	WD 14	WD 13	WD 12	WD 11	WD 10	WD 9	WD 8	WD 7	WD 6	WD 5	WD 4	WD 3	WD 2	WD 1	WD 0

Figure 18 Write Data to CGRAM Instruction

Read Data from CGRAM (R12)

RD15-0 : Read 16-bit data from the CGRAM. When the data is read to the microcomputer, the first-word read immediately after the CGRAM address setting is latched from the CGRAM to the internal read-data latch. The data on the data bus (DB15–0) becomes invalid and the second-word read is normal.

When bit processing, such as a logical operation, is performed within the HD66753, only one read can be processed since the latched data in the first word is used.

For the clock-synchronized serial interface, the 5-byte data is invalid. For details, see the Serial Data Transfer section.

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	1	RD 15	RD 14	RD 13	RD 12	RD 11	RD 10	RD 9	RD 8	RD 7	RD 6	RD 5	RD 4	RD 3	RD 2	RD 1	RD 0

Figure 19 Read Data from CGRAM Instruction

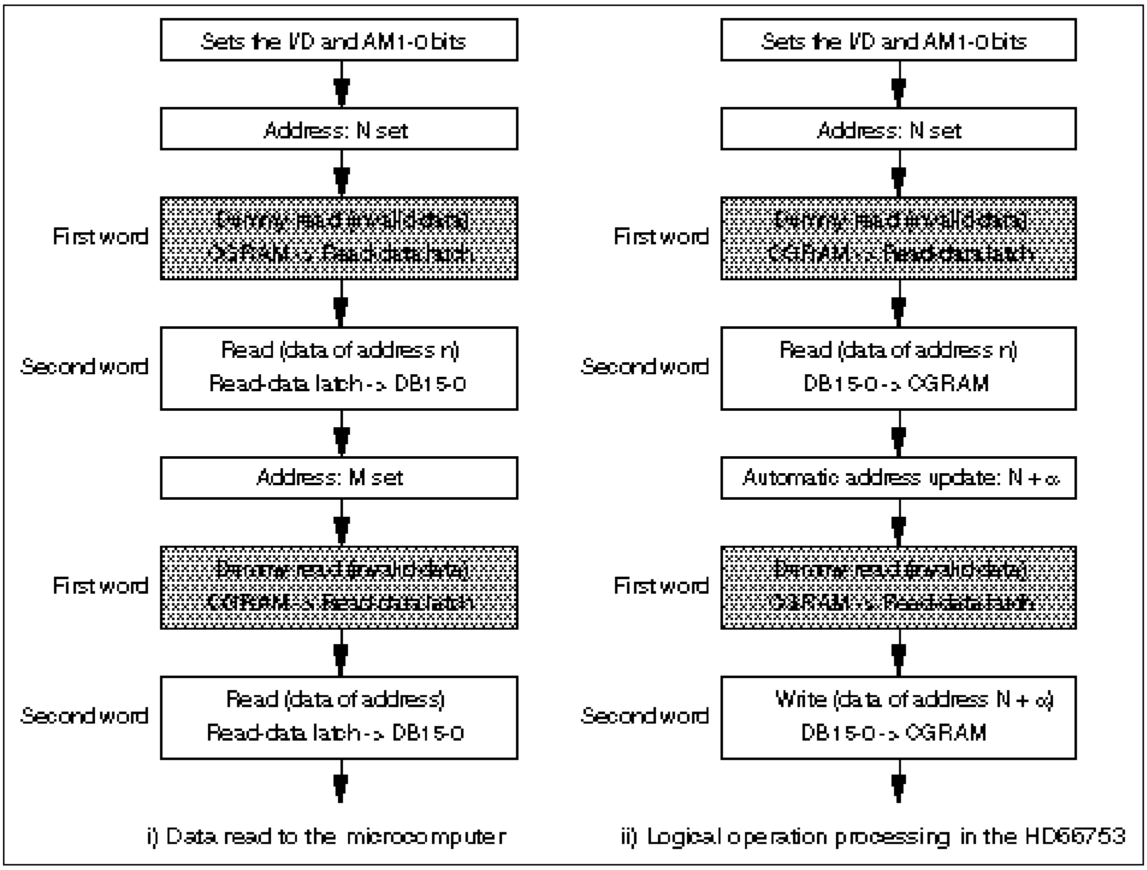


Figure 20 CGRAM Read Sequence

Table 18 Instruction List

Reg. No.	Register Name	R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
				Upper Code								Lower Code							
IR	Index	0	0	*	*	*	*	*	*	*	*	*	*	*	ID4	ID3	ID2	ID1	ID0
SR	Status read	1	0	L7	L6	L5	L4	L3	L2	L1	L0	0	C6	C5	C4	C3	C2	C1	C0
R00	Start oscillation	0	1	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	1
	Device code read	1	1	0	0	0	0	0	1	1	1	0	1	0	1	0	0	1	1
R01	Driver output control	0	1	*	*	*	*	*	*	CMS	SGS	*	*	*	NL4	NL3	NL2	NL1	NL0
R02	LCD-driving-waveform control	0	1	*	*	*	*	*	*	*	*	*	B/C	EOR	NW4	NW3	NW2	NW1	NW0
R03	Power control	0	1	*	*	*	BS2	BS1	BS0	BT1	BT0	PS1	PS0	DC1	DC0	AP1	AP0	SLP	STB
R04	Contrast control	0	1	*	*	*	*	*	VR2	VR1	VR0	*	CT6	CT5	CT4	CT3	CT2	CT1	CT0
R05	Entry mode	0	1	*	*	*	*	*	*	*	*	*	*	*	I/D	AM1	AM0	LG1	LG0
R06	Rotation	0	1	*	*	*	*	*	*	*	*	*	*	*	*	*	RT2	RT1	RT0
R07	Display control	0	1	*	*	*	*	*	*	*	SPT	*	*	GSH1	GSH0	GSL1	GSL0	REV	D
R08	Cursor control	0	1	*	*	*	*	*	*	*	*	*	*	*	*	*	C	CM1	CM0
R09	NOOP	0	1	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*
R0A	NOOP	0	1	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*
R0B	Horizontal cursor position	0	1	HE7	HE6	HE5	HE4	HE3	HE2	HE1	HE0	HS7	HS6	HS5	HS4	HS3	HS2	HS1	HS0
R0C	Vertical cursor position	0	1	VE7	VE6	VE5	VE4	VE3	VE2	VE1	VE0	VS7	VS6	VS5	VS4	VS3	VS2	VS1	VS0
R0D	1st screen driving position	0	1	SE17	SE16	SE15	SE14	SE13	SE12	SE11	SE10	SS17	SS16	SS15	SS14	SS13	SS12	SS11	SS10
R0E	2nd screen driving position	0	1	SE27	SE26	SE25	SE24	SE23	SE22	SE21	SE20	SS27	SS26	SS25	SS24	SS23	SS22	SS21	SS20
R10	RAM write data mask	0	1	WM15	WM14	WM13	WM12	WM11	WM10	WM9	WM8	WM7	WM6	WM5	WM4	WM3	WM2	WM1	WM0
R11	RAM address set	0	1	*	*	*		AD12-8 (upper))								AD7-0 (lower)			
R12	RAM data write	0	1				Write data (upper)								Write data (lower)				
	RAM data read	1	1				Read data (upper)								Read data (lower)				

Note: '*' means 'doesn't matter'.

Table 18 Instruction List (cont)

Reg. No.	Register Name	Description	Execution Cycle
IR	Index	Sets the index register value.	0
SR	Status read	Reads the driving raster-row position (L7-0) and contrast setting (C6-0).	0
R00	Start oscillation	Starts the oscillation mode.	10 ms
	Device code read	Reads 0753H.	0
R01	Driver output control	Sets the common driver shift direction (CMS), segment driver shift direction (SGS), and driving duty ratio (NL4-0).	0
R02	LCD-driving-waveform control	Sets the LCD drive AC waveform (B/C), and EOR output (EOR) or the number of n-raster-rows (NW4-0) at C-pattern AC drive.	0
R03	Power control	Sets the sleep mode (SLP), standby mode (STB), LCD power on (AP1-0), boosting cycle (DC1-0), boosting output multiplying factor (BT1-0), reference power supply (PS1-0), and LCD drive bias value (BS2-0).	0
R04	Contrast control	Sets the contrast adjustment (CT6-0) and regulator adjustment (VR2-0).	0
R05	Entry mode	Specifies the logical operation (LG1-0), AC counter mode (AM1-0), and increment/decrement mode (I/D).	0
R06	Rotation	Specifies the amount of write-data rotation (RT2-0).	0
R07	Display control	Specifies display on (D), black-and-white reversed display (REV), grayscale mode (GS), double-height display on (DHE), and partial scroll (PS1-0).	0
R08	Cursor control	Specifies cursor display on (C) and cursor display mode (CM1-0).	0
R09	NOOP	No operation	0
R0A	NOOP	No operation	0
R0B	Horizontal cursor position	Sets horizontal cursor start (HS6-0) and end (HE6-0).	0
R0C	Vertical cursor position	Sets vertical cursor start (VS6-0) and end (VE6-0).	0
R0D	1st screen driving position	Sets 1st screen driving start (SS17-10) and end (SE17-10).	0
R0E	2nd screen driving position	Sets 2nd screen driving start (SS27-20) and end (SE27-20).	0
R10	RAM write data mask	Specifies write data mask (WM15-0) at RAM write.	0
R11	RAM address set	Initially sets the RAM address to the address counter (AC).	0
R12	RAM data write	Writes data to the RAM.	0
	RAM data read	Reads data from the RAM.	0

Reset Function

The HD66753 is internally initialized by RESET input. Because the busy flag (BF) indicates a busy state (BF = 1) during the reset period, no instruction or CGRAM data access from the MPU is accepted. The reset input must be held for at least 1 ms. Do not access the CGRAM or initially set the instructions until the R-C oscillation frequency is stable after power has been supplied (10 ms).

Instruction Set Initialization:

1. Start oscillation executed
2. Driver output control (NL4–0 = 10000, SGS = 0, CMS = 0)
3. B-pattern waveform AC drive (B/C = 0, ECR = 0, NW4–0 = 00000)
4. Power control (PS1–0 = 00, DC1–0 = 00, AP1–0 = 00: LCD power off, SLP = 0: Sleep mode off, STB = 0: Standby mode off)
5. 1/11 bias drive (BS2–0 = 000), Three-times step-up (BT1–0 = 00), Weak contrast (CT6–0 = 0000000), 2.8-times output voltage for LCD-drive reference voltage generator (VR2–0 = 000)
6. Entry mode set (I/D = 1: Increment by 1, AM1–0 = 00: Horizontal move, LG1–0 = 00: Replace mode)
7. Rotation (RT2–0 = 000: No shift)
8. Display control (SPT = 0: GSH1-0 = GSL1-0 = 00, REV = 0, GS = 0, D = 0: Display off)
9. Cursor control (C = 0: Cursor display off, CM1–0 = 00)
10. 1st screen division (SS17–10 = 00000000, SE17–10 = 00000000)
11. 2nd screen division (SS27–20 = 00000000, SE27–20 = 00000000)
12. Window cursor display position (HS7–0 = HE7–0 = VS7–0 = VE7–0 = 00000000)
13. RAM write data mask (WM15–0 = 0000H: No mask)
14. RAM address set (AD12–0 = 000H)

CGRAM Data Initialization:

This is not automatically initialized by reset input but must be initialized by software while display is off (D = 0).

Output Pin Initialization:

1. LCD driver output pins (SEG/COM): Outputs GND level
2. Step-up circuit output pins (VLOUT): Outputs Vcc level
3. Oscillator output pin (OSC2): Outputs oscillation signal

Parallel Data Transfer

16-bit Bus Interface

Setting the IM2/1/0 (interface mode) to the GND/GND/GND level allows 68-system E-clock-synchronized 16-bit parallel data transfer. Setting the IM2/1/0 to the GND/Vcc/GND level allows 80-system 16-bit parallel data transfer. When the number of buses or the mounting area is limited, use an 8-bit bus interface.

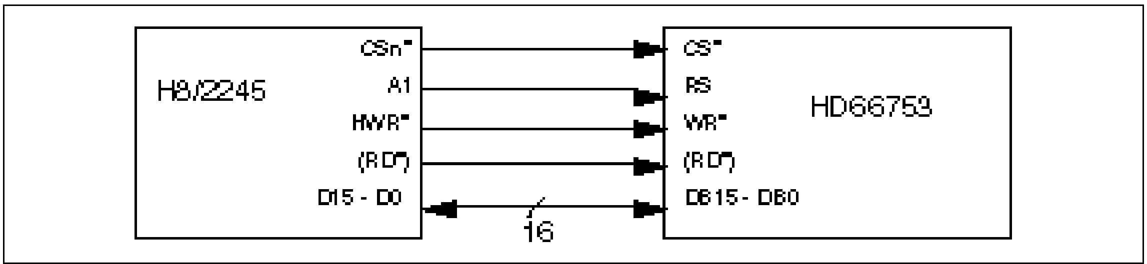


Figure 21 Interface to 16-bit Microcomputer

8-bit Bus Interface

Setting the IM2/1/0 (interface mode) to the GND/GND/Vcc level allows 68-system E-clock-synchronized 8-bit parallel data transfer using pins DB15–DB8. Setting the IM2/1/0 to the GND/Vcc/Vcc level allows 80-system 8-bit parallel data transfer. The 16-bit instructions and RAM data are divided into eight upper/lower bits and the transfer starts from the upper eight bits. Fix unused pins DB7–DB0 to the Vcc or GND level. Note that the upper bytes must also be written when the index register is written to.

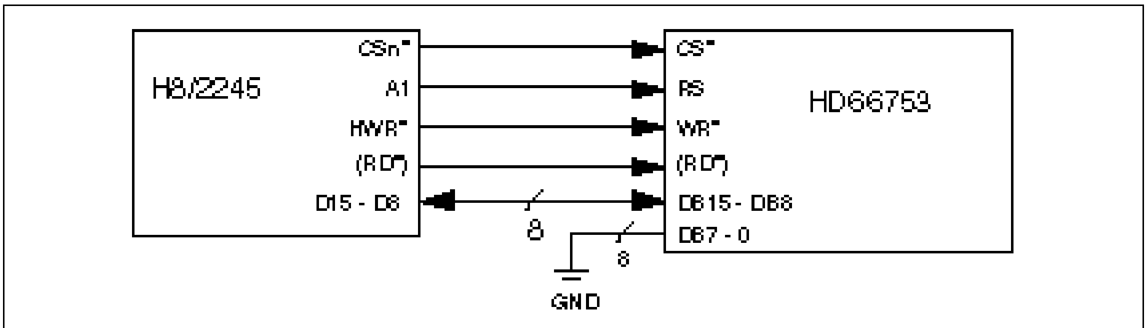


Figure 22 Interface to 8-bit Microcomputer

Note: Transfer synchronization function for an 8-bit bus interface
The HD66753 supports the transfer synchronization function which resets the upper/lower counter to count upper/lower 8-bit data transfer in the 8-bit bus interface. Noise causing transfer mismatch between the eight upper and lower bits can be corrected by a reset triggered by consecutively writing a 00H instruction four times. The next transfer starts from the upper eight bits. Executing synchronization function periodically can recover any runaway in the display system.

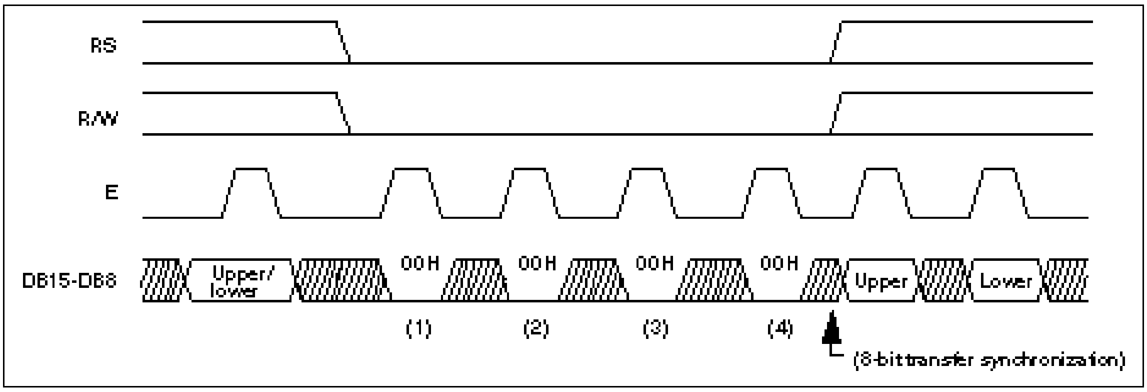


Figure 23   8-bit Transfer Synchronization

Serial Data Transfer

Setting the IM1 and IM2 pins (interface mode pins) to the Vcc or GND level allows standard clock-synchronized serial data transfer, using the chip select line (CS*), serial data line (SDA), and serial transfer clock line (SCL). For a serial interface, the IM0/ID pin function uses an ID pin.

The HD66753 initiates serial data transfer by transferring the start byte at the falling edge of CS* input. It ends serial data transfer at the rising edge of CS* input.

The HD66753 is selected when the 6-bit chip address in the start byte transferred from the transmitting device matches the 6-bit device identification code assigned to the HD66753. The HD66753, when selected, receives the subsequent data string. The least significant bit of the identification code can be determined by the ID pin. The five upper bits must be 01110. Two different chip addresses must be assigned to a single HD66753 because the seventh bit of the start byte is used as a register select bit (RS): that is, when RS = 0, an index register can be written to or the status can be read from, and when RS = 1, an instruction can be written to or the data can be written to or read from RAM. Read or write is selected according to the eighth bit of the start byte (R/W bit) as shown in table 19.

After receiving the start byte, the HD66753 receives or transmits the subsequent data byte-by-byte. The data is transferred with the MSB first. Since all the instructions in the HD66753 are configured by 16 bits, they are internally executed after two bytes have been transferred with the MSB first (DB15-0). The HD66753 internally receives the first byte as upper eight bits of instructions, and the second byte as lower eight bits.

Five bytes of RAM read data after the start byte are invalid. The HD66753 starts to read correct RAM data from the sixth byte.

Table 19 Start Byte Format

Transfer Bit	S	1	2	3	4	5	6	7	8
Start byte format	Transfer start	Device ID code						RS	R/W
		0	1	1	1	0	ID		

Note: ID bit is selected by the IM0/ID pin.

Table 20 RS and R/W Bit Functions

RS	R/W	Function
0	0	Writes index register
0	1	Reads status
1	0	Writes instructions and RAM data
1	1	Reads RAM data

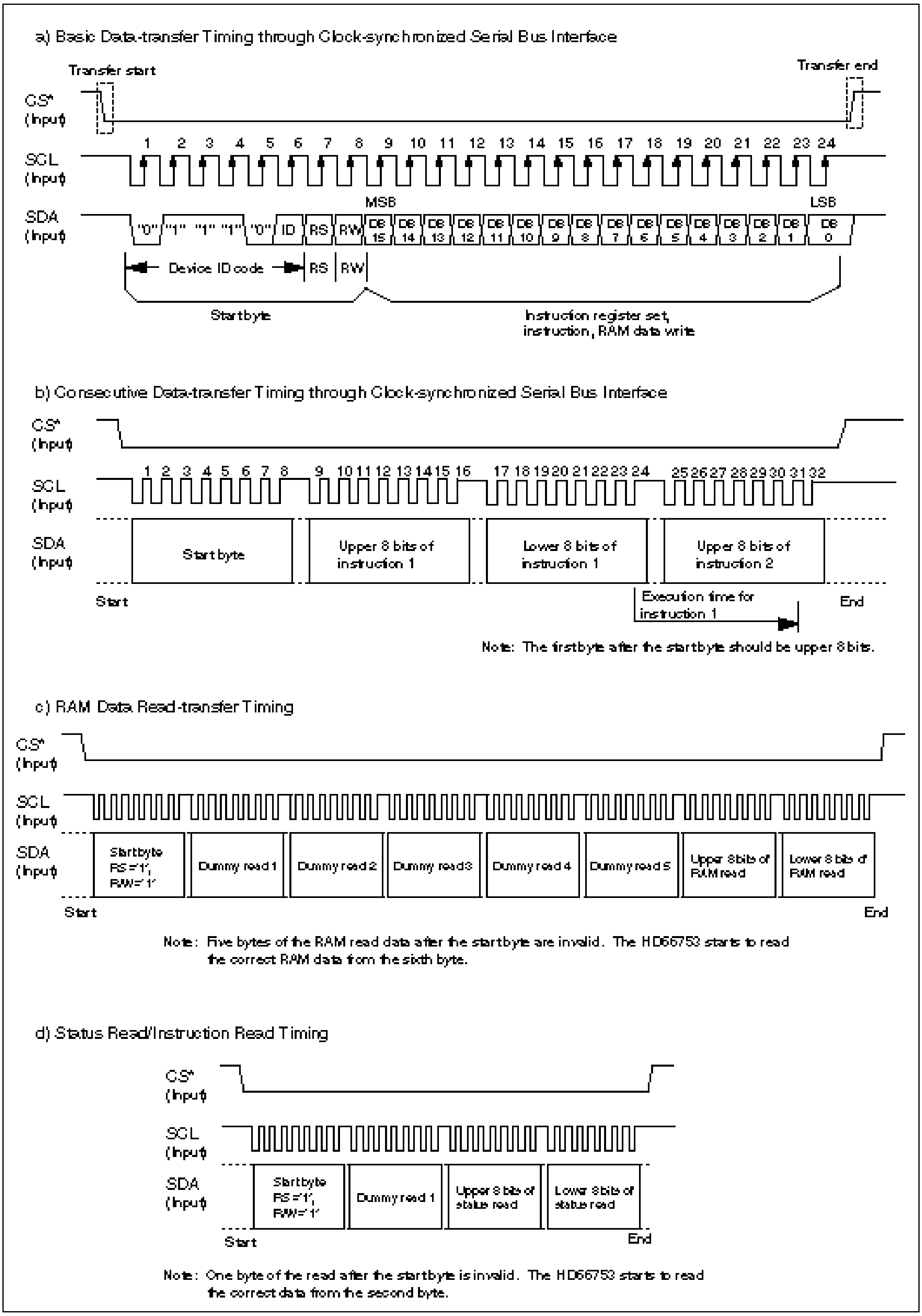


Figure 24 Clock-synchronized Serial Interface Timing Sequence

Graphics Operation Function

The HD66753 can greatly reduce the load of the microcomputer graphics software processing through the 16-bit bus architecture and graphics-bit operation function. This function supports the following:

1. A write data mask function that selectively rewrites some of the bits in the 16-bit write data.
2. A bit rotation function that shifts and writes the data sent from the microcomputer in a bit unit.
3. A logical operation function that writes the data sent from the microcomputer and the original RAM data by a logical operation.

Since the display data in the graphics RAM (CGRAM) can be quickly rewritten, the load of the microcomputer processing can be reduced in the large display screen when a font pattern, such as kanji characters, is developed for any position (BiTBLT processing).

The graphics bit operation can be controlled by combining the entry mode register, the bit set value of the RAM-write-data mask register, and the read/write from the microcomputer.

Table 21 Graphics Operation

	Bit Setting			
Operation Mode	**I/D**	**AM**	**LG**	**Operation and Usage**
Write mode 1	0/1	00	00	Horizontal data replacement, horizontal-border drawing
Write mode 2	0/1	01	00	Vertical data replacement, font development, vertical-border drawing
Write mode 3	0/1	10	00	Vertical data replacement with two-word width, kanji-font development
Read/write mode 1	0/1	00	01 10 11	Horizontal data replacement with logical operation, horizontal-border drawing
Read/write mode 2	0/1	01	01 10 11	Vertical data replacement with logical operation, vertical-border drawing
Read/write mode 3	0/1	10	01 10 11	Horizontal data replacement with two-word-width logical operation

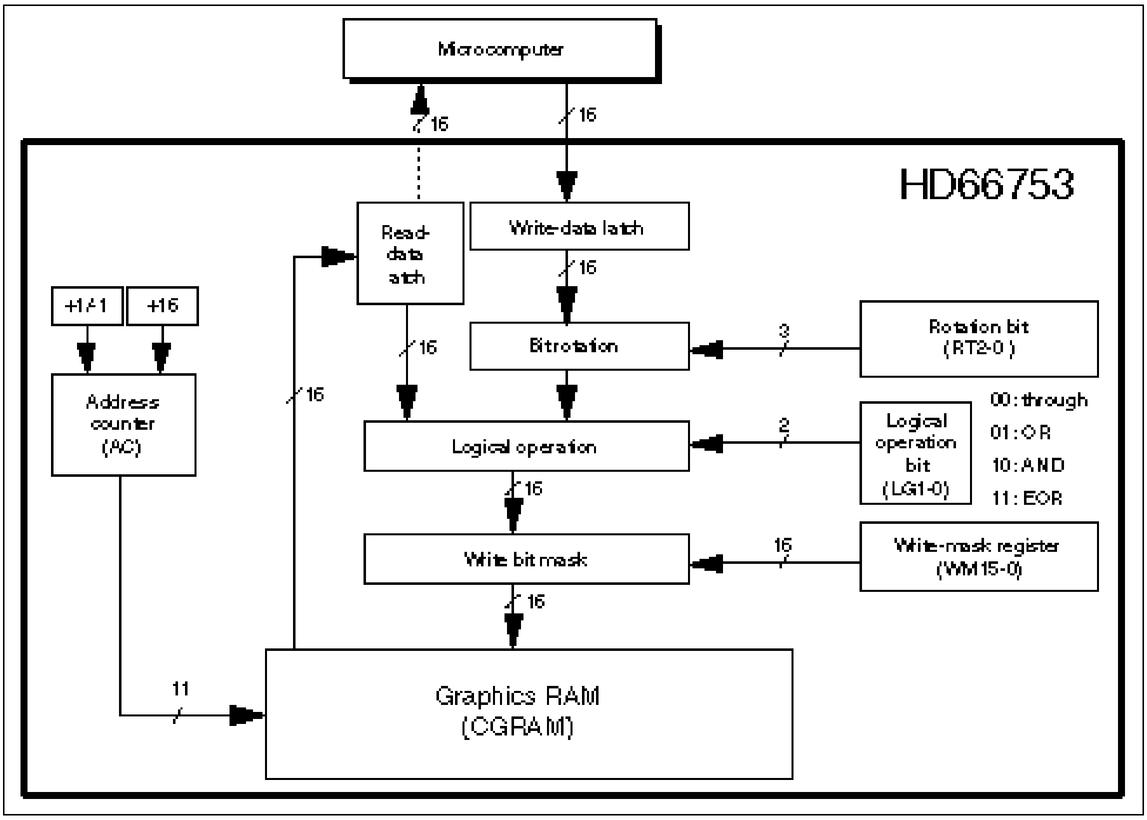


Figure 25 Data Processing Flow of the Graphics Bit Operation

1. Write mode 1: AM1–0 = 00, LG1–0 = 00

   This mode is used when the data is horizontally written at high speed. It can also be used to initialize the graphics RAM (CGRAM) or to draw borders. The rotation function (RT2–0) or write-data mask function (WM15–0) are also enabled in these operations. After writing, the address counter (AC) automatically increments by 1 (I/D = 1) or decrements by 1 (I/D = 0), and automatically jumps to the counter edge one-raster-row below after it has reached the left edge of the graphics RAM.

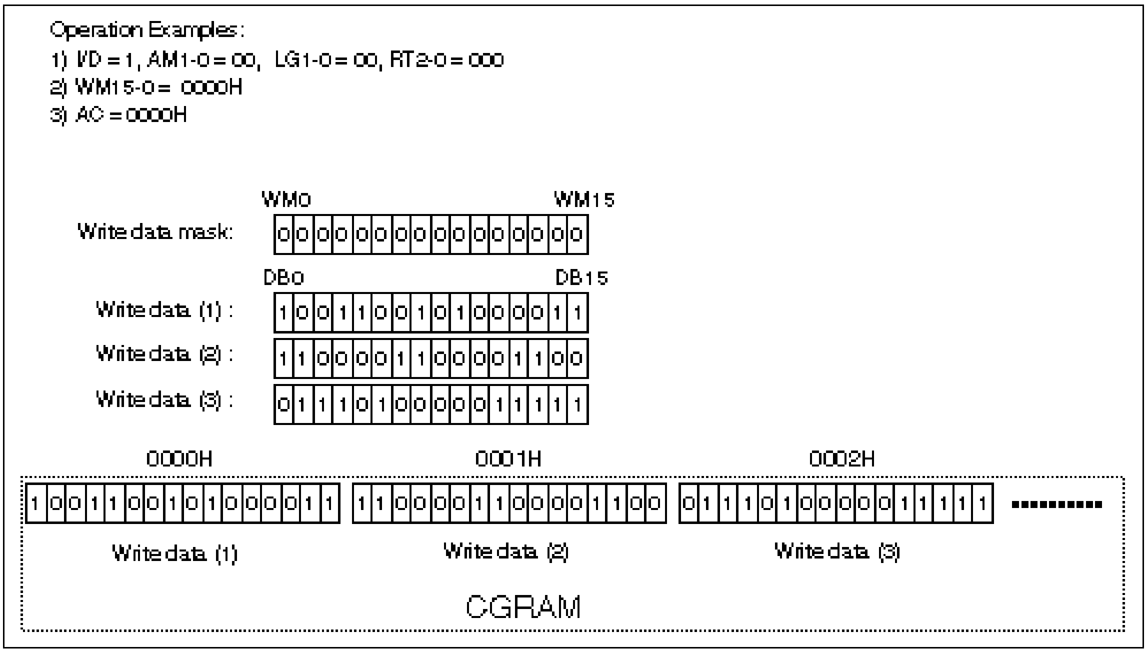


Figure 26 Writing Operation of Write Mode 1

2. Write mode 2: AM1–0 = 01, LG1–0 = 00

   This mode is used when the data is vertically written at high speed. It can also be used to initialize the graphics RAM (CGRAM), develop the font pattern in the vertical direction, or draw borders. The rotation function (RT2–0) or write-data mask function (WM15–0) are also enabled in these operations. After writing, the address counter (AC) automatically increments by 20, and automatically jumps to the upper-right edge (I/D = 1) or upper-left edge (I/D = 0) following the I/D bit after it has reached the lower edge of the graphics RAM.

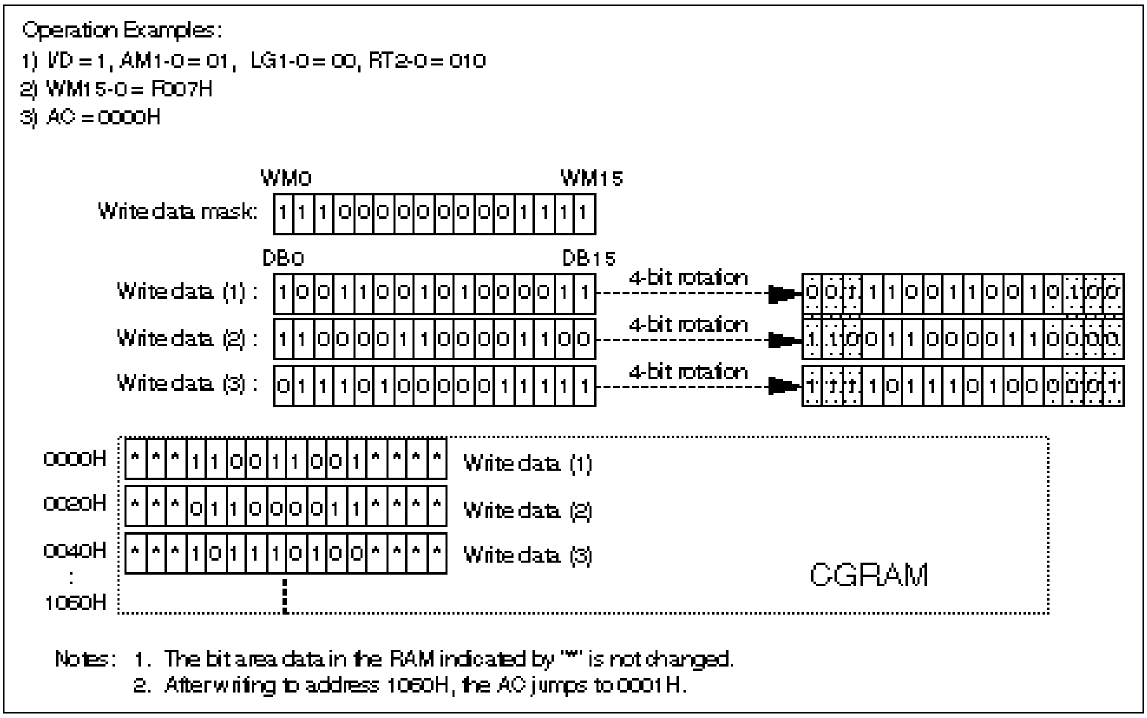


Figure 27 Writing Operation of Write Mode 2

3. Write mode 3: AM1–0 = 10, LG1–0 = 00

   This mode is used when the data is written at high speed by vertically shifting bits. It can also be used to write the 16-bit data for two words into the graphics RAM (CGRAM), develop the font pattern, or transfer the BiTBLT as a bit unit. The rotation function (RT2–0) or write-data mask function (WM15–0) are also enabled in these operation. However, although the write-data mask function masks the bit position set with the write-data mask register (WM15–0) at the odd-times (such as the first or third) write, the function masks the bit position that reversed the setting value of the write-data mask register (WM15–0) at the even-times (such as the second or fourth) write. After the odd-times writing, the address counter (AC) automatically increments by 1 (I/D = 1) or decrements by 1 (I/D = 0). After the even-times writing, the AC automatically increments or decrements by –1 + 20 (I/D = 1) or +1 + 20 (I/D = 0). The AC automatically jumps to the upper edge after it has reached the lower edge of the graphics RAM.

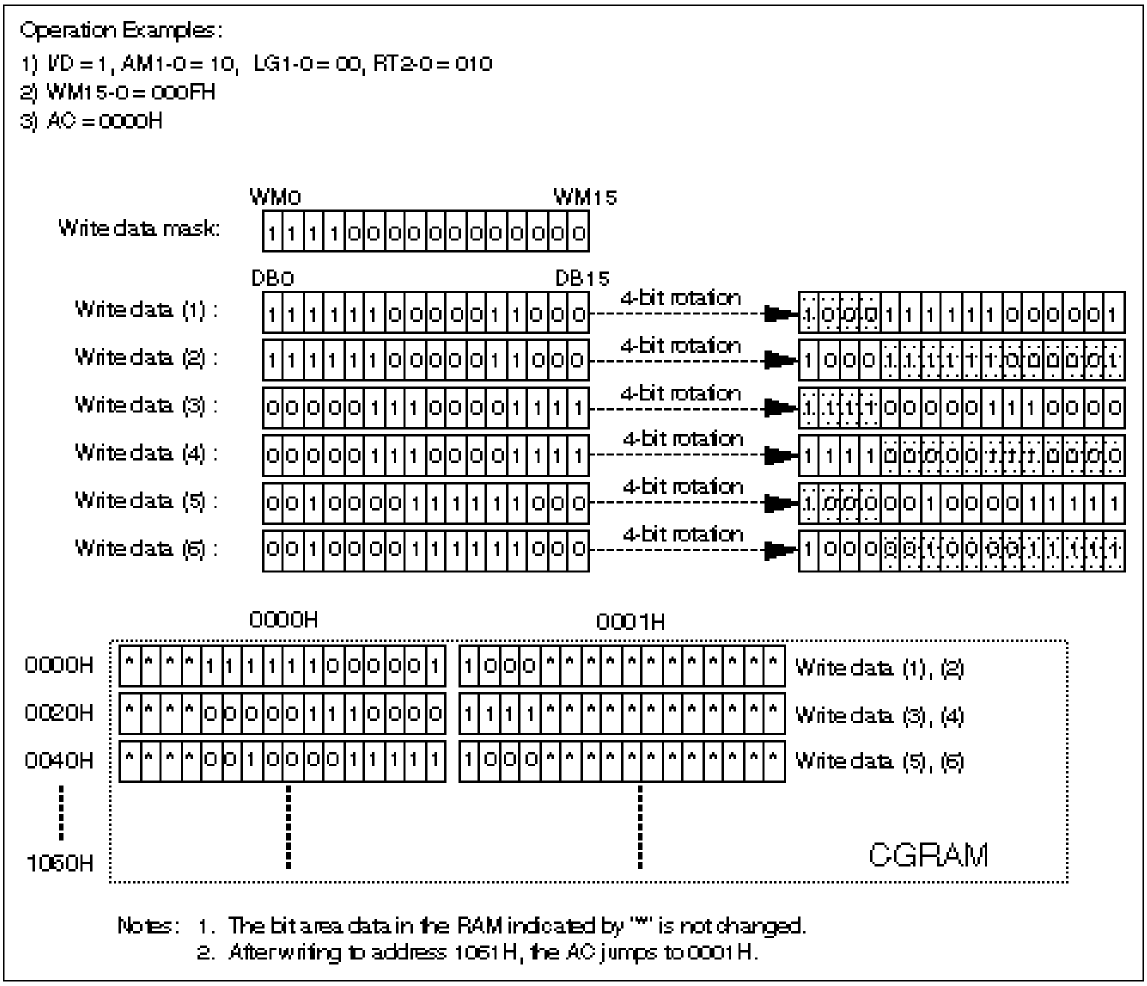


Figure 28 Writing Operation of Write Mode 3

4. Read/Write mode 1: AM1–0 = 00, LG1–0 = 01/10/11

This mode is used when the data is horizontally written at high speed by performing a logical operation with the original data. It reads the display data (original data), which has already been written in the graphics RAM (CGRAM), performs a logical operation with the write data sent from the microcomputer, and rewrites the data to the CGRAM. This mode can read the data during the same bus cycle as for the write operation since the read operation of the original data does not latch the read data into the microcomputer and temporarily holds it in the read-data latch. (However, the bus cycle must be the same as the read cycle.) The rotation function (RT2–0) or write-data mask function (WM15–0) are also enabled in these operations. After writing, the address counter (AC) automatically increments by 1 (I/D = 1) or decrements by 1 (I/D = 0), and automatically jumps to the counter edge one-raster-row below after it has reached the left or right edges of the graphics RAM.

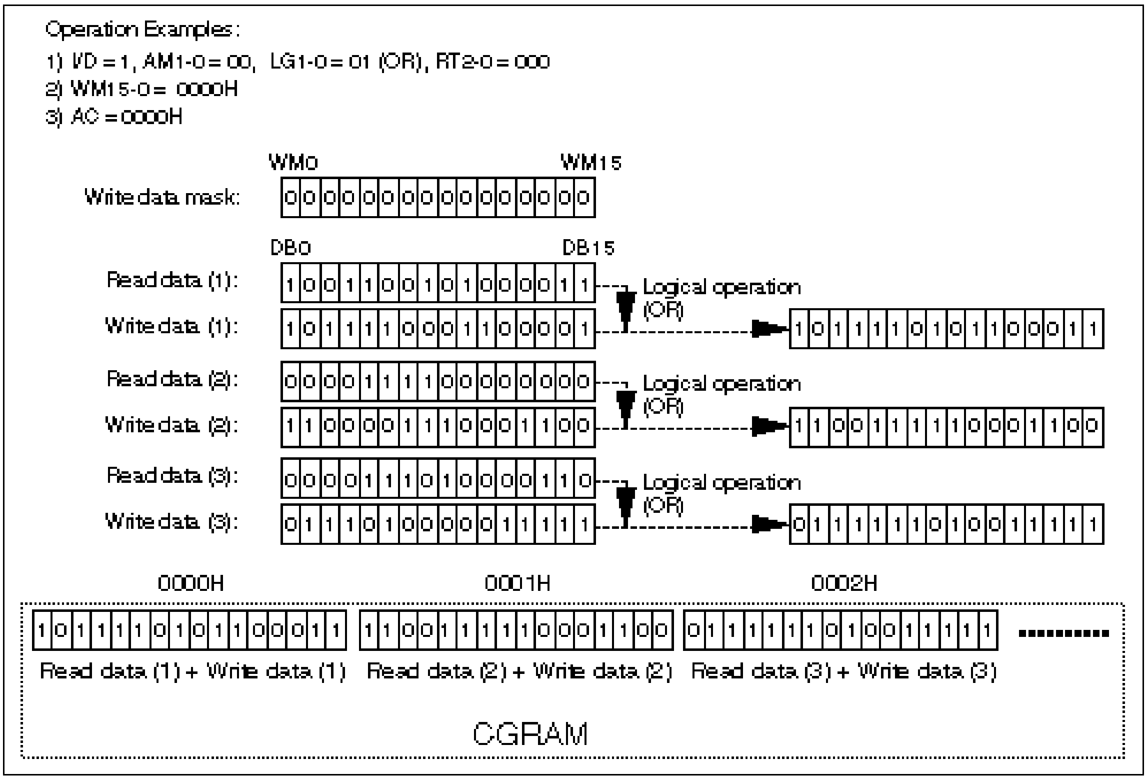


Figure 29 Writing Operation of Read/Write Mode 1

5. Read/Write mode 2: AM1–0 = 01, LG1–0 = 01/10/11

   This mode is used when the data is vertically written at high speed by performing a logical operation with the original data. It reads the display data (original data), which has already been written in the graphics RAM (CGRAM), performs a logical operation with the write data sent from the microcomputer, and rewrites the data to the CGRAM. This mode can read the data during the same bus cycle as for the write operation since the read operation of the original data does not latch the read data into the microcomputer and temporarily holds it in the read-data latch. The rotation function (RT2–0) or write-data mask function (WM15–0) are also enabled in these operations. After writing, the address counter (AC) automatically increments by 20, and automatically jumps to the upper-right edge (I/D = 1) or upper-left edge (I/D = 0) following the I/D bit after it has reached the lower edge of the graphics RAM.

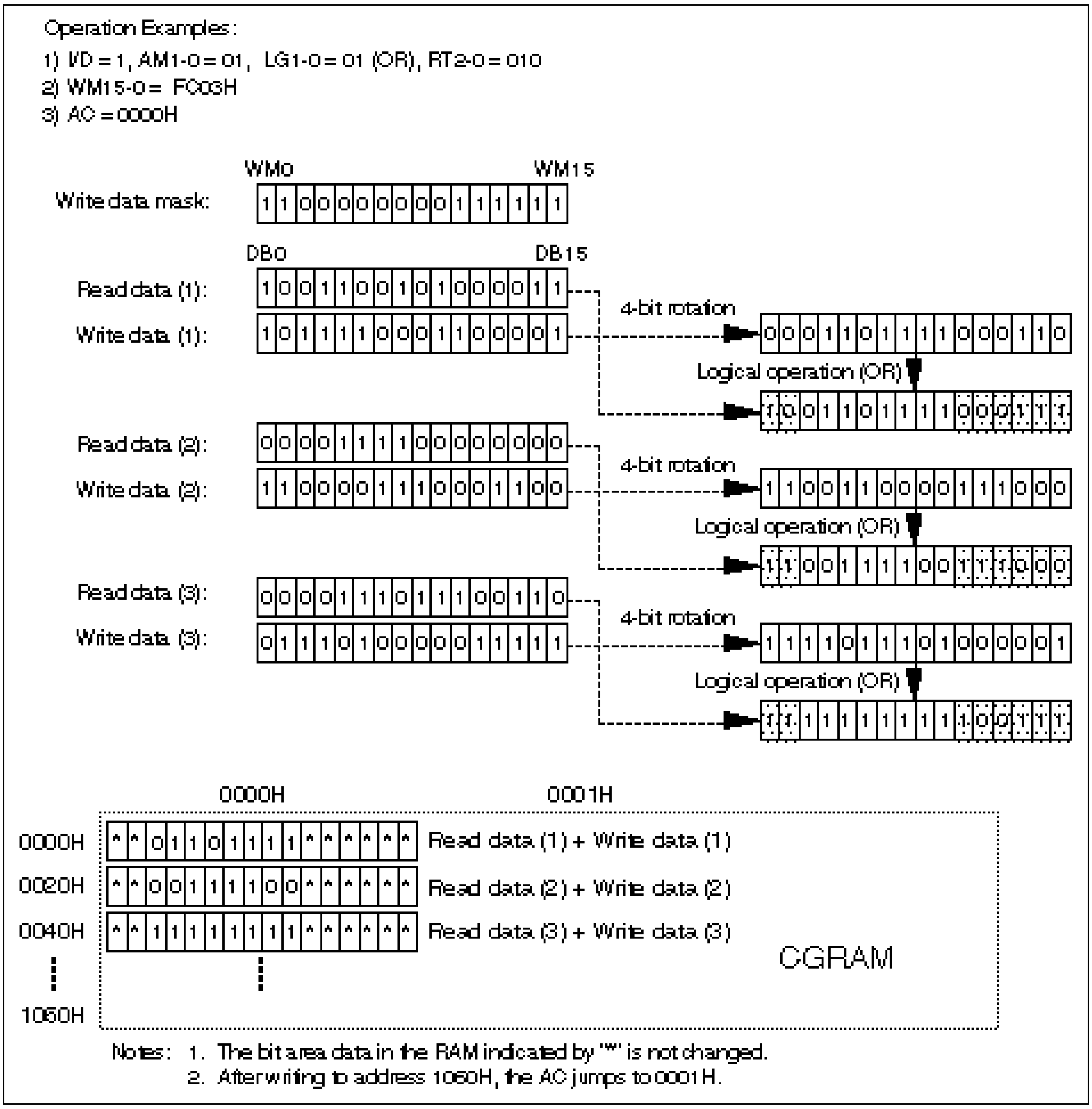


Figure 30 Writing Operation of Read/Write Mode 2

6. Read/Write mode 3: AM1–0 = 10, LG1–0 = 01/10/11

   This mode is used when the data is written with high speed by vertically shifting bits and by performing logical operation with the original data. It can be also used to write the 16-bit data for two words into the graphics RAM (CGRAM), develop the font pattern, or transfer the BiTBLT as a bit unit. This mode can read the data during the same bus cycle as for the write operation since the read operation of the original data does not latch the read data into the microcomputer and temporarily holds it in the read-data latch. The rotation function (RT2–0) or write-data mask function (WM15–0) are also enabled in these operations. However, although the write-data mask function masks the bit position set with the write-data mask register (WM15–0) at the odd-times (such as the first or third) write, the function masks the bit position which reversed the setting value of the write-data mask register (WM15–0) at the even-times (such as the second or fourth) write. After the odd-times writing, the address counter (AC) automatically increments by 1 (I/D = 1) or decrements by 1 (I/D = 0). After the even-times writing, the AC automatically increments or decrements by –1 + 20 (I/D = 1) or +1 + 20 (I/D = 0). The AC automatically jumps to the upper edge after it has reached the lower edge of the graphics RAM.

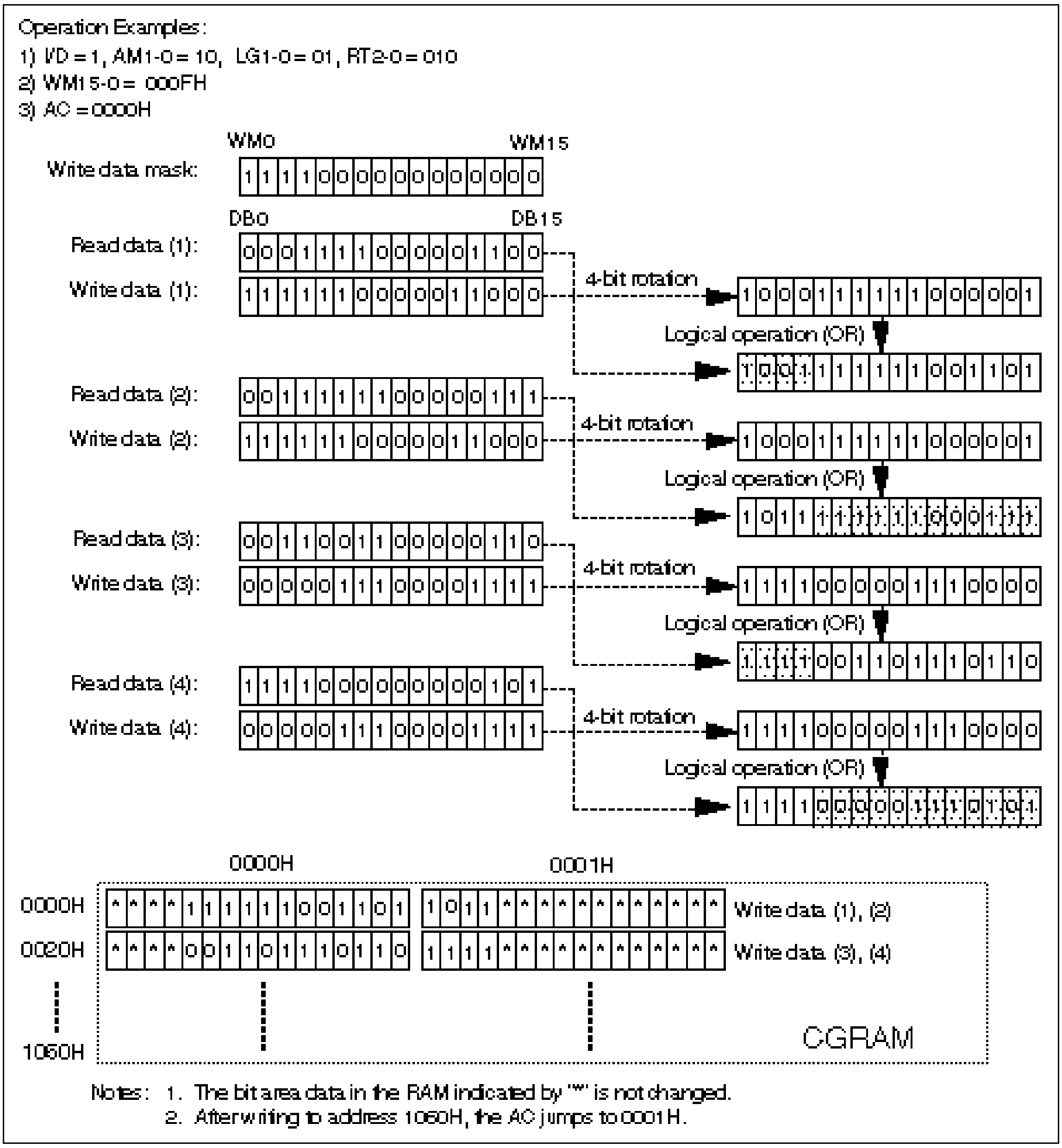


Figure 31 Writing Operation of Read/Write Mode 3

Oscillation Circuit

The HD66753 can either be supplied with operating pulses externally (external clock mode) or oscillate using an internal R-C oscillator with an external oscillator-resistor (external resistor oscillation mode). Note that in R-C oscillation, the oscillation frequency is changed according to the internal capacitance value, the external resistance value, or operating power-supply voltage.

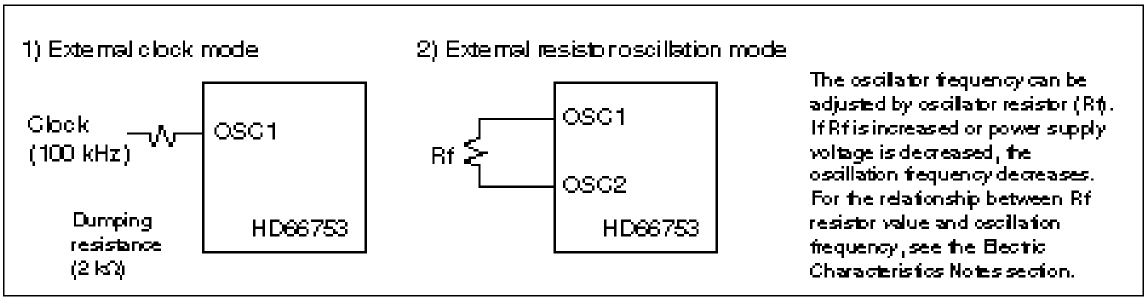


Figure 32 Oscillation Circuits

Table 22 Relationship between Liquid Crystal Drive Duty Ratio and Frame Frequency

LCD Duty	NL4–0 Set Value	Recommended Drive Bias Value	Frame Frequency	One-frame Clock
1/24	02H	1/6	72 Hz	1392
1/32	03H	1/6	71 Hz	1408
1/40	04H	1/7	71 Hz	1400
1/48	05H	1/8	72 Hz	1392
1/56	06H	1/8	71 Hz	1400
1/64	07H	1/9	71 Hz	1408
1/72	08H	1/9	69 Hz	1440
1/80	09H	1/10	69 Hz	1440
1/88	0AH	1/10	71 Hz	1408
1/96	0BH	1/10	69 Hz	1440
1/104	0CH	1/11	69 Hz	1456
1/112	0DH	1/11	69 Hz	1456
1/120	0EH	1/11	69 Hz	1440
1/128	0FH	1/11	71 Hz	1408
1/132	10H	1/11	69 Hz	1452

Note: The frame frequency above is for 100-kHz operation and proportions the oscillation frequency (fosc).

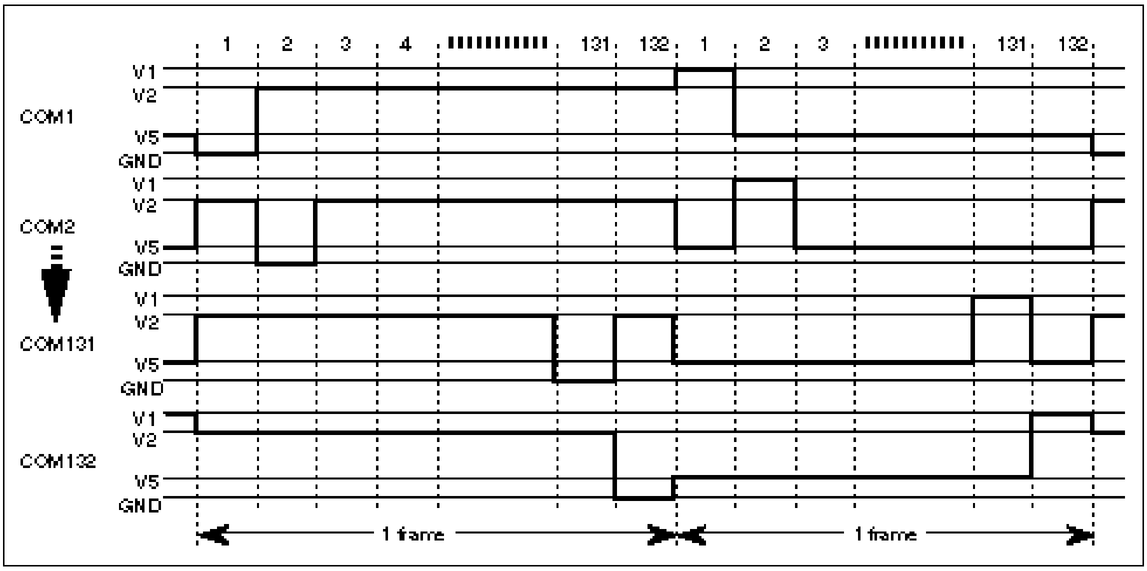
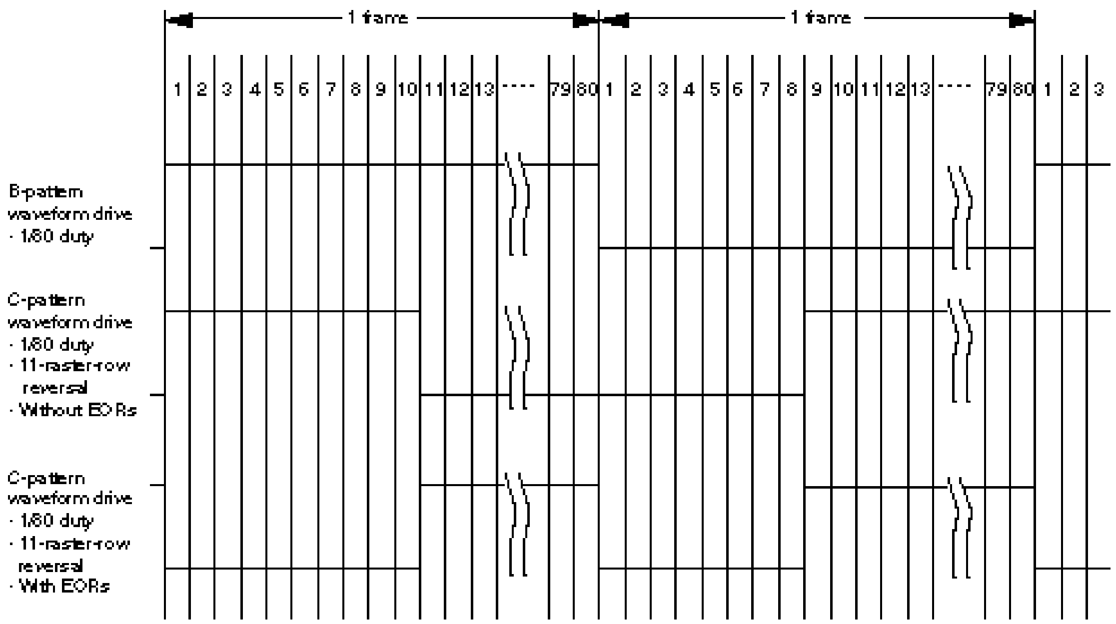


Figure 33 LCD Drive Output Waveform (B-pattern AC Drive with 1/132 Multiplexing Duty Ratio)

n-raster-row Reversed AC Drive

The HD66753 supports not only the LCD reversed AC drive in a one-frame unit (B-pattern waveform) but also the n-raster-row reversed AC drive which alternates in an n-raster-row unit from one to 32 raster-rows (C-pattern waveform). When a problem affecting display quality occurs, such as crosstalk at high-duty driving of more than 1/64 duty, the n-raster-row reversed AC drive (C-pattern waveform) can improve the quality. Determine the number of raster-rows n (NW bit set value + 1) for alternating after confirmation of the display quality with the actual LCD panel. However, if the number of AC raster-rows is reduced, the LCD alternating frequency becomes high. Because of this, the charge or discharge current is increased in the LCD cells.



Note: Specify the number of AC drive raster-rows and the necessity of EOR so that the DC bias is not generated for the liquid crystal.

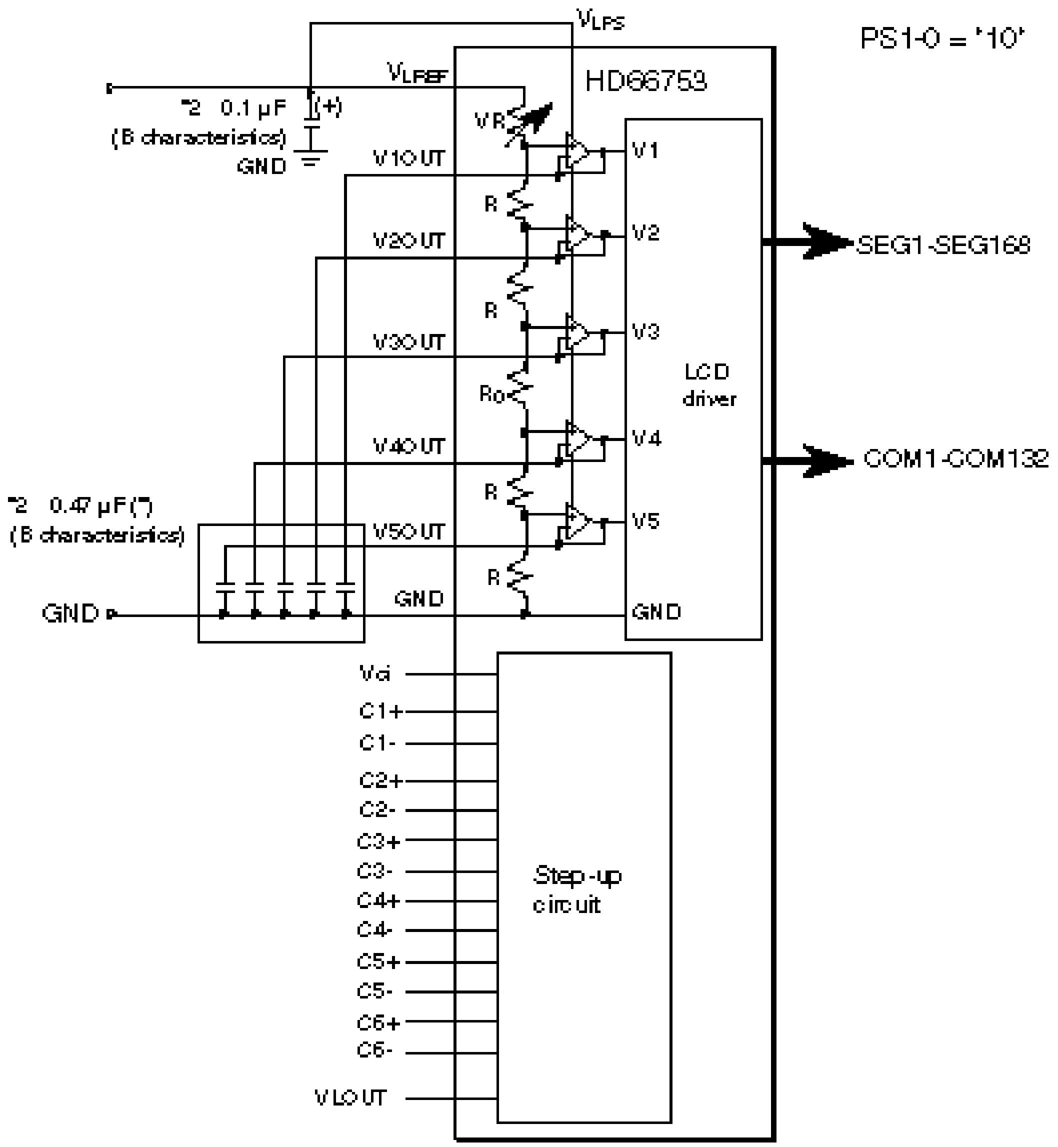
Figure 34 Example of an AC Signal under n-raster-row Reversed AC Drive

Liquid Crystal Display Voltage Generator

When External Power Supply and Internal Operational Amplifiers are Used

To supply LCD drive voltage directly from the external power supply without using the internal step-up circuit, circuits should be connected as shown in figure 35. Here, contrast can be adjusted by software through the CT bits of the contrast adjustment register. Since the VLREF input is the reference voltage to determine the LCD drive voltage, fluctuation of the voltage must be minimized.

The HD66753 incorporates a voltage-follower operational amplifier for each V1 to V5 to reduce current flowing through the internal bleeder-resistors, which generate different levels of liquid-crystal drive voltages. Thus, potential difference between V_{LPS} and V1 must be 0.1 V or higher, and that between V4 and GND must be 1.4 V or higher. Note that the OPOFF pin must be grounded when using the operational amplifiers. Place a capacitor of about 0.47 µF (B characteristics) between each internal operational amplifier (V1OUT to V5OUT outputs) and GND and stabilize the output level of the operational amplifier. Adjust the capacitance value of the stabilized capacitor after the LCD panel has been mounted and the screen quality has been confirmed.



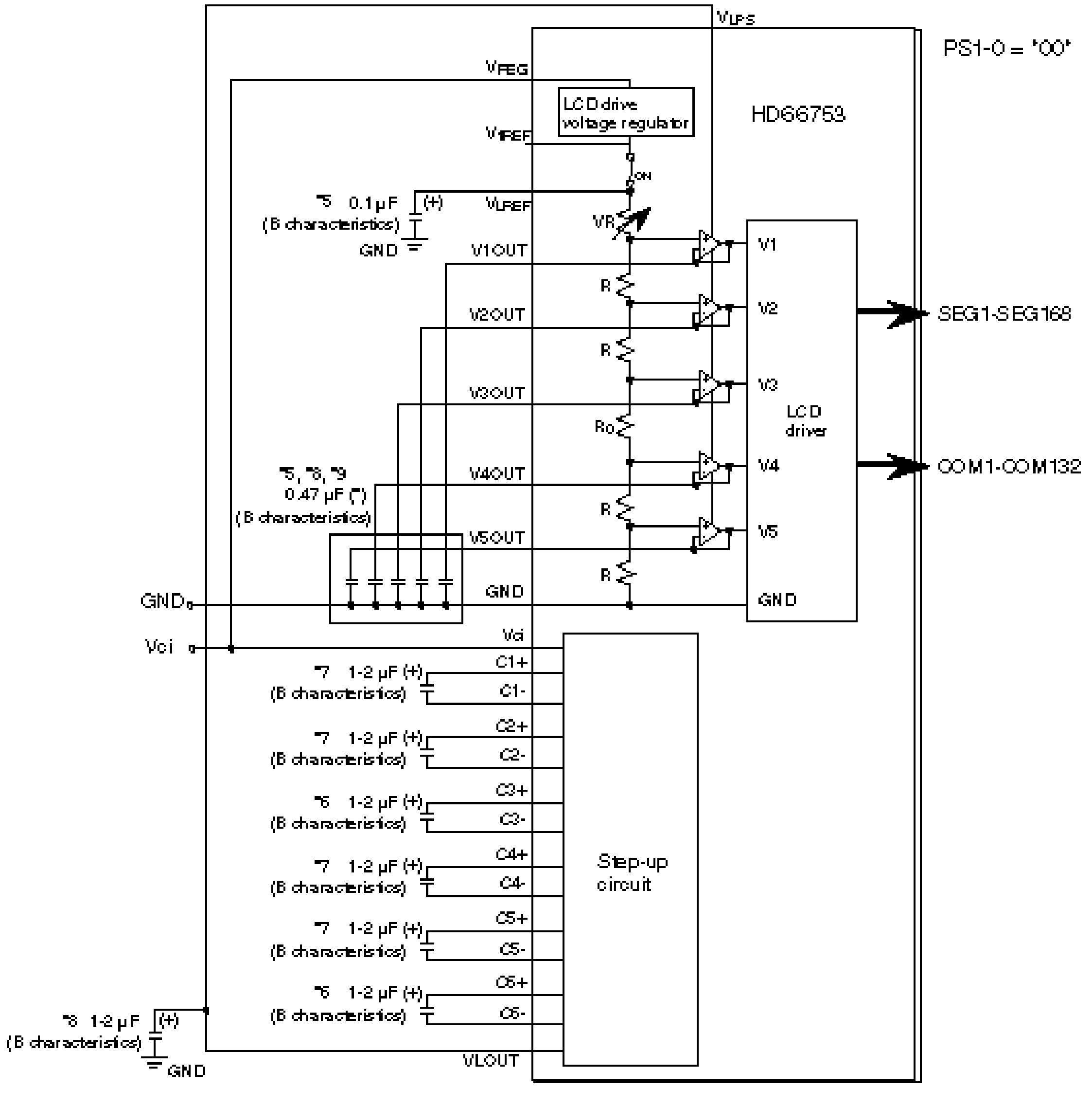
Notes: 1. Adjust the capacitance value of the capacitor after the LCD panel has been mounted.
2. Use the capacitors with breakdown voltages equal to or higher than the VLPS voltage for connecting to V1OUT through V5OUT. Determine the capacitor breakdown voltages by checking VLPS voltage fluctuation.

Figure 35 External Power Supply Circuit for LCD Drive Voltage Generation

When an Internal Booster and Internal Operational Amplifiers are Used

To supply LCD drive voltage using the internal step-up circuit, circuits should be connected as shown in figure 36. Generate a higher voltage (VLPS) of the internal operational amplifier than the output voltage (V1REF) of the LCD drive voltage regulator. Here, contrast can be adjusted through the CT bits of the contrast control instruction.

The HD66753 incorporates a voltage-follower operational amplifier for each of V1 to V5 to reduce current flowing through the internal bleeder-resistors, which generate different liquid-crystal drive voltages. Thus, potential difference between V_{LPS} and V1 must be 0.1 V or higher, and that between V4 and GND must be 1.4 V or higher. Note that the OPOFF pin must be grounded when using the operational amplifiers. Place a capacitor of about 0.47 µF (B characteristics) between each internal operational amplifier (V1OUT to V5OUT outputs) and GND and stabilize the output level of the operational amplifier. Adjust the capacitance value of the stabilized capacitor after the LCD panel has been mounted and the screen quality has been confirmed.



Notes: 1. The reference voltage input (Vci) must be adjusted so that the output voltage after boosting will not exceed the absolute maximum rating for the liquid-crystal power supply voltage (20.5 V).
2. Vci is both a reference voltage and power supply for the step-up circuit; obtain sufficient current.
3. Polarized capacitors must be connected correctly.
4. Circuits for temperature compensation should be based on the sample circuits in figures 37 and 38.
5. Adjust the capacitance value of the stabilized capacitor after the LCD panel has been mounted.
6. The breakdown voltage of the capacitors connected to C3+/C3- and C6+/C6- should be three times or higher than the Vci voltage.
7. The breakdown voltage of the capacitors connected to C1+/C1-, C2+/C2-, C4+/C4-, and C5+/C5- should be equal to or higher than the Vci voltage.
8. The breakdown voltage of the capacitors connected to VLOUT and V1OUT through V5OUT should be n times or higher than the Vci voltage (n: step-up magnification).
9. Determine the breakdown voltages of the capacitors used in 6 to 8 above by checking Vci voltage fluctuation.

Figure 36 Internal Step-up Circuit for LCD Drive Voltage Generation

Temperature can be compensated either through the CT bits by software, by controlling the reference voltage for the LCD drive voltage regulator (VREG pin) using a thermistor, or by controlling the reference output voltage of the LCD drive voltage regulator (V1REF pin).

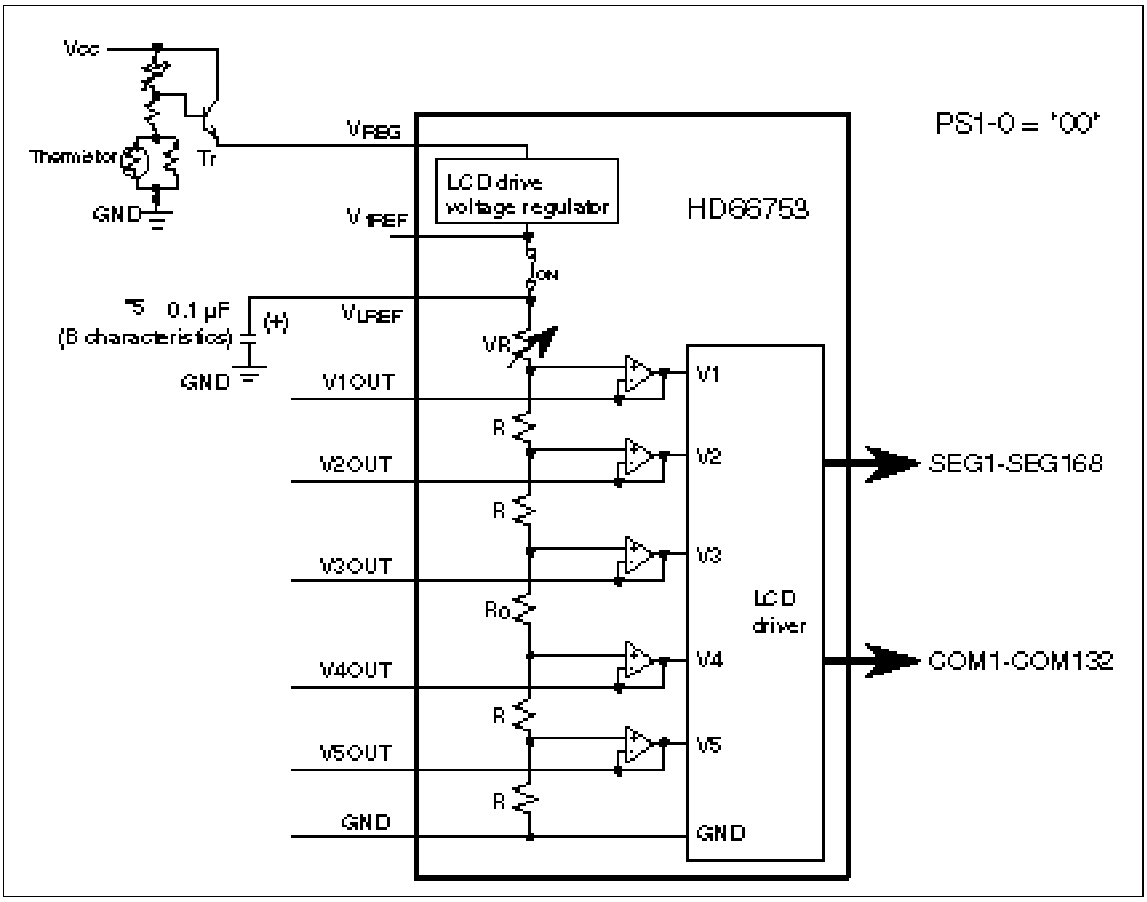


Figure 37 Temperature Compensation Circuits (1)

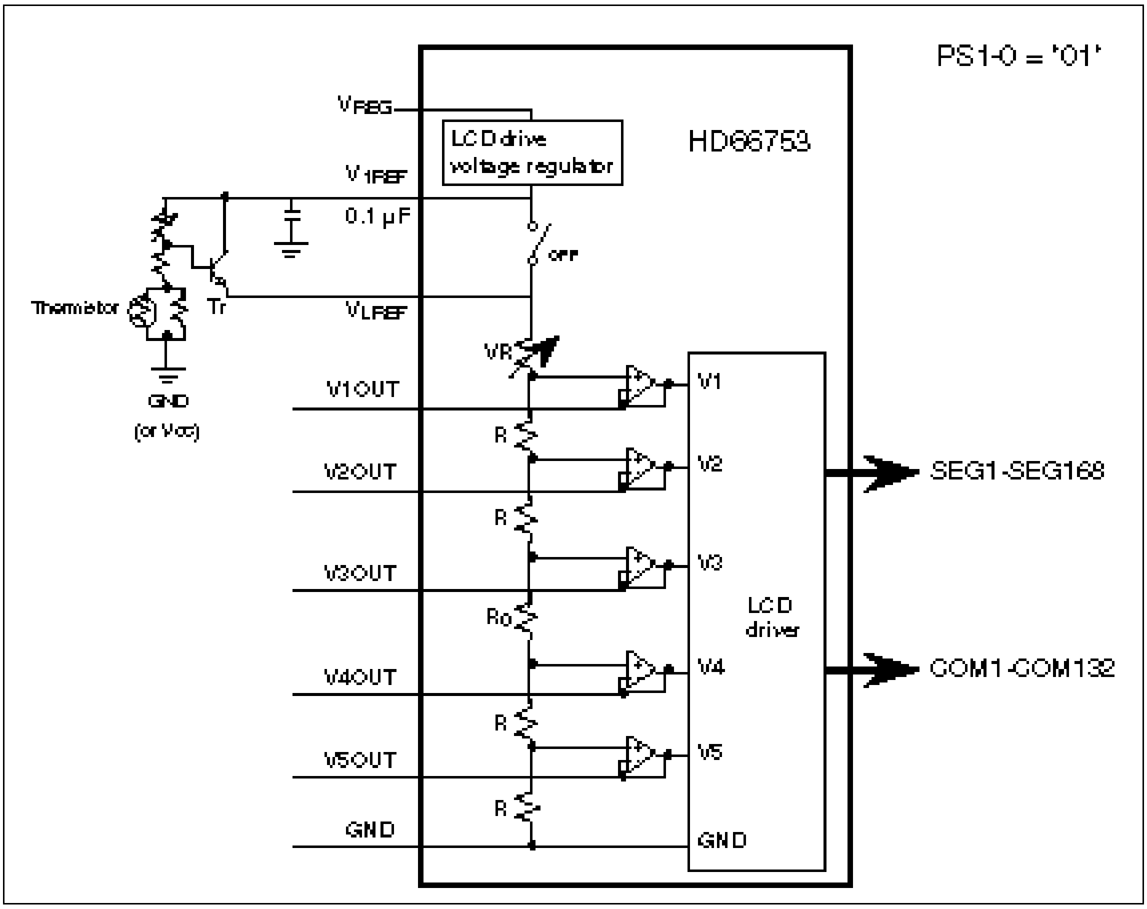


Figure 38 Temperature Compensation Circuits (2)

Countermeasures for Screen Quality when Using On-chip Operational Amplifier

The HD66753 is an on-chip LCD driver that has an LCD power supply for high duty. Screen quality is affected by the load current of the high-duty LCD panel used. When the bias (1/11 bias, 1/10 bias, 1/9 bias, etc.) is high and the displayed pattern is completely or almost completely white, the white sections may appear dark.

If this happens, execute the following countermeasures to improve screen quality.

(1) After the change in the V4OUT/V3OUT level is verified, insert about 1 MΩ between V4OUT and GND or VLPS and V3OUT and then adjust the screen quality (see the following figures). By inserting resistance, the current consumption increases as much as the boosting factor of the resistance current. Adjust the resistance after checking the screen quality and the increase in current consumption.

(2) Decrease the drive bias and use the new bias level after verifying that the potential differences between V4OUT and GND or VLPS and V3OUT are sufficient.

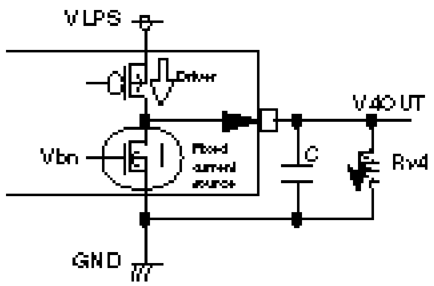


Figure 39 Countermeasure for V4OUT Output

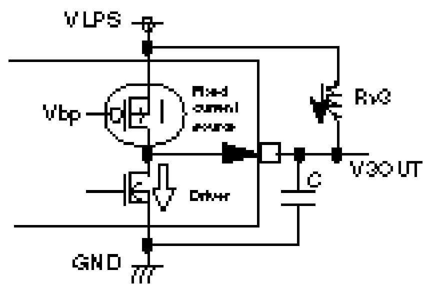


Figure 40 Countermeasure for V3OUT Output

Note: The actual LCD drive voltage VLREF used must not exceed 16.5 V.

Switching the Step-up Factor

Instruction bits (BT1/0 bits) can optionally select the step-up factor of the internal step-up circuit. According to the display status, power consumption can be reduced by changing the LCD drive duty and the LCD drive bias, and by controlling the step-up factor for the minimum requirements. For details, see the Partial-display-on Function section.

According to the maximum step-up factor, external capacitors need to be connected. For example, when the maximum step-up is six times or five times, capacitors between C6+ and C6– or between C5+ and C5– are needed as in the case of the seven-times step-up. When the step-up is three-times, capacitors between C1+ and C1– or between C4+ and C4– are not needed.

Place a capacitor with a breakdown voltage of three times or more the Vci-GND voltage between C6+ and C6– and between C3+ and C3–, a capacitor with a breakdown voltage larger than the Vci-GND voltage between C1+ and C1–, C2+ and C2–, C4+ and C4–, and C5+ and C5–, and a capacitor with a breakdown voltage of n times or more the Vci-GND voltage to VLOUT (n: step-up factor) (see figure 37).

Note: Determine the capacitor breakdown voltages by checking Vci voltage fluctuation.

Table 23 VLOUT Output Status

BT1	BT0	VLOUT Output Status
0	0	Three-times step-up output
0	1	Five-times step-up output
1	0	Six-times step-up output
1	1	Seven-times step-up output

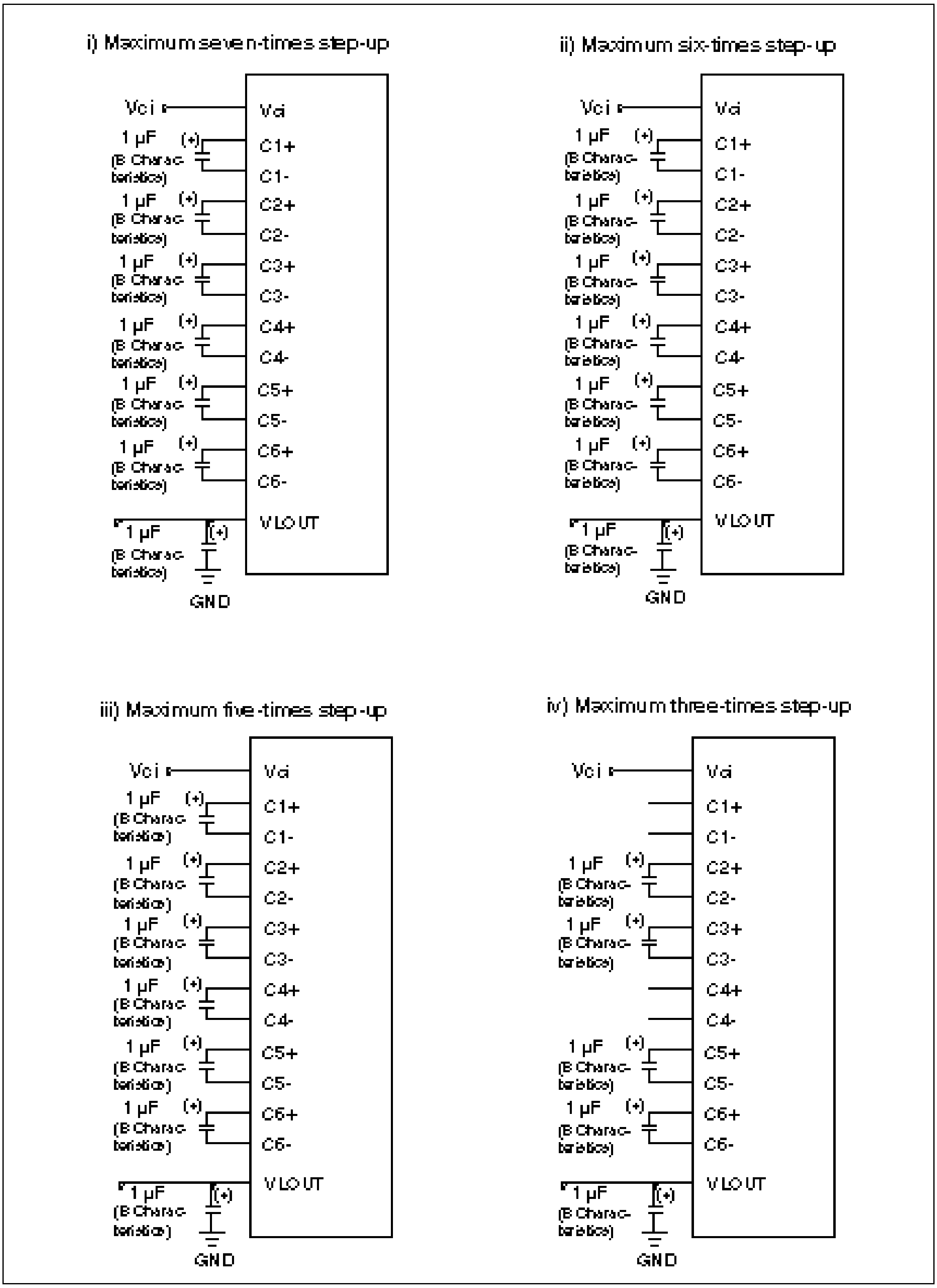


Figure 41 Step-up Circuit Output Factor Switching

Example of Power-supply Voltage Generator for More Than Seven-times Step-up Output

The HD66753 incorporates a step-up circuit for up to seven-times step-up. However, the LCD drive voltage (VLREF) will not be enough for seven-times step-up from Vcc when the power-supply voltage of Vcc is low or when the LCD drive voltage is high for the high-contrast LCD display. In this case, the reference voltage (Vci) for step-up can be set higher than the power-supply voltage of Vcc.

When the step-up factor is high, the current driving ability is lowered and insufficient display quality may result. In this case, the step-up ability can be improved by decreasing the step-up factor as shown in the step-up circuit in figure 42.

Set the Vci input voltage for the step-up circuit to 3.6 V or less. Control the Vci voltage so that the step-up output voltage (VLOUT) should be less than the absolute maximum ratings (20.5 V).

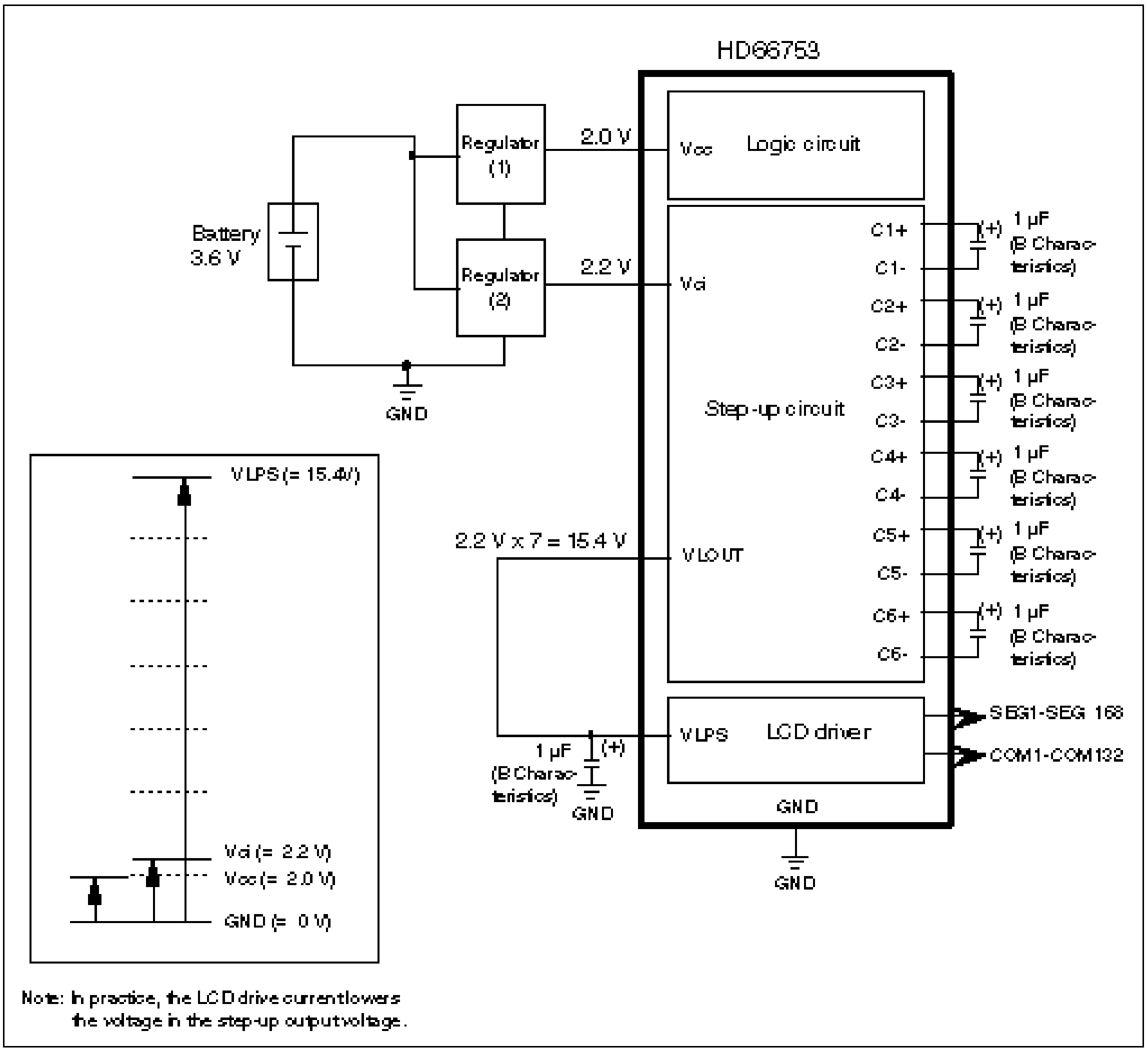


Figure 42 Usage Example of Step-up Circuit at Vci > Vcc

Precautions when Switching Boosting Circuit

The boosting factor of the HD66753 can be switched between 3, 5, 6, and 7 times by instruction. When the factor is switched, there is a transition period before the voltage from VLOUT stabilizes. When VLOUT is used as the VLPS, the boosting factor is changed by switching the BT bit, and the supply voltage for the VLPS is changed, a direct current may be applied to the LCD display if the display is on during the transition period.

When the output voltage of the VLOUT pin is changed, the display must be switched off and on after the output voltage stabilizes.

Table 24 Instructions Accompanying Change in Boosting Factor (example)

Display Contents	Instructions	
All display drive in 1/128 duty to 1/48 duty drive	(1) Display control (R7)	0x0000
	(2) Power control (R1)	0x1914
	(3) 10-ms wait	
	(4) Contrast control (R4)	0x0006
	(5) Driver output control (R1)	0x0245
	(6) Display control (R7)	0x0005

Contrast Adjuster

Software can adjust 128-step contrast for an LCD by varying the liquid-crystal drive voltage (potential difference between V_{LREF} and V1) through the CT bits of the contrast adjustment register (electron volume function). The value of a variable resistor between V_{LREF} and V1 (VR) can be precisely adjusted in a 0.05 x R unit within a range from 0.05 x R through 6.40 x R, where R is a reference resistance obtained by dividing the total resistance.

The HD66753 incorporates a voltage-follower operational amplifier for each of V1 to V5 to reduce current flowing through the internal bleeder resistors, which generate different liquid-crystal drive voltages. Thus, CT5-0 bits must be adjusted so that potential difference between V_{LPS} and V1 is 0.1 V or higher and that between V4 and GND is 1.4 V or higher when liquid-crystal drives, particularly when the VR is small.

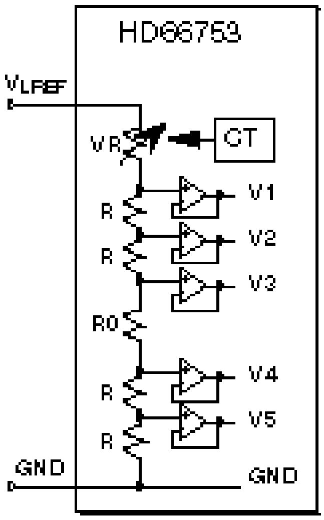


Figure 43 Contrast Adjuster

Table 25 Contrast Adjustment Bits (CT) and Variable Resistor Values

CT Set Value							Variable Resistor Value (VR)	Potential Difference between V1 and GND	Display Color
CT6	CT5	CT4	CT3	CT2	CT1	CT0			
0	0	0	0	0	0	0	6.40 × R	(Small)	(Weak)
0	0	0	0	0	0	1	6.35 × R	▲	▲
0	0	0	0	0	1	0	6.30 × R		
0	0	0	0	0	1	1	6.25 × R		
0	0	0	0	1	0	0	6.20 × R		
0	0	0	0	1	0	1	6.15 × R		
0	0	0	0	1	1	0	6.10 × R		
0	0	0	0	1	1	1	6.05 × R		
0	0	0	1	0	0	0	6.00 × R		
0	0	0	1	0	0	1	5.95 × R		
0	0	0	1	0	1	0	5.90 × R		
0	0	0	1	0	1	1	5.85 × R		
0	0	0	1	1	0	0	5.80 × R		
			⋮				⋮		
0	1	1	1	1	1	1	3.25 × R		
1	0	0	0	0	0	0	3.20 × R		
1	1	0	0	0	0	1	3.15 × R		
1	0	0	0	0	1	0	3.10 × R		
1	0	0	0	0	1	1	3.05 × R		
1	0	0	0	1	0	0	3.00 × R		
1	0	0	0	1	0	1	2.95 × R		
1	0	0	0	1	1	0	2.90 × R		
1	0	0	0	1	1	1	2.85 × R		
1	0	0	1	0	0	0	2.80 × R		
1	0	1	1	0	0	1	2.75 × R		
			⋮				⋮		
1	1	1	1	1	0	0	0.20 × R		
1	1	1	1	1	0	1	0.15 × R	▼	▼
1	1	1	1	1	1	0	0.10 × R		
1	1	1	1	1	1	1	0.05 × R	(Large)	(Bright)

Table 26 Contrast Adjustment per Bias Drive Voltage

Bias	LCD Drive Voltage: V_{DR}	Contrast Adjustment Range
1/11 bias drive	$\frac{11 \times R}{11 \times R + VR} \times (V_{LREF}\text{-}GND)$	- LCD drive voltage adjustment range: $0.775 \times (V_{LREF}\text{-}GND) \le V_{DR} \le 0.995 \times (V_{LREF}\text{-}GND)$ - Limit of potential difference between V4 and GND: $\frac{2 \times R}{11 \times R + VR} \times (V_{LREF}\text{-}GND) \ge 1.4$ [V] - Limit if potential difference between VLPS and V1: $\frac{VR}{11 \times R + VR} \times (V_{LREF}\text{-}GND) \ge 0.1$ [V]
1/10 bias drive	$\frac{10 \times R}{10 \times R + VR} \times (V_{LREF}\text{-}GND)$	- LCD drive voltage adjustment range: $0.757 \times (V_{LREF}\text{-}GND) \le V_{DR} \le 0.995 \times (V_{LREF}\text{-}GND)$ - Limit of potential difference between V4 and GND: $\frac{2 \times R}{10 \times R + VR} \times (V_{LREF}\text{-}GND) \ge 1.4$ [V] - Limit if potential difference between VLPS and V1: $\frac{VR}{10 \times R + VR} \times (V_{LREF}\text{-}GND) \ge 0.1$ [V]
1/9 bias drive	$\frac{9 \times R}{9 \times R + VR} \times (V_{LREF}\text{-}GND)$	- LCD drive voltage adjustment range: $0.737 \times (V_{LREF}\text{-}GND) \le V_{DR} \le 0.994 \times (V_{LREF}\text{-}GND)$ - Limit of potential difference between V4 and GND: $\frac{2 \times R}{9 \times R + VR} \times (V_{LREF}\text{-}GND) \ge 1.4$ [V] - Limit if potential difference between VLPS and V1: $\frac{VR}{9 \times R + VR} \times (V_{LREF}\text{-}GND) \ge 0.1$ [V]
1/8 bias drive	$\frac{8 \times R}{8 \times R + VR} \times (V_{LREF}\text{-}GND)$	- LCD drive voltage adjustment range: $0.714 \times (V_{LREF}\text{-}GND) \le V_{DR} \le 0.993 \times (V_{LREF}\text{-}GND)$ - Limit of potential difference between V4 and GND: $\frac{2 \times R}{8 \times R + VR} \times (V_{LREF}\text{-}GND) \ge 1.4$ [V] - Limit if potential difference between VLPS and V1: $\frac{VR}{8 \times R + VR} \times (V_{LREF}\text{-}GND) \ge 0.1$ [V]
1/7 bias drive	$\frac{7 \times R}{7 \times R + VR} \times (V_{LREF}\text{-}GND)$	- LCD drive voltage adjustment range: $0.686 \times (V_{LREF}\text{-}GND) \le V_{DR} \le 0.993 \times (V_{LREF}\text{-}GND)$ - Limit of potential difference between V4 and GND: $\frac{2 \times R}{7 \times R + VR} \times (V_{LREF}\text{-}GND) \ge 1.4$ [V] - Limit if potential difference between VLPS and V1: $\frac{VR}{7 \times R + VR} \times (V_{LREF}\text{-}GND) \ge 0.1$ [V]
1/6 bias drive	$\frac{6 \times R}{6 \times R + VR} \times (V_{LREF}\text{-}GND)$	- LCD drive voltage adjustment range: $0.652 \times (V_{LREF}\text{-}GND) \le V_{DR} \le 0.992 \times (V_{LREF}\text{-}GND)$ - Limit of potential difference between V4 and GND: $\frac{2 \times R}{6 \times R + VR} \times (V_{LREF}\text{-}GND) \ge 1.4$ [V] - Limit if potential difference between VLPS and V1: $\frac{VR}{6 \times R + VR} \times (V_{LREF}\text{-}GND) \ge 0.1$ [V]
1/5 bias drive	$\frac{5 \times R}{5 \times R + VR} \times (V_{LREF}\text{-}GND)$	- LCD drive voltage adjustment range: $0.610 \times (V_{LREF}\text{-}GND) \le V_{DR} \le 0.990 \times (V_{LREF}\text{-}GND)$ - Limit of potential difference between V4 and GND: $\frac{2 \times R}{5 \times R + VR} \times (V_{LREF}\text{-}GND) \ge 1.4$ [V] - Limit if potential difference between VLPS and V1: $\frac{VR}{5 \times R + VR} \times (V_{LREF}\text{-}GND) \ge 0.1$ [V]
1/4 bias drive	$\frac{4 \times R}{4 \times R + VR} \times (V_{LREF}\text{-}GND)$	- LCD drive voltage adjustment range: $0.556 \times (V_{LREF}\text{-}GND) \le V_{DR} \le 0.988 \times (V_{LREF}\text{-}GND)$ - Limit of potential difference between V4 and GND: $\frac{2 \times R}{4 \times R + VR} \times (V_{LREF}\text{-}GND) \ge 1.4$ [V] - Limit if potential difference between VLPS and V1: $\frac{VR}{4 \times R + VR} \times (V_{LREF}\text{-}GND) \ge 0.1$ [V]

Liquid-crystal-display Drive-bias Selector

An optimum liquid-crystal-display bias value can be selected using the BS2-0 bits, according to the liquid crystal drive duty ratio setting (NL4-0 bits). The liquid-crystal-display drive duty ratio and bias value can be displayed while switching software applications to match the LCD panel display status. The optimum bias value calculated using the following expression is a logical optimum value. Driving by using a lower value than the optimum bias value provides lower logical contrast and lower liquid-crystal-display voltage (the potential difference between V1 and GND), which results in better image quality. When the liquid-crystal-display voltage is insufficient even if a seven-times step-up circuit is used, when the step-up driving ability is lowered by setting a high factor for the step-up circuit, or when the output voltage is lowered because the battery life has been reached, the display can be made easier to see by lowering the liquid-crystal-display bias.

The liquid crystal display can be adjusted by using the contrast adjustment register (CT6-0 bits) and selecting the step-up output level (BT1/0 bits).

$$\text{Optimum bias value for 1/N duty ratio drive voltage} = \frac{1}{\sqrt{N} + 1}$$

Table 27 Optimum Drive Bias Values

LCD drive duty ratio	1/132	1/128	1/120	1/112	1/104	1/96	1/88	1/80	1/72	1/64	1/32	1/24	1/16
(NL4-0 set value)	10H	0FH	0EH	0DH	0CH	0BH	0AH	09H	08H	07H	03H	02H	01H
Optimum drive bias value	1/11	1/11	1/11	1/11	1/11	1/10	1/10	1/10	1/9	1/9	1/6	1/6	1/5
(BS2-0 set value)	000	000	000	000	000	001	001	001	010	010	101	101	110

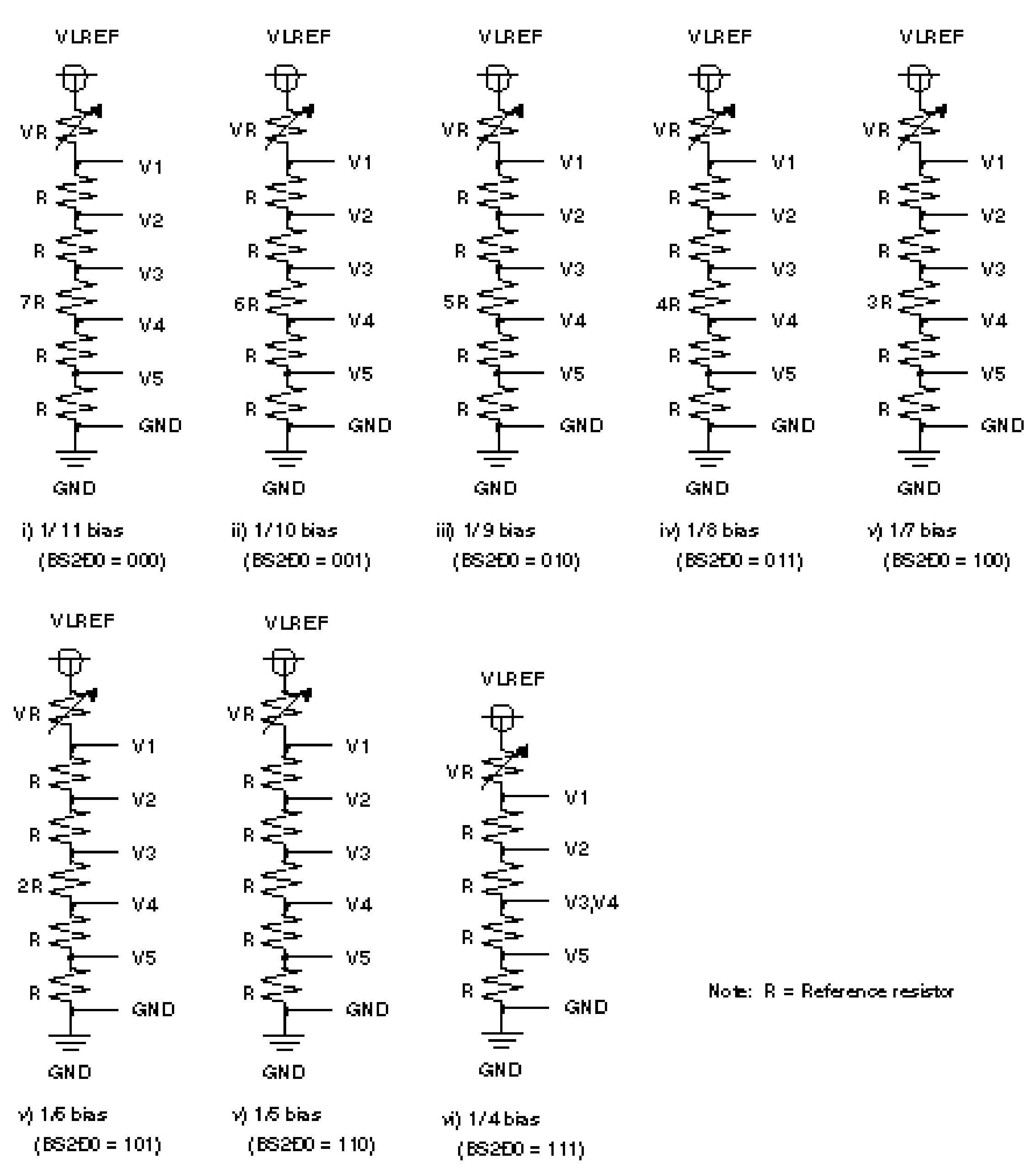


Figure 44 Liquid Crystal Display Drive Bias Circuit

Four-grayscale Display Function

The HD66753 supports the four-grayscale monochrome display function. The four-grayscale monochrome display is used for the display data of the two-bit pixel set sent to the CGRAM. There are four grayscale levels: always unlit, weak middle level, bright middle level, and always lit. In the middle-level grayscale display, the GSL1-0 and GSH1-0 bits can select the grayscale level, respectively.

The frame rate control (FRC) method, which is used for grayscale control, can reduce charge/discharge current in the LCD glass during grayscale display.

Table 28 Relationships between the CGRAM Data and the Display Contents

Upper Bit	Lower Bit	Liquid Crystal Display
0	0	Non-selected (unlit)
0	1	GSL1-0 = 00: 1/4-level grayscale (one frame lit during a four-frame period) GSL1-0 = 01: 1/3-level grayscale (one frame lit during a three-frame period) GSL1-0 = 10: 2/4-level grayscale (two frames lit during a four-frame period) GSL1-0 = 11: Lit (no grayscale control)
1	0	GSH1-0 = 00: 3/4-level grayscale (three frames lit during a four-frame period) GSH1-0 = 01: 2/3-level grayscale (two frames lit during a three-frame period) GSH1-0 = 10: 2/4-level grayscale (two frames lit during a four-frame period) GSH1-0 = 11: Lit (no grayscale control)
1	1	Selected (lit)

Note: Upper bits: DB15, DB13, DB11, DB9, DB7, DB5, DB3, and DB1
Lower bits: DB14, DB12, DB10, DB8, DB6, DB4, DB2, and DB0

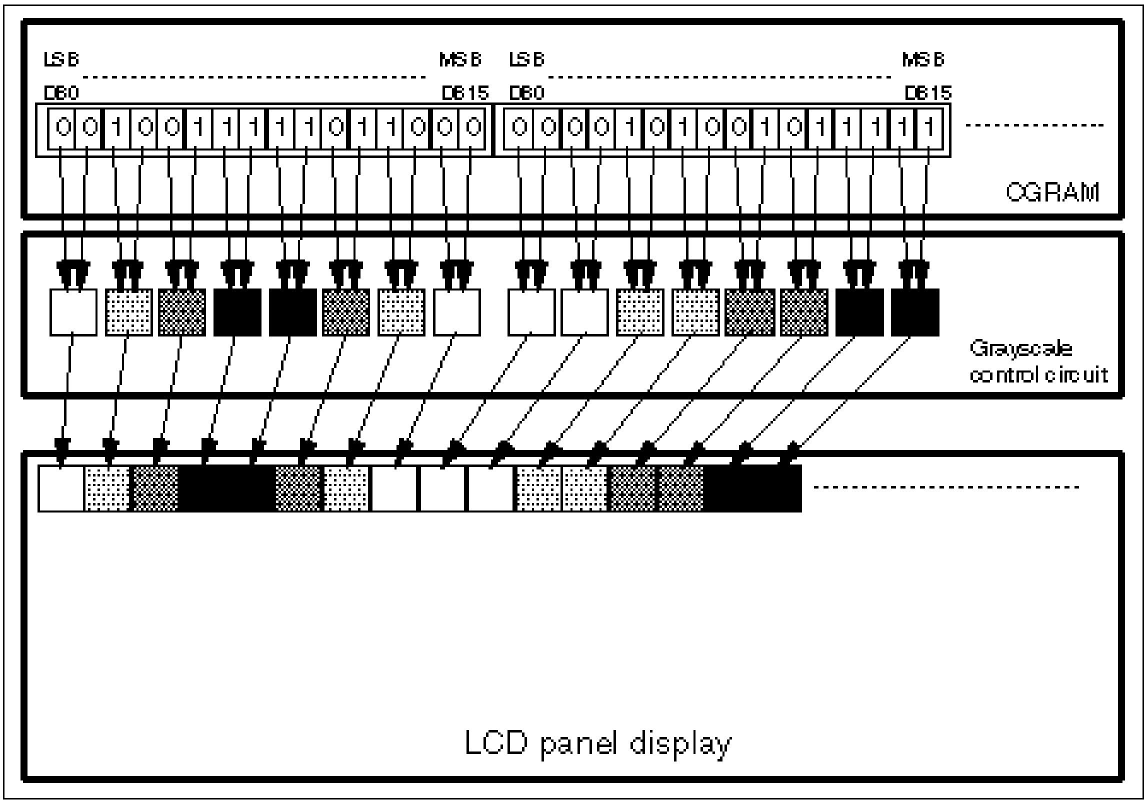


Figure 45 Four-grayscale Monochrome Display

Window Cursor Display Function

The HD66753 displays the window cursor by specifying a window area. The horizontal display position of the window cursor is specified with the horizontal cursor position register (HS6-0 to HE6-0), and the vertical display position is specified with the vertical cursor position register (VS6-0 or VE6-0). In these display position setting registers, ensure that HS6-0 ≤ HE6-0 and VS6-0 ≤ VE6-0. If these relationships are not satisfied, normal display cannot be attained. In addition, if the setting is VS6-0 = VE6-0 = 00H, a cursor is displayed on a raster-row at the most-upper edge of the screen.

This window cursor can automatically display the hardware-supported block cursor, highlight window, or menu bar. The CM1-0 bits select the following four displays in each window cursor:

1. White-blink cursor (CM1-0 = 00): Alternately blinks between the normal display and an all-white (unlit) display
2. Black-blink cursor (CM1-0 = 01): Alternately blinks between the normal display and an all-black (all lit) display
3. Black-and-white reversed cursor (CM1-0 = 10): Normal black-and-white-reversed display (without blinking)
4. Black-and-white reversed blinking cursor (CM1-0 = 11): Alternately blinks between the normal display and a black-and-white-reversed display

The above blinking display is switched in a 32-frame unit. To set a range of the window cursor, specify the display area.

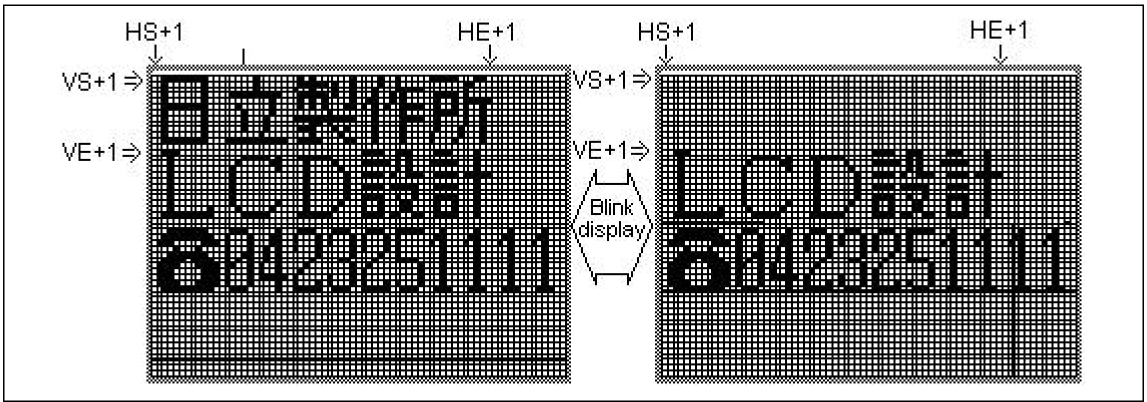


Figure 46 White Blink Cursor Display

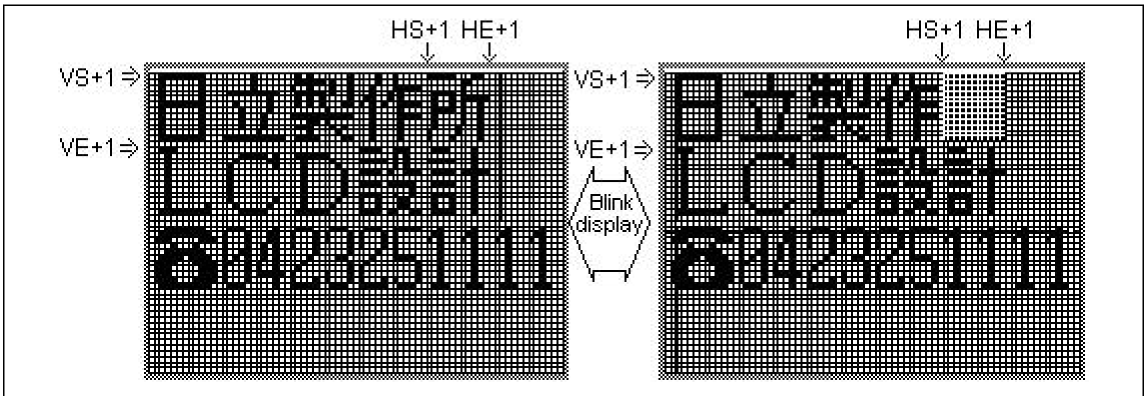


Figure 47 Black Blink Cursor Display

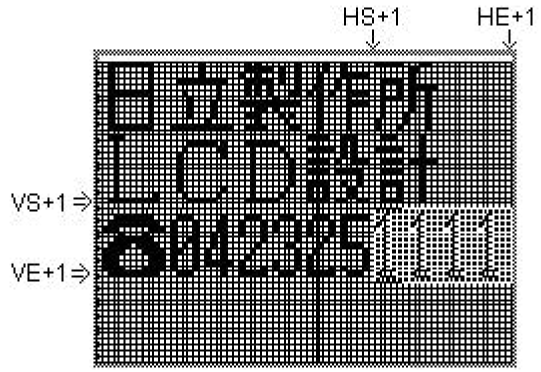


Figure 48 Black-and-white Reversed Cursor Display

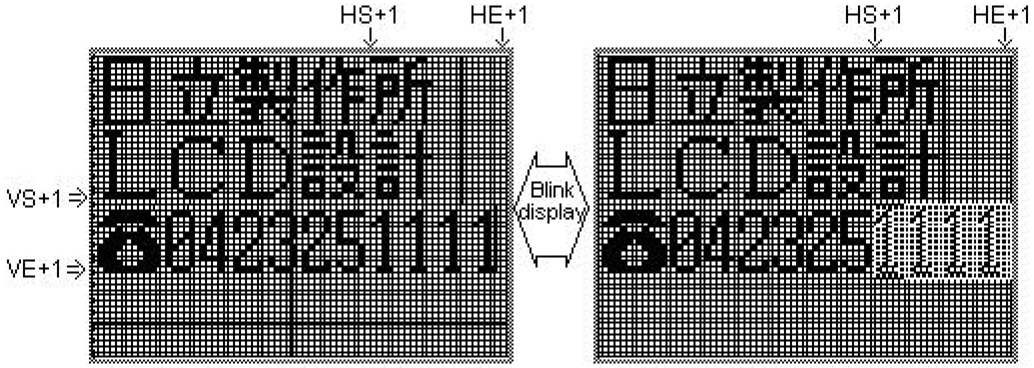


Figure 49 Black-and-white Reversed Blink Cursor Display

Reversed Display Function

The HD66753 can display graphics display sections by black-and-white reversal. Black-and-white reversal can be easily displayed when the REV bit in the display control register is set to 1.

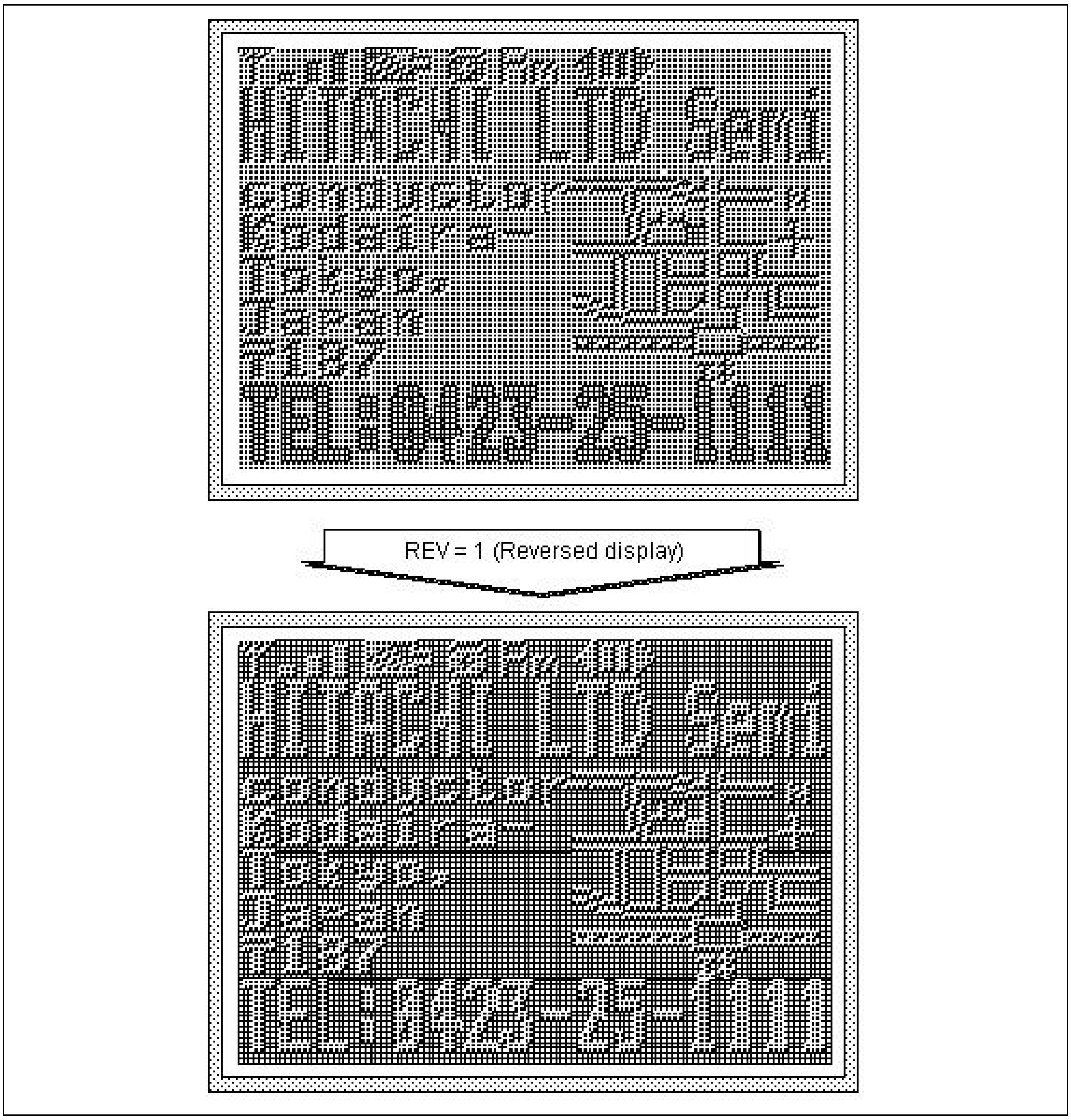


Figure 50 Reversed Display

Screen-division Driving Function

The HD66753 can select and drive two screens at any position with the screen-driving position registers (R0D and R0E). Any two screens required for display are selectively driven and a duty ratio is lowered by LCD-driving duty setting (NL4-0), thus reducing LCD-driving voltage and power consumption.

For the 1st division screen, start line (SS17-10) and end line (SE17-10) are specified by the 1st screen-driving position register (R0D). For the 2nd division screen, start line (SS27-20) and end line (SE27-20) are specified by the 2nd screen-driving position register (R0E). The 2nd screen control is effective when the SPT bit is 1. The total count of selection-driving lines for the 1st and 2nd screens must correspond to the LCD-driving duty set value.

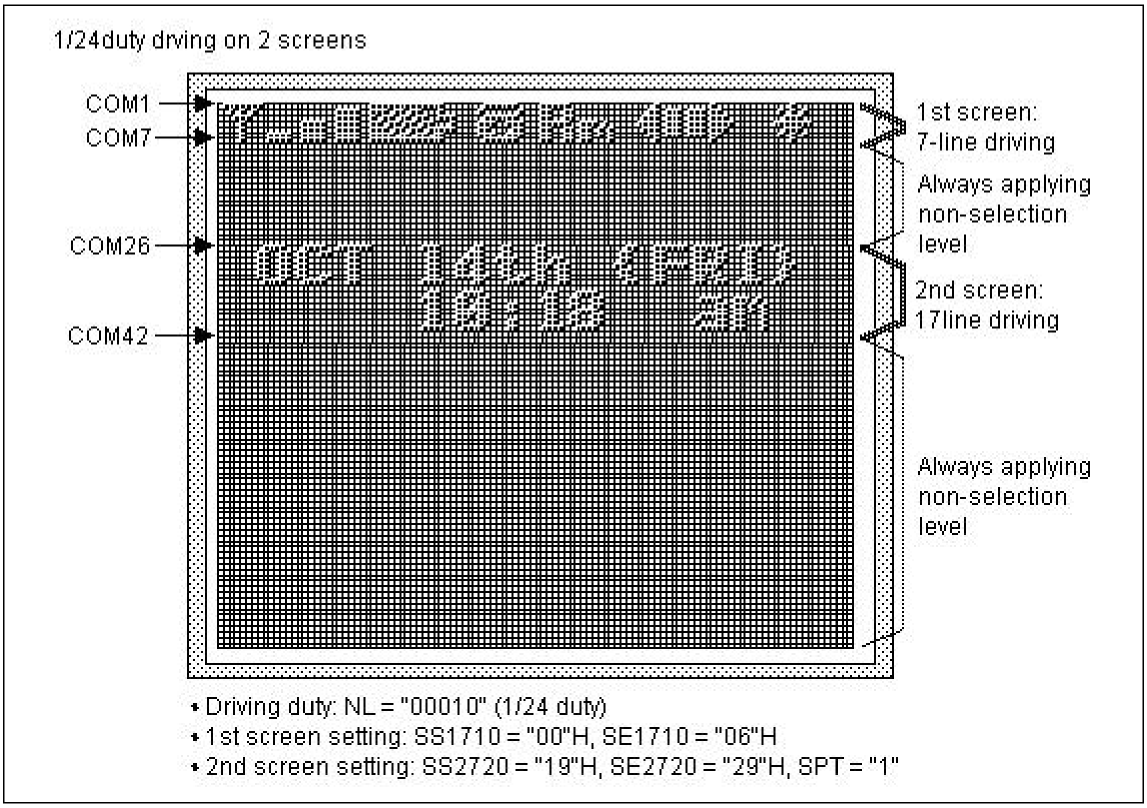


Figure 51 Display Example in 2-screen Division Driving

Restrictions on the 1st/2nd Screen Driving Position Register Settings

The following restrictions must be satisfied when setting the start line (SS17-10) and end line (SE17-10) of the 1st screen driving position register (R0D) and the start line (SS27-20) and end line (SE27-20) of the 2nd screen driving position register (R0D) for the HD66753. Note that incorrect display may occur if the restrictions are not satisfied.

Table 29 Restrictions on the 1st/2nd Screen Driving Position Register Settings

	1st Screen Driving (STP = 0)	2nd Screen Driving (STP = 1)
Register setting	SS17-10 ≤ SE17-0 ≤ 83H	SS17-10 ≤ SE17-10 < SS17-10 ≤ SE17-0 ≤ 83H
Display operation	• Time-sharing driving for COM pins (SS1+1) to (SE1+1) • Non-selection level driving for others	• Time-sharing driving for COM pins (SS1+1) to (SE1+1) and (SS2+1) to (SE2+1) • Non-selection level driving for others

Notes: 1. When the total line count in screen division driving settings is less than the duty setting, non-selection level driving is performed without the screen division driving setting range.
2. When the total line count in screen division driving settings is larger than the duty setting, the start line, the duty-setting line, and the lines between them are displayed and non-selection level driving is performed for other lines.
3. For the 1st screen driving, the SS27-20 and SE27-20 settings are ignored.

Sleep Mode

Setting the sleep mode bit (SLP) to 1 puts the HD66753 in the sleep mode, where the device stops all internal display operations, thus reducing current consumption. Specifically, LCD operation is completely halted. Here, all the SEG (SEG1 to SEG168) and COM (COM1 to COM132) pins output the GND level, resulting in no display. If the AP1-0 bits in the power control register are set to 00 in the sleep mode, the LCD drive power supply can be turned off, reducing the total current consumption of the LCD module.

Table 30 Comparison of Sleep Mode and Standby Mode

Function	Sleep Mode (SLP = 1)	Standby Mode (STB = 1)
LCD control	Turned off	Turned off
R-C oscillation circuit	Operates normally	Operation stopped

Standby Mode

Setting the standby mode bit (STB) to 1 puts the HD66753 in the standby mode, where the device stops completely, halting all internal operations including the R-C oscillation circuit, thus further reducing current consumption compared to that in the sleep mode. Specifically, all the SEG (SEG1 to SEG168) and COM (COM1 to COM132) pins for the time-sharing drive output the GND level, resulting in no display. If the AP1-0 bits are set to 00 in the standby mode, the LCD drive power supply can be turned off.

During the standby mode, no instructions can be accepted other than the start-oscillation instruction. To cancel the standby mode, issue the start-oscillation instruction to stabilize R-C oscillation before setting the STB bit to 0.

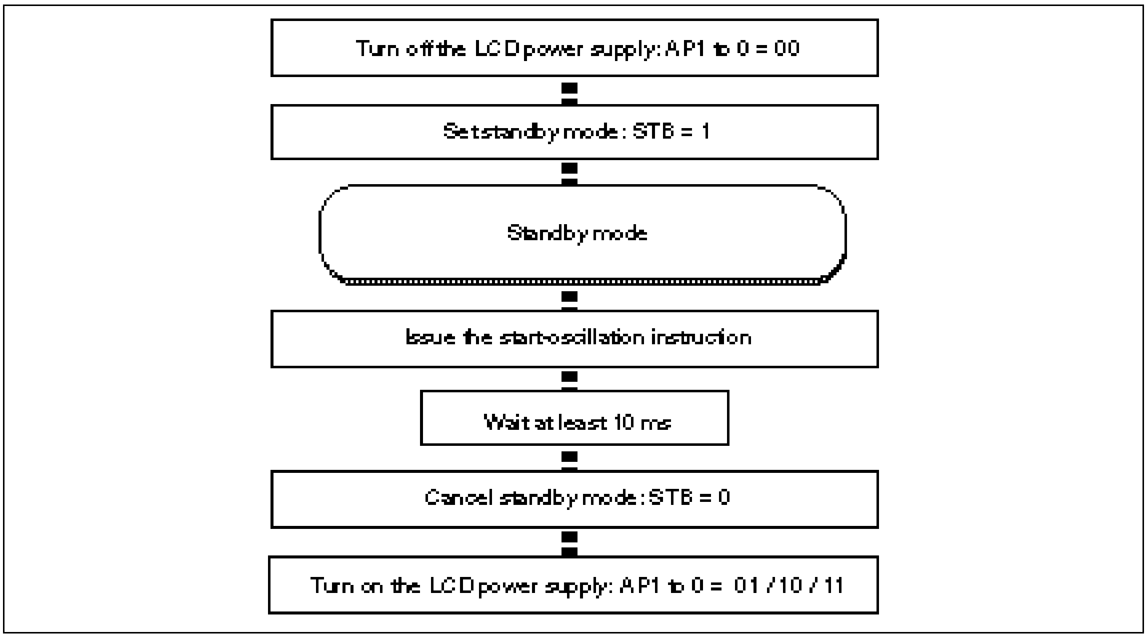


Figure 52 Procedure for Setting and Canceling Standby Mode

Absolute Maximum Ratings

Item	Symbol	Unit	Value	Notes*
Power supply voltage (1)	V_{CC}	V	–0.3 to +4.6	1, 2
Power supply voltage (2)	V_{LPS} – GND	V	–0.3 to +20.5	1, 3
Input voltage	Vt	V	–0.3 to V_{CC} + 0.3	1
Operating temperature	Topr	°C	–40 to +85	1, 4
Storage temperature	Tstg	°C	–55 to +110	1, 5

Notes: 1. If the LSI is used above these absolute maximum ratings, it may become permanently damaged. Using the LSI within the following electrical characteristics limits is strongly recommended for normal operation. If these electrical characteristic conditions are also exceeded, the LSI will malfunction and cause poor reliability.

2. VCC > GND must be maintained.
3. VLPS > GND must be maintained.
4. For bare die and wafer products, specified up to 85 C.
5. This temperature specifications apply to the TCP package.

DC Characteristics (V_{CC} = 1.7 to 3.6 V, Ta = –40 to +85°C*[1])

Item	Symbol	Min	Typ	Max	Unit	Test Condition	Notes
Input high voltage	V_{IH}	0.7 V_{CC}	—	V_{CC}	V		2, 3
Input low voltage	V_{IL}	–0.3	—	0.15 V_{CC}	V	V_{CC} = 1.7 to 2.4 V	2, 3
		–0.3	—	0.15 V_{CC}	V	V_{CC} = 2.4 to 3.6 V	2, 3
Output high voltage (1) (DB0-15 and SDA pins)	V_{OH1}	0.75 V_{CC}	—	—	V	I_{OH} = –0.1 mA	2
Output low voltage (1) (DB0-15 and SDA pins)	V_{OL1}	—	—	0.2 V_{CC}	V	V_{CC} = 1.7 to 2.4 V, I_{OL} = 0.1 mA	2
		—	—	0.15 V_{CC}	V	V_{CC} = 2.4 to 3.6 V, I_{OL} = 0.1 mA	2
Driver ON resistance (COM pins)	R_{COM}	—	3	10	kΩ	±Id = 0.05 mA, V_{LPS} = 10 V	4
Driver ON resistance (SEG pins)	R_{SEG}	—	3	10	kΩ	±Id = 0.05 mA, V_{LPS} = 10 V	4
I/O leakage current	I_{Li}	–1	—	1	µA	Vin = 0 to V_{CC}	5
Current consumption during normal operation (V_{CC} – GND)	I_{OP}	—	70	100	µA	R-C oscillation, V_{CC} = 3 V, Ta = 25 °C, f_{OSC} = 70 kHz (1/120 duty), RAM write: checker pattern	6, 7
Current consumption during standby mode (V_{CC} – GND)	I_{ST}	—	0.1	5	µA	V_{CC} = 3 V, Ta = 25°C	6, 7
LCD drive power supply current (V_{LPS} – GND)	I_{LPS}	—	28	40	µA	V_{CC} = 3 V, V_{LPS} = 15 V, 1/11 bias, Ta = 25 °C, f_{OSC} = 70 kHz, amount of fixed current in the operational amplifier: small	7
LCD drive voltage (V_{LPS} – GND)	V_{LPS}	5.0	—	19.5	V		8
VREG input voltage (VREG pin)	V_{REG}	—	1.3	2.5	V	VREG external input (PS1-0 = 10), Ta = 25 °C	
V1REF output voltage (V1REF pin)	V_{1REF}	—	13.0	—	V	VREG = 1.3 V, Ta = 25 °C, 11 times of VREG (VR2-0 = 111), V1REF ≤ VLPS – 0.5 V	

Note: For the numbered notes, refer to the Electrical Characteristics Notes section following these tables.

Step-up Circuit Characteristics

Item	Symbol	Min	Typ	Max	Unit	Test Condition	Notes
Three-times step-up output voltage (VLOUT pin)	V_{UP2}	7.6	8.0	8.1	V	V_{CC} = Vci = 2.7 V, I_O = 30 µA, C = 1 µF, f_{OSC} = 100 kHz, Ta = 25°C	11
Five-times step-up output voltage (VLOUT pin)	V_{UP5}	13.0	13.3	13.5	V	V_{CC} = Vci = 2.7 V, I_O = 30 µA, C = 1 µF, f_{OSC} = 100 kHz, Ta = 25°C	11
Six-times step-up output voltage (VLOUT pin)	V_{UP6}	12.7	12.9	13.2	V	V_{CC} = Vci = 2.2 V, I_O = 30 µA, C = 1 µF, f_{OSC} = 100 kHz, Ta = 25°C	11
Seven-times step-up output voltage (VLOUT pin)	V_{UP7}	14.9	15.1	15.4	V	V_{CC} = Vci = 2.2 V, I_O = 30 µA, C = 1 µF, f_{OSC} = 100 kHz, Ta = 25°C	11
Use range of step-up output voltages	V_{UP2} V_{UP5} V_{UP6} V_{UP7}	Vcc	—	16.5	V	For two- to seven-times step-up	11

Note: For the numbered notes, refer to the Electrical Characteristics Notes section following these tables.

AC Characteristics (V_{CC} = 1.7 to 3.6 V, Ta = –40 to +85°C*[1])

Clock Characteristics (V_{CC} = 1.7 to 3.6 V)

Item	Symbol	Min	Typ	Max	Unit	Test Condition	Notes
External clock frequency	fcp	50	75	150	kHz		9
External clock duty ratio	Duty	45	50	55	%		9
External clock rise time	trcp	—	—	0.2	µs		9
External clock fall time	tfcp	—	—	0.2	µs		9
R-C oscillation clock	f_{OSC}	59	74	89	kHz	Rf = 330 kΩ, V_{CC} = 3 V	10

Note: For the numbered notes, refer to the Electrical Characteristics Notes section following these tables.

68-system Bus Interface Timing Characteristics

(Vcc = 1.7 to 2.4 V)

Item		Symbol	Min	Typ	Max	Unit	Test Condition
Enable cycle time	Write	t_{CYCE}	600	—	—	ns	Figure 60
	Read	t_{CYCE}	800	—	—		
Enable high-level pulse width	Write	PW_{EH}	120	—	—	ns	Figure 60
	Read	PW_{EH}	350	—	—		
Enable low-level pulse width	Write	PW_{EL}	300	—	—	ns	Figure 60
	Read	PW_{EL}	400	—	—		
Enable rise/fall time		t_{Er}, t_{Ef}	—	—	25	ns	Figure 60
Setup time (RS, R/W to E, CS*)		t_{ASE}	50	—	—	ns	Figure 60
Address hold time		t_{AHE}	20	—	—	ns	Figure 60
Write data setup time		t_{DSWE}	60	—	—	ns	Figure 60
Write data hold time		t_{HE}	20	—	—	ns	Figure 60
Read data delay time		t_{DDRE}	—	—	300	ns	Figure 60
Read data hold time		t_{DHRE}	5	—	—	ns	Figure 60

(Vcc = 2.4 to 3.6 V)

Item		Symbol	Min	Typ	Max	Unit	Test Condition
Enable cycle time	Write	t_{CYCE}	380	—	—	ns	Figure 60
	Read	t_{CYCE}	500	—	—		
Enable high-level pulse width	Write	PW_{EH}	70	—	—	ns	Figure 60
	Read	PW_{EH}	250	—	—		
Enable low-level pulse width	Write	PW_{EL}	150	—	—	ns	Figure 60
	Read	PW_{EL}	200	—	—		
Enable rise/fall time		t_{Er}, t_{Ef}	—	—	25	ns	Figure 60
Setup time (RS, R/W to E, CS*)		t_{ASE}	50	—	—	ns	Figure 60
Address hold time		t_{AHE}	20	—	—	ns	Figure 60
Write data setup time		t_{DSWE}	60	—	—	ns	Figure 60
Write data hold time		t_{HE}	20	—	—	ns	Figure 60
Read data delay time		t_{DDRE}	—	—	200	ns	Figure 60
Read data hold time		t_{DHRE}	5	—	—	ns	Figure 60

80-system Bus Interface Timing Characteristics

(Vcc = 1.7 to 2.4 V)

Item		Symbol	Min	Typ	Max	Unit	Test Condition
Bus cycle time	Write	t_{CYCW}	600	—	—	ns	Figure 61
	Read	t_{CYCR}	800	—	—	ns	Figure 61
Write low-level pulse width		PW_{LW}	120	—	—	ns	Figure 61
Read low-level pulse width		PW_{LR}	350	—	—	ns	Figure 61
Write high-level pulse width		PW_{HW}	300	—	—	ns	Figure 61
Read high-level pulse width		PW_{HR}	400	—	—	ns	Figure 61
Write/Read rise/fall time		t_{WRr}, $_{WRf}$	—	—	25	ns	Figure 61
Setup time (RS to CS*, WR*, RD*)		t_{AS}	50	—	—	ns	Figure 61
Address hold time		t_{AH}	20	—	—	ns	Figure 61
Write data setup time		t_{DSW}	60	—	—	ns	Figure 61
Write data hold time		t_{H}	20	—	—	ns	Figure 61
Read data delay time		t_{DDR}	—	—	300	ns	Figure 61
Read data hold time		t_{DHR}	5	—	—	ns	Figure 61

(Vcc = 2.4 to 3.6 V)

Item		Symbol	Min	Typ	Max	Unit	Test Condition
Bus cycle time	Write	t_{CYCW}	380	—	—	ns	Figure 61
	Read	t_{CYCR}	500	—	—	ns	Figure 61
Write low-level pulse width		PW_{LW}	70	—	—	ns	Figure 61
Read low-level pulse width		PW_{LR}	250	—	—	ns	Figure 61
Write high-level pulse width		PW_{HW}	150	—	—	ns	Figure 61
Read high-level pulse width		PW_{HR}	200	—	—	ns	Figure 61
Write/Read rise/fall time		$t_{WRr, WRf}$	—	—	25	ns	Figure 61
Setup time (RS to CS*, WR*, RD*)		t_{AS}	50	—	—	ns	Figure 61
Address hold time		t_{AH}	20	—	—	ns	Figure 61
Write data setup time		t_{DSW}	60	—	—	ns	Figure 61
Write data hold time		t_{H}	20	—	—	ns	Figure 61
Read data delay time		t_{DDR}	—	—	200	ns	Figure 61
Read data hold time		t_{DHR}	5	—	—	ns	Figure 61

Clock-synchronized Serial Interface Timing Characteristics

(Vcc = 1.7 to 2.4 V)

Item		Symbol	Min	Typ	Max	Unit	Test Condition
Serial clock cycle time	Write (receive)	t_{SCYC}	100	—	2000	ns	Figure 62
	Read (send)	t_{SCYC}	250	—	2000	ns	Figure 62
Serial clock high-level width	Write (receive)	t_{SCH}	40	—	—	ns	Figure 62
	Read (send)	t_{SCH}	120	—	—	ns	Figure 62
Serial clock low-level width	Write (receive)	t_{SCL}	40	—	—	ns	Figure 62
	Read (send)	t_{SCL}	120	—	—	ns	Figure 62
Serial clock rise/fall time		t_{scf} , t_{scr}	—	—	20	ns	Figure 62
Chip-select setup time		t_{CSU}	20	—	—	ns	Figure 62
Chip-select hold time		t_{CH}	60	—	—	ns	Figure 62
Serial input data setup time		t_{SISU}	30	—	—	ns	Figure 62
Serial input data hold time		t_{SIH}	30	—	—	ns	Figure 62
Serial output data delay time		t_{SCD}	—	—	200	ns	Figure 62
Serial output data hold time		t_{SCH}	5	—	—	ns	Figure 62

(Vcc = 2.4 to 3.6 V)

Item		Symbol	Min	Typ	Max	Unit	Test Condition
Serial clock cycle time	Write (receive)	t_{SCYC}	100	—	2000	ns	Figure 62
	Read (send)	t_{SCYC}	250	—	2000	ns	Figure 62
Serial clock high-level width	Write (receive)	t_{SCH}	40	—	—	ns	Figure 62
	Read (send)	t_{SCH}	120	—	—	ns	Figure 62
Serial clock low-level width	Write (receive)	t_{SCL}	40	—	—	ns	Figure 62
	Read (send)	t_{SCL}	120	—	—	ns	Figure 62
Serial clock rise/fall time		t_{scf} , t_{scr}	—	—	20	ns	Figure 62
Chip-select setup time		t_{CSU}	20	—	—	ns	Figure 62
Chip-select hold time		t_{CH}	60	—	—	ns	Figure 62
Serial input data setup time		t_{SISU}	30	—	—	ns	Figure 62
Serial input data hold time		t_{SIH}	30	—	—	ns	Figure 62
Serial output data delay time		t_{SCD}	—	—	200	ns	Figure 62
Serial output data hold time		t_{SCH}	5	—	—	ns	Figure 62

Reset Timing Characteristics (V_{CC} = 1.7 to 3.6 V)

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Reset low-level width	t_{RES}	1	—	—	ms	Figure 63

Electrical Characteristics Notes

1. For bare die products, specified up to +85°C.
2. The following three circuits are I/O pin configurations (figure 53).

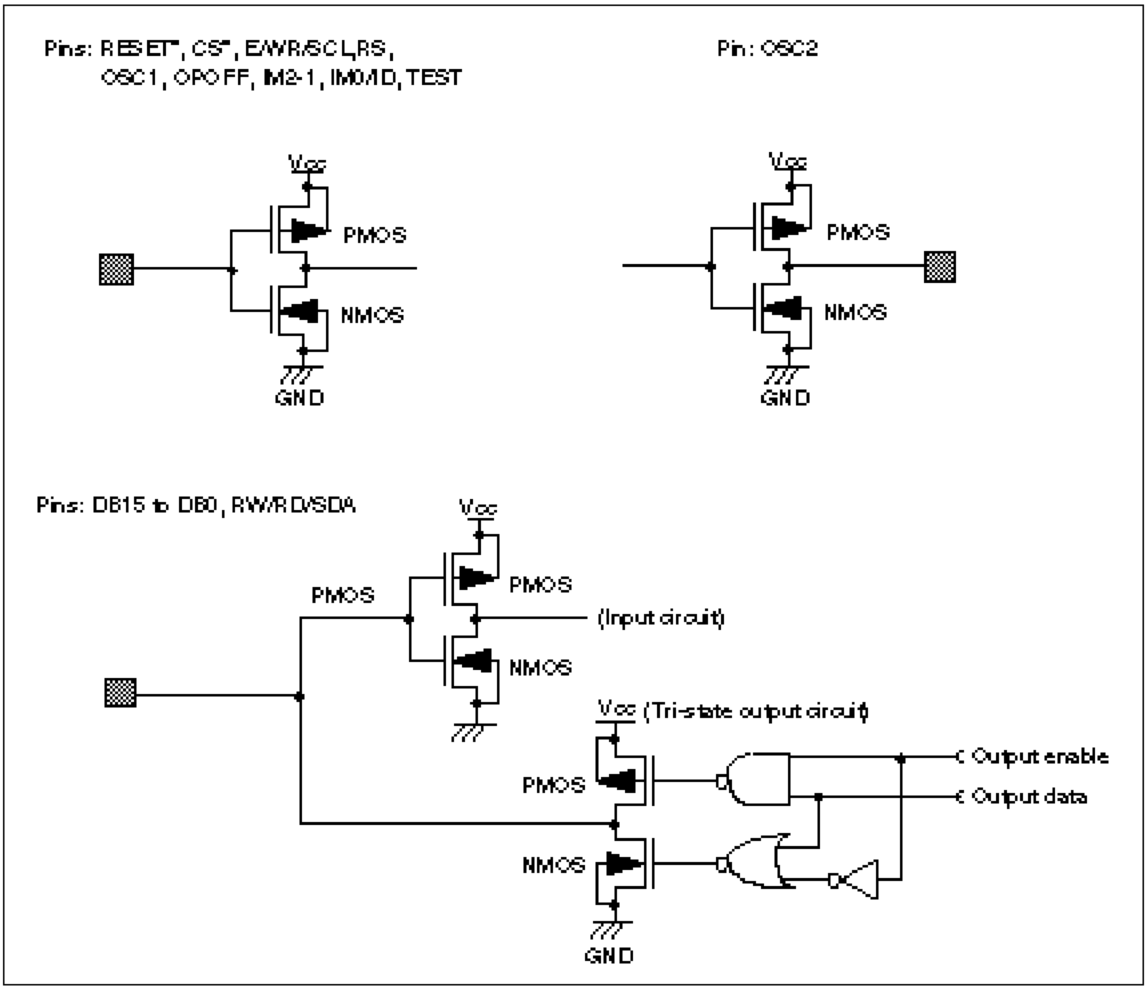


Figure 53 I/O Pin Configuration

3. The TEST pin must be grounded and the IM1/0 and OPOFF pins must be grounded or connected to Vcc.
4. Applies to the resistor value (RCOM) between power supply pins V1OUT, V2OUT, V5OUT, GND and common signal pins, and resistor value (RSEG) between power supply pins V1OUT, V3OUT, V4OUT, GND and segment signal pins.
5. This excludes the current flowing through output drive MOSs.
6. This excludes the current flowing through the input/output units. The input level must be fixed high or low because through current increases if the CMOS input is left floating.
7. The following shows the relationship between the operation frequency (fosc) and current consumption (Icc) (figure 54).

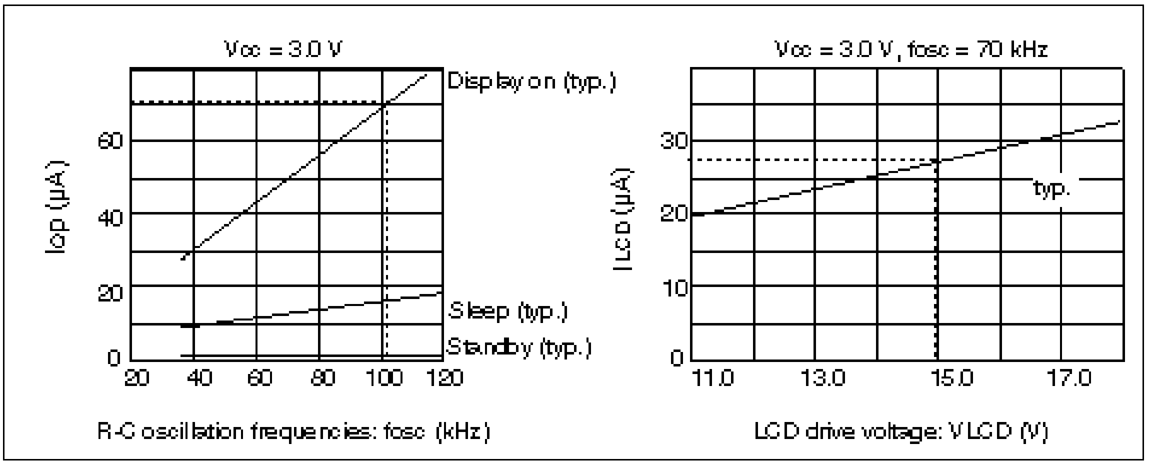


Figure 54 Relationship between the Operation Frequency and Current Consumption

8. Each COM and SEG output voltage is within ±0.15 V of the LCD voltage (Vcc, V1, V2, V3, V4, V5) when there is no load.
9. Applies to the external clock input (figure 55).

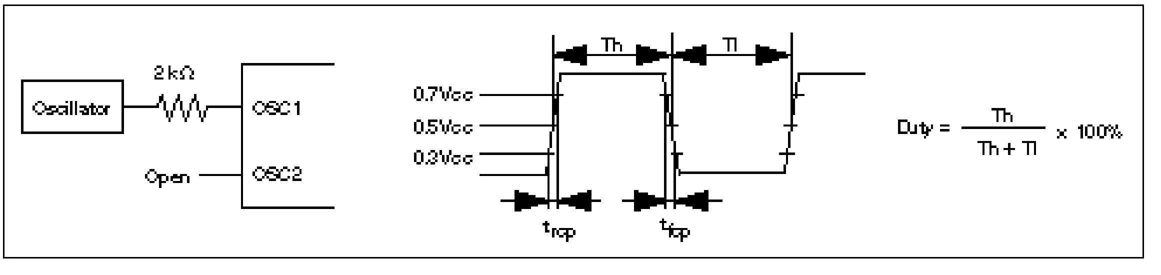


Figure 55 External Clock Supply

10. Applies to the internal oscillator operations using external oscillation resistor Rf (figure 56 and table 31).

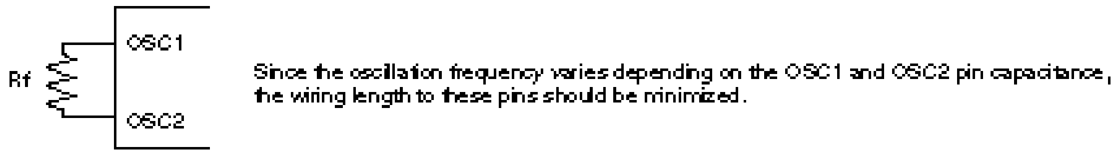


Figure 56 Internal Oscillation

Table 31 External Resistance Value and R-C Oscillation Frequency (Referential Data)

External Resistance (Rf)	R-C Oscillation Frequency: fosc			
	Vcc = 1.8 V	Vcc = 2.2 V	Vcc = 3.0 V	Vcc = 3.6 V
200 kΩ	89 kHz	103 kHz	115 kHz	121 kHz
270 kΩ	70 kHz	80 kHz	88 kHz	92 kHz
300 kΩ	65 kHz	73 kHz	80 kHz	83 kHz
330 kΩ	60 kHz	68 kHz	74 kHz	77 kHz
360 kΩ	55 kHz	62 kHz	68 kHz	71 kHz
390 kΩ	52 kHz	58 kHz	64 kHz	66 kHz
430 kΩ	48 kHz	53 kHz	58 kHz	60 kHz
470 kΩ	44 kHz	48 kHz	52 kHz	54 kHz

11. The step-up characteristics test circuit is shown in figure 57.

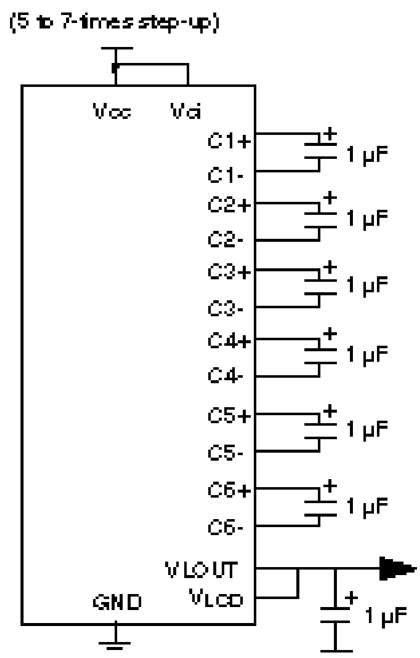


Figure 57 Step-up Characteristics Test Circuit

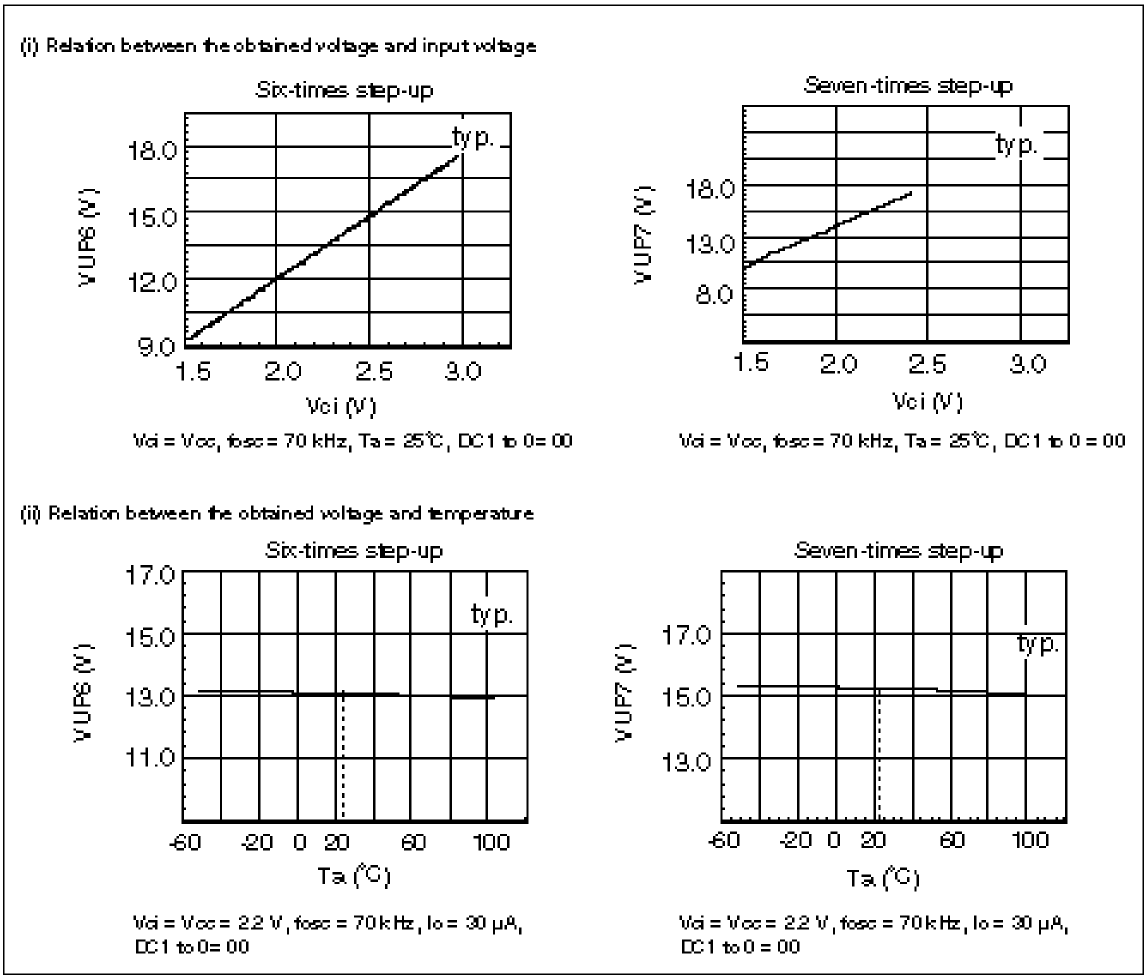


Figure 58 Step-up

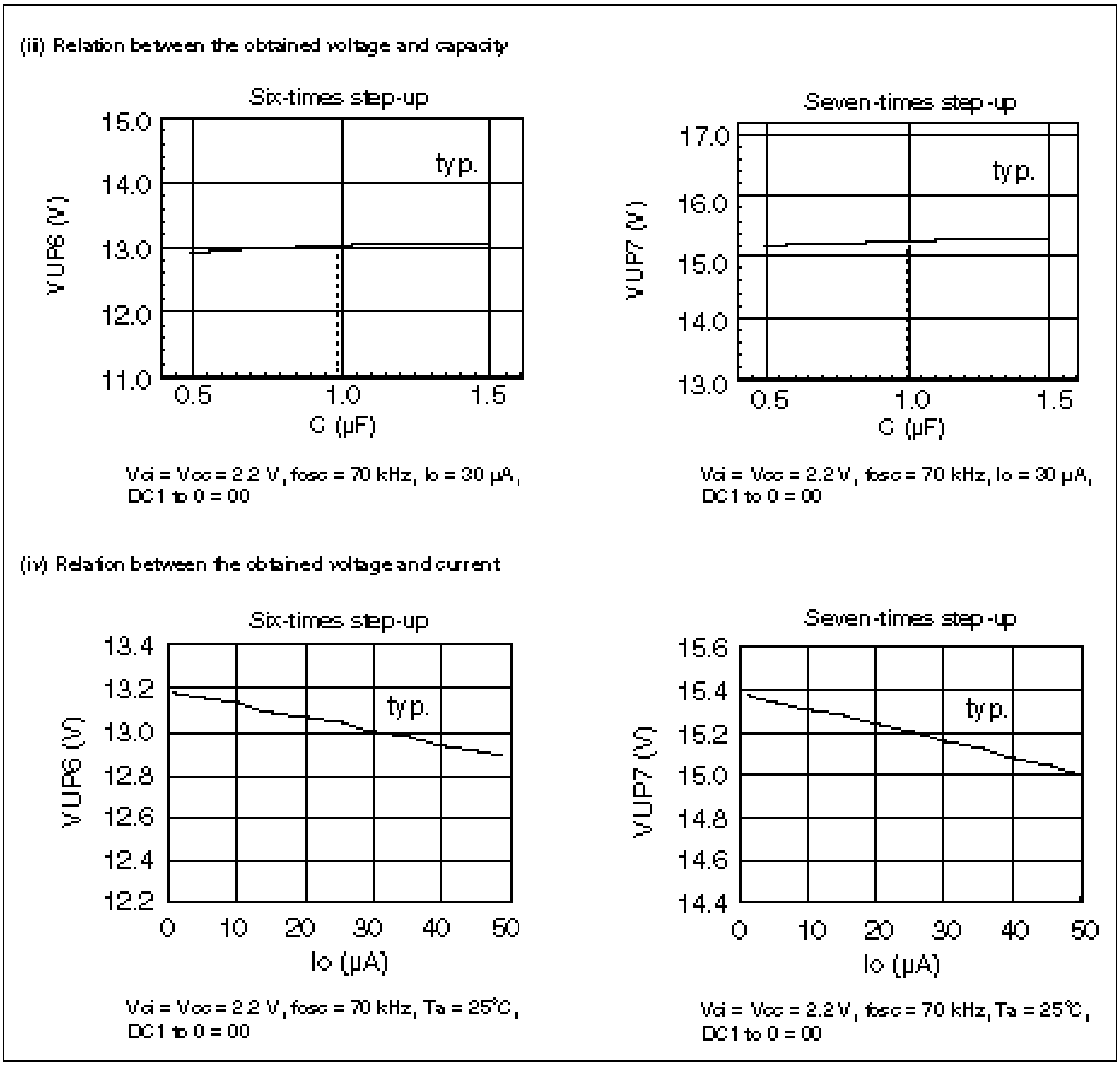


Figure 58 Step-up (cont)

AC Characteristics Test Load Circuits

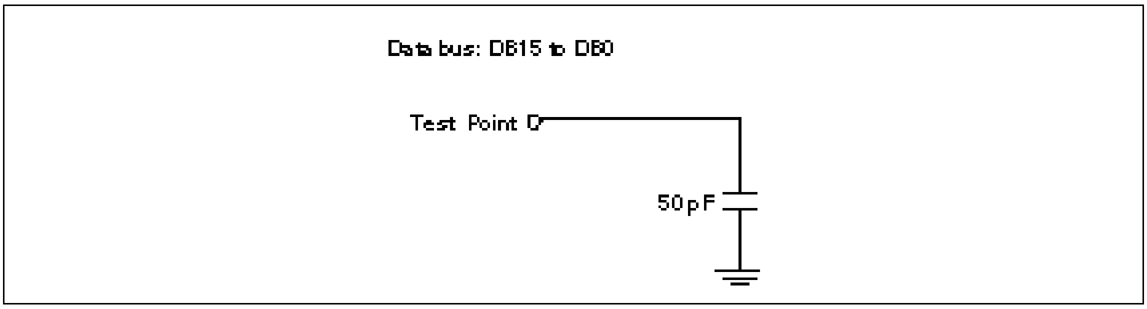


Figure 59 Load Circuit

Timing Characteristics

68-system Bus Operation

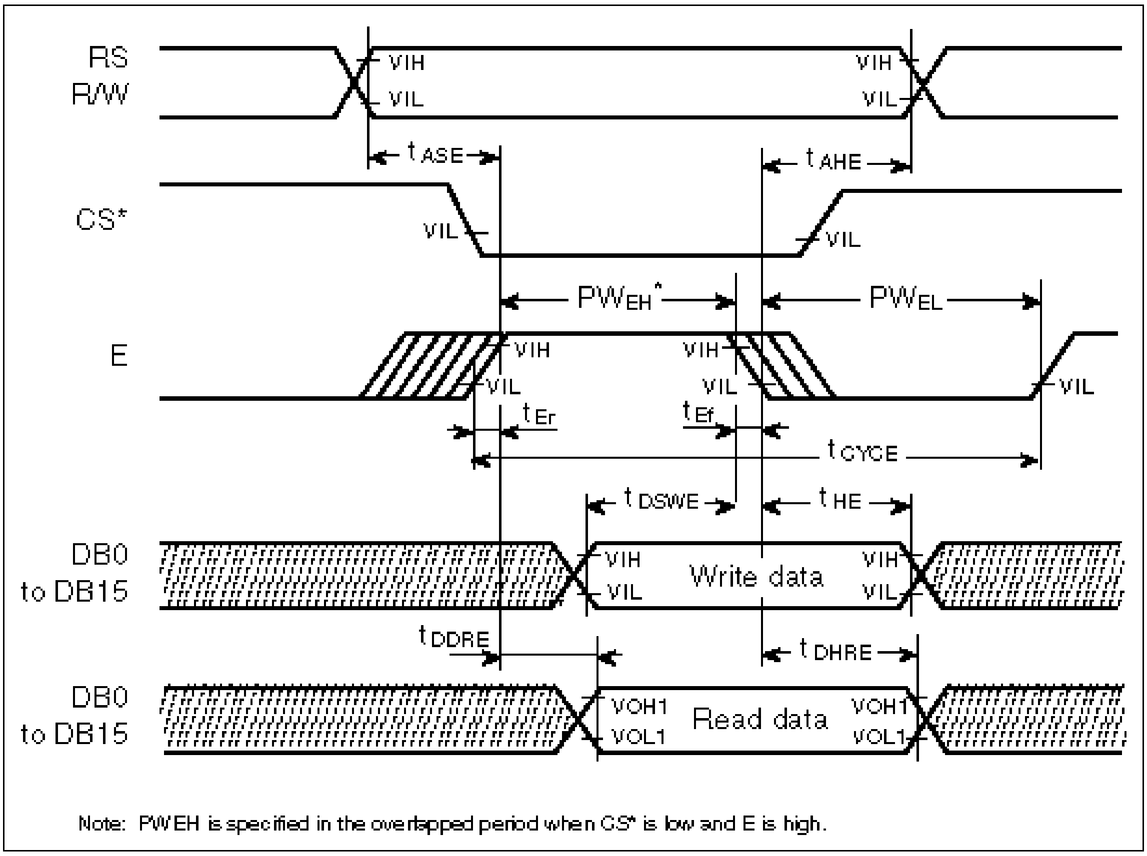


Figure 60   68-system Bus Timing

80-system Bus Operation

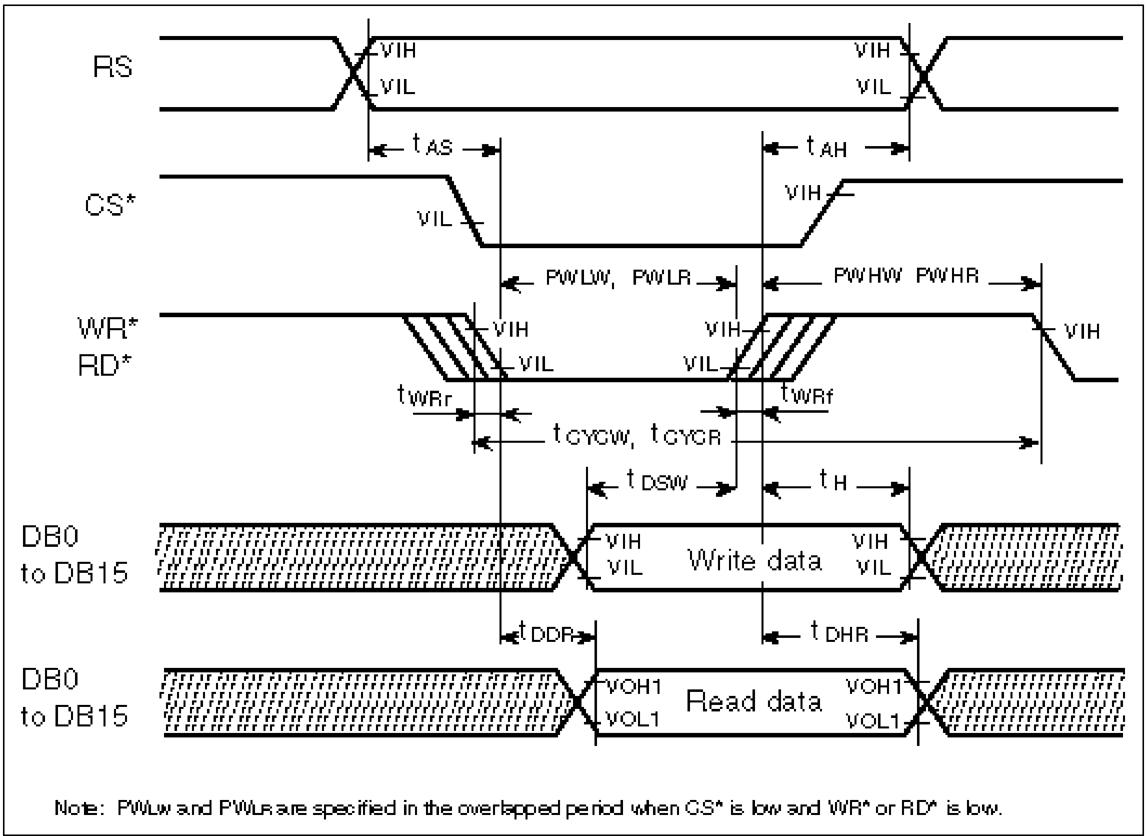


Figure 61 80-system Bus Timing

Clock-synchronized Serial Operation

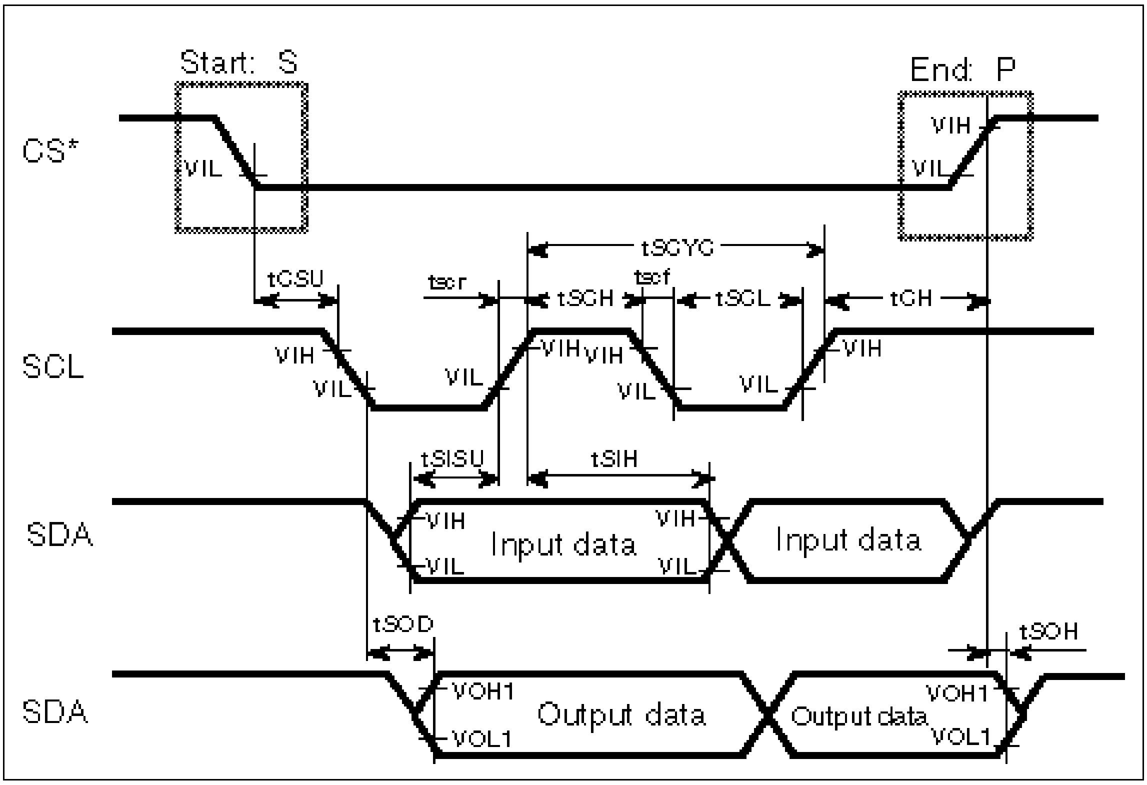


Figure 62 Clock-synchronized Serial Interface Timing

Reset Operation

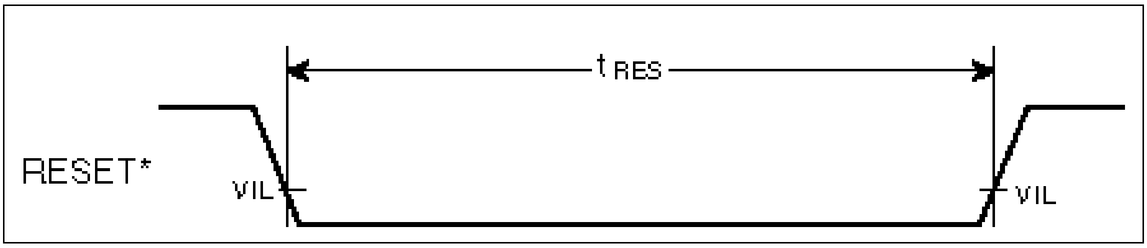


Figure 63 Reset Timing

Power-on/off Sequence

To prevent pulse lighting of LCD screens at power-on/off, the power-on/off sequence is activated as shown below. However, since the sequence depends on LCD materials to be used, confirm the conditions by using your own system.

Power-on Sequence

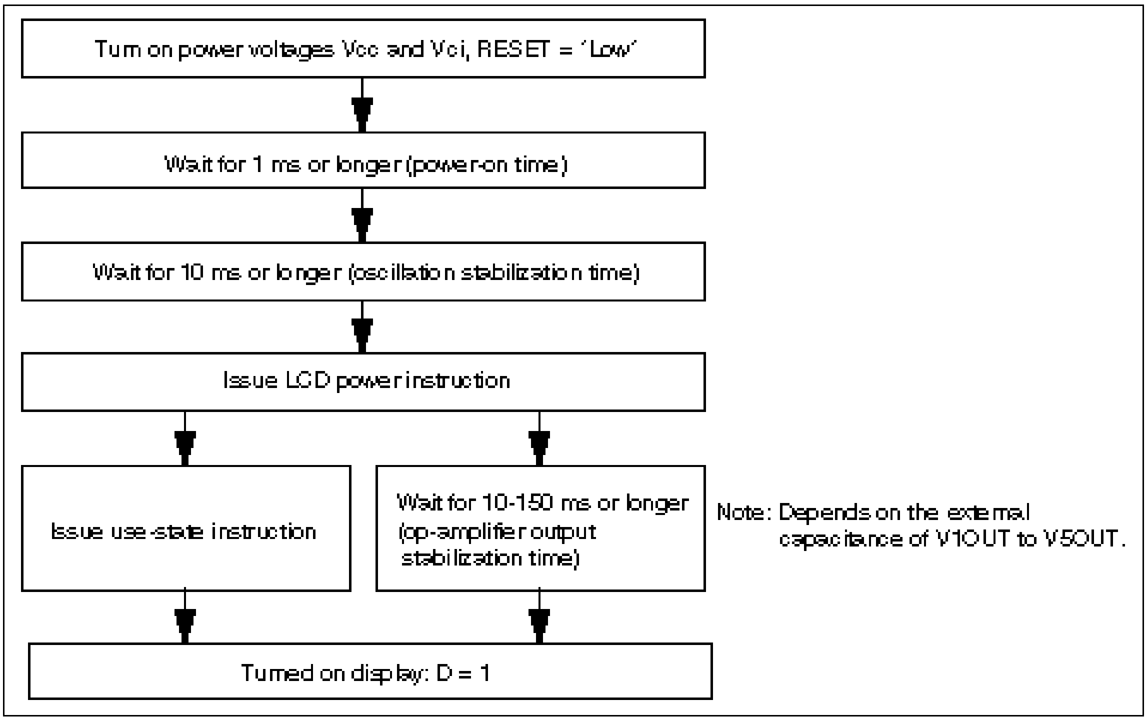


Figure 64 Power-on Sequence

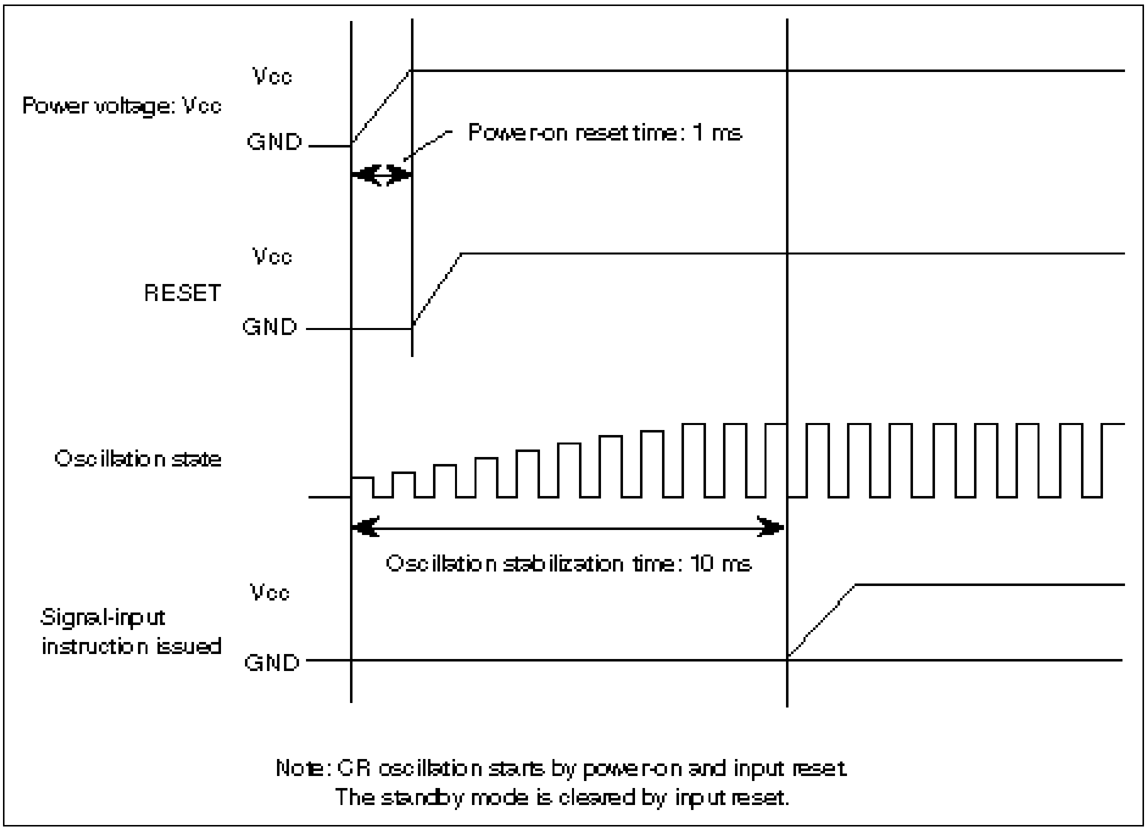


Figure 65 Power-on Timing

Power-off Sequence

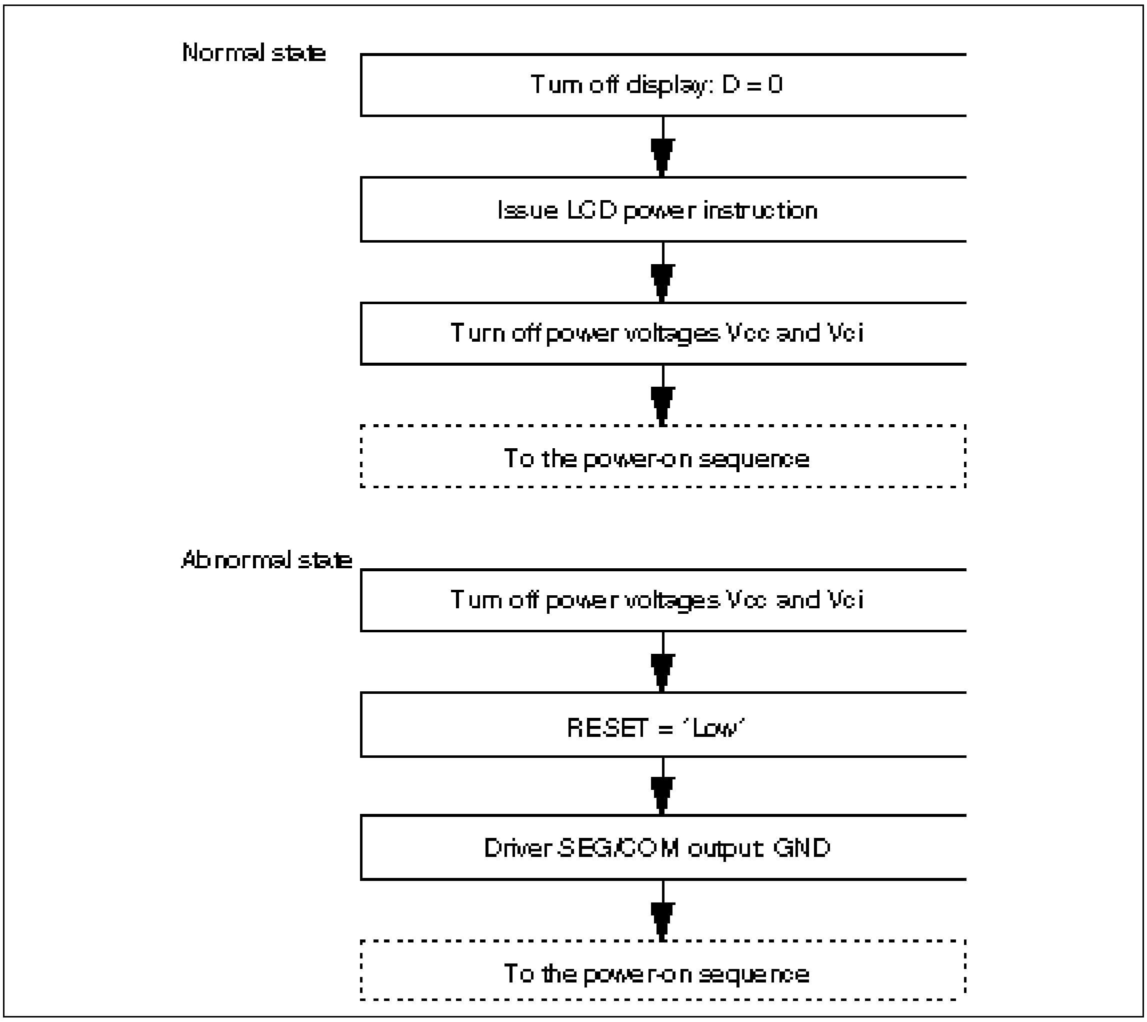


Figure 66 Power-off Sequence

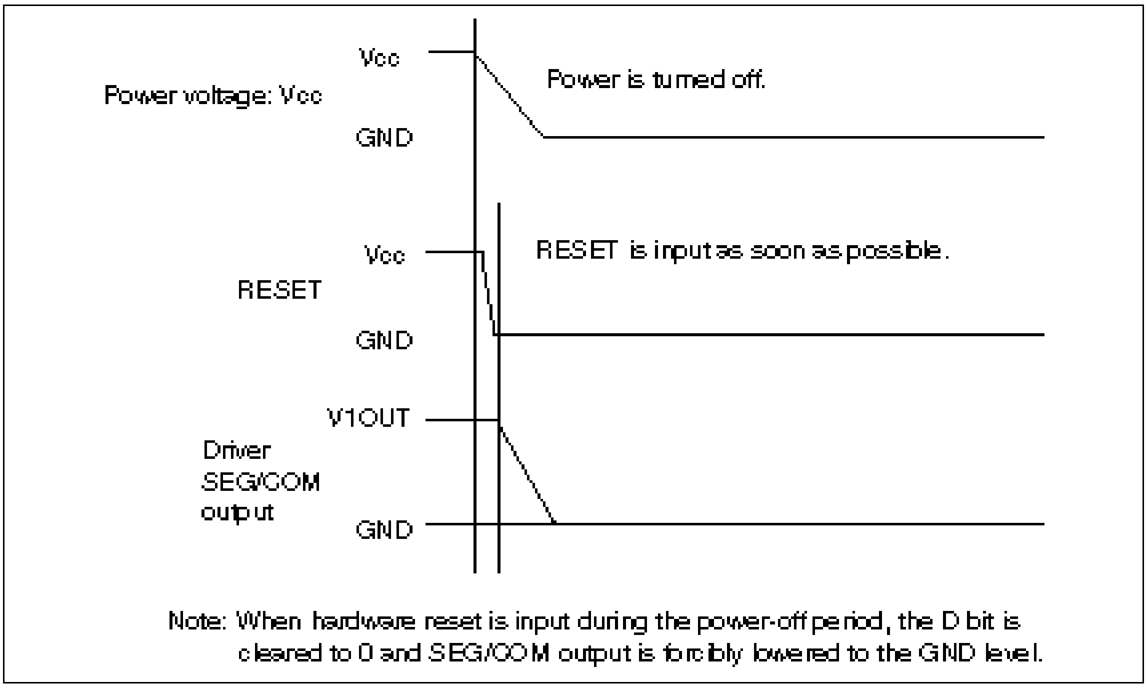


Figure 67 Power-off Timing