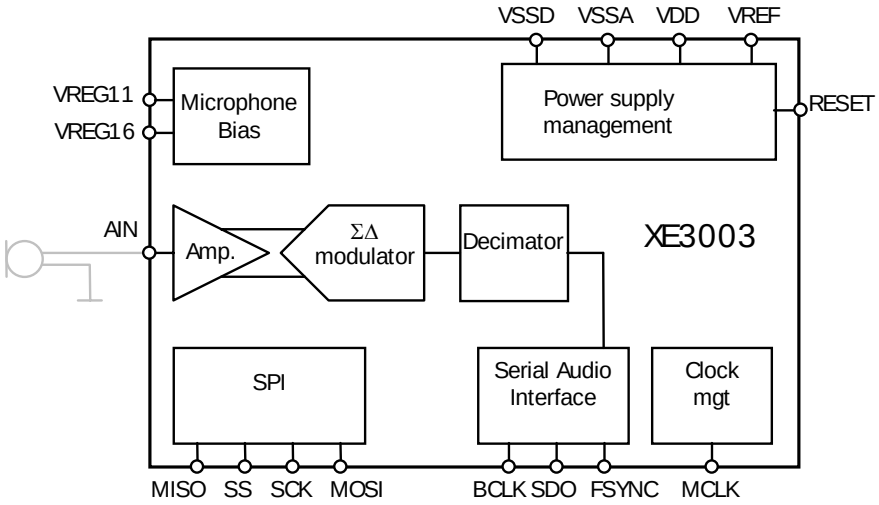



# XE3003

## Low-Power Audio ADC

### GENERAL DESCRIPTION

The XE3003 is an ultra low-power ADC (Analog to Digital Converter) for voice and audio applications.

It includes a microphone supply, programmable preamplifier, 16-bit ADC, Serial Peripheral Interface (SPI), serial audio interface (PCM) as well as the power and clock management for the ADC. The sampling frequency of the ADC can be adjusted from 4 kHz to 48 kHz.

### FEATURES

- Ultra low-power consumption, below 2 mW
- Low-voltage operation down to 1.8 V
- Single supply voltage
- Adjustable sampling frequency: 4 – 48 kHz
- Digital format: 16 bit 2s complement
- Only a minimum of external components
- Easy interfacing to various DSPs
- Direct connection to microphone
- Various programming options

### APPLICATIONS

- Wireless Microphones
- Bluetooth™ headset
- Hands-free telephony
- Digital hearing instruments
- Consumer and multimedia applications
- All battery-operated portable audio devices

### QUICK REFERENCE DATA

- Supply voltage range 1.8- 3.6 V
- Typ. current (@3V and fs = 20 kHz) 0.24 mA
- Sampling frequency range 4– 48 kHz
- Typical dynamic range ADC 78 dB
- Typ. power supply rejection 60 dB

### ORDERING INFORMATION

| Part | Package | Temperature range |
|---|---|---|
| XE3003I034 | TSSOP 16 pins | -20 to 70° C |

# Table of contents

# 1 DEVICE DESCRIPTION

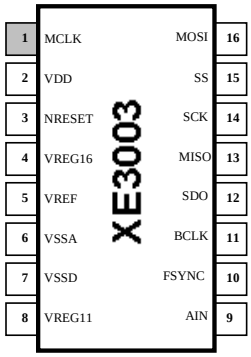



Figure 1: Pin layout of the XE3003

The XE3003 is available in a TSSOP16 package. Detailed information is found in section 7, Mechanical Information.

## 1.1 TERMINAL DESCRIPTIONS XE3003

| Terminals | | Type [1] | Description |
|---|---|---|---|
| XE3006 | Name | | |
| 1 | MCLK | DI | Master Clock. MCLK derives the internal clock of the ADC. |
| 2 | VDD | AI | Digital power supply |
| 3 | NRESET | ZI/O | Reset signal generated by the ADC. If required, the reset signal can be applied externally to initialize all the internal ADC registers. |
| 4 | VREG16 | AO | Regulator voltage 1.6 V. Can be used to supply the microphone. |
| 5 | VREF | AO | Reference voltage |
| 6 | VSSA | AI | Analog ground |
| 7 | VSSD | AI | Digital ground |
| 8 | VREG11 | AO | ADC Regulated microphone output supply voltage 1.1 V |
| 9 | AIN | AI | ADC Analog input signal |
| 10 | FSYNC | DI/O | Serial audio interface Frame Synchronization |
| 11 | BCLK | DI/O | Serial audio interface Bit Clock |
| 12 | SDO | ZO | Serial audio interface Data Output |
| 13 | MISO | ZO | SPI Master In Slave Out |
| 14 | SCK | DI PD | SPI Serial Clock |
| 15 | SS | DI PU | SPI Slave Select |
| 16 | MOSI | DI PD | SPI Master Out Slave In |

Note: (1) AI = Analog Input AO = Analog Output
DI = Digital Input DO = Digital Output
DI/O = Digital In or Out ZO = Hi Impedance or Output
PU = internal Pull Up PD = internal Pull Down
ZI/O = Hi impedance In or Out

# 2 FUNCTIONAL DESCRIPTION

The XE3003 - ADC is typically used as an audio converter for voice and audio applications between a Digital Signal Processor (DSP) and an analogue interface – the microphone.

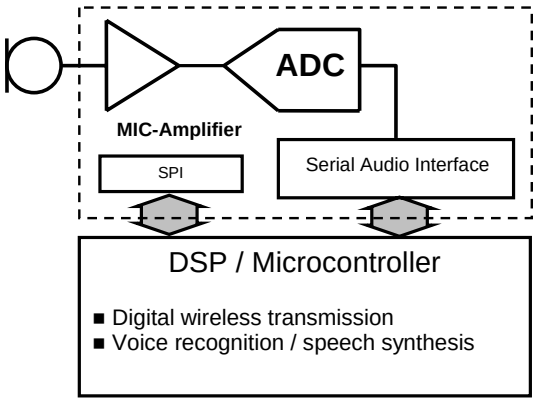



Figure 2: Typical usage of the XE3003

This chapter provides a brief description of the audio ADC features. The configuration of the ADC is defined by programming registers through a serial interface. A detailed description of the registers defining details of the ADC setup can be found in sections 3 and 6. Digital audio samples are passed through the Serial Audio Interface for further processing on the DSP.

## 2.1 DEVICE FUNCTIONS

### 2.1.1 ADC Signal Channel

The ADC channel is a chain of programmable amplifier, band-pass filter, sigma-delta modulator and a decimation filter. The amplifier gain is programmable to 5x (default) and 20x. The band-pass filter has cut-off frequencies proportional to the sampling rate. The sigma-delta modulator operates at a frequency of 64 times the sampling rate. The analog modulator is followed by a digital decimation filter. The digital output data (16 bits, 2's complement format) is made available through the Serial Audio Interface. The format of the Serial Audio interface can be selected through register J.

With the default register settings, the ADC can run at a sampling frequency up to 20 kHz. When used with a sampling frequency higher than 20 kHz, then register C has to be changed.

The whole ADC chain can be powered-down through register I.

For further details about configuring the ADC see section 6 – Register Description.

### 2.1.2 MIC Input

The programmable pre-amplifier and the microphone bias sources VREG11 or VREG16 are optimized to operate with electret microphones. VREG11 provides a 1.1 V reference voltage. The VREG11 can deliver up to 50 µA. VREG11 is enabled through control register E. VREG16 is a regulated voltage of typically 1.6 V and can deliver up to 1 mA.VREG16 is always enabled.

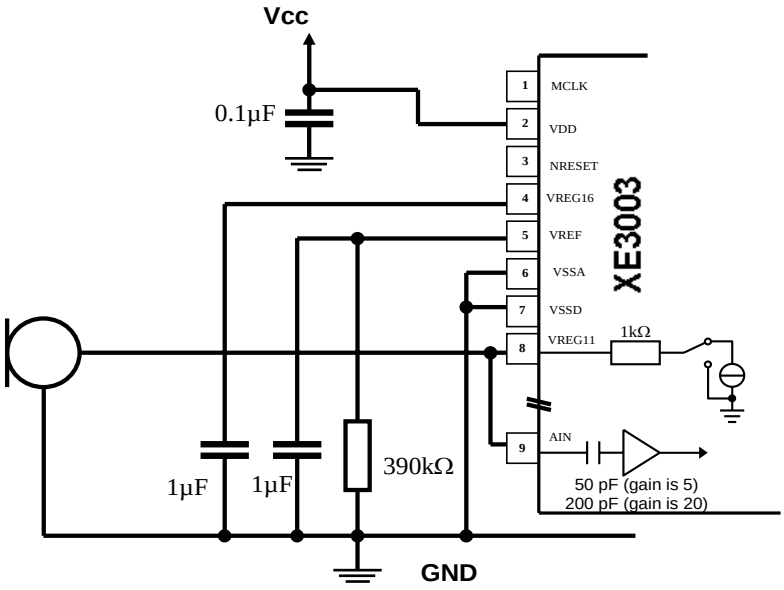



Figure 3: Typical microphone interface (1.1 V / 50µA bias through VREG11)

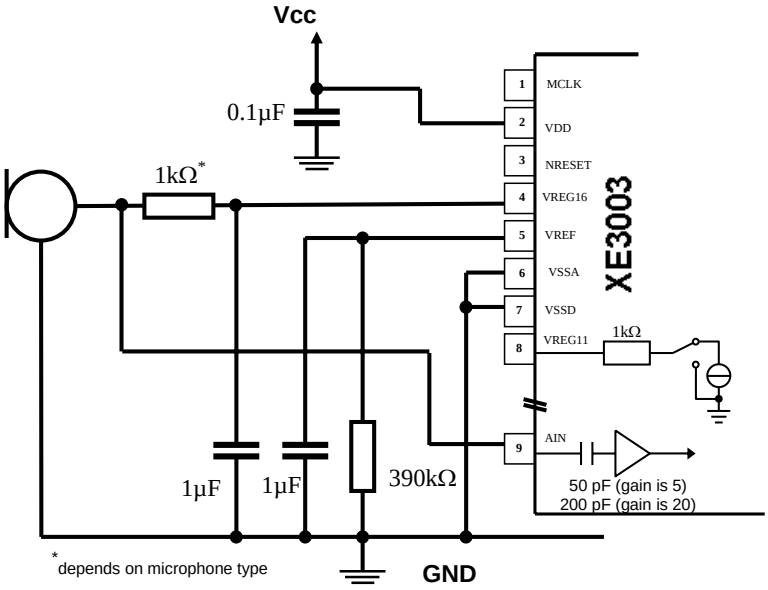



Figure 4: Typical microphone interface (1.6 V / max. 1mA bias through VREG16)

### 2.1.3 Operating Frequency

A master clock (MCLK) has to be applied to the XE3003. The clock frequency of the signal applied to the MCLK pin may vary between 1.024 MHz minimum and 33.9 MHz maximum. The maximum internal clock signal frequency (MCLK/div_factor) should not exceed 12.288 MHz.

The div_factor can be set by the user in register I to 1,2 or 4. The default value for div_factor is '1'.

### 2.1.4 Serial Audio Interface

The Serial Audio Interface is a 3-wire interface for communication of audio data. It operates on the bit serial clock BCLK and the frame synchronization signal FSYNC. The sampling frequency of the ADC corresponds to the rate at which the Audio Serial Interface will put out succeeding frames. One frame always corresponds to one sample. One frame always contains 2 channels.

Synchronizing the Serial Audio Interface to the MCLK is recommended. FSYNC and MCLK must have a fixed ratio as defined by the following relation:

FSYNC = Sampling frequency = frame rate = MCLK/(256 x div_factor).

The pin BCLK defines the time when the data must be shifted out of (pin SDO) the ADC. The number of BCLK periods in one FSYNC period is 32. The user can select to use the first 16 clock cycles (channel 1) or the second 16 clock cycles (channel 2) of BLCK to shift out the data samples.

The table below shows some examples of the relationships between MCLK, BCLK and FSYNC

| MCLK | Div_factor | BCLK | FSYNC |
|---|---|---|---|
| 2048 kHz | 1 | 256 kHz | 8 kHz |
| 8192 kHz | 4 | 256 kHz | 8 kHz |
| 5120 kHz | 1 | 640 kHz | 20 kHz |
| 22579.2 kHz | 2 | 1411.2 kHz | 44.1 kHz |

The table below shows the possible functional configurations of the serial audio interface

| ADC | supported protocol |
|---|---|
| master | LFS (Long Frame Sync) |
| slave | LFS, LFS Optimization and SFS (Short Frame Sync) |

By default the Serial Audio Interface operates in slave, SFS mode. In slave mode the user needs to generate the signals BLCK, FSYNC and supply to the ADC.

In master mode the ADC generates the BLCK and FSYNC signals. In that case the BLCK operates at 32 times the frequency of FSYNC. The ADC master mode can be used with the LFS protocol only.

The register J is used for the different setups of the serial audio interface.

### 2.1.5 Serial Peripheral Interface - SPI

The SPI interface is used to control register values. It is a serial communications interface that is independent of the rest of the ADC. It allows the device to communicate synchronously with a microprocessor or DSP. The ADC interface only implements a slave controller.
A detailed description can be found in section 3.3.

### 2.1.6 Start-up and Initialization

The ADC generates its own power on reset signal after a power supply is connected to the VDD pin. The reset signal is made available for the user at the pin NRESET. The rising edge of the NRESET indicates that the startup sequence of the ADC has finished. In most applications the NRESET pin can be left open.

The NRESET signal generated by the ADC is used to initialize the various blocks in the device and guarantees a correct start-up of the circuit. The start-up sequence that is automatically carried out upon power-up of the device is listed below and illustrated in Figure 5.

1) NRESET is low (0V) when the device is not powered and remains low for a short time when VDD (upper curve in Figure 5) is applied. The low state sustains while VDD, VREG16, VREF are stabilizing.

2) As soon as the MCLK signal is present, a counter is activated that counts $2^{21}$ periods of the MCLK. After this moment the NRESET is in the high state (VDD).

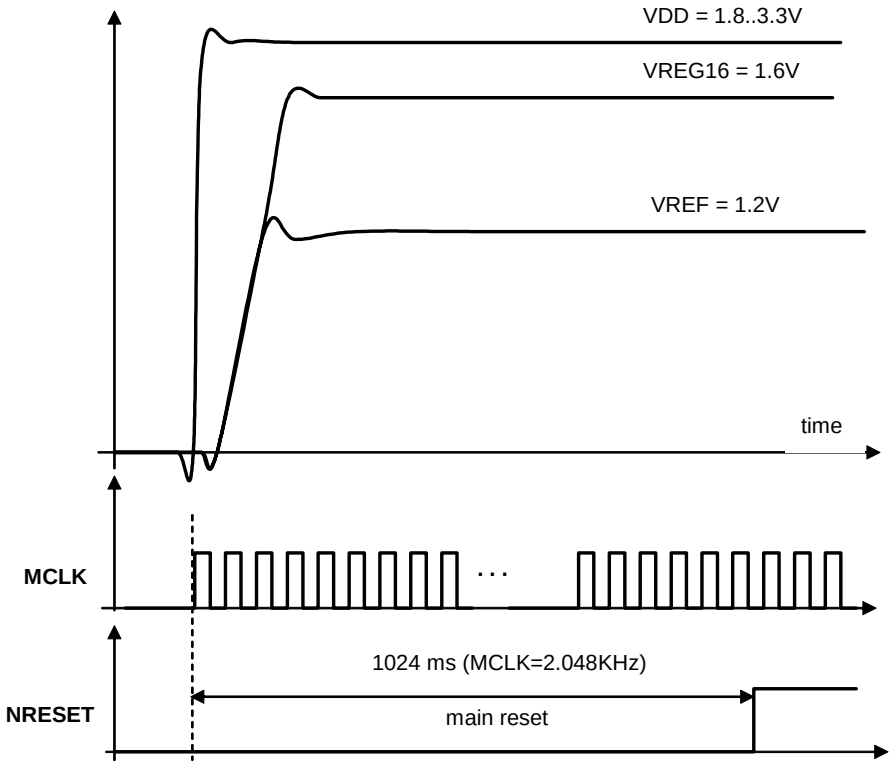



Figure 5: Startup sequence and NRESET signal after power-on.

The user can use the NRESET pin in 3 different ways and combinations:

1) Leave the NRESET pin not connected. In this case the ADC will startup as described in figure 5.
2) Use the NRESET pin as an output to indicate, to e.g. a microcontroller, that the ADC finished its power up sequence and that the ADC is ready to operate.
3) Use the NRESET pin to force a re-initialization of the registers to their default values. In this case the user has to force the NRESET to 0V for at least 32 periods of the MCLK. The circuit which forces the NRESET to 0V should be able to sink at least 50 µA.

Figure 6 shows the block diagram of the CODEC reset.

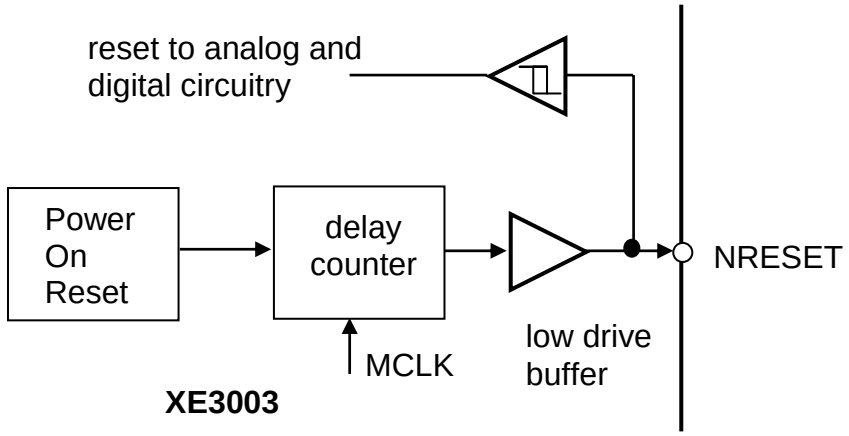



Figure 6: ADC reset circuitry

## 2.2 POWER-DOWN FUNCTIONS

### 2.2.1 Software Power-Down

Register I allows for the selective power down of the ADC signal channel. The wake-up time, after powering down the device is typically 200µs. The maximum standby current is 96µA, depending highly upon the Master clock (MCLK), see 4.3.4.2 Low Power Modes.

### 2.2.2 Hardware Power-Down

The device has no power-down pin. However, by holding down (0 V) the NRESET pin (resetting the device) as well as the pins MCLK, BCLK and FSYNC, the power consumption will reach the standby current of typically 16µA. Use the standard procedure for power up (see start-up and initialization procedure) after a hardware power down the registers setup procedure must be applied.

# 3 SERIAL COMMUNICATIONS

## 3.1 SERIAL AUDIO INTERFACE

The Serial Audio Interface is a 3-wire interface for communication of the audio data. The 3 terminals are listed below:

- BCLK: Bit serial clock, one clock cycle corresponds to one data bit transmitted or received.
- FSYNC: Frame Synchronization. This signal indicates the start of a data word. The frequency of the FSYNC corresponds to the sample frequency of the ADC.
- SDO: Serial Data Out, data received from ADC and sent to external device.

The clock (BCLK) and synchronization (FSYNC) signals are used for sending the audio data. The synchronization signal FSYNC must have a fixed ratio with the master clock signal MCLK.

The Serial Audio Interface supports two formats that are commonly used for audio/voice ADCs and that are referred to as SFS (Short Frame Synchronization) and LFS (Long Frame Synchronization). Data can be transmitted in 2 channels. Which channel is selected depends on the programmed values in the registers. The two interface protocols are shown below.

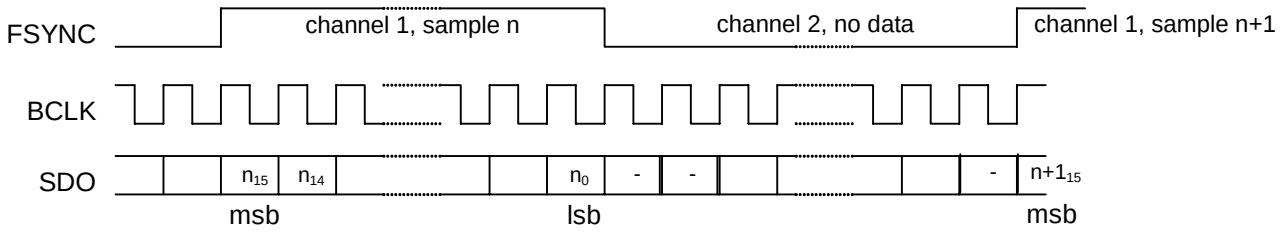



Figure 7: Audio interface timing LFS mode, channel 1

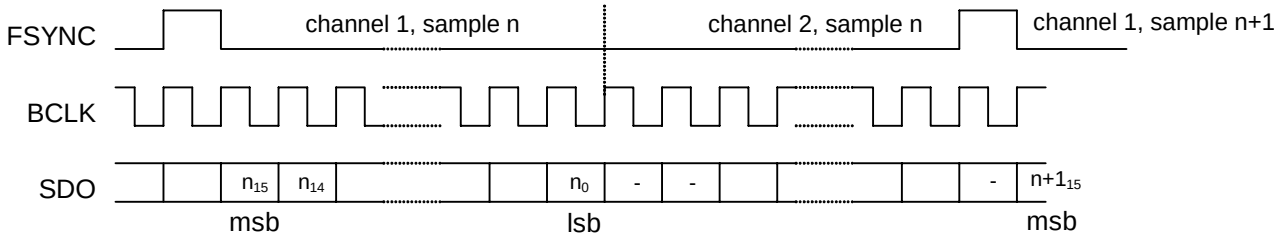



Figure 8: Audio interface timing in SFS mode, channel 1

SDO data will change on the rising edge of the BCLK. The SDO data should be read on the falling edge of the BLCK. Each rising edge of the FSYNC indicates the start of a new sample.

### 3.1.1 LFS optimization

For receiving, 32 clock cycles in one frame is always required (figure 7 and 8). This is even the case when only 16 bits have to be received. In most cases this can be easily handled with a DSP and microcontroller.

If the user wants to send a minimum of BLCK cycles, it is possible to shorten channel 1 (channel 2 can not be shortened).

In the LFS mode the possibility exists to shorten the number of BLCK cycles to 17 instead of 32. In this case the data is received in channel 2. Channel 1 is shortened to one BLCK cycle only.

**Note! This optimization is possible in slave mode only.**

The figure 9 shows this special LFS mode.

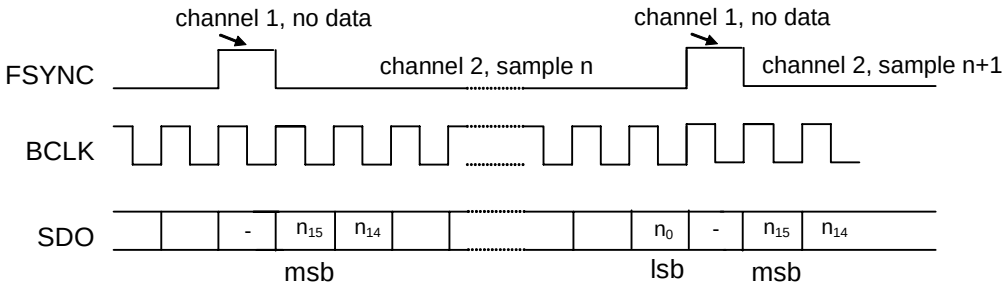



Figure 9: Audio interface timing in LFS mode, 17 BLCK cycles, channel 2

### 3.2 REGISTER PROGRAMMING

The control registers define the configuration of the ADC and define the various modes of operation. During power-up, all registers will be configured with default values. The control register set consists of 9 registers. A detailed description is provided in section 6.

The control registers can be changed in the two following ways:

1. Logic values at SPI pins during power-up

There are 3 bits inside the registers which are configured depending on the logic values of the pins SS, SCK and MOSI during the power up startup sequence as described in section 2.1.6.

| Value at power up | Influenced bits of registers | comments |
|---|---|---|
| SS = 1<br>SS = 0 | Register I(0)=0<br>Register I(0)=1 | MCLKDIV division by 1<br>MCLKDIV division by 2 |
| SCK = 0<br>SCK = 1 | Register J(0)=1<br>Register J(0)=0 | SFS protocol<br>LFS protocol |
| MOSI = 0<br>MOSI = 1 | Register E(2) = 0<br>Register E(2) = 1 | preamplifier gain x5<br>preamplifier gain x20 |

Using the SPI pins at startup, the user is able to configure the ADC in the corresponding setups without reprogramming through the SPI interface and protocol. In best case the SPI interface can then be completely omitted and the 3 SPI pins can be fixed to ‘0’ or ‘1’.

2. Programming through SPI interface after power-up

Once the device has been powered up, the configuration registers can be modified at all times (also when the device is active) through the SPI interface.

The following section describes the SPI protocol which is required to change the control registers from their default values.

### 3.3 SERIAL PERIPHERAL INTERFACE - SPI

The Serial Peripheral Interface (SPI) allows the device to communicate synchronously with other devices such as a microprocessor or a DSP. The ADC interface only implements a slave controller. This section describes the communication from master (e.g. DSP) to slave (ADC pin MOSI) and from slave (ADC pin MISO) to a master (e.g. DSP).

Four lines are used to transmit data between the slave and master:

- MOSI (Master Out, Slave In) data from master to slave, synchronous with the SPI clock (SCK).
- MISO (Master In, Slave Out) data from slave to master, synchronous with the SPI clock (SCK).
- SCK (Serial Clock) synchronizes the data bits of MOSI and MISO.
- SS (Slave Select) Slave devices are selected by activating SS.

#### 3.3.1 Protocol

During SPI communication, data is simultaneously transmitted and received.

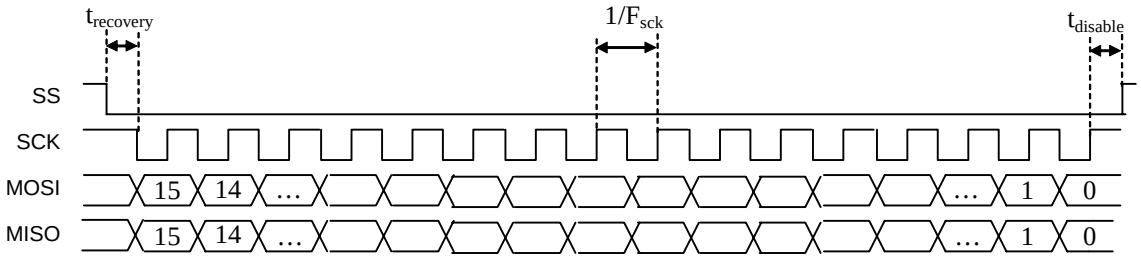



Figure 10: SPI signal timing

The master puts data on the MOSI line on the falling edge of SCK; the slave reads the data on the rising edge of SCK. The slave puts data on the MISO line on the falling edge of SCK; the master reads the data on the rising edge of SCK. Transmission in either direction is by 2 bytes with MSB first.

The SS pin should be kept low during the whole transfer of data.

There are three timing constraints:

- Recovery time ($t_{recovery}$) between the falling edge of SS and the falling edge of SCK.
- Disable time ($t_{disable}$) between the last rising edge of SCK and the rising edge of SS.
- SCK frequency ($F_{SCK}$)

| Delay | Min | Max | Unit | Comments |
|---|---|---|---|---|
| $t_{recover}$ | 125 | - | ns | |
| $t_{disable}$ | 2 x $T_{master}$ | - | ns | $T_{master}$ = clock period of the master clock MCLK |
| $F_{SCK}$ | | 0.5 x $F_{master}$ | Hz | $F_{master}$ = frequency of the master clock MCLK |

### 3.3.2 SPI Interface Modes

There are two SPI modes: read and write.

#### *3.3.2.1 Read Mode*

Read communication always takes place in pairs of bytes. A read request of 2 bytes is sent on the MOSI line. The content of the addressed register, one byte, is dumped on the MISO line during the transmission of the second byte on the MOSI. The formats of one byte are the following:

| bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| mosi | 1 | 1 | 0 | msb | | A (4:0) | | lsb |

| bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| miso | msb | | | D(7:0) | | | | lsb |

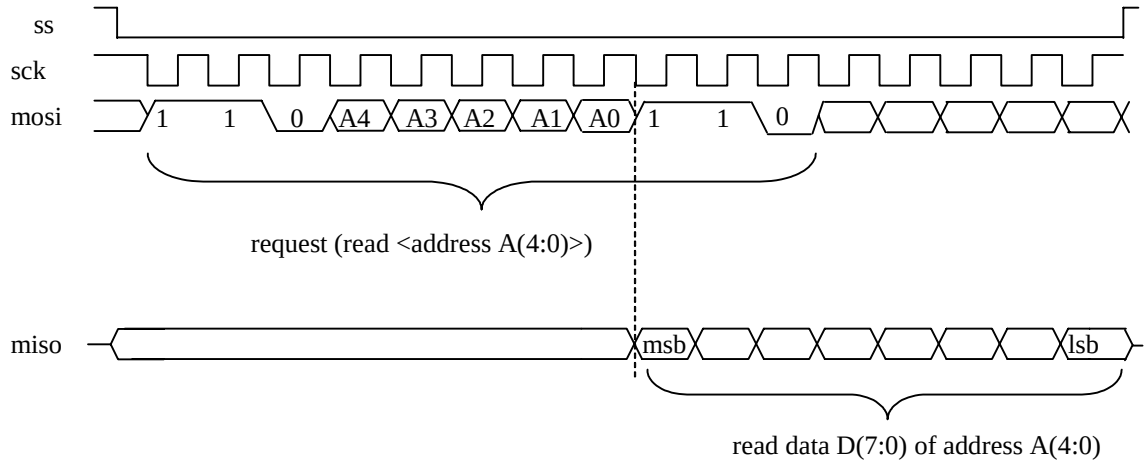



Figure 11: SPI signal timing in read mode

#### *3.3.2.2 Write Mode*

Write communication always takes place in pairs of bytes. The format of the 2 bytes is:

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| mosi | 1 | 0 | 0 | msb | | A(4:0) | | lsb |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| mosi | msb | | | D(7:0) | | | | lsb |

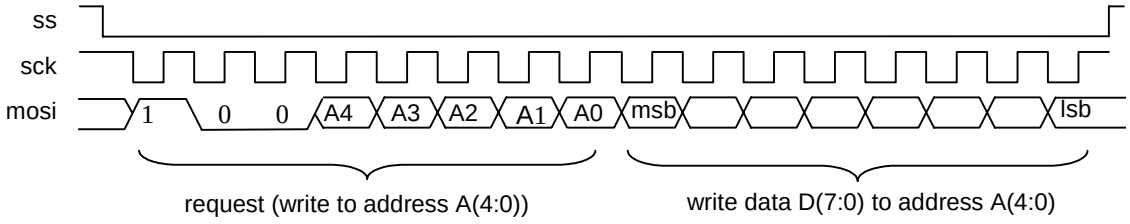



Figure 12: SPI signal timing in write mode

# 4 SPECIFICATIONS

## 4.1 ABSOLUTE MAXIMUM RATINGS

Stresses above those listed in the following table may cause permanent failure. Exposure to absolute ratings for extended periods may affect device reliability.

The values are in accordance with the Absolute Maximum Rating System (IEC 134).
All voltages are referenced to ground (VSSA and VSSD).
Analog and digital grounds are equal (VSSA = VSSD).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| VDD | Supply voltage | | -0.3 | 3.65 | V |
| Tstg | Storage temperature | | -65 | 150 | °C |
| TA | Operating free-air temperature, TA | | -20 | 70 | °C |
| Ves | Electrostatic discharge protection | 1) | | 500 | V |
| Ilus | Static latchup current | 2) | 10 | 98 | mA |
| Vlud | Dynamic latchup voltage | 2) | | 50 | V |

1) Tested according MIL883C Method 3015.6, class JEDEC 1B (Standardized Human Body Model: 100 pF, 1500 Ω, 3 pulses, protection related to substrate).
2) Static and dynamic latchup values are valid at 27 °C.

## 4.2 RECOMMENDED OPERATING CONDITIONS

All voltages referenced to ground (VSSA and VSSD).

| | Min | Typ | Max | Unit |
|---|---|---|---|---|
| Supply voltage, VDD | 1.8 | 3.0 | 3.6 | V |
| Analog signal peak input voltage, AIN (gain = 20x) | | | 65 | mV |
| Analog signal peak input voltage, AIN (gain = 5x) | | | 270 | mV |
| Differential output load resistance | 16 | 32 | | Ohm |
| Master clock frequency | 1.024 | | 33 | MHz |
| ADC conversion rate | | 20 | 48 | kHz |
| Operating free-air temperature, TA | -20 | | 70 | °C |

### 4.3 ELECTRICAL CHARACTERISTICS

The operating conditions in this section are: VDD = 3.0 V, T = 25°C.

#### 4.3.1 Digital Inputs and Outputs, FSYNC = 20 kHz, output not loaded

| | Parameter | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| VOH | High-level output voltage, DOUT | IO = -360uA | 2.4 | | VDD+0.5 | V |
| VOL | Low-level output voltage, DOUT | IO = 2mA | VSSD-0.5 | | 0.4 | V |
| IIH | High-level input current, any digital input | VIH = 3.3 V | | | 10 | uA |
| IIL | Low-level input current, any digital input | VIL = 0.6 V | | | 10 | uA |
| Ci | Input capacitance | | | | 10 | pF |
| Co | Output capacitance | | | | 10 | pF |

#### 4.3.2 ADC Dynamic Performance, FSYNC = 20 kHz

| | Parameter | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| SNR | Signal-to-noise ratio | Pre-amp gain = 5x<br>Vin=250mV (full scale) | 72 | 78 | | dB |
| THD | Total harmonic distortion | ¼ full scale | | 0.5 | | % |
| Flo | Low cut-off frequency (-3 dB), See Note 1 | FSYNC = 20 kHz | 60 | 70 | 80 | Hz |
| Fhi | High cut-off frequency (-3 dB), See Note 2 | FSYNC = 20 kHz | | 10 | | kHz |
| GD | Group delay | FSYNC = 20 kHz | | | 150 | us |

Note 1) Flo is proportional to FSYNC
Note 2) Fhi equals FSYNC/2

#### 4.3.3 ADC Channel Characteristics, FSYNC = 20 kHz

| | Parameter | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Vip | Peak input voltage (single ended) | Pre-amp gain = 5x | | | 270 | mV |
| | | Pre-amp gain = 20x | | | 65 | |
| Vneq | Equivalent input noise | A-weighted, 100 Hz-10 kHz<br>pre-amp gain = 5x | | | 20 | µV rms |
| | | A-weighted, 100 Hz-10 kHz<br>pre-amp gain = 20x | | | 5 | |
| | Dynamic range | Pre-amp gain = 5x<br>Vin=250mV (full scale) | 72 | 78 | | dB |
| PSRR | Power supply rejection ratio, input referred | Up to 1 kHz | | 60 | | dB |
| Cin | Input capacitor | Preamp-gain = 5x | | 50 | | pF |
| | | Preamp gain = 20x | | 200 | | |
| Rin | Input resistance VIN – VSSA | | 1 | | | MOhm |
| Eg | gain error | VDD 1.8-3.3V | | +/- 0.1 | | [%] |
| | offset error | VDD 1.8-3.3V | | -60 | | LSB |
| | input noise | VDD 1.8-3.3V | | 6.7 | | LSB |
| INL | Integral non linearity | VDD 1.8-3.3V | | +/- 5 | | LSB |
| DNL | Differential non linearity | VDD 1.8-3.3V | | +/- 0.1 | | LSB |

### 4.3.4 Power Supply

#### *4.3.4.1 Regulated supply characteristics @ T = 25°C*

| | Parameter | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| VREF | reference Voltage | 1µF capacitor 390kΩ resistor | | 1.2 | | V |
| VREG11 | regulated Voltage 1.1V | | | 1.1 | | V |
| I_vreg11 | available current | | | 35 | 50 | µA |
| R_vreg11 | output impedance | | | 1 | 1.5 | kOhm |
| VREG16 | regulated Voltage 1.6V | 1µF capacitor | 1.5 | 1.6 | | V |
| I_vreg16 | available output current | | | | 1 | mA |
| VREF PSRR | power supply rejection ratio, input referred | up to 1 kHz | | 60 | | dB |
| VREG11 PSRR | power supply rejection ratio, input referred | up to 1 kHz | | 60 | | dB |
| VREG16 PSRR | power supply rejection ratio, input referred | up to 1 kHz | | 40 | | dB |

#### *4.3.4.2 Low power mode*

Stand-by mode @ VDD = 3.0V, T = 25°C

| | Parameter | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Istb1 | Supply current in standby mode | ADC off, MCLK = 5 MHz, | | 28 | 56 | µA |
| Istb2 | Supply current in standby mode | ADC off, MCLK = 12.2880 MHz | | 48 | 96 | µA |
| Istb3 | Supply current in standby mode | NRESET mode MCLK = 0 | | 20 | 40 | µA |

Stand-by mode @ VDD = 1.8V, T = 25°C

| | Parameter | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Istb1 | Supply current in standby mode | ADC off, MCLK = 5 MHz, | | 25 | 50 | µA |
| Istb2 | Supply current in standby mode | ADC off, MCLK = 12.2880 MHz | | 31 | 62 | µA |
| Istb3 | Supply current in standby mode | NRESET mode MCLK = 0 | | 16 | 32 | µA |

#### *4.3.4.3 Normal operation*

Normal operations @ VDD = 3.0V, FSYNC = 20 kHz, T = 25°C, Register C(7:0) = 0xF0

| | Parameter | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| IADC | Supply current ADC | ADC on<br>FSYNC = 20 kHz | | 240 | 480 | µA |

Normal operations @ VDD = 3.0V, FSYNC = 48 kHz, T = 25°C, Register C(7:0) = 0xC4

| | Parameter | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| IADC | Supply current ADC | ADC on<br>FSYNC = 48 kHz | | 600 | 1200 | µA |

Normal operations @ VDD = 1.8V, FSYNC = 20 kHz, T = 25°C, Register C(7:0) = 0xF0

| | Parameter | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| IADC | Supply current ADC | ADC on<br>FSYNC = 20 kHz | | 200 | 400 | µA |

Normal operations @ VDD = 1.8V, FSYNC = 48 kHz, T = 25°C, Register C(7:0) = 0xC4

| | Parameter | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| IADC | Supply current ADC | ADC on<br>FSYNC = 48 kHz | | 505 | 1010 | µA |

### 4.3.5 Timing Requirements of serial audio interface

| Ref. No. * | Characteristics | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| 1 | Master Clock Frequency for MCLK = 1/ T | | 1024 | 5.12 | 33 | MHz |
| 1 | MCLK Duty Cycle | | 45 | | 55 | % |
| 2 | Rise Time for All Digital Signals | | | | 10 | ns |
| 3 | Fall Time for All Digital Signals | | | | 10 | ns |
| 4 | Hold time BCLK or FSYNC high after MCLK low | | T/4 | | | ns |
| 5 | Setup time BCLK or FSYNC high to MCLK low | | T/4 | | | ns |
| 6 | Hold time BCLK or FSYNC low after MCLK low | $C_{Load}$ = 10pF | T/4 | | | ns |
| 7 | Setup time BCLK or FSYNC low to MCLK low | | T/4 | | | ns |
| 8 | Bit Clock Frequency for BCLK = 1 / $T_{BCLK}$ | | | 32xFSYNC | MCLK/2 | MHz |
| 9 | Setup time data input SDI to BCLK low | | not applicable | | | ns |
| 10 | Hold time data input SDI after BCLK low | | not applicable | | | ns |
| 11 | Delay time SDO valid after BCLK high | | | | $T_{BCLK}$/4 | ns |
| 12 | Setup time data input FSYNC to BCLK low | | $T_{BCLK}$/4 | | | ns |
| 13 | Hold time data input FSYNC after BCLK low | | $T_{BCLK}$/4 | | | ns |

*****see figure 13,14 for LFS and 15, 16 for SFS mode

#### *4.3.5.1 Timing diagram of the serial audio interface – LFS mode*

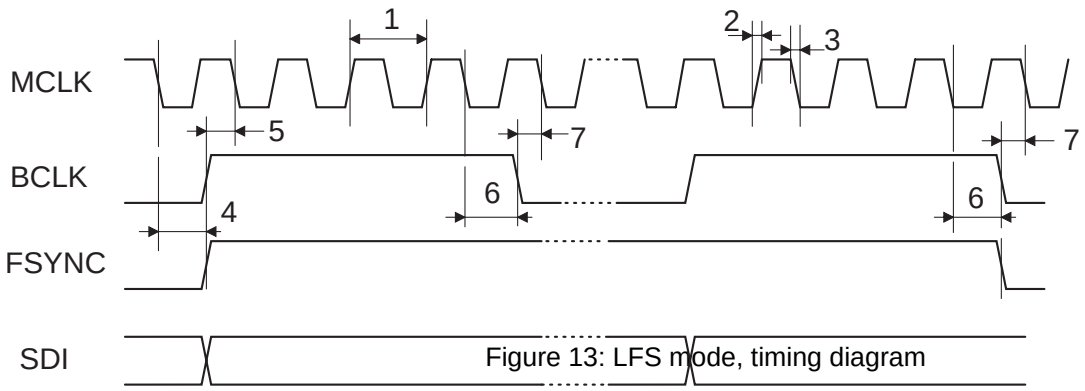



Figure 13: LFS mode, timing diagram

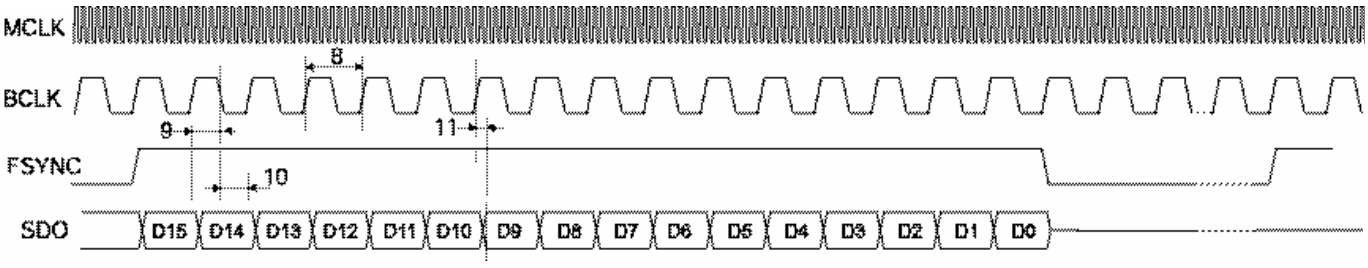



Figure 14: LFS mode, zoom timing diagram

#### *4.3.5.2 Timing diagram of the serial audio interface – SFS mode*

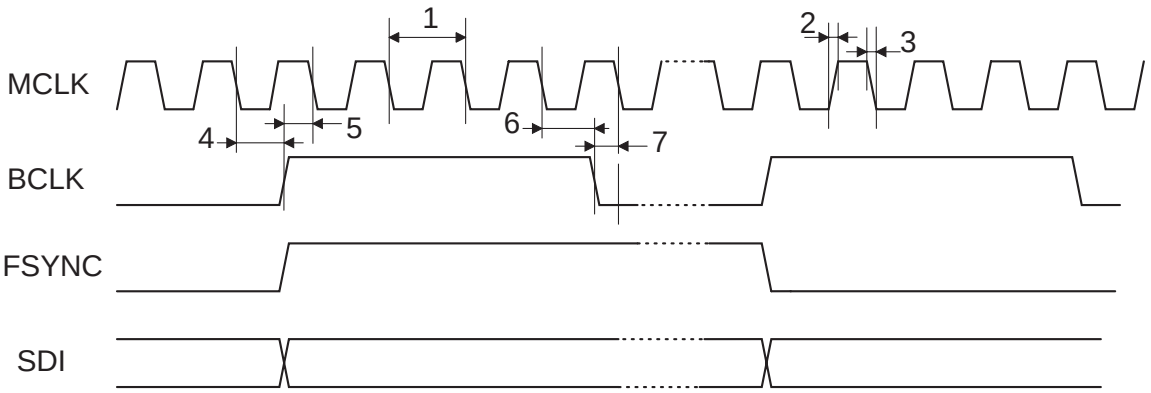



Figure 15: SFS mode, timing diagram

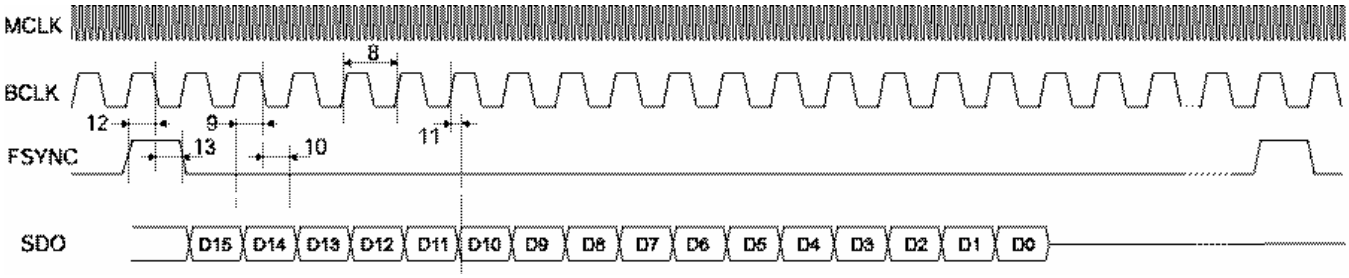



Figure 16: SFS mode, zoom timing diagram

### 4.3.6 Timing Requirements of the Serial Peripheral Interface

| Ref. No. * | Characteristics | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| 1 | Serial Clock Frequency for SCK = 1 / TSCK | | | | MCLK/2 | MHz |
| 1 | MCLK Duty Cycle | | 45 | | 55 | % |
| 2 | Recovery Time | | 125 | | | ns |
| 3 | Disable Time | $C_{Load}$ = 10pF | 2T | | | ns |
| 4 | Setup time MISO valid to SCK high | | TSCK/4 | | | ns |
| 5 | Hold time MISO valid after SCK high | | TSCK/4 | | | ns |
| 6 | Delay time MOSI valid after SCK low | | TSCK/4 | | | ns |

* see figure 17

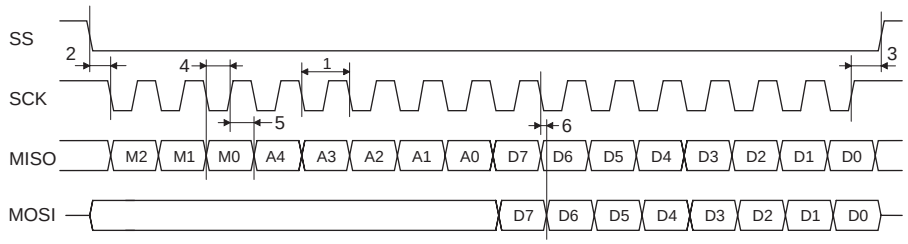



Figure 17: Serial Peripheral Interface timing

# 5 APPLICATION INFORMATION

## 5.1 APPLICATION SCHEMATICS – XE3003

### 5.1.1 Typical Application schematic - microphone bias through VREG11 (1.1 V / 50 µA)

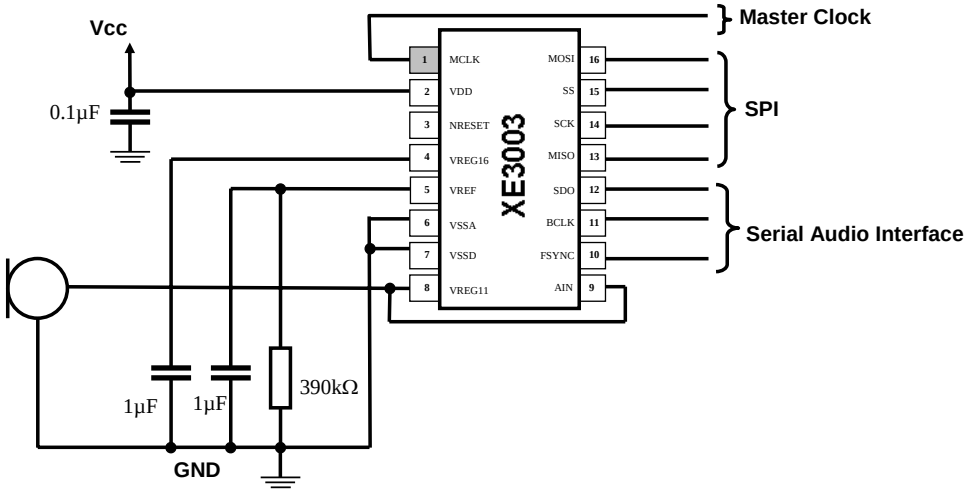
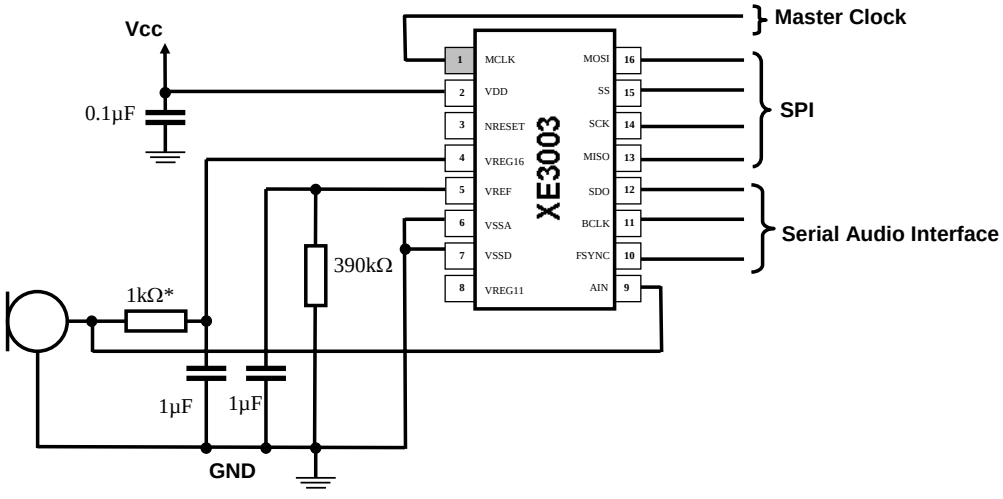



Figure 18: Typical Application with microphone bias through VREG11 (1.1V / 50µA)

### 5.1.2 Typical Application schematic - microphone bias through VREG16 (1.6 V)




* depends on microphone type

Figure 19: Typical Application with microphone bias through VREG16 (1.6V / max. 1mA)

# 6 REGISTER DESCRIPTION

## 6.1 REGISTER FUNCTIONAL SUMMARY

The following registers can be programmed by the SPI to configure the operation modes. See also section 3.2 Register Programming.

| Name | Description |
|---|---|
| Register C | ADC current setting. The data in this register has the following functions: |
| | • Adjust the ADC current for FSYNC > 20kHz |
| | • 0xF0 for FSYNC<= 20 kHz, 0xC4 for FSYNC > 20 kHz. |
| Register E | Analog Input. The data in this register has the following functions: |
| | • Enable/disable microphone bias source of 1.1 V |
| | • Gain setting of pre-amplifier. |
| Register I | Function enable and clock division. The data in this register has the following functions: |
| | • Enable/disable ADC channel (pre-amplifier, ADC, decimation filter) |
| | • Division of master clock |
| Register J | Audio Interface Configuration. The data in this register has the following functions: |
| | • Channel select receive |
| | • Select master / slave mode |
| | • Output impedance |
| | • Channel select transmit |
| | • Select short / long frame sync |

### 6.2 REGISTER DEFINITIONS

The complete register setup consists of 11 registers of 8 bits each, as shown in the table below. All registers are preconfigured with the default values and do not have to be programmed by the user if no changes in the setup are required.
The registers C, E, I and J can be used to configure the XE3003 differently than the default setup.

| Register | Address (hex) | Name | Default value (hex) |
|---|---|---|---|
| A | 0x00 | Reserved | 0x48 |
| B | 0x01 | Reserved | 0x8F |
| C | 0x02 | ADC current | 0xF0 |
| D | 0x03 | Reserved | 0x00 |
| E | 0x04 | Analog input | 0x08/0x0C |
| F | 0x05 | Reserved | 0x82 |
| G | 0x06 | Reserved | 0x00 |
| H | 0x07 | Reserved | 0x00 |
| I | 0x08 | Block on/off and clock division | 0x00/0x01 |
| J | 0x09 | Audio interface configuration | 0x25/0x24 |
| K | 0x0A | Reserved | 0x00 |

| Register C (7:0) address 0x02 | ADC current | Default value: 0xF0 | Description |
|---|---|---|---|
| 7:0 | ADC current | 0xF0 | 0xF0 for FSYNC<= 20 kHz,<br>0xC4 for FSYNC > 20 kHz. |

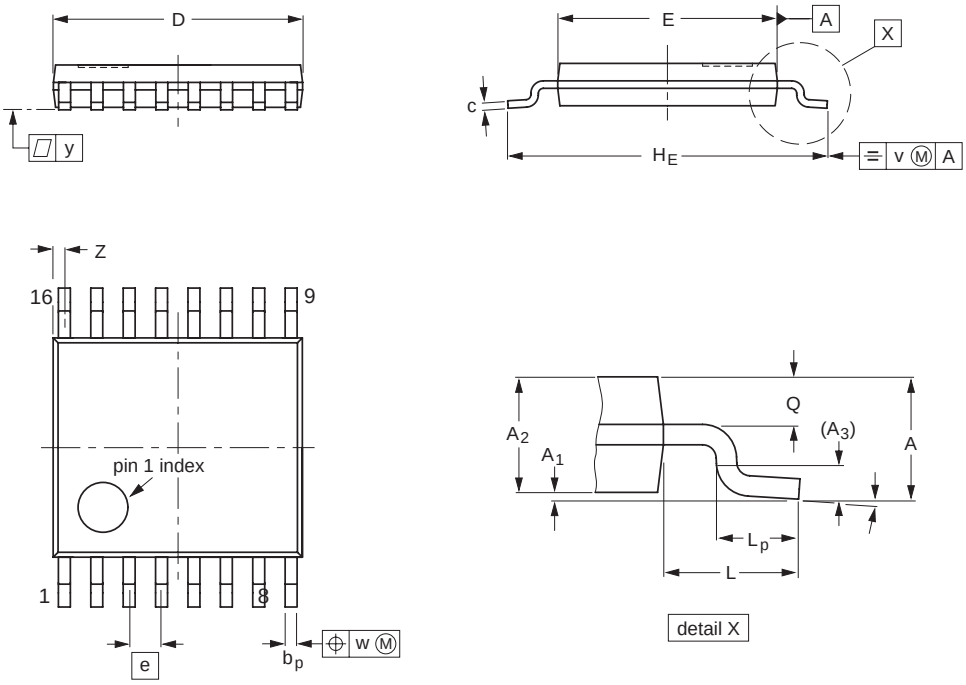
| Register E (7:0) address 0x04 | ADC input | Default value 0x08/0x0C | Description |
|---|---|---|---|
| 7 | VMIC_EN | 0 | Generation of the microphone supply at pin VREG11:<br>1: enables VREG11<br>0: disables VREG11 |
| 6:3 | reserved | 0001 | reserved |
| 2 | PREAMP_ GAIN | 0 or 1 | Gain of preamplifier:<br>0: 5x (280 mV peak)<br>1: 20x (70 mV peak)<br><br>The default is depending on the logic value of the pin MOSI during startup (see section 3.2)<br>MOSI=0, default will be set to 0<br>MOSI=1, default will be set to 1 |
| 1:0 | reserved | 00 | reserved |

| Register I (7:0) address 0x08 | block on/off and clock division | Default value 0x00/0x01 | Description |
|---|---|---|---|
| 7:4 | | 0000 | reserved |
| 3 | reserved | 0 | reserved |
| 2 | EN_ADC | 0 | 0: enable<br>1: disable AD converter (Preamp + ADC + decimator) |
| 1:0 | MCLKDIV | 00 or 01 | Division factor of the master clock:<br>00: 1<br>01: 2<br>10: reserved<br>11: 4<br><br>The default is depending on the logic value of the pin SS during startup (see section 3.2 Register Programming)<br>SS=0, default will be set to 1<br>SS=1, default will be set to 0 |

| Register J (7:0) address 0x09 | Audio interface configuration | Default value 0x25/ 0x24 | Description |
|---|---|---|---|
| 7 | reserved | 0 | reserved |
| 6 | RX_FIRST_ SECOND | 0 | 0: Receive audio data in the first 16-bit channel after the frame synchronization.<br>1: Receive audio data in the second 16-bit channel after the frame synchronization. |
| 5 | reserved | 1 | reserved |
| 4 | MASTER | 0 | 1: enable audio interface in master mode (only for LFS)<br>0: enable audio interface in slave mode (LFS, LFS Optimization or SFS) |
| 3 | SDO_HI_EN | 0 | 0: SDO is continuously in output mode for both data channels.<br>1: SDO is in output mode when transmitting a channel with data (J(2) or J(1)=1).<br>It is switched automatically into high-impedance state when a channel with no data is transmitted (J(2) or J(1)=0). |
| 2 | TX_FIRST | 1 | 1: transmit the audio data in the first 16-bit channel after the frame synchronization.<br>0: do no transmit data in the first channel. |
| 1 | TX_SECOND | 0 | 1: transmit the audio data in the second 16-bit channel after the frame synchronization.<br>0: do no transmit data in the second channel. |
| 0 | PROTOCOL | 0 or 1 | 1: Short Frame Synchronization mode (slave mode).<br>0: Long Frame Synchronization mode (master or slave mode).<br><br>The default is depending on the logic value of the pin SCK during startup (see section 3.2 Register Programming)<br>SCK=0, default will be set to 1<br>SCK=1, default will be set to 0 |

# 7 MECHANICAL INFORMATION

## 7.1 XE3003 PACKAGE SIZE (TSSOP16)




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | D (1) | E (2) | e | $H_E$ | L | $L_p$ | Q | v | w | y | Z (1) | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.10 | 0.15<br>0.05 | 0.95<br>0.80 | 0.25 | 0.30<br>0.19 | 0.2<br>0.1 | 5.1<br>4.9 | 4.5<br>4.3 | 0.65 | 6.6<br>6.2 | 1.0 | 0.75<br>0.50 | 0.4<br>0.3 | 0.2 | 0.13 | 0.1 | 0.40<br>0.06 | $8^o$<br>$0^o$ |

Figure 20: TSSOP16 Plastic Thin Shrink Small Outline Package; 16 leads; body width 4.4 mm

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