D2833, MARCH 1984—REVISED SEPTEMBER 1987

- **'HC677 is a 16-Bit Address Comparator with Enable**
- **'HC678 is a 16-Bit Address Comparator with Latch**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

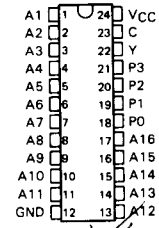
description

The 'HC677 and 'HC678 address comparators simplify addressing of memory boards and/or other peripheral devices. The four P inputs are normally hard wired with a preprogrammed address. An internal decoder determines what input information applied to the 16 A inputs must be low or high to cause a low state at the output (Y). For example, a positive-logic bit combination of 0111 (decimal 7) at the P input determines that inputs A1 through A7 must be low and that inputs A8 through A16 must be high to cause the output to go low. Equality of the address applied at the A inputs to the preprogrammed address is indicated by the output being low.

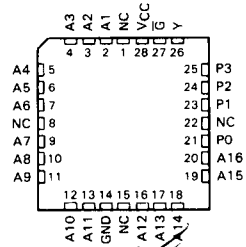
The 'HC677 features an enable input ($\overline{G}$). When $\overline{G}$ is low, the device is enabled. When $\overline{G}$ is high, the device is disabled and the output is high regardless of the A and P inputs. The 'HC678 features a transparent latch and a latch enable input (C). When C is high, the device is in the transparent mode. When C is low, the previous logic state of Y is latched.

The SN54HC677 and SN54HC678 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC677 and SN74HC678 are characterized for operation from −40°C to 85°C.

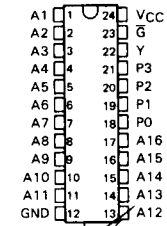
SN54HC677 . . . JT PACKAGE
SN74HC677 . . . DW OR NT PACKAGE
(TOP VIEW)



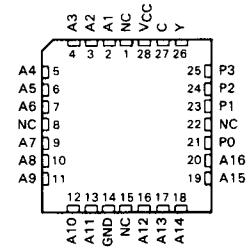
SN54HC677 . . . FK PACKAGE
(TOP VIEW)



SN54HC678 . . . JT PACKAGE
SN74HC678 . . . DW OR NT PACKAGE
(TOP VIEW)



SN54HC678 . . . FK PACKAGE
(TOP VIEW)



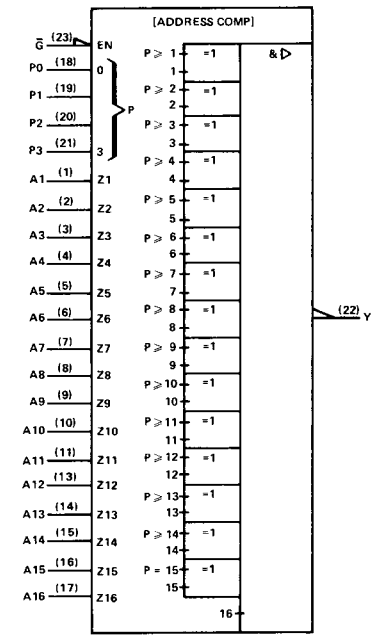
NC—No internal connection

FUNCTION TABLE

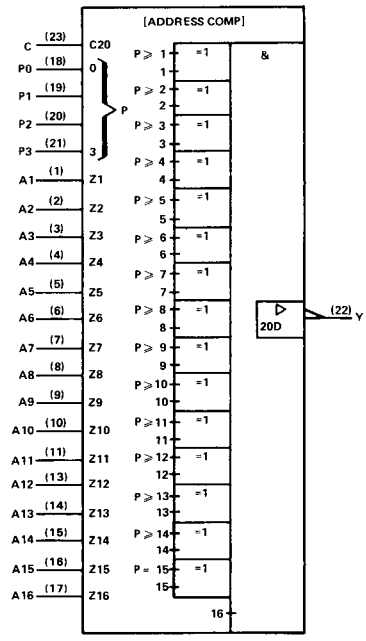
'HC677	'HC678	INPUTS COMMON TO 'HC677 AND 'HC678																				OUTPUT
$\overline{G}$	C	P3	P2	P1	P0	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12	A13	A14	A15	A16	Y
L	H	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	L	L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	L	L	H	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	L	L	H	H	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	L	H	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	L	H	L	H	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	L
L	H	L	H	H	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	L
L	H	L	H	H	H	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	L
L	H	H	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	L
L	H	H	L	L	H	L	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	L
L	H	H	L	H	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	H	H	L
L	H	H	L	H	H	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	H	L
L	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	L
L	H	H	H	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	H	H	H	L
L	H	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	H	L
L	H	H	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	L
L	H	All other combinations																				H
H		'HC677: Any combination																				H
	L	'HC678: Any combination																				Latched

logic symbols†

'HC677



'HC678



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, JT, and NT packages.

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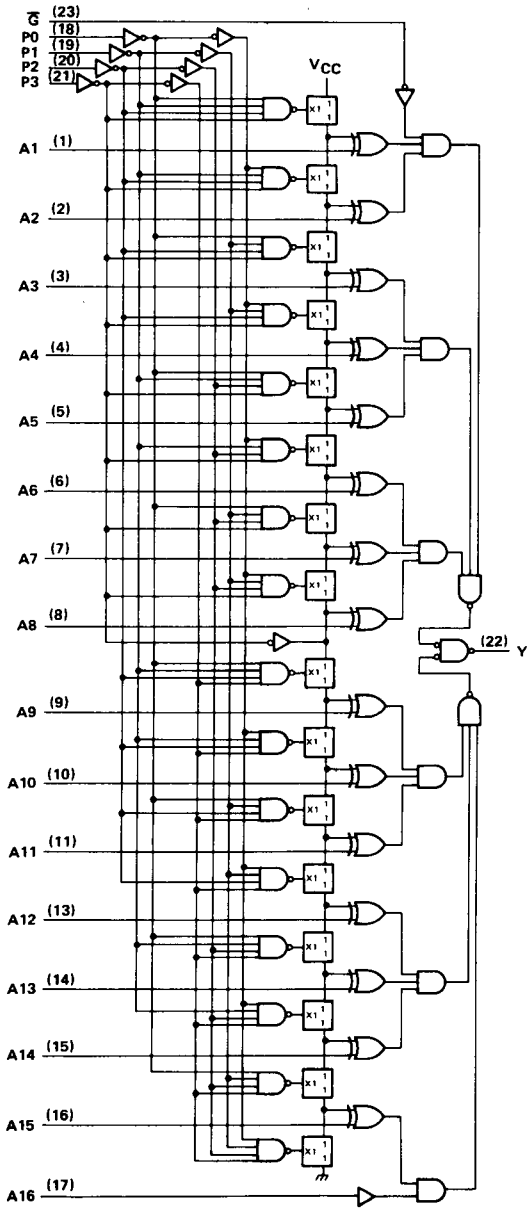
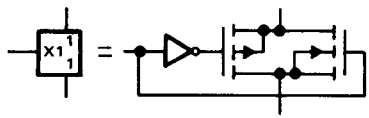
'HC677 logic diagram (positive logic)

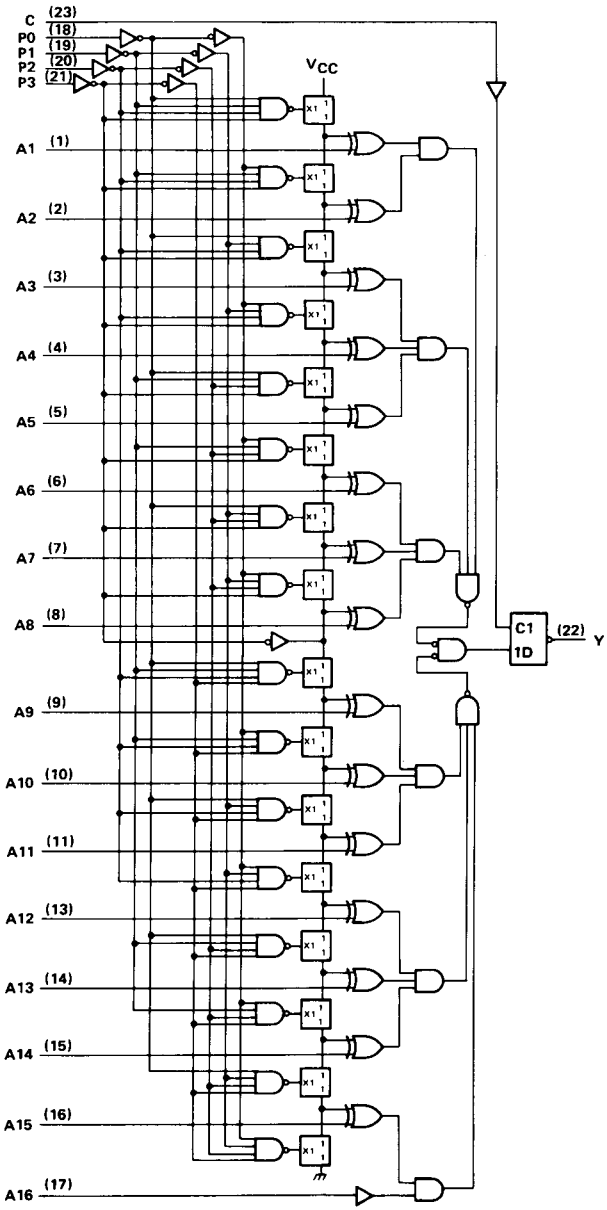


Pin numbers shown are for DW, JT, and NT packages.

In order to understand the implementation of this device, it is essential that the function of the vertical string of transmission gates be understood. A schematic of one of these gates is shown below. If the input to the transmission gate labeled "X1" is high, then the transmission path between the two ports labeled "1" is on. If the "X1" input is low, then the transmission path between the two ports labeled "1" is off. Only one of the 16 transmission gates can be off while the device is operating; which one is off is determined by inputs P0 through P3. The lines going from the string of transmission gates to the exclusive-OR gates located above the transmission gate that is off will be high. The lines going to the exclusive-OR gates located below that transmission gate will be low.



'HC678 logic diagram (positive logic)



Pin numbers shown are for DW, JT, and NT packages.

An explanation of the function of the string of transmission gates appears with the 'HC677 logic diagram on the previous page.

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absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) . . . . . ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC} . . . . . ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±25 mA
Continuous current through V_{CC} or GND pins . . . . . ±50 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or JT package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: DW or NT package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SN54HC677 SN54HC678			SN74HC677 SN74HC678			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage		2	5	6	2	5	6	V
V_{IH} High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
	V_{CC} = 4.5 V	3.15			3.15			
	V_{CC} = 6 V	4.2			4.2			
V_{IL} Low-level input voltage	V_{CC} = 2 V	0		0.3	0		0.3	V
	V_{CC} = 4.5 V	0		0.9	0		0.9	
	V_{CC} = 6 V	0		1.2	0		1.2	
V_I Input voltage		0		V_{CC}	0		V_{CC}	V
V_O Output voltage		0		V_{CC}	0		V_{CC}	V
t_t Input transition (rise and fall) times	V_{CC} = 2 V	0		1000	0		1000	ns
	V_{CC} = 4.5 V	0		500	0		500	
	V_{CC} = 6 V	0		400	0		400	
T_A Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HC677 SN54HC678		SN74HC677 SN74HC678		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}, I_{OH} = −20 μA	2 V	1.9	1.998		1.9		1.9		V
		4.5 V	4.4	4.499		4.4		4.4		
		6 V	5.9	5.999		5.9		5.9		
	V_I = V_{IH} or V_{IL}, I_{OH} = −4 mA	4.5 V	3.98	4.30		3.7		3.84		
	V_I = V_{IH} or V_{IL}, I_{OH} = −5.2 mA	6 V	5.48	5.80		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
		4.5 V		0.001	0.1		0.1		0.1	
		6 V		0.001	0.1		0.1		0.1	
	V_I = V_{IH} or V_{IL}, I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
	V_I = V_{IH} or V_{IL}, I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0	6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0, I_O = 0	6 V			8		160		80	μA
C_i		2 to 6 V		3	10		10		10	pF

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC677		SN74HC677		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Any P	Y	2 V		130	625		937		781	ns
			4.5 V		50	125		187		156	
			6 V		40	112		169		141	
t_{pd}	Any A	Y	2 V		90	150		225		187	ns
			4.5 V		18	30		45		37	
			6 V		15	27		40		34	
t_{pd}	$\overline{G}$	Y	2 V		70	125		187		156	ns
			4.5 V		14	25		37		31	
			6 V		12	22		33		27	
t_t		Y	2 V		38	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

C_{pd}	Power dissipation capacitance	No load, T_A = 25°C	40 pF typ

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

timing requirement over recommended operating free-air temperature range (unless otherwise noted)

		V_{CC}	T_A = 25°C			SN54HC678		SN74HC678		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, enable C high	2 V	75			112		94		ns
		4.5 V	15			23		19		
		6 V	13			19		16		
t_{su}	Setup time, P0 thru P3 before enable C↓	2 V	500			750		625		ns
		4.5 V	100			150		125		
		6 V	85			128		106		
t_{su}	Setup time, A1 thru A16 before enable C↓	2 V	100			150		125		ns
		4.5 V	20			30		25		
		6 V	18			27		22		
t_h	Hold time, P0 thru P3 or A1 thru A16 after enable C↓	2 V	5			5		5		ns
		4.5 V	5			5		5		
		6 V	5			5		5		

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC678		SN74HC678		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Any P	Y	2 V		130	625		937		781	ns
			4.5 V		50	125		187		156	
			6 V		40	112		169		141	
t_{pd}	Any A	Y	2 V		115	175		262		219	ns
			4.5 V		23	35		52		44	
			6 V		21	31		46		39	
t_{pd}	C	Y	2 V		95	150		225		187	ns
			4.5 V		19	30		45		37	
			6 V		17	27		40		34	
t_t		Y	2 V		38	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

C_{pd}	Power dissipation capacitance	No load, T_A = 25°C	40 pF typ

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

TYPICAL APPLICATION INFORMATION

The 'HC677 and 'HC678 can be wired to recognize any one of 2^{16} addresses. The number of "lows" in the address determines the input pattern for the P inputs. Then those system address lines that are low in the address to be recognized are connected to the lowest numbered A inputs of the address comparator and the system address lines that are high are connected to the highest numbered A inputs.

For example, assume the comparator is to enable a device when the 16-bit system address is:

A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
H	H	L	L	H	H	L	L	H	H	L	L	H	H	H	H

Since the address contains 6 lows and 10 highs, the following connections are made.

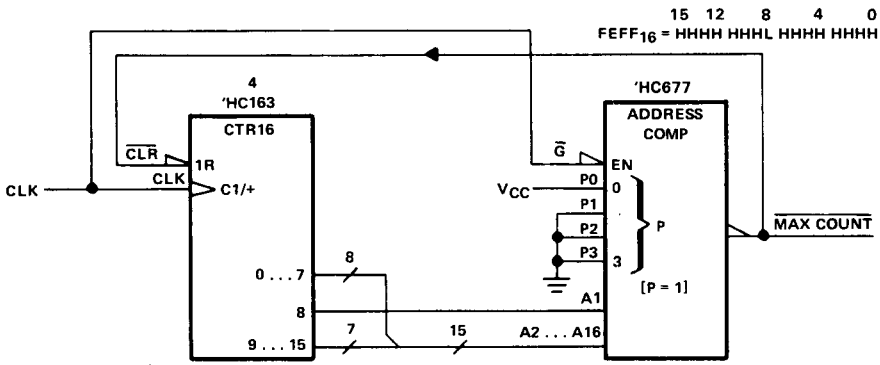
P3 to 0 V, P2 to V_{CC}, P1 to V_{CC}, and P0 to 0 V.

System address lines A13, A12, A9, A8, A5, and A4 to comparator inputs A1 through A6 in any convenient order.

The remaining eight system address lines to comparator inputs A7 through A16 in any convenient order.

The output provides an active-low enabling signal.

The following circuit is a modulo-N synchronous counter. The 'HC163 is connected to provide a low-level clear signal when N = $FEFF_{16}$.



MODULO-N SYNCHRONOUS COUNTER