MPY016K

VLSI Multiplier

16 x 16 Bit, 40ns

The TRW MPY016K is a video-speed 16 x 16 bit parallel multiplier which operates at a 40ns cycle time (25MHz multiplication rate). The multiplicand and the multiplier may be independently specified as two's complement or unsigned magnitude, yielding a full precision 32-bit product.

Individually clocked input and output registers are provided to maximize system throughput and simplify bus interfacing. These registers are positive-edge-triggered D-type flip-flops. The Most Significant Product (MSP) and Least Significant Product (LSP) can be multiplexed through a dedicated output port, or the LSP can share a bidirectional port with the Y input. All outputs are three-state.

Built with TRW's OMICRON-B™ 1-micron bipolar process, the MPY016K is pin compatible with the industry standard MPY016H and operates with three times the speed at comparable power dissipation. The MPY016K is the industry's first true video-speed 16-bit multiplier.

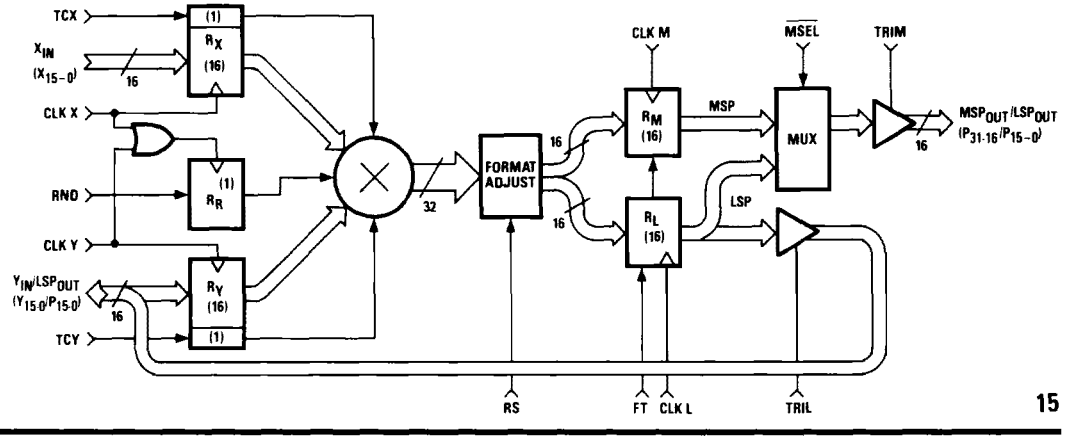
Features

- 40ns Multiply Time: MPY016K-1 (Worst Case)
- 45ns Multiply Time: MPY016K (Worst Case)
- Pin Compatible With TRW MPY016H
- 16 x 16 Bit Parallel Multiplication With 32-Bit Output
- Two Least Significant Product Output Modes: Multiplexed With Most Significant Product Or Multiplexed With Y Input
- Output Registers Can Be Made Transparent
- Three-State TTL Output
- Two's Complement, Unsigned Magnitude, Or Mixed Mode Multiplication
- Fully TTL Compatible
- Proven High-Reliability Radiation Hard Bipolar Process
- Single +5V Power Supply
- Available In A 64 Pin Ceramic DIP

Applications

- Array Processors
- Video Processors
- Radar Signal Processors
- FFT Processors
- General Purpose Digital Signal Processors
- Microcomputer/Minicomputer Accelerators

Functional Block Diagram



TRW LSI Products Inc.
P.O. Box 2472
La Jolla, CA 92038

Phone: (619) 457-1000
FAX: (619) 455-6314

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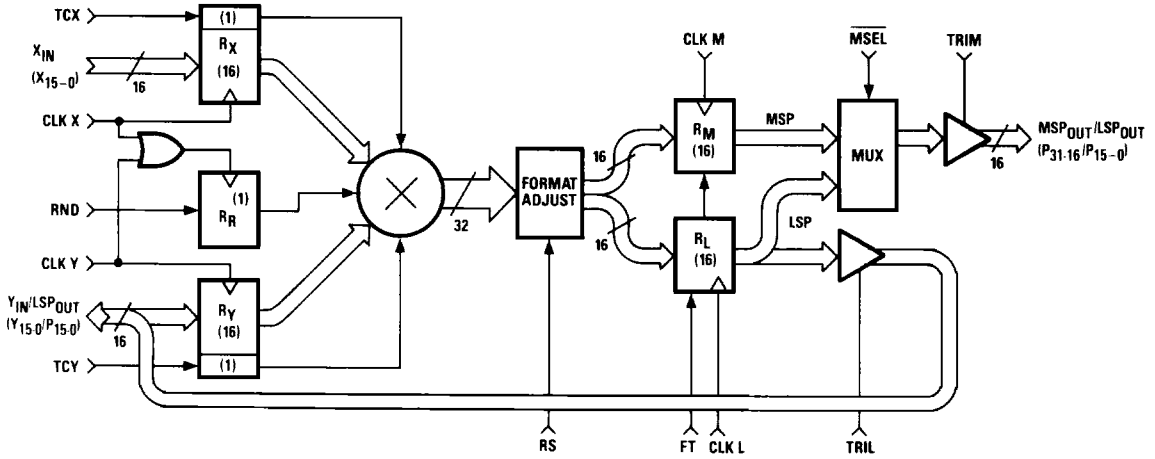
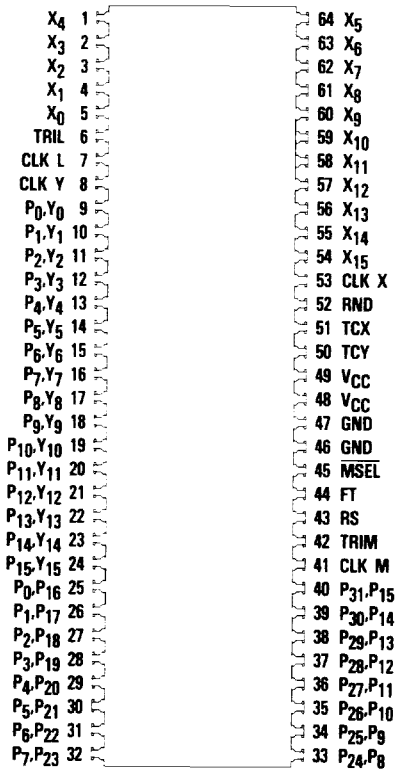
Functional Block Diagram



Pin Assignments



64 Lead DIP – J1 Package

Functional Description

General Information

The MPY016K has three functional sections: Input registers, an asynchronous multiplier array, and output registers. The input registers store the two 16-bit numbers which are to be multiplied and the instruction which controls the output rounding. The rounding control is used when a single-word output is desired. Each input operand is stored independently, simplifying multiplication by a constant. The asynchronous multiplier array is a network of AND gates and adders, designed to handle two's complement or unsigned magnitude numbers. The output registers hold the product as two 16-bit words, the Most Significant Product (MSP) and the Least Significant Product (LSP). Three-state output drivers allow the MPY016K to be used on a bus, or allow the least and most significant outputs to be multiplexed over the same 16-bit output lines. The Least Significant Product (LSP) is multiplexed with the Y input.

Power

The MPY016K operates from a single +5.0V supply. All power and ground lines must be connected. Note that the device is pin-compatible with the MPY016H, which has an additional ground pin; this is a control lead in the MPY016K. A ground on this pin (which must exist in all MPY016H applications) will cause the MPY016K to function like an MPY016H.

Name	Function	Value	J1 Package
V_{CC}	Positive Supply Voltage	+5.0V	Pins 48, 49
GND	Ground	0.0V	Pins 46, 47

Data Inputs

The MPY016K has two 16-bit two's complement or unsigned magnitude data inputs, labeled X and Y. The Most Significant Bits (MSBs), denoted X_{15} and Y_{15}, carry the sign information for the two's complement notation. The remaining bits are denoted X_0 through X_{14} and Y_0 through Y_{14} (with X_0 and Y_0 the Least Significant Bits). The input and output formats for fractional two's complement, fractional unsigned magnitude, fractional mixed mode, integer two's complement, integer unsigned magnitude, and integer mixed mode notation are shown in Figures 1 through 6, respectively. The Y inputs are multiplexed with the LSP outputs, and hence can only be used when the TRIL control is in a HIGH state. This is true whether or not the LSP is also multiplexed out through the MSP output port.

Name	Function	Value	J1 Package
X_{15}	X Data MSB	TTL	Pin 54
X_{14}		TTL	Pin 55
X_{13}		TTL	Pin 56
X_{12}		TTL	Pin 57
X_{11}		TTL	Pin 58
X_{10}		TTL	Pin 59
X_9		TTL	Pin 60
X_8		TTL	Pin 61
X_7		TTL	Pin 62
X_6		TTL	Pin 63
X_5		TTL	Pin 64
X_4		TTL	Pin 1
X_3		TTL	Pin 2
X_2		TTL	Pin 3
X_1		TTL	Pin 4
X_0	X Data LSB	TTL	Pin 5

Data Inputs (Cont.)

Name	Function	Value	J1 Package
Y_{15}	Y Data MSB	TTL	Pin 24
Y_{14}		TTL	Pin 23
Y_{13}		TTL	Pin 22
Y_{12}		TTL	Pin 21
Y_{11}		TTL	Pin 20
Y_{10}		TTL	Pin 19
Y_{9}		TTL	Pin 18
Y_{8}		TTL	Pin 17
Y_{7}		TTL	Pin 16
Y_{6}		TTL	Pin 15
Y_{5}		TTL	Pin 14
Y_{4}		TTL	Pin 13
Y_{3}		TTL	Pin 12
Y_{2}		TTL	Pin 11
Y_{1}		TTL	Pin 10
Y_{0}	Y Data LSB	TTL	Pin 9

Data Outputs

The MPY016K has a 32-bit two's complement or unsigned magnitude output which is the product of the two input data values. This output is divided into two 16-bit output words, the Most Significant Product (MSP) and Least Significant Product (LSP). The Most Significant Bit (MSB) of both the MSP and the LSP is the sign bit if fractional two's complement notation is used (TCX = TCY = 1, RS = 0). The input and output formats for fractional two's complement, fractional unsigned magnitude, fractional mixed mode, integer two's complement, integer unsigned magnitude, and integer mixed mode notation are shown in Figures 1 through 6, respectively.

If $\overline{\text{MSEL}}$ is LOW, the LSP output can be taken from the Y input pins only when TRIL is LOW. Care must be taken to enable these shared input lines only at the proper time. If $\overline{\text{MSEL}}$ is HIGH, the LSP output is made available at the MSP lines, as well as at the Y input pins. For an output from the MSP lines to be read, the TRIM control must be active.

RS is an output format control. A HIGH on RS deletes the sign bit from the LSP and shifts the MSP down one bit. This is mandatory for unsigned magnitude, mixed mode, or integer two's complement operation.

Name	Function	Value	J1 Package
P_{31}	Product MSB	TTL	Pin 40
P_{30}		TTL	Pin 39
P_{29}		TTL	Pin 38
P_{28}		TTL	Pin 37
P_{27}		TTL	Pin 36
P_{26}		TTL	Pin 35
P_{25}		TTL	Pin 34
P_{24}		TTL	Pin 33
P_{23}		TTL	Pin 32
P_{22}		TTL	Pin 31
P_{21}		TTL	Pin 30
P_{20}		TTL	Pin 29
P_{19}		TTL	Pin 28
P_{18}		TTL	Pin 27
P_{17}		TTL	Pin 26
P_{16}		TTL	Pin 25

Data Outputs (Cont.)

Name	Function	Value	J1 Package
			MUXED
			Input/Ouput
P_{15}		TTL	Pin 24/Pin 40
P_{14}		TTL	Pin 23/Pin 39
P_{13}		TTL	Pin 22/Pin 38
P_{12}		TTL	Pin 21/Pin 37
P_{11}		TTL	Pin 20/Pin 36
P_{10}		TTL	Pin 19/Pin 35
P_9		TTL	Pin 18/Pin 34
P_8		TTL	Pin 17/Pin 33
P_7		TTL	Pin 16/Pin 32
P_6		TTL	Pin 15/Pin 31
P_5		TTL	Pin 14/Pin 30
P_4		TTL	Pin 13/Pin 29
P_3		TTL	Pin 12/Pin 28
P_2		TTL	Pin 11/Pin 27
P_1		TTL	Pin 10/Pin 26
P_0	Product LSB	TTL	Pin 9/Pin 25

Clocks

The MPY016K has four clock lines, one for each input register and one for each product register. Data and two's complement instructions present at the inputs of these registers are loaded into the registers at the rising edge of the appropriate clock. The RND input is registered, clocked in at the rising edge of the logical OR of both CLK X and CLK Y. Special attention to the clock signals is required if normally HIGH clock signals are used. Problems with loading this control signal can be avoided by the use of normally LOW clocks.

Name	Function	Value	J1 Package
CLK X	Clock Input Data X	TTL	Pin 53
CLK Y	Clock Input Data Y	TTL	Pin 8
CLK L	Clock LSP Register	TTL	Pin 7
CLK M	Clock MSP Register	TTL	Pin 41

Controls

The MPY016K has eight control lines.

FT — A control line which makes the output register transparent if it is HIGH.

TRIM, TRIL — Three-state enable lines for the MSP and the LSP. The output driver is in the high-impedance state when TRIM or TRIL is HIGH, and enabled when the appropriate control is LOW.

RS — RS is an output format control. A HIGH level on RS deletes the sign bit from the LSP and shifts the MSP down one bit. This is mandatory for unsigned magnitude, mixed mode, and two's complement integer operations.

$\overline{\text{MSEL}}$ — $\overline{\text{MSEL}}$ is an output multiplex control. When $\overline{\text{MSEL}}$ is LOW, the MSP is available to the output three-state drivers at the MSP port, and the LSP is available to the output three-state drivers at the LSP/Y input port. When $\overline{\text{MSEL}}$ is HIGH, the LSP is available to both three-state drivers and the MSP is not available.

RND — When RND is HIGH, a one is added to the MSB of the LSP. Note that this bit depends on the state of the RS control. If RS is LOW when RND is HIGH, a one will be added to the 2^{-16} bit (P_{14}). If RS is HIGH when RND is HIGH, a one will be added to the 2^{-15} bit (P_{15}). In either case, the LSP output will reflect this addition when RND is HIGH. Note also that rounding always occurs in the positive direction; in some systems this may introduce a systematic bias.

TCX, TCY — Control how the device interprets data on the X and Y inputs. A HIGH on TCX or TCY makes the appropriate input a two's complement input, while a LOW makes the appropriate input a magnitude only input.

FT, RS, $\overline{\text{MSEL}}$, TRIM, and TRIL are not registered. The TCX input is registered, and clocked in at the rising edge of the X clock signal, CLK X. The TCY input is also registered, and clocked in at the rising edge of the Y clock signal, CLK Y. The RND input is registered, and clocked in at the rising edge of the logical OR of both CLK X and CLK Y. Special attention is required if normally HIGH clock signals are used. Problems with loading of these control signals can be avoided by the use of normally LOW clocks.

Name	Function	Value	J1 Package
RND	Round Control Bit	TTL	Pin 52
TCX	X Input Two's Complement	TTL	Pin 51
TCY	Y Input Two's Complement	TTL	Pin 50
FT	Output Register Feedthrough	TTL	Pin 44
RS	Output Register Shift	TTL	Pin 43
MSEL	Output Select	TTL	Pin 45
TRIM	MSP Three-State Control	TTL	Pin 42
TRIL	LSP Three-State Control	TTL	Pin 6

Figure 1. Fractional Two's Complement Notation

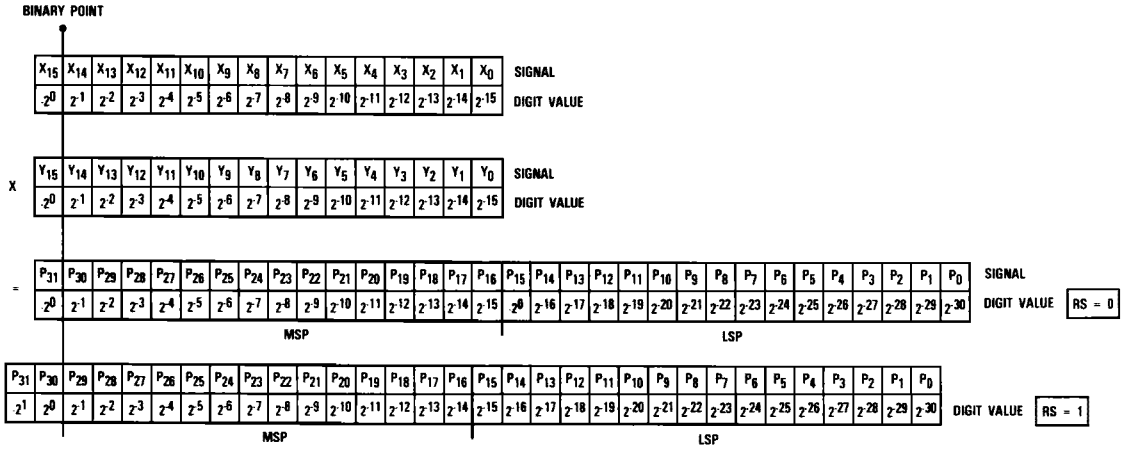


Figure 2. Fractional Unsigned Magnitude Notation

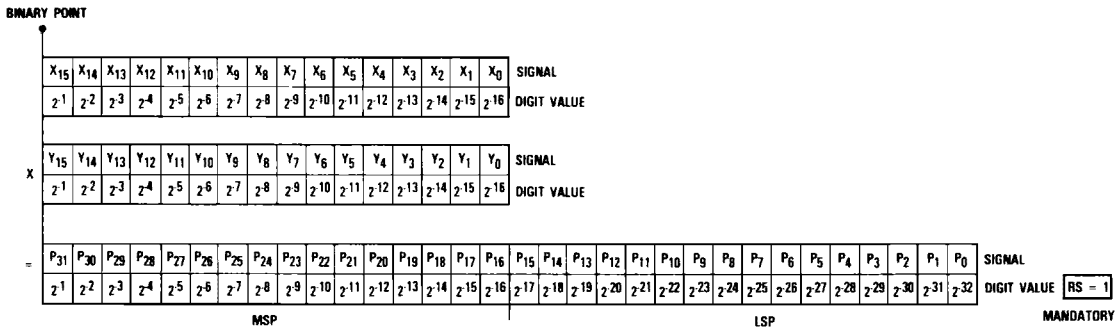


Figure 3. Fractional Mixed Mode Notation

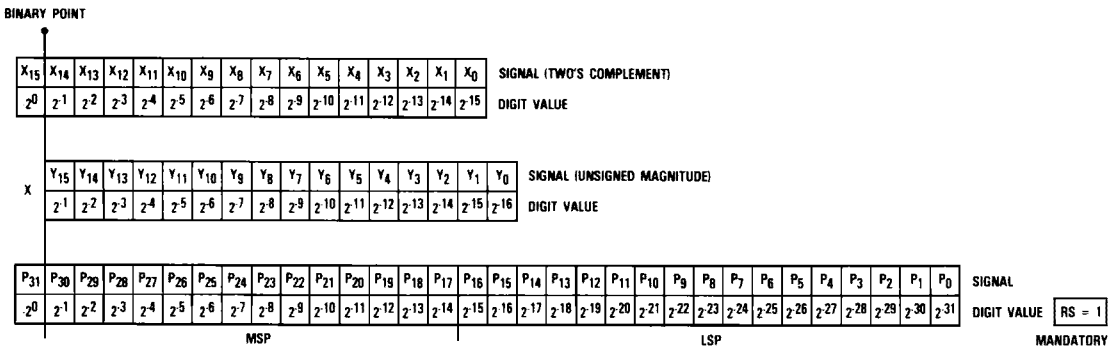


Figure 4. Integer Two's Complement Notation

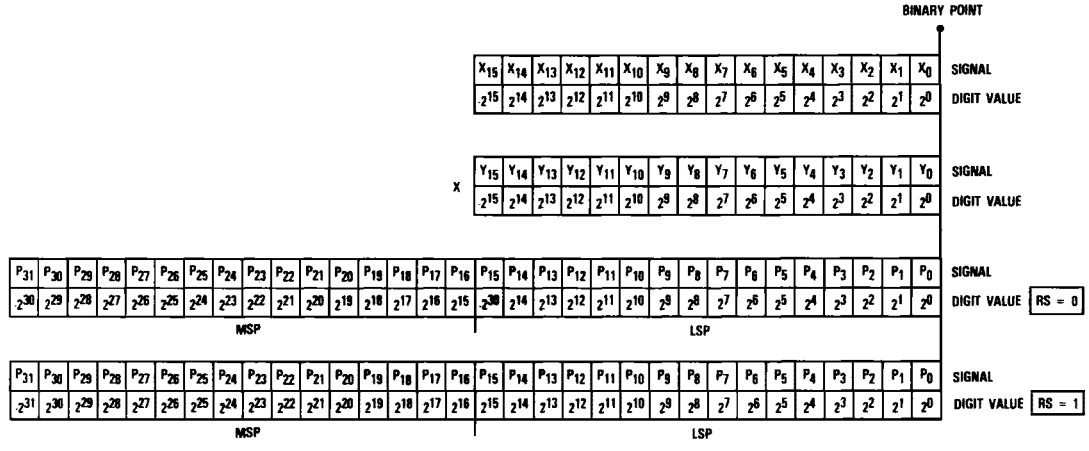


Figure 5. Integer Unsigned Magnitude Notation

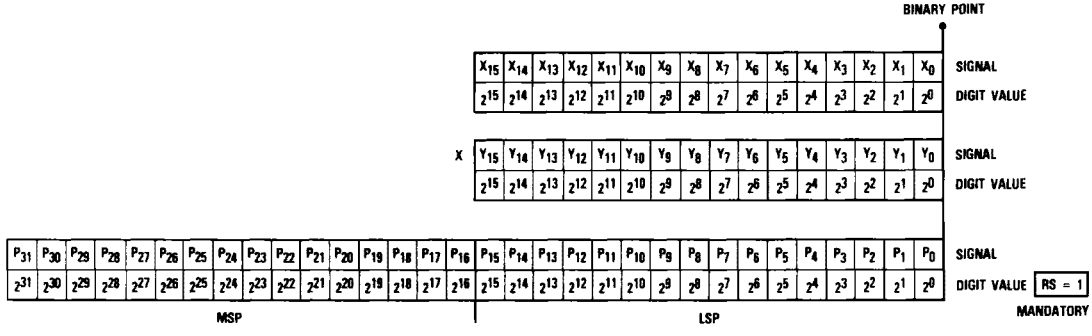


Figure 6. Integer Mixed Mode Notation

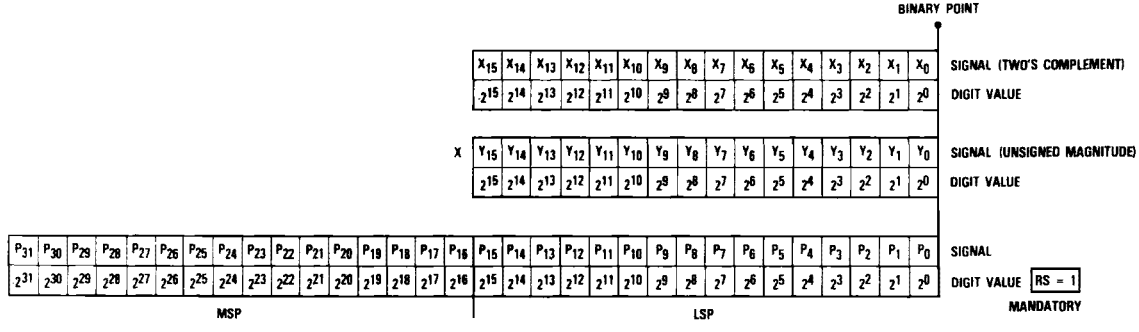


Figure 7. Timing Diagram, Non-Multiplexed Output

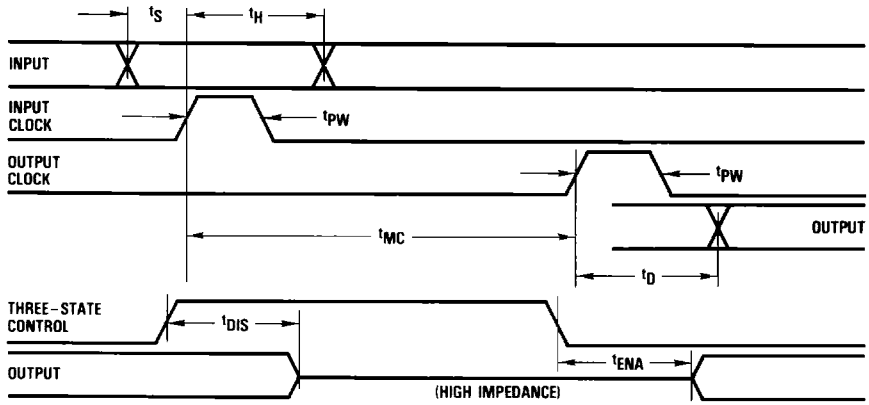


Figure 8. Timing Diagram, Unclocked Mode, Non-Multiplexed Output

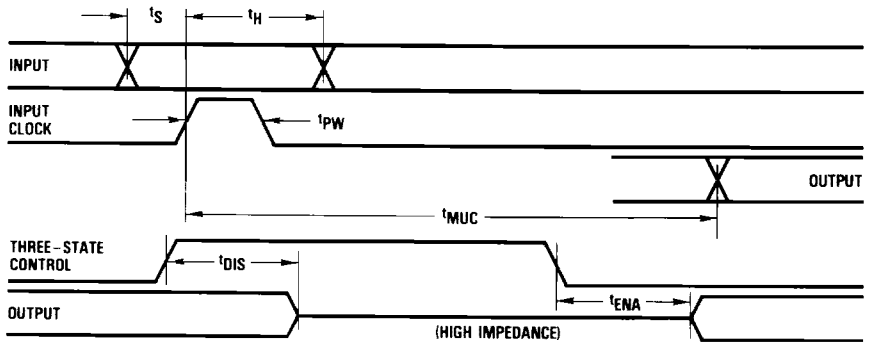


Figure 9. Timing Diagram, Multiplexed Output

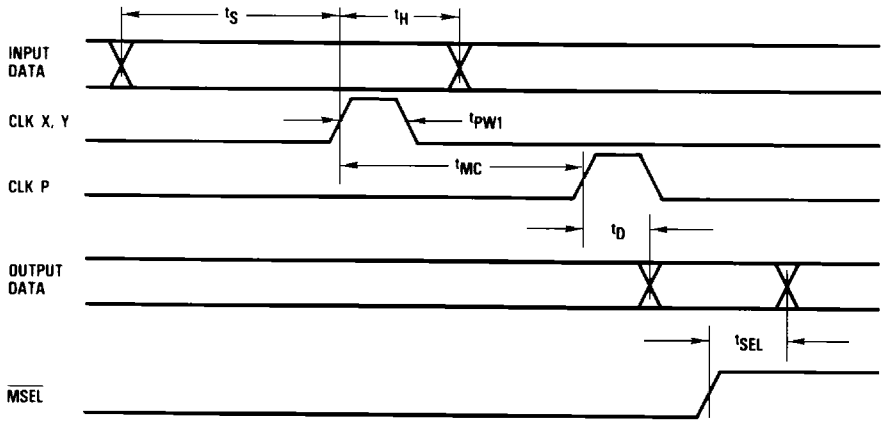
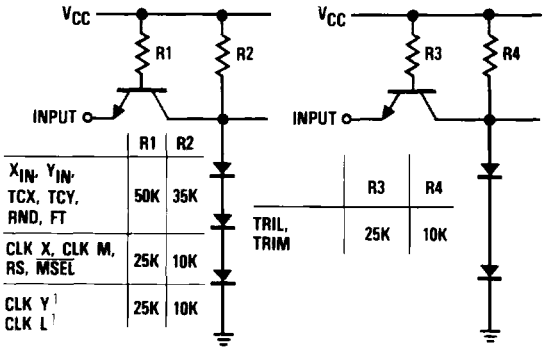


Figure 10. Equivalent Input Circuit



	R1	R2
X_{IN}, Y_{IN}, TCX, TCY, RND, FT	50K	35K
CLK X, CLK M, RS, $\overline{MSEL}$	25K	10K
CLK Y[1] CLK L[1]	25K	10K

	R3	R4
TRIL, TRIM	25K	10K

Note 1. CLK Y and CLK L each drive two equivalent inputs.

Figure 11. Equivalent Output Circuit

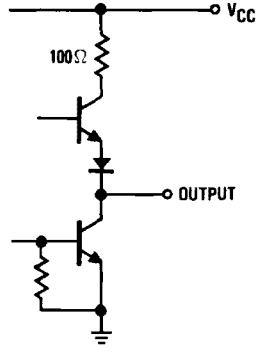


Figure 12. Test Load

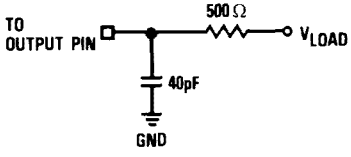
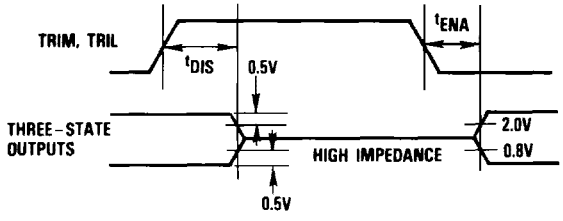


Figure 13. Transition Levels For Three-State Measurements



Application Notes

Mixed Mode Multiplication

There are several applications in which mixed mode multiplication may be advantageous. For example, inputs to a digital signal processor are often generated as unsigned magnitude numbers (e.g., data from an analog-to-digital converter). These numbers are effectively all positive values. In contrast, filter coefficients must often be negative. As a result, either the data must be converted to two's complement notation (which requires an additional bit), or the multiplier must be capable of mixed mode operation. The MPY016K provides this capability by independently specifying the mode of the multiplicand (X) and the multiplier (Y) on the TCX and TCY pins. No additional circuitry is required and the resulting product is in two's complement notation.

Multiplication By A Constant

Multiplication by a constant requires that the constant be loaded into the desired input register, and that the desired register not be loaded again until a new constant is desired. The multiply cycle then consists of loading new data and strobing the output register.

Selection Of Numeric Format

Essentially, the difference between integer, mixed, and fractional notation in system design is only conceptual. For example, the MPY016K does not differentiate between this operation:

$$6 \times 2 = 12$$

and this operation:

$$(6/8) \times (2/8) = 12/64.$$

The difference lies in constant scale factors (in this case, a factor of 8 in the multiplier and multiplicand and a factor of 64 in the product). However, these scale factors do have implications for hardware design. Because common good design practice assigns a fixed value to any given line (and input and output signals often share the same line), the scale factors determine the connection of the output pins of any multiplier in a system. As a result, only two choices are normally made: integer and fractional notation. If integer notation is used, the Least Significant Bits of the multiplier, multiplicand, and product all have the same value. If fractional notation is used, the Most Significant Bits of the multiplier, multiplicand, and product all have the same value. These formats are illustrated in detail in Figures 1 through 6.

Register Shift (RS) Control

In two's complement notation, the acceptable range of values for a given word size is not the same for positive and negative numbers. The largest negative number is one LSB larger than the largest positive number. This is true for either fractional or integer notation. A problem can arise when the largest representable negative number is multiplied by itself. This should give a positive number of the same magnitude. However, the largest representable positive number is one LSB less than this value. As a result, this product cannot be correctly represented without using one additional output bit. The MPY016K has a Register Shift (RS) control that permits shifting of the result to provide a correct answer for every two's complement multiplication. When RS is active, the value of all bits in the MSP is doubled (i.e. shifted left one position), which provides the capability to represent the largest possible product. The MSB of the Least Significant Product is changed from a duplicate of the sign bit to the necessary bit to fill in the output word. The effects of this control are illustrated in Figures 1 and 4. Note that for unsigned magnitude operation, the RS control must be HIGH.

Absolute maximum ratings (beyond which the device will be damaged) [1]

Supply Voltage	−0.5 to +7.0V
Input	
Applied voltage	−0.5 to +5.5V [2]
Forced current	−6.0 to +6.0mA
Output	
Applied voltage	−0.5 to +5.5V [2]
Forced current	−0.1 to +6.0mA [3,4]
Short-circuit duration (single output in high state to ground)	1 sec
Temperature	
Operating, case	−60 to +140°C
junction	175°C
Lead, soldering (10 seconds)	300°C
Storage	−65 to +150°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range, and measured with respect to GND.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.

Operating conditions

Parameter		Temperature Range						Units
		Standard			Extended			
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.75	5.0	5.25	4.5	5.0	5.5	V
t_{PWL}	Clock Pulse Width, LOW	15			22			ns
t_{PWH}	Clock Pulse Width, HIGH	15			22			ns
t_S	Input Setup Time (MPY016K)	20			25			ns
	(MPY016K-1)	20			20			ns
t_H	Input Hold Time	0			2			ns
V_{IL}	Input Voltage, Logic LOW			0.8			0.8	V
V_{IH}	Input Voltage, Logic HIGH	2.0			2.0			V
I_{OL}	Output Current, Logic LOW			4.0			4.0	mA
I_{OH}	Output Current, Logic HIGH			−400			−400	μA
T_A	Ambient Temperature, Still Air	0		70				°C
T_C	Case Temperature				−55		+125	°C

Electrical characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
I_{CC}	Supply Current	V_{CC} = MAX, Static[1]					
		T_A = 0°C to 70°C		875			mA
		T_A > 25°C[2]		860			mA
		T_C = -55°C to +125°C				1050	mA
		T_C > 35°C				960	mA
		V_{CC} = 5.0V					
		T_A > 25°C		840			mA
		T_C > 35°C				920	mA
I_{IL}	Input Current, Logic LOW	V_{CC} = MAX, V_I = 0.4V					
		X_{IN}, Y_{IN}, TCY, TCX, FT, RND		-0.2		-0.2	mA
		CLK Y, CLK L		-1.2		-1.2	mA
		CLK X, CLK M, $\overline{\text{MSEL}}$, TRIM, TRIL, RS		-0.6		-0.6	mA
I_{IH}	Input Current, Logic HIGH	V_{CC} = MAX, V_I = 2.4V					
		X_{IN}, Y_{IN}, TCY, TCX, FT, RND		50		50	μA
		CLK Y, CLK L		100		100	μA
		CLK X, CLK M, $\overline{\text{MSEL}}$, TRIM, TRIL, RS		50		50	μA
I_I	Input Current, Max Input Voltage	V_{CC} = MAX, V_I = 5.5V		1.0		1.0	mA
V_{OL}	Output Voltage, Logic LOW	V_{CC} = MAX, I_{OL} = MAX		0.5		0.5	V
V_{OH}	Output Voltage, Logic HIGH	V_{CC} = MIN, I_{OH} = MAX	2.4		2.4		V
I_{OZL}	Hi-Z Output Leakage Current, Output LOW	V_{CC} = MAX, V_I = 0.4V					
		Non-Shared Pins		-40		-50	μA
		Shared Pins		-200		-200	μA
I_{OZH}	Hi-Z Output Leakage Current, Output HIGH	V_{CC} = MAX, V_I = 2.4V					
		Non-Shared Pins		40		50	μA
		Shared Pins		50		50	μA
I_{OS}	Short Circuit Output Current	V_{CC} = MAX, One pin to ground, one second duration, output HIGH.	-4	-50	-4	-50	mA
C_I	Input Capacitance	T_A = 25°C, F = 1MHz		10		10	pF
C_O	Output Capacitance	T_A = 25°C, F = 1MHz		10		10	pF

Notes:

1. Worst case, all inputs and outputs LOW.
2. Part has a negative temperature coefficient, i.e., power consumption falls as temperature increases.

Switching characteristics within specified operating conditions [1]

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
t_{MC}	Multiply Time, Clocked	V_{CC} = Min, MPY016K		45		50	ns
		MPY016K-1		40		45	ns
t_{MUC}	Multiply Time, Unclocked	V_{CC} = Min MPY016K		75		85	ns
		MPY016K-1		70		75	ns
t_D	Output Delay	V_{CC} = Min, Test Load: V_{LOAD} = 2.2V MPY016K		30		35	ns
		MPY016K-1		30		30	ns
t_{SEL}	Output Multiplex Select Delay	V_{CC} = Min, Test Load: V_{LOAD} = 2.2V		20		25	ns
t_{ENA}	Three-State Output Enable Delay	V_{CC} = Min, Test Load: V_{LOAD} = 1.8V		30		35	ns
t_{DIS}	Three-State Output Disable Delay	V_{CC} = Min, Test Load: V_{LOAD} = 2.6V (t_{DIS0}) [2] V_{LOAD} = 0.0V (t_{DIS1}) [2]		30		35	ns

Notes 1. All transitions are measured at a 1.5V level except for t_{DIS} and t_{ENA}, which are shown in Figure 13.

2. t_{DIS1} denotes the transition from logical 1 to three-state.
t_{DIS0} denotes the transition from logical 0 to three-state.

Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
MPY016KJ1C	STD – T_A = 0°C to 70°C	Commercial	64 Pin Ceramic DIP	016KJ1C
MPY016KJ1C1	STD – T_A = 0°C to 70°C	Commercial	64 Pin Ceramic DIP	016KJ1C1
MPY016KJ1A	EXT – T_C = –55°C to 125°C	High Reliability	64 Pin Ceramic DIP	016KJ1A
MPY016KJ1A1	EXT – T_C = –55°C to 125°C	High Reliability	64 Pin Ceramic DIP	016KJ1A1