PRELIMINARY DATA SHEET

gm5060

C5060-DAT-01D

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Genesis Microchip Inc.
165 Commerce Valley Dr. West • Thornhill • ON • Canada L3T 7V8 • Tel: (905) 889-5400 • Fax: (905) 889-5422
2150 Gold Street • PO Box 2150 • Alviso • CA • USA 95002 • Tel: (408) 262-6599 • Fax: (408) 262-6365
4F, No. 24, Ln 123, Sec 6, Min-Chung E. Rd. • Taipei • Taiwan • Tel: (2) 2791-0118 • Fax: (2) 2791-0196
www.genesis-microchip.com / info@genesis-microchip.com

Document history

Document	Description	Date
C5060-DAT-01A	Initial Release	January 2001
C5060-DAT-01B	• Removed section 4.3.1. • Included max. speed for SDDS clock in section 4.3.3. • Corrected OSD RAM size to 3594 words in section 4.15. • In Table 12 changed input clock to 165MHz. • In Table 16 changed entries for Power Consumption and Supply Current. • In Table 17 changed TMDS Clock to 165MHz. Changed ADC Clock to 162MHz. • Changed Speed in Section 6 to 162MHz.	February 2001
C5060-DAT-01C	• In section 3, corrected references to certain signals. • In Table 16 modified entries for Outputs. • In Table 17 changed F_CLK Frame Store Clock speed to 144MHz.	April 2001
C5060-DAT-01D	• In first sentence of section 4.15.1.4, corrected reference to bit setting.	April 2001

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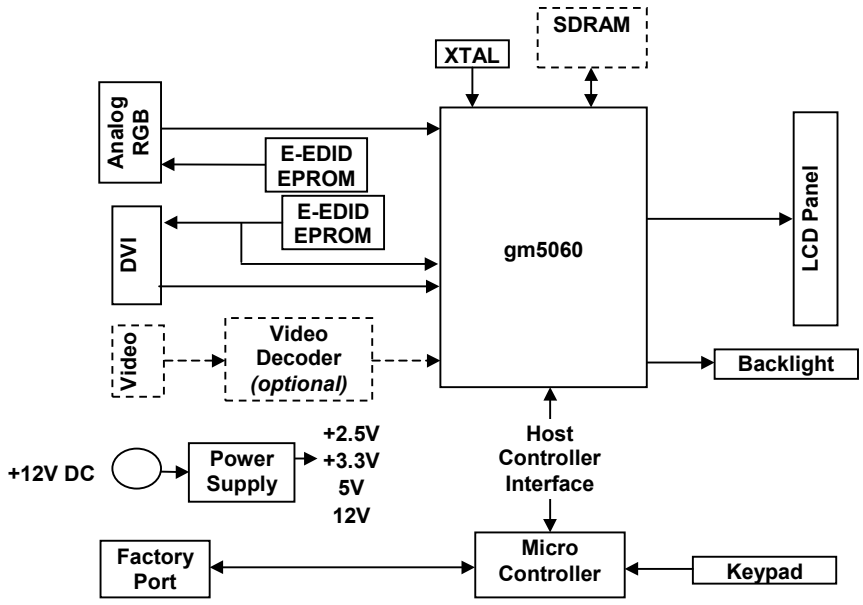
1. OVERVIEW

The gm5060 is a graphics processing IC providing high-quality images for LCD monitors up to UXGA resolutions. It combines a triple ADC, the Genesis Ultra-Reliable DVI ™ receiver with digital content protection, a high quality zoom and shrink scaling engine, frame rate conversion, an on-screen display (OSD) controller, a microprocessor and many other functions in a single device. This high level of integration enables simple, flexible, cost-effective solutions featuring fewer required components.

1.1 gm5060 System Design Example

Figure 1 below shows a typical dual interface LCD monitor system based on the gm5060. Designs based on the gm5060 have reduced system cost and simplified hardware and firmware design because only a minimal number of components are required in the system.

Figure 1. gm5060 System Design Example



1.2 gm5060 Features

FEATURES

- Zoom and shrink scaling (all resolutions up to UXGA)
- Frame rate conversion
- Integrated 8-bit triple-channel ADC / PLL
- Integrated Genesis Ultra-Reliable DVI ™ receiver (DVI 1.0)
- Integrated High-bandwidth Digital Content Protection (HDCP)
- Embedded microcontroller simplifies OSD creation
- On-chip versatile OSD engine
- All system clocks synthesized from a single external crystal
- Programmable gamma correction (CLUT)
- Hue, Saturation, Brightness, Contrast and Gamma controls for RGB and YUV signals
- RealColor ™ fleshtone adjustment
- PWM backlight intensity control
- 5 Volt tolerant inputs

- **High-Quality Advanced Scaling**
  - Fully programmable zoom/shrink ratios
  - Independent horizontal / vertical zoom and shrink
  - Variable sharpness control
  - Moiré cancellation

- **Analog RGB Input Port**
  - Supports up to UXGA 60Hz input
  - UXGA 75 and 85Hz recovery mode using sub-sampling

- **Ultra-Reliable DVI ™ Receiver**
  - Single link on-chip DVI receiver
  - Operating up to 165 MHz
  - Direct connect to all DVI compliant TMDS transmitters
  - High-bandwidth Digital Content Protection (HDCP)
  - Enhanced protection of HDCP secret keys

- **Digital Video Port**
  - 8-bit ITU-R BT656 input video
  - Seamless connection to commercially available video capture devices

APPLICATIONS

- Multi-synchronous UXGA LCD monitors with dual analog/digital interface

- **Auto-Configuration / Auto-Detection**
  - Phase and image positioning
  - Input format detection

- **Frame Store Interface**
  - 48-bit SDRAM interface
  - Optional use of data compression for more flexibility and lower system solution cost
  - Support for up to 143MHz SDRAM or SGRAM

- **On-chip OSD Controller**
  - Bit-mapped OSD capability
  - On-chip RAM for downloadable fonts
  - Horizontal and vertical stretch of OSD images
  - Blinking, transparency and blending

- **Output Format**
  - Double wide up to UXGA 60Hz output (135MHz)

- **Operating Modes**
  - Frame rate conversion and scaling of images
  - Bypass mode with no filtering and/or frame buffering
  - 1:1 centering
  - De-interlaced zoom
  - Frame Sync and Free Run display synchronization modes

- **Highly Integrated Solution Provides Lowest System Cost**

- **Simplicity of Design Speeds Time to Market**

- **Complete reference design kit available (software and hardware)**

PACKAGE

- 292-pin PBGA

2. PINOUT DIAGRAM

The gm5060 is available in a 292-pin PBGA (Ball Gate Array) package. Figure 2 below provides the ball locations for all signals.

Power and Ground:

DGND	Periphery and Core Digital Ground
DVDD_3.3	Periphery Digital Vdd (3.3V supply)
DVDD_2.5	Core Digital Vdd (2.5V supply)
PGND	PLL Ground
PLLVDD_3.3	PLL Vdd (3.3V supply)
AGND	Analog Ground
AVDD_3.3	Analog Vdd (3.3V supply)
AVDD_2.5	Analog Vdd (2.5V supply)

Pinout Legend:

DVI
High Frequency Clock
ADC
DDS and PLL

Figure 2. gm5060 Pinout Diagram

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	
A	N / C	AGND	AGND	AGND	N / C	AVDD_2.5	AVDD_2.5	AVDD_2.5	AVDD_2.5	AVDD_2.5	AVDD_2.5	VCLK	YUV5	YUV2	DBRED7	DBRED4	DBRED1	DBGRN6	DBGRN3	DBGRN2	A
B	AGND	AVDD_3.3	AGND	AGND	N / C	AVDD_3.3	AVDD_3.3	AVDD_3.3	AVDD_3.3	REXT	AVDD_3.3	YUV7	YUV4	YUV1	DBRED6	DBRED3	DBRED0	DBGRN5	DBGRN1	DBGRN0	B
C	BLUE+	BLUE-	AVDD_3.3	AGND	AGND	RXC+	AGND	RX0+	RX1+	RX2+	AGND	YUV6	YUV3	YUV0	DBRED5	DBRED2	DBGRN7	DBGRN4	DBBLU7	DBBLU6	C
D	GREEN-	GREEN+	AVDD_3.3	AGND	AGND	RXC-	AGND	RX0-	RX1-	RX2-	AGND	DVDD_2.5	DVDD_3.3	DVDD_2.5	DVDD_3.3	DVDD_3.3	DVDD_2.5	DBBLU5	DBBLU4	DBBLU3	D
E	RED+	RED-	AVDD_3.3	AGND													DVDD_3.3	DBBLU2	DBBLU1	DBBLU0	E
F	N / C	PLLVDD_3.3	PLLGND	PLLVDD_3.3													DVDD_2.5	DEN	DVS	DHS	F
G	PLLVDD_3.3	PLLGND	PLLVDD_3.3	PLLGND													DVDD_3.3	GPIO6 / DFSYNCn	GPIO7 / DOVL	**DCLK**	G
H	PLLVDD_3.3	PLLGND	PLLGND	**XTAL**				DGND	DGND	DGND	DGND	DGND	DGND				DARED7	DARED6	DARED5	DARED4	H
J	PLLVDD_3.3	PLLGND	PLLVDD_3.3	**TCLK**				DGND	DGND	DGND	DGND	DGND	DGND				DVDD_3.3	DARED3	DARED2	DARED1	J
K	VSYNC	N / C	PLLGND	DVDD_2.5				DGND	DGND	DGND	DGND	DGND	DGND				DVDD_2.5	DARED0	DAGRN7	DAGRN6	K
L	GPIO5	HSYNC	**EXTCLK**	DVDD_3.3				DGND	DGND	DGND	DGND	DGND	DGND				DVDD_3.3	DAGRN3	DAGRN4	DAGRN5	L
M	GPIO4	GPIO3	GPIO2	GPIO1 / PWM1				DGND	DGND	DGND	DGND	DGND	DGND				DVDD_2.5	DAGRN0	DAGRN1	DAGRN2	M
N	GPIO0 / PWM0	DDC_SCL	DDC_SDA	DVDD_2.5				DGND	DGND	DGND	DGND	DGND	DGND				DVDD_3.3	DABLU5	DABLU6	DABLU7	N
P	HCLK / SCL	HFSn / SDA	HDATA3	HDATA2													DVDD_2.5	DABLU2	DABLU3	DABLU4	P
R	HDATA1	HDATA0	IRQn	IRQINn / GPIO8													DVDD_3.3	FSDATA47	DABLU0	DABLU1	R
T	RESETn	DGND	**FSCLK**	DVDD_3.3													DVDD_2.5	FSDATA44	FSDATA45	FSDATA46	T
U	FSCKE	FSWE	FSCAS	DVDD_2.5	DVDD_3.3	DVDD_3.3	DVDD_2.5	DVDD_3.3	DVDD_2.5	DVDD_3.3	DVDD_2.5	DVDD_3.3	DVDD_3.3	DVDD_2.5	DVDD_3.3	DVDD_2.5	DVDD_3.3	FSDATA41	FSDATA42	FSDATA43	U
V	FSRAS	FSADDR13	FSADDR8	FSADDR5	FSADDR2	FSDATA0	FSDATA3	FSDATA6	FSDATA7	FSDATA10	FSDATA15	FSDQM2	FSDATA19	FSDATA22	FSDATA25	FSDATA28	FSDATA31	FSDATA34	FSDATA39	FSDATA40	V
W	FSADDR12	FSADDR10	FSADDR7	FSADDR4	FSADDR1	FSDATA1	FSDATA4	FSDQM0	FSDATA8	FSDATA11	FSDATA14	FSDQM3	FSDATA18	FSDATA21	FSDATA24	FSDATA27	FSDATA30	FSDATA33	FSDATA36	FSDATA38	W
Y	FSADDR11	FSADDR9	FSADDR6	FSADDR3	FSADDR0	FSDATA2	FSDATA5	FSDQM1	FSDATA9	FSDATA12	FSDATA13	FSDATA16	FSDATA17	FSDATA20	FSDATA23	FSDATA26	FSDATA29	FSDATA32	FSDATA35	FSDATA37	Y

3. PIN LIST

I/O Legend: **I** = Input **O** = Output **P** = Power **G**= Ground

Table 1. ADC Signals

Name	I/O	Ball#	Description
RED+	I	E1	Positive analog input for Red channel.
RED-	I	E2	Negative analog input for Red channel.
GREEN+	I	D2	Positive analog input for Green channel.
GREEN-	I	D1	Negative analog input for Green channel.
BLUE+	I	C1	Positive analog input for Blue channel.
BLUE-	I	C2	Negative analog input for Blue channel.
HSYNC	I	L2	ADC input horizontal sync. [Input, schmitt trigger (400mV typical hysteresis), 5V-tolerant]
VSYNC	I	K1	ADC input vertical sync. [Input, schmitt trigger (400mV typical hysteresis), 5V-tolerant]

Table 2. DVI Receiver Signals

Name	I/O	Ball#	Description
REXT	I	B10	External termination resistor. A 1% 1K ohm resistor must be connected from this pin to AVDD_3.3 (3.3V analog power supply).
RX2+	I	C10	TMDS input channel 2+ RED , imbedded CTL3
RX2-	I	D10	TMDS input channel 2- RED , imbedded CTL3
RX1+	I	C9	TMDS input channel 1+ GREEN
RX1-	I	D9	TMDS input channel 1- GREEN
RX0+	I	C8	TMDS input channel 0+ BLUE
RX0-	I	D8	TMDS input channel 0- BLUE
RXC+	I	C6	TMDS input clock pair
RXC-	I	D6	TMDS input clock pair
DDC_SCL	I	N2	DDC Interface for DVI-HDCP communication. This is SCL for slave-only DDC communication. [Input, schmitt trigger (400mV typical hysteresis), 5V-tolerant]
DDC_SDA	IO	N3	DDC Interface for DVI-HDCP communication. This is SDA for slave-only DDC communication. [Bi-directional, 4mA drive output, schmitt trigger input (400mV typical hysteresis), 5V-tolerant]

Table 3. RCLK and FCLK PLL Signals

Name	I/O	Ball#	Description
TCLK	O	J4	Feedback connection to 14.3 MHz crystal. Genesis recommends the use of a 14.3 MHz crystal. If the reference clock source is a clock oscillator, this pin should be grounded through a 2.7K pulldown resistor. In this case, the frequency restrictions are: Min = 14MHz Max = 24MHz. [3.3V level]
XTAL	I	H4	Crystal oscillator input. Connect to 14.3 MHz crystal. If a 14.3 MHz crystal is not used as the reference clock source, the input clock frequency restrictions are: Min = 14MHz Max = 24MHz. [3.3V level]

Table 4. Video Input Port Signals

Name	I/O	Ball#	Description
VCLK	I	A12	Input sample clock (27MHz) from video decoder. [Input, 5V-tolerant]
YUV7	I	B12	Input YUV data in ITU-R BT656 format with embedded SAV and EAV.
YUV6		C12	These inputs feature internal pull-downs. Any external pull-ups used on these inputs should not exceed
YUV5		A13	10k ohms. Larger values run the risk of lowering the input high voltage to a value that would create
YUV4		B13	large currents in the input pads.
YUV3		C13	YUV(7:0) incorporate General Purpose Inputs (GPIs) . See Section 4.18.1.
YUV2		A14	[Input, 100KΩ pull-down, 5V-tolerant]
YUV1		B14	
YUV0		C14	

Table 5. Host Controller Interface Signals

Name	I/O	Ball#	Description
HCLK / SCL	I	P1	Host Protocol input clock. HCLK for 6-wire nibble, SCL for 2-wire mode. [Input, schmitt trigger (400mV typical hysteresis), 5V-tolerant]
HFSn / SDA	IO	P2	Host Protocol framing signal for 6-wire nibble mode. Also used as SDA (open drain) signal for 2-wire mode. [Bi-directional, 4mA drive output, schmitt trigger input (400mV typical hysteresis), 5V-tolerant]
HDATA3 HDATA2 HDATA1 HDATA0	IO	P3 P4 R1 R2	Host Protocol data nibble for 6-wire mode. The upper nibble byte(3:0) is transferred first followed by lower nibble byte(7:4). [Bi-directional, 8mA drive output, schmitt trigger input (400mV typical hysteresis), 5V-tolerant]
IRQn	O	R3	Interrupt output pin is active low and open drain. [Output, open drain, 8mA drive, 5V-tolerant]
IRQINn / GPIO8	IO	R4	Interrupt input to internal 8051 OCM is active low. OCM interrupt#0. This signal is also GPIO8. Always open drain when in GPO mode. [Bi-directional, schmitt trigger input (400mV typical hysteresis), 5V-tolerant, 8mA drive output]
RESETn	I	T1	Hardware Reset signals is active low. [Input, schmitt trigger (400mV typical hysteresis), 5V-tolerant]
EXTCLK	I	L3	For test purposes. Alternate input clock to drive display when Display DDS is not used. [Input, 5V-tolerant]
GPIO0 / PWM0	IO	N1	General purpose input/output signal or PWM0. Open drain option via register bit. [Bi-directional, 8mA drive output, schmitt trigger input (400mV typical hysteresis), 5V-tolerant]
GPIO1 / PWM1	IO	M4	General purpose input/output signal or PWM1. Open drain option via register bit. [Bi-directional, 8mA drive output, schmitt trigger input (400mV typical hysteresis), 5V-tolerant]
GPIO2	IO	M3	General purpose input/output signals. Open drain option via register bit. [Bi-directional, 8mA drive output, schmitt trigger input (400mV typical hysteresis), 5V-tolerant]
GPIO3	IO	M2	General purpose input/output signals. Open drain option via register bit. [Bi-directional, 8mA drive output, schmitt trigger input (400mV typical hysteresis), 5V-tolerant]
GPIO4	IO	M1	General purpose input/output signals. Open drain option via register bit. [Bi-directional, 8mA drive output, schmitt trigger input (400mV typical hysteresis), 5V-tolerant]
GPIO5	IO	L1	General purpose input/output signals. Open drain option via register bit. [Bi-directional, 8mA drive output, schmitt trigger input (400mV typical hysteresis), 5V-tolerant]

Table 6. Display Port Signals

Name	I/O	Ball#	Description
GPIO6 / DFSYNCn	IO	G18	GPIO6 by default. Open drain GPO option via register bit. If DFSYNCn is register bit enabled, manual synchronization of display timing causes display timing to jump to its H and V lock load location. [Bi-directional, 8mA drive output, schmitt trigger input (400mV typical hysteresis), 5V-tolerant]
GPIO7 / DOVL	IO	G19	GPIO7 by default. Open drain GPO option via register bit. If DOVL is register bit enabled, overlay valid display pixels are indicated by active DOVL. [Bi-directional, 8mA drive output, schmitt trigger input (400mV typical hysteresis), 5V-tolerant]
DCLK	O	G20	Display output clock. [Tristate output, programmable drive 0-24 mA, not 5V-tolerant]
DVS	O	F19	Display vertical sync. [default = active high] [Tristate output, programmable drive 0-24 mA, not 5V-tolerant]
DHS	O	F20	Display horizontal sync. [default = active high] [Tristate output, programmable drive 0-24 mA, not 5V-tolerant]

Name	I/O	Ball#	Description
DEN	O	F18	Display Enable frames the output background window. [Tristate output, programmable drive 0-24 mA, not 5V-tolerant]
DARED7 DARED6 DARED5 DARED4 DARED3 DARED2 DARED1 DARED0	IO	H17 H18 H19 H20 J18 J19 J20 K18	Display output red data (even or left pixel). [Tristate output, programmable drive 0-24 mA, not 5V-tolerant]
DAGRN7 DAGRN6 DAGRN5 DAGRN4 DAGRN3 DAGRN2 DAGRN1 DAGRN0	IO	K19 K20 L20 L19 L18 M20 M19 M18	Display output green data (even or left pixel). [Tristate output, programmable drive 0-24 mA, not 5V-tolerant]
DABLU7 DABLU6 DABLU5 DABLU4 DABLU3 DABLU2 DABLU1 DABLU0	IO	N20 N19 N18 P20 P19 P18 R20 R19	Display output blue data (even or left pixel). [Tristate output, programmable drive 0-24 mA, not 5V-tolerant]
DBRED7 DBRED6 DBRED5 DBRED4 DBRED3 DBRED2 DBRED1 DBRED0	IO	A15 B15 C15 A16 B16 C16 A17 B17	Display output red data (odd or right pixel). [Tristate output, programmable drive 0-24 mA, not 5V-tolerant]
DBGRN7 DBGRN6 DBGRN5 DBGRN4 DBGRN3 DBGRN2 DBGRN1 DBGRN0	IO	C17 A18 B18 C18 A19 A20 B19 B20	Display output green data (odd or right pixel). [Tristate output, programmable drive 0-24 mA, not 5V-tolerant]
DBBLU7 DBBLU6 DBBLU5 DBBLU4 DBBLU3 DBBLU2 DBBLU1 DBBLU0	IO	C19 C20 D18 D19 D20 E18 E19 E20	Display output blue data (odd or right pixel). [Tristate output, programmable drive 0-24 mA, not 5V-tolerant]

Table 7. Frame Store Interface Signals

Name	I/O	Ball#	Description
FSCLK	O	T3	SDRAM clock. This signal is rising edge active. [Tri-state output, Programmable Drive, 0-24mA, not 5V-tolerant]
FSCKE	O	U1	SDRAM clock enable. This signal is active high. [Tri-state output, 8mA drive, 5V-tolerant]
FSRAS	O	V1	SDRAM row address strobe. This signal is active low [Tri-state output, 8mA drive, 5V-tolerant]
FSCAS	O	U3	SDRAM column address strobe. This signal is active low. [Tri-state output, 8mA drive, 5V-tolerant]
FSWE	O	U2	SDRAM write enable. This signal is active low. [Tri-state output, 8mA drive, 5V-tolerant]
FSDQM3 FSDQM2 FSDQM1 FSDQM0	O	W12 V12 Y8 W8	SDRAM data masks. Each bit enables one of four SDRAM byte “lanes”. This allows host OSD access to the SDRAM to be byte oriented. This signal is active high. Bit 0 enables FSDATA(7:0). Bit 1 enables FSDATA(15:8). Bit 2 enables FSDATA(23:16). Bit 3 enables FSDATA(31:24). [Tri-state output, 8mA drive, 5V-tolerant]
FSADDR13 FSADDR12 FSADDR11 FSADDR10 FSADDR9 FSADDR8 FSADDR7 FSADDR6 FSADDR5 FSADDR4 FSADDR3 FSADDR2 FSADDR1 FSADDR0	IO	V2 W1 Y1 W2 Y2 V3 W3 Y3 V4 W4 Y4 V5 W5 Y5	SDRAM multiplexed address bus. FSADDR[13:0] are used for bootstrapping configuration. See Section 4.16.1. [Bi-directional, 8mA drive output, 5V-tolerant]

FSDATA47	IO	R18	SDRAM data bus. Optionally programmable to 48 or 32 bits wide. Default is 32 bits wide.
FSDATA46		T20	[Bi-directional, 8mA drive output, 100KΩ pull-down, 5V-tolerant]
FSDATA45		T19	
FSDATA44		T18	
FSDATA43		U20	
FSDATA42		U19	
FSDATA41		U18	
FSDATA40		V20	
FSDATA39		V19	
FSDATA38		W20	
FSDATA37		Y20	
FSDATA36		W19	
FSDATA35		Y19	
FSDATA34		V18	
FSDATA33		W18	
FSDATA32		Y18	
FSDATA31		V17	
FSDATA30		W17	
FSDATA29		Y17	
FSDATA28		V16	
FSDATA27		W16	
FSDATA26		Y16	
FSDATA25		V15	
FSDATA24		W15	
FSDATA23		Y15	
FSDATA22		V14	
FSDATA21		W14	
FSDATA20		Y14	
FSDATA19		V13	
FSDATA18		W13	
FSDATA17		Y13	
FSDATA16		Y12	
FSDATA15		V11	
FSDATA14		W11	
FSDATA13		Y11	
FSDATA12		Y10	
FSDATA11		W10	
FSDATA10		V10	
FSDATA9		Y9	
FSDATA8		W9	
FSDATA7		V9	
FSDATA6		V8	
FSDATA5		Y7	
FSDATA4		W7	
FSDATA3		V7	
FSDATA2		Y6	
FSDATA1		W6	
FSDATA0		V6	

Table 8. Power and Ground Signals

Group Name	I/O	Ball #	Description
PLLGND	G	F3, G2, G4, H2, H3, J2, K3	Analog PLL / DDS Ground
PLLVDD_3.3	P	F2, F4, G1, G3, H1, J1, J3	Analog PLL / DDS 3.3VDC Bypass to PLLGND (0.1uF)
AGND	G	A2, A3, A4, B1, B3, B4, C4, C5, C7, C11, D4, D5, D7, D11, E4	Analog Ground
AVDD_2.5	P	A6, A7, A8, A9, A10, A11	Analog 2.5VDC Supply Bypass to AGND (0.1uF)
AVDD_3.3	P	B2, B6, B7, B8, B9, B11, C3, D3, E3	Analog 3.3VDC Supply Bypass to AGND (0.1uF)
DGND	G	H8, H9, H10, H11, H12, H13, J8, J9, J10, J11, J12, J13, K8, K9, K10, K11, K12, K13, L8, L9, L10, L11, L12, L13, M8, M9, M10, M11, M12, M13, N8, N9, N10, N11, N12, N13, T2	Digital Ground (Periphery and Core Logic)
DVDD_2.5	P	D17, D14, D12, F17, K4, K17, M17, N4, P17, T17, U4, U7, U9, U11, U14, U16	Digital VDD, 2.5VDC (Core Logic. Bypass to DGND, 0.1uF)
DVDD_3.3	P	D16, D15, D13, E17, G17, J17, L4, L17, N17, R17, T4, U5, U6, U8, U10, U12, U13, U15, U17	Digital VDD, 3.3VDC (I/O pins. Bypass to DGND, 0.1uF)

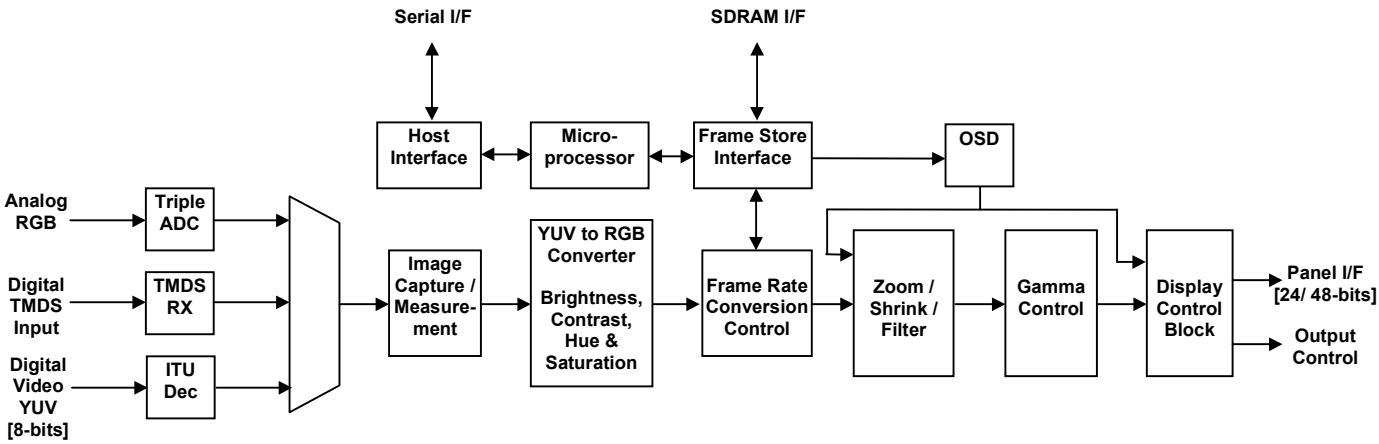
Table 9. No Connects

Group Name	I/O	Ball #	Description
N / C	-	A1, A5, B5, F1, K2	No Connect. Leave these pins floating.

4. FUNCTIONAL DESCRIPTION

A functional block diagram is illustrated below. Each of the functional units shown is described in the following sections.

Figure 3. gm5060 Functional Block Diagram



4.1 Clocking Options

The gm5060 features four clock inputs. All additional clocks are internal clocks derived from one or more of these four, using Direct Digital Synthesis (DDS).

TCLK is generated using an external crystal (recommended) or an external clock oscillator, as shown in Figure 4.

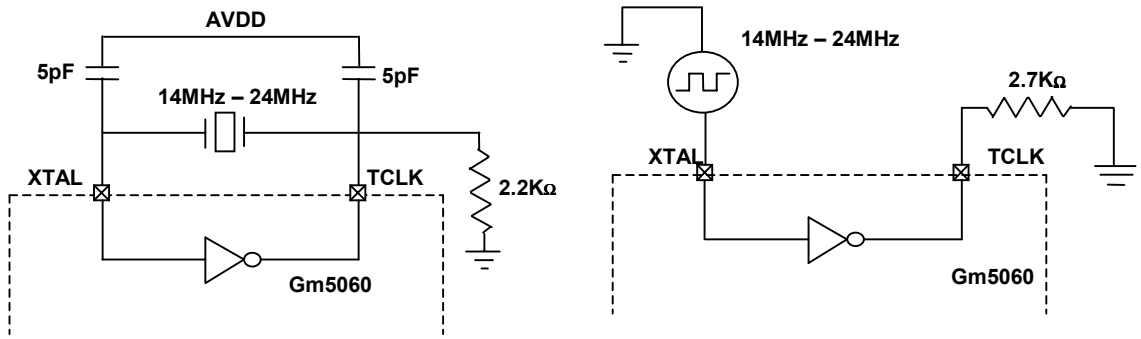


Figure 4. Clock Generation Options for gm5060

Note that different crystal oscillators may have values for recommended capacitive and resistive loading that are different from the values shown above.

1) Input Clock (TCLK). The external connection to the oscillator is via the TCLK and XTAL pads. A 14.3MHz crystal source is recommended, as internal PLL and logic circuits derive the required clock frequencies from this single source by default. Other crystal frequencies may be used (as indicated in Figure 4), but require custom bootstrapping and programming. In lieu of using a crystal oscillator, XTAL can be driven by a single-ended TTL/CMOS input clock (e.g. for testing of the IC) -- the TCLK pin should be grounded through a 2.7k pulldown resistor to maintain the correct duty cycle for the clock.

2) TMDS Differential Input Clock (RC+ and RC-)

3) Video Clock (VCLK) input pin

4) Host Interface Transfer Clock (HCLK for 6-Wire nibble; SCL for 2-wire serial)

4.1.1 Synthesized Clocks

The gm5060 synthesizes all additional clocks internally: Clock inputs to the DDDS and FCLK PLL (as shown in the figure below) are selected via a host interface register.

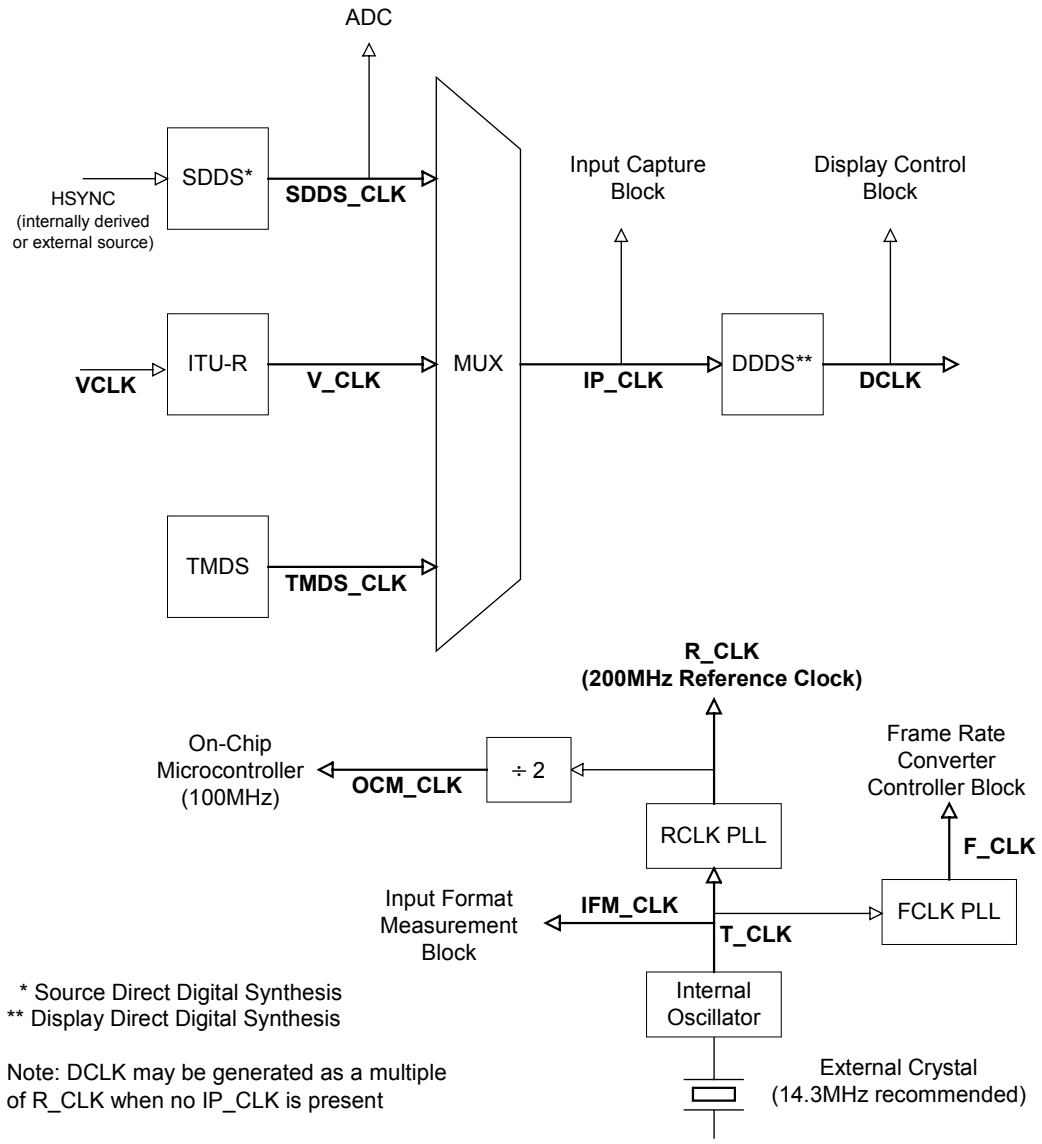


Figure 5. Internal Clock Sources

4.2 Hardware and Software Resets

4.2.1 Hardware Reset

Hardware Reset is performed by holding the RESETn pin low for a minimum of 1us. A TCLK input (see Clock Options above) must be applied during and after the reset. When the reset period is complete and RESETn is de-asserted, the power-up sequence is as follows:

1. Reset all registers of all types to their default state (this is 00h unless otherwise specified in the gm5060 Register Listing).
2. Force each clock domain into reset. Reset will remain asserted for 64 local clock domain cycles following the de-assertion of RESETn.
3. Operate the OCM_CLK domain at the T_CLK frequency.
4. Preset the RCLK PLL to output ~200MHz clock (assumes 14.3MHz TCLK crystal frequency).
5. Wait for RCLK PLL to Lock, then switch the OCM_CLK domain to operate from the bootstrap selected clock.
6. The OCM remains in reset until register enabled.

4.2.2 Software Reset

Software Reset is performed by programming the HOST_CONTROL register bit SOFT_RESET=0. The SOFT_RESET bit will self clear to '0' upon completion of reset. A software reset will:

1. Reset all active registers and status registers. Pending and read/write registers are not effected by Software Reset.

2. Force each clock domain to remain in reset for 64 local clock domain cycles and then begin operation.

Software Reset will not reset the analog sections of the RCLK PLL, FCLK PLL, SDDS, DDDS, DVI, or ADC. Software reset will not affect the IFM, Host, or OCM.

4.3 Analog to Digital Converter

The gm5060 chip has three ADC's (analog-to-digital converters), one for each color (red, green, and blue).

4.3.1 Pin Connection

The RGB signals are connected to the gm5060 as described below:

Table 10. Pin Connection for RGB Input with HSYNC/VSYNC

Pin Name	ADC Signal Name
Red+	Red
Red-	Terminate as illustrated in Figure 6
Green+	Green
Green-	Terminate as illustrated in Figure 6
Blue+	Blue
Blue-	Terminate as illustrated in Figure 6
HSYNC	Horizontal Sync (Terminate as illustrated in Figure 6)
VSYNC	Vertical Sync (Terminate as with HSYNC illustrated in Figure 6)

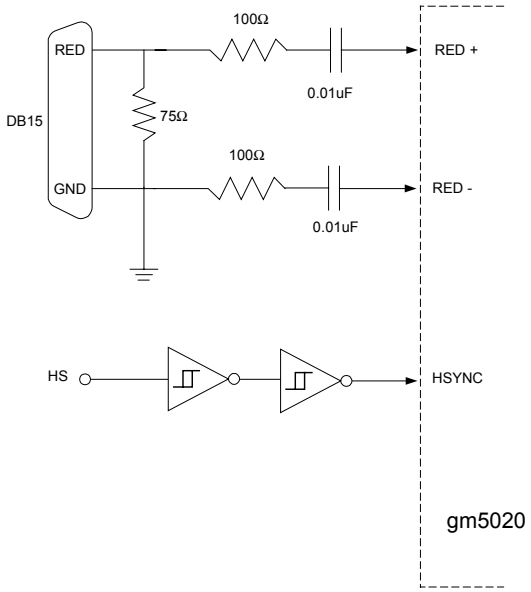


Figure 6. Example Signal Terminations

Please note that it is very important to follow the recommended layout guidelines for the circuit shown in Figure 6. These are described in "gm5060 Layout Guidelines" document number C5060-APN-01.

4.3.2 ADC Characteristics

The table below summarizes the characteristics of the ADC:

Table 11. ADC Characteristics

	MIN	TYP	MAX	NOTE
RGB Track & Hold Amplifiers				
Band Width		290MHz		
Settling Time to 1 %		5. 2ns		Full Scale Input = 0.75V, BW=290MHz (*)
Full Scale Adjust Range @ R,G,B Inputs	0.55 V		0.90 V	
Full Scale Adjust Sensitivity		+/- 1 LSB		Measured @ ADC Output (**)
Zero Scale Adjust Range				For a larger DC offset from an external video source, the AC coupling feature is used to remove the offset.
Zero Scale Adjust Sensitivity		+/- 1 LSB		Measured @ ADC Output
ADC + RGB Track & Hold Amplifiers				
Sampling Frequency (fs)	20 MHz		162MHz	
Differential Non-Linearity (DNL)		+/-0.5 LSB		fs = 135MHz
Integral Non-Linearity (INL)		+/- 1.5 LSB		fs =135 MHz
Channel to Channel Matching		+/- 0.5 LSB		
Effective Number of Bits (ENOB)		7 Bits		fin = 1 MHz, fs = 80 MHz Vin= -1 dB below full scale = 0.75V

(*) Guaranteed by design (**) Independent of full scale R,G,B input

The gm5060 ADC has a built in clamp circuit. By inserting series capacitors (about 10 nF), the DC offset of an external video source can be removed. The clamp pulse position and width are programmable.

4.3.3 Clock Recovery Circuit

The SDDS (Source Direct Digital Synthesis) clock recovery circuit generates the clock (max. 162MHz) used to sample analog RGB data (IPCLK or source clock). This circuit is locked to HSYNC of the incoming video signal.

Patented digital clock synthesis technology makes the gm5060 clock circuits resistant to temperature/voltage drift. Using DDS (Direct Digital Synthesis) technology, the clock recovery circuit can generate any IPCLK clock frequency within the range of 10MHz to 162MHz.

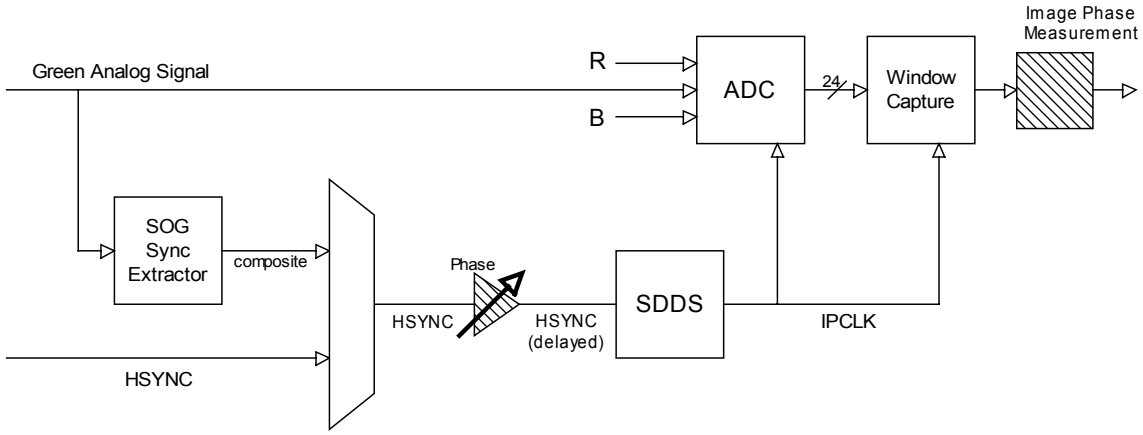


Figure 7. gm5060 Clock Recovery

4.3.4 Sampling Phase Adjustment

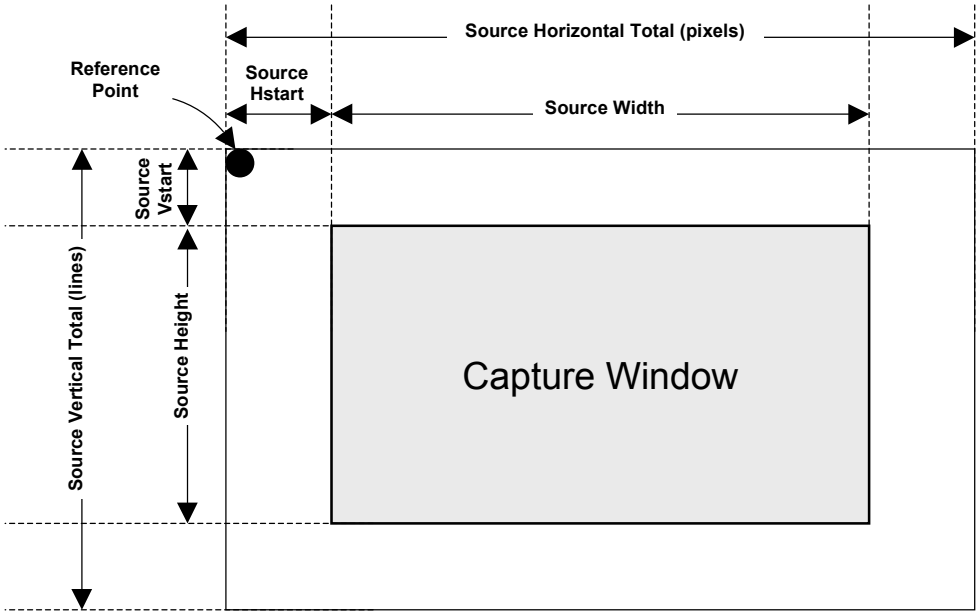
The ADC sampling phase is adjusted by delaying the HSYNC input to the DDS. The delay value is programmable. Using an external microcontroller routine, the accuracy of the sampling phase may be checked, and the result read from a register. This feature enables accurate auto-adjustment of the ADC sampling phase.

4.3.5 ADC Capture Window

Figure 8 below illustrates the capture window used for the ADC input. In the horizontal direction the capture window is defined in IPCLKs (equivalent to a pixel count). In the vertical direction it is defined in lines.

All the parameters beginning with “Source” are programmed gm5060 registers values. Note that the vertical total is solely determined by the input.

Figure 8. Capture Window



The Reference Point marks the leading edge of the first internal HSYNC following the leading edge of an internal VSYNC.

Horizontal parameters are defined in terms of single pixel increments relative to the internal horizontal sync. Vertical parameters are defined in terms of single line increments relative to the internal vertical sync.

For ADC interlaced inputs, the gm5060 may be programmed to automatically determine the field type (even or odd) from the VSYNC/HSYNC relative timing. See Input Format Measurement, Section 4.6.

4.3.5.1. Image Data Capture Interface

For ADC and DVI inputs, the input active window size is defined by programming register parameters in the Host Interface. Only pixels transferred into the device during the Input Active Window are used as source data for frame rate conversion and the scaling processor.

The maximum number of active pixels per line is 2047, the minimum is 50 pixels. The maximum number of active lines per input field is 2047, the minimum is 50 lines.

The maximum number of total pixels per line including blanking is 4096. The maximum number of total lines per input field including blanking is 2048.

4.3.5.2. HSYNC / VSYNC Delay For ADC Inputs

The active input region captured by the gm5060 is specified with respect to internal HSYNC and VSYNC. By default, internal syncs are equivalent to the HSYNC and VSYNC driven in at the selected input port, and forces the captured region to be bounded by HSYNC and VSYNC timing. The gm5060 provides an internal HSYNC and VSYNC delay capability for ADC inputs, which removes this limitation. By delaying the sync seen internally, the gm5060 can capture data which actually spans across the sync.

HSNYC and VSYNC delay may be used for image positioning. Taken to an extreme, the intentional movement of images across apparent HSYNC and VSYNC boundaries creates a horizontal and/or vertical wrap effect.

HSYNC is delayed by a programmed number of selected input clocks.

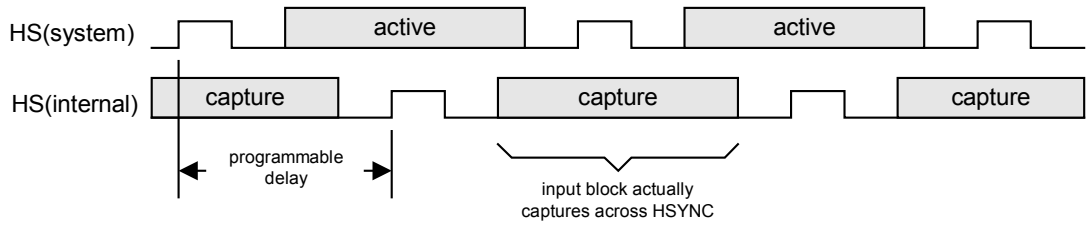


Figure 9. HSYNC Delay

Delayed horizontal sync may be used to solve a potential problem with VSYNC jitter with respect to HSYNC. VSYNC and HSYNC are generally driven active coincidentally, but with different paths to the gm5060 (HSYNC is often regenerated from a PLL). As a result, VSYNC may be seen earlier or later. Because VSYNC is used to reset the line counter and HSYNC is used to increment it, any difference in the relative position of HSYNC and VSYNC is seen on-screen as vertical jitter. By delaying the HSYNC a small amount, it can be ensured that VSYNC will always reset the line counter prior to it being incremented by the “first” HSYNC.

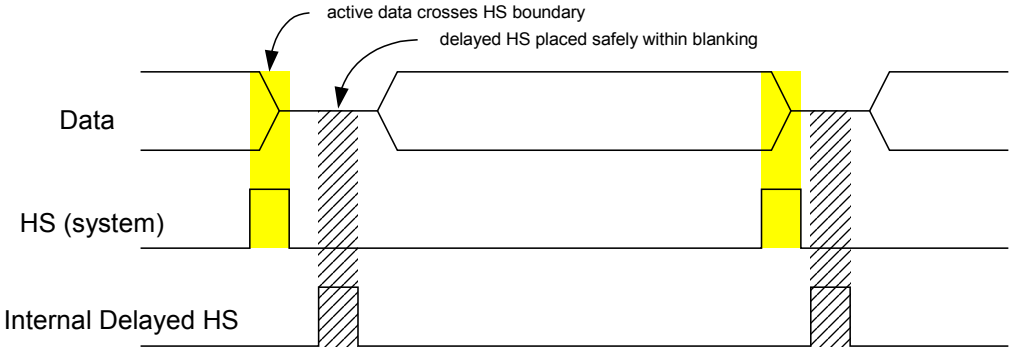


Figure 10. Active Data Crosses HSYNC Boundary

4.4 DVI Receiver Block

The Ultra-Reliable DVI™ receiver block of the gm5060 is compliant with DVI1.0 single link specifications. Digital Visual Interface (DVI) is a standard that uses Transition Minimized Differential Signalling protocol (TMDS). This block supports an input clock frequency ranging from 20 MHz to 165 MHz.

4.4.1 DVI Receiver Characteristics

Table 12 summarizes the characteristics of the four Receiver Pair inputs. Please note that it is very important to follow the recommended layout guidelines for these signals. These are described in "gm5060 Layout Guidelines" document number C5060-APN-01.

Table 12. DVI Receiver Characteristics

	MIN	TYP	MAX	NOTE
DC Characteristics				
Differential Input Voltage	150mV		1200mV	
Input Common Mode Voltage	AVDD –300m V		AVDD -37mV	
Behavior when Transmitter Disable	AVDD -10mV		AVDD +10mV	
AC Characteristics				
Input clock frequency	20 MHz		165MHz	
Input differential sensitivity (Peak-to-peak)	150mV			
Max differential input (peak-to-peak)			1560 mV	
Allowable Intra-Pair skew at Receiver			250 ps	Input clock = 165MHz
Allowable Inter-Pair skew at Receiver			4.0 ns	
Worst case differential input clock jitter tolerance			188 ps	

Through register programming, the receiver unit may be placed in one of three states:

- **Active:** The receiver block is fully on and running.
- **Standby:** Only the RXC channel remains active. Data and other control signals are not decoded.
- **Off:** The receiver block is powered down.

4.4.2 DVI Capture Window

There are two modes of operation available when defining the active window; DE-regeneration mode, and Auto mode.

When using the (default) DE-regeneration mode, DE (Display Enable), HSYNC and VSYNC are internally synthesized by examining the active regions of each line and compensating for possible source timing errors and/or embedded HSYNC / VSYNC jitter. DE-regeneration may be used to stabilize the display image. In this mode, the usual active window parameters must be programmed as with ADC inputs (see Section 4.3.5.).

The Auto mode allows the active window code embedded in the TMDS signal to define the active window automatically. In this mode, only the active width and active length parameters obtained by performing Input Format Measurement (IFM) need be programmed.

4.4.3 HDCP (High-Bandwidth Digital Content Protection System)

The HDCP system allows for authentication of a video receiver, decryption of encoded video data at the receiver, and renew-ability of that authentication during transmission. The gm5060 implements circuitry to allow for authentication and decryption of video as specified by the HDCP 1.0 protocol for DVI inputs.

For enhanced security, Genesis provides a means of storing and accessing the secret key given to individual monitor units in an encrypted format.

Further details of the protocol and theory of the system can be found in the *High-bandwidth Digital Content Protection System* specification, proposed by Intel Corporation.

4.5 ITU-R BT656 Video Input

The gm5060 accepts an 8-bit YCbCr 4:2:2 video data stream conforming to ITU-R BT656 (D-1) standards. This data, and the 27 MHz clock used to sample it, are provided by an external video decoder. The ITU-R BT656 format provides no separate horizontal or vertical sync (HSYNC, VSYNC) to the gm5060. The active window is not programmed, it is interpreted from codes embedded in the data stream.

4.5.1 ITU-R BT656 Capture Window

The input port extracts the active data, field type, and the horizontal and/or vertical blanking contained in the input stream. Note that Cb and Cr (shown in the figure below) correspond to U and V respectively. The extracted data is converted to 24-bit YCbCr 4:4:4 format.

Horizontal and vertical sync signals required for Input Lock Event timing are internally generated in this case.

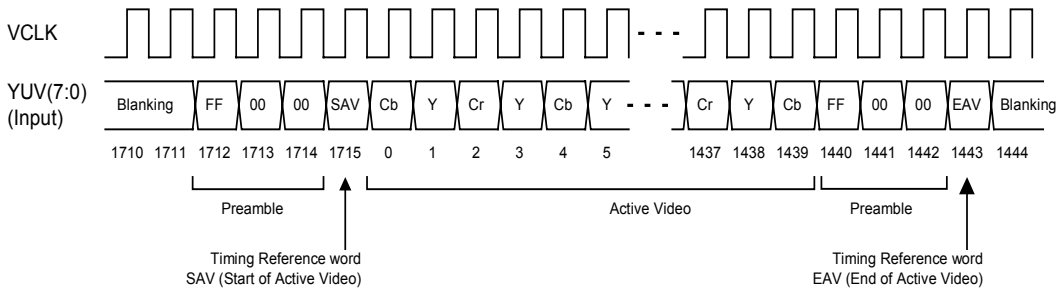


Figure 11. ITU-R BT656 Input

4.5.2 YCbCr Color Adjustment

The gm5060 provides color adjustment controls to modify the hue, saturation, contrast, and brightness of incoming YCbCr data. These controls are also available for the analog or digital RGB inputs and are described in Section 4.8 below.

4.5.3 YCbCr Input Clamping

YCbCr input to the gm5060 is always automatically clamped to restrict the input data to ITU-R BT601 levels:

Y Bottom clamping:	Y data < 16 is clamped to 16.
Y Top clamping:	Y data > 235 is clamped to 235.
CbCr Bottom clamping:	CbCr data < 16 is clamped to 16.
CbCr Top clamping:	CbCr data > 240 is clamped to 240.

4.6 Input Format Measurement

The gm5060 has an Input Format Measurement block (the IFM) providing the capability of measuring the horizontal and vertical timing parameters of the input video source. This information may be used to determine the video format and to detect a change in the input format. It is also capable of detecting the field type of interlaced formats.

The IFM features a host programmable reset, separate from the regular gm5060 soft reset. This reset disables the IFM, reducing power consumption. The IFM is capable of operating while gm5060 is running in power down mode.

Horizontal measurements are measured in terms of the selected IFM_CLK (either T_CLK or R_CLK/4), while vertical measurements are measured in terms of HSYNC pulses.

For an overview of the internally synthesized clocks, see Section 4.1.

4.6.1 Measurement

The IFM is able to measure the horizontal period and active high pulse width of the HSYNC signal, in terms of the selected clock period (either T_CLK or R_CLK/4.). Horizontal measurements are performed on only a single line per frame (or field). The line used is programmable. It is able to measure the vertical period and VSYNC pulse width in terms of rising edges of HSYNC. When using C-SYNC or sync-on-green input mode, these measurements use the internally synthesized HSYNC and VSYNC signals.

Once enabled, measurement begins on the rising VSYNC and is completed on the following rising VSYNC. Measurements are made on every field / frame until disabled.

4.6.2 Format Change Detection

The IFM is able to detect changes in the input format relative to the last measurement and then alert both the system and the embedded microprocessor. The microprocessor sets a measurement difference threshold separately for horizontal and vertical timing. If the current field / frame timing is different from the previously captured measurement by an amount exceeding this threshold, a status bit is set. An interrupt can also be programmed to occur.

4.6.3 Watchdog

The watchdog monitors input VSYNC / HSYNC. When any HSYNC period exceeds the programmed timing threshold (in terms of the selected IFM_CLK), a register bit is set. When any VSYNC period exceeds the programmed timing threshold (in terms HSYNC pulses), a second register bit is set. An interrupt can also be programmed to occur.

4.6.4 Internal Odd/Even Field Detection (For Interlaced Inputs to ADC Only)

The IFM has the ability to perform field decoding of interlaced inputs to the ADC. The user specifies start and end values to outline a "window" relative to HSYNC. If the VSYNC leading edge occurs within this window, the IFM signals the start of an ODD field. If the VSYNC leading edge occurs outside this window, an EVEN field is indicated (the interpretation of odd and even can be reversed). The window start and end points are selected from a predefined set of values.

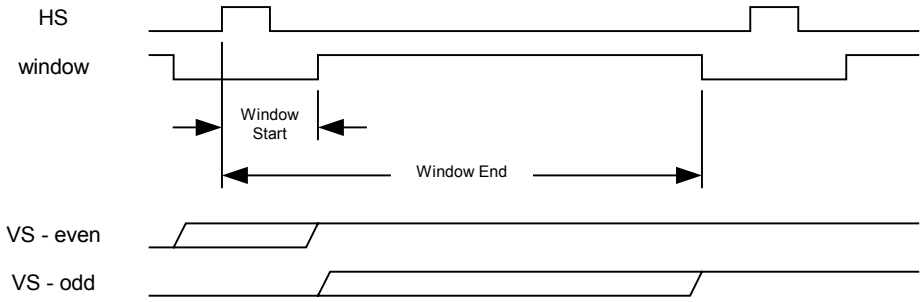


Figure 12. ODD/EVEN Field Detection

Note: ITU-R BT656 inputs do not require the above field detection feature; the field type is embedded in the data stream.

4.7 Input Pixel Measurement

The gm5060 provides a number of pixel measurement functions intended to assist in configuring system parameters such as pixel clock, SDDS sample clocks per line and phase setting, centering the image, or adjusting the contrast and brightness.

4.7.1 Image Phase Measurement

This function measures the sampling phase quality over a selected active window region. This feature may be used when programming the source DDS to select the proper phase setting. Please refer to the gm5060 Programming Guide for the optimized algorithm.

4.7.2 Image Boundary Detection

The gm5060 performs measurements to determine the image boundary. This information is used when programming the Active Window and centering the image.

4.7.3 Image Auto Balance

The gm5060 performs measurements on the input data that is used to adjust brightness and contrast.

4.8 Digital Color Controls

The gm5060 provides digital adjustment of the captured image data, allowing control over the image black level, contrast, brightness, hue and saturation.

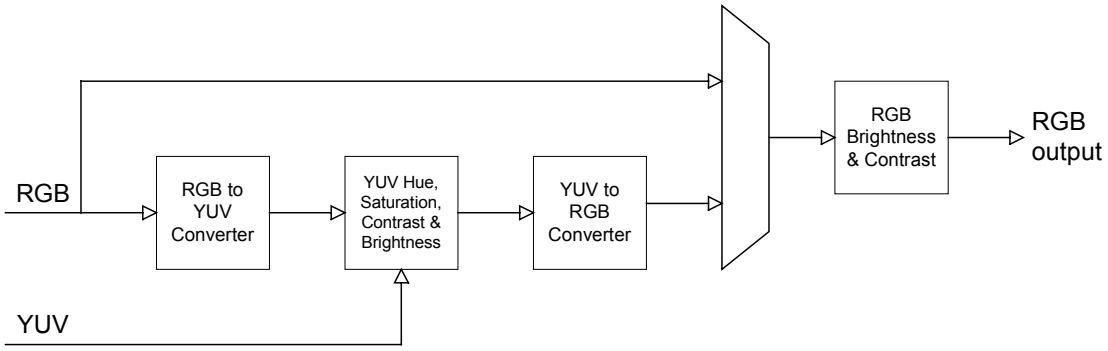


Figure 13. RGB and YUV Color Controls

4.8.1 YUV Hue / Saturation Controls

Color adjustment can be performed in the CbCr domain. These controls are available for RGB graphics input as well as for the CbCr video input. By default these functions are disabled, and color adjustment is not performed.

The functions are defined as follows:

Hue is a pure rotation of the CbCr (color) vector through an angle.

Saturation is a multiplicative factor applied to both Cb and Cr equally.

Contrast is a multiplicative factor applied to Y.

Brightness is an additive factor applied to Y.

The equations for these controls are as follows:

Y(out) = (Y - YBlackLevel) * Contrast + Brightness

Cb(out) = (Cb * cos(Hue) + Cr * sin(Hue)) * Saturation = Cb * Sat*cos(Hue) + Cr * Sat*sin(Hue)

Cr(out) = (Cr * cos(Hue) - Cb * sin(Hue)) * Saturation = Cr * Sat*cos(Hue) - Cb * Sat*sin(Hue)

Parameters are used directly in the associated multiplication and summation operations as programmed.

4.8.2 RGB Black Level / Contrast / Brightness

The black level adjustment is a subtractive stage, lowering each input pixel by a programmable value. This may be used to adjust the baseline black value of the input data.

R(out) = (R - RedBlackLevel) * RedContrast + RedBrightness
G(out) = (G - GreenBlackLevel) * GreenContrast + GreenBrightness
B(out) = (B - BlueBlackLevel) * BlueContrast + BlueBrightness

For example, if the lowest valued pixel expected to be encountered is 16, then 16 could be subtracted from all input pixels, making the pixel value 16 (or lower) black. The desired black level is maintained through the following contrast (multiplicative) stage.

The contrast adjustment increases or decreases the slope of the input / output function as shown below.

The brightness adjustment is a straight additive stage, increasing each pixel value by a programmed amount (saturating at 255).

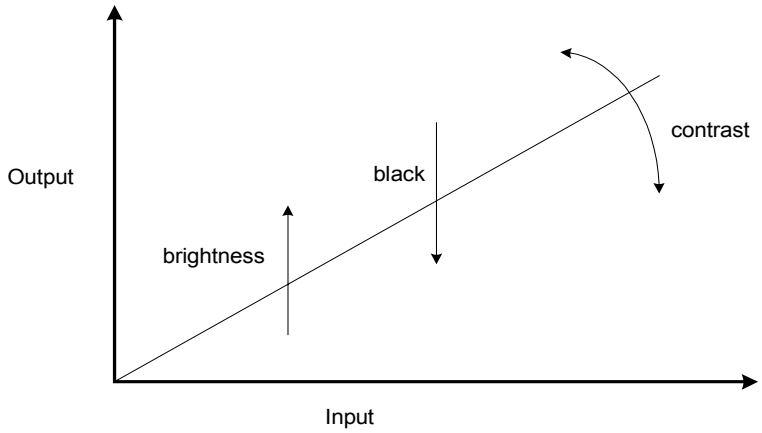


Figure 14. Black / Contrast / Brightness Transfer Function

4.8.3 RealColor™ Flesh tone Adjustment

The human eye is more sensitive to variations of flesh tones than other colors; for example, the user may not care if the color of grass is modified slightly during image capture and/or display. However, if skin tones are modified by even a small amount, it is unacceptable. The gm5060 features flesh tone adjustment capabilities. This feature is not based on lookup tables, but rather a manipulation of YUV-channel parameters. Flesh tone adjustment is available for all inputs.

4.9 Frame Store Interface

The external frame buffer provides the storage required for the frame rate conversion process and the integrated OSD.

4.9.1 Supported SDRAM Devices

The gm5060 operates seamlessly with commercially available SDRAM / SGRAM devices with operating frequencies of 143MHz.

gm5060 requires a 48-bit frame store data bus. The depth of the devices must be at least 1M words to support a full UXGA frame. Thus, for example three 1Mx16 devices can be used.

4.9.2 Adjustable Frame Store Interface Delays

The interface setup/hold times and propagation delay to the external DRAM can be adjusted. This is done by programming registers to achieve the timing values indicated in Section 5.2 (IO timing for FSC).

4.9.3 Frame Store Bandwidth Requirements

All data coming into and flowing out of the gm5060 frame rate converter must pass through the frame store interface. 143MHz operation is required to provide enough bandwidth to support the combined bandwidth demands of the input and output ports (UXGA 60Hz).

The FCLK PLL synthesizes the F_CLK to drive the FRC logic and Framestore Interface Clock. The FCLK PLL must be programmed such that: F_CLK < (DCLK x 3). This restriction should impose no functional limitations.

4.9.4 SDRAM Power On Sequence

SDRAM's have a power-on sequence that must be performed before they can be reliably accessed. This consists of a pre-charge cycle, 20 refresh cycles, and an MRS cycle. (The MRS – mode register setting – programs the DRAM for burst size, access latency, etc.) The gm5060 automatically performs this sequence.

4.9.5 SDRAM Power Down

SDRAM devices typically have a low power, non-operational mode. The gm5060 supports this feature by providing a power down sequence controller, enabled via a host-programmed register. This feature should always be used before disabling the framestore interface. A soft reset is required after bringing the SDRAMs back from power-down mode.

4.9.6 Pan and Crop Operations

When performing crop and/or pan operations, the frame store controller extracts a rectangular portion of the image in the frame store. This rectangular portion of the image may be displayed at native resolution, or scaled to the display resolution. Note that frame tear may result if a single frame buffer is used.

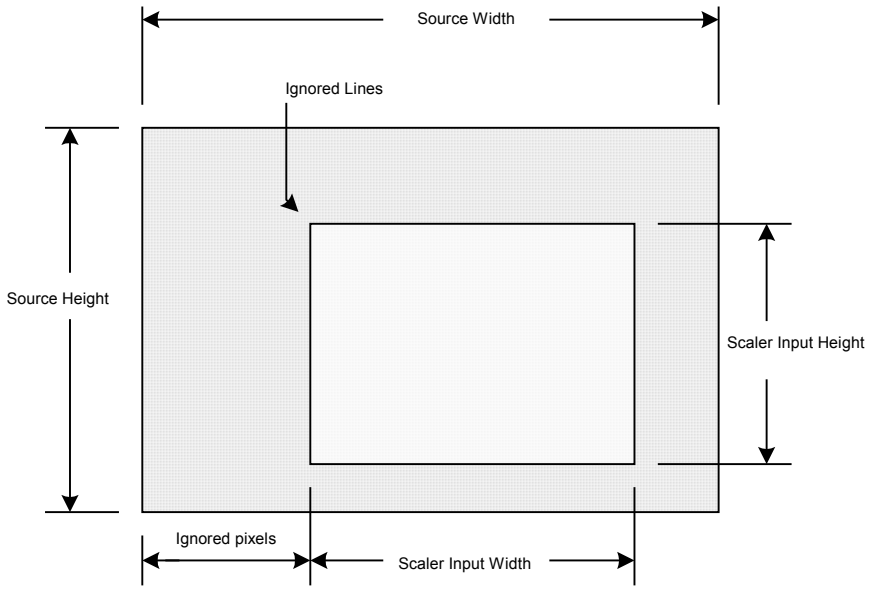


Figure 15. FRC Required Parameters

For the DVI input DS in DE-Regeneration mode and the ADC input, cropping can be performed by defining the active window (i.e., the 'Source' parameters in the diagram above) as a subset of the actual active data.

4.9.7 Freeze Frame

Freeze frame capability is made available by disabling the input capture during VBI. This does not disrupt the flow of data from the frame store. During freeze frame, adjusting the contrast and brightness controls will have no affect on the displayed image.

4.9.8 Interlaced Formats and De-interlacing

The FRC is able to accept vertically interlaced images. These images may be de-interlaced via a static mesh technique. Static mesh de-interlacing takes lines from an odd and even field pair and meshes them together, doubling the number of output lines. This technique is often used to de-interlace static graphics inputs.

4.9.9 Input Dithering / Compression

gm5060 provides the option to compress input pixel data from 24-bits to 18-bits before output to the frame store. This reduces the amount of frame store memory required to perform frame rate conversion with minimal impact to image quality. For example, when

dithering is used UXGA operation is supported with a 32-bit frame store data bus instead of a 48-bit frame store data bus (i.e. two SDRAM devices instead of three).

Both random and ordered dithering algorithms are available to compress input pixel data. These are the same as the output dithering algorithms as described in section 4.14.2. The input and output dithering functions of the 5060 can be programmed independently.

4.10 Display Synchronization

Refer to Section 4.1.1 for information regarding internal clock synthesis.

The gm5060 supports two display synchronization modes:

- **Frame Sync Mode:** The display frame rate is synchronized to the input frame or field rate. This mode is used in most cases – with or without frame rate conversion.
- **Free Run Mode:** No synchronization. This mode is used when there is no valid input timing, or for testing purposes.

4.10.1 Frame Sync Mode

Display synchronization is normally done using frame sync mode. In this mode, a 'lock event' (defined in the input timing) is used to determine the frame boundaries in the display timing (display lock load).

4.10.1.1. Input Lock Event and Display Lock Load

The programmable input Lock Event and display Lock Load parameters represent the mechanism for synchronization. The Lock Event represents a chosen pixel location within the input field or frame. When the Lock Event location is reached, the gm5060 Display Timing Generator is reloaded with the Lock Load values. Hence, the display timing is "corrected" or "aligned" to the proper location. This process automatically synchronizes the output to the input, and when properly programmed, prevents gm5060 internal buffer overflow / underflow when no frame buffer is present.

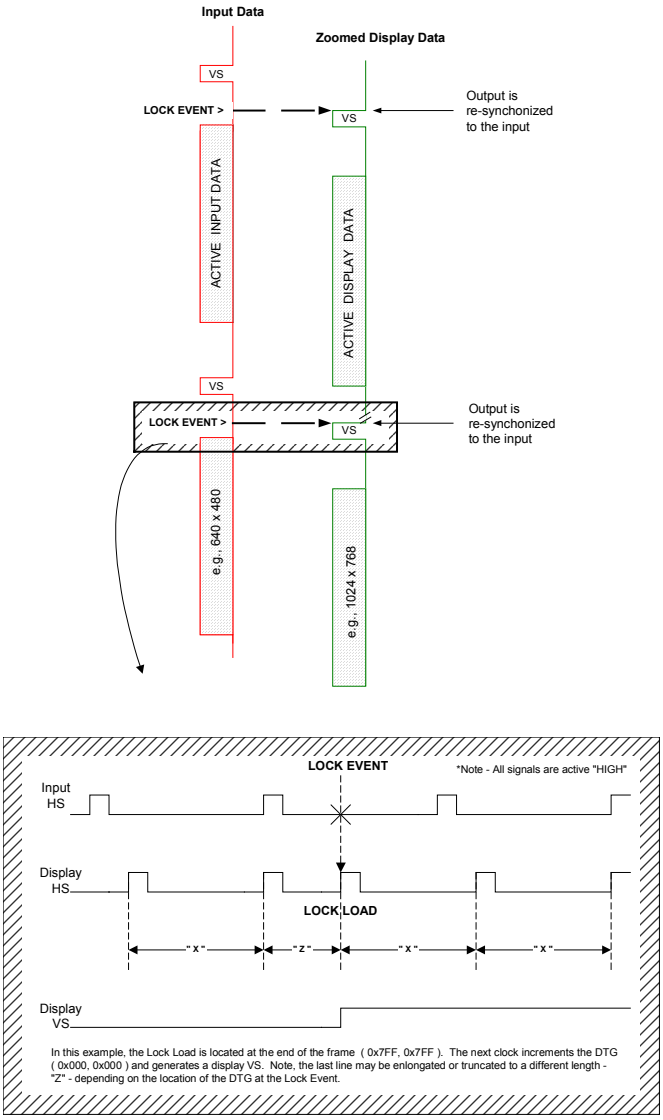


Figure 16. Lock Event Timing (Frame Sync Mode)

Because the Lock Event / lock load combination may cause a small aberration in the display timing (due to a longer or shorter display line period), the lock load is usually programmed to occur in the display vertical front porch. This allows display devices with PLLs the maximum time to recover before active video resumes.

4.10.2 Display Free-Run Mode

Free-run mode is used when there is no valid input timing (i.e. to display OSD messages or a splash screen). In free-run mode, the display timing is determined only by the values programmed into the display window and timing registers.

Input lock events do not cause display timing synchronization in free-run mode. Lock load programming is ignored in Free Run Mode.

4.10.3 Manual Synchronization

The gm5060 Display Timing Generator (DTG) may be forced to the lock load values by asserting the DFSYNCn pin. This may be thought of as a "manual" lock event. This manual mechanism is separately enabled via a host register bit.

4.11 Zoom Scaling

The gm5060 zoom scaler uses an advanced third generation adaptive scaling technique proprietary to Genesis Microchip Inc., and provides high quality scaling of real time video and graphics images. An input field/frame is scalable in both the vertical and horizontal dimensions.

Interlaced fields may be spatially de-interlaced by vertically scaling and repositioning the input fields to align with the output display's pixel map.

4.11.1 Adaptive Contrast Enhancement (ACE)

When zoom scaling, the gm5060 features the ability to sharpen text and graphics images. This is performed on an adaptive basis by detecting pulse and step functions on the input, and adjusting phase values accordingly.

4.11.2 Moiré Cancellation

The gamma curve can affect the energy distribution of pixels when scaled to different areas of the screen. This is an example of the Moiré effect. The gm5060 has hardware features to negate the Moiré effect, improving the scaling quality.

4.11.3 Variable Scaling

The gm5060 scaling filter can combine its advanced scaling with a pixel-replication type scaling function. This is useful for improving the sharpness and definition of graphics when scaling at high zoom factors (such as VGA to UXGA).

4.12 Bypass Options

The gm5060 has the capability to completely bypass internal processing. In this case, captured input signals and data are passed, with a small register latency, straight through to the display output.

The gm5060 is also able to bypass frame rate conversion. This allows the IC to operate without external SDRAM when the display frame timing is synchronized to the input timing.

The gm5060 is also able to bypass the zoom filter.

4.13 Gamma LUT

The gm5060 provides an 8 to 10-bit look up table (LUT) for each input color channel intended for Gamma correction. A 10-bit output results in an improved color depth control. The 10-bit output is then dithered down to 8 bits (or 6 bits) per channel at the display (see section 4.14.2 below). The LUT is user programmable to provide an arbitrary transfer function. Gamma correction occurs after the zoom/shrink scaling block.

The LUT has a host programmable bypass enable. If bypassed, the LUT does not require programming.

4.14 Display Output Interface

The Display Output Port provides data and control signals that permit the gm5060 to connect to a variety of flat panel or CRT devices. The output interface is configurable for 18 or 24-bit RGB pixels, either single or double pixel wide. All display data and timing signals are synchronous with the DCLK output clock.

4.14.1 Programming the Display Timing

Display timing signals provide timing information so the Display Port can be connected to an external display device. Based on values programmed in registers, the Display Output Port produces the horizontal sync (DHS), vertical sync (DVS), and data enable (DEN) control signals. The figure below provides the registers that define the output display timing.

Horizontal values are programmed in single pixel increments relative to the leading edge of the horizontal sync signal. Vertical values are programmed in line increments relative to the leading edge of the vertical sync signal.

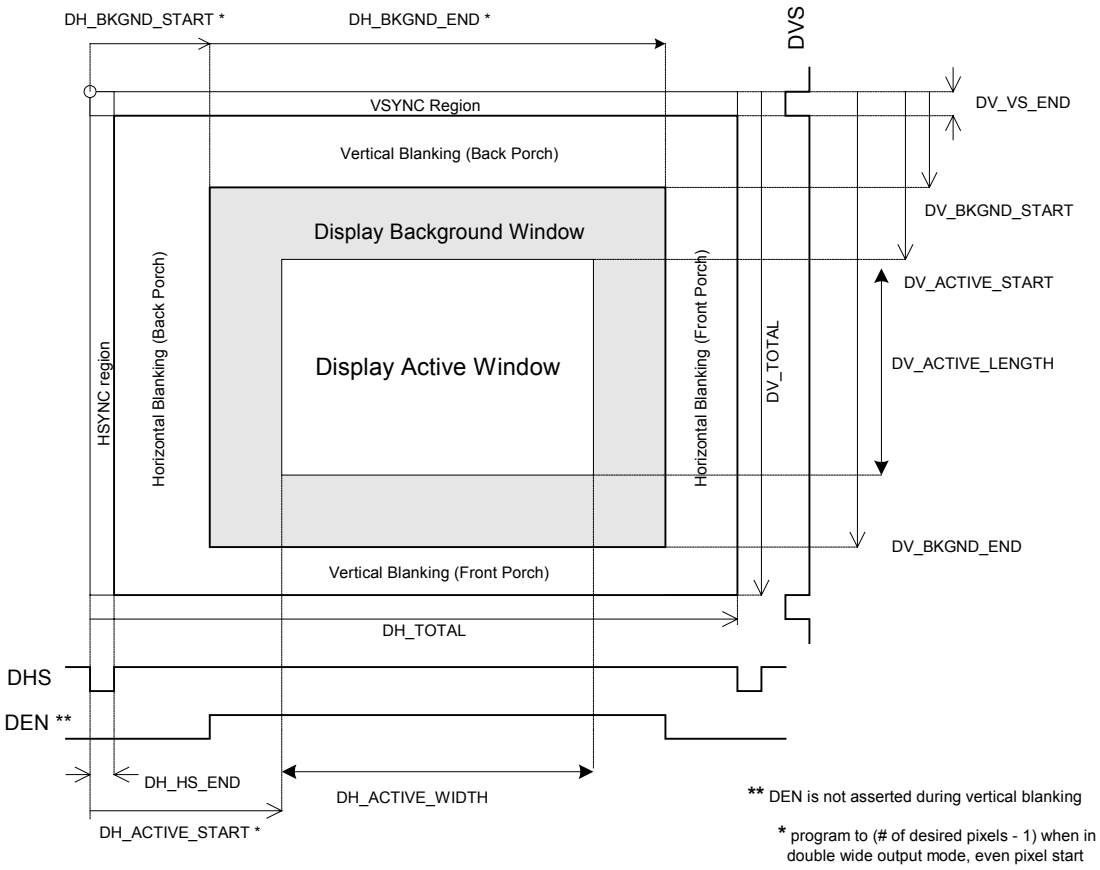


Figure 17. Display Windows and Timing

The double wide output will only support an even number of horizontal pixels.

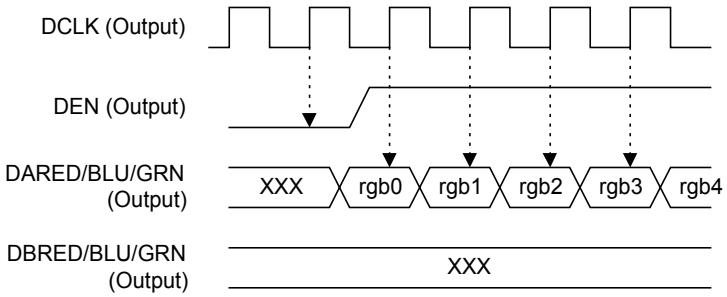


Figure 18. Single Pixel Width Display Data

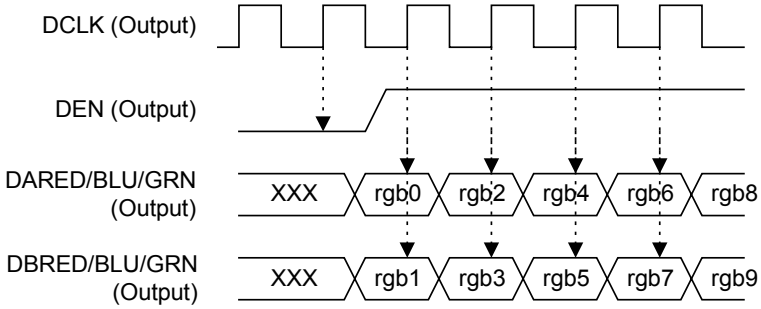


Figure 19. Double Pixel Wide Display Data

4.14.2 Output Dithering

The Gamma LUT outputs a 10-bit value for each color channel. This value is dithered down to either 8-bits for 24-bit per pixel panels, or 6-bits for 18-bit per pixel panels.

Dithering works by spreading the quantization error over neighboring pixels both spatially and temporally. The benefit of dithering is that the eye will tend to average neighboring pixels and a smooth image free of contours will be perceived.

All grey scales are available on the panel output whether using 8-bit panel (dithering from 10 to 8 bits per pixel) or using 6-bit panel (dithering from 10 down to 6 bits per pixel).

The input and output dithering functions of the gm5060 can be programmed independently to perform either random or ordered dithering. It is preferred to use ordered dithering at the output when driving a 6-bit panel.

4.15 OSD

The gm5060 OSD controller supports both character-mapped and bitmapped modes. A user programmable palette of 256 true colors (255 colors, + 1 transparent) is available.

In character mapped mode, a maximum of four colors per character are available.

In bitmapped mode, any pixel can be assigned any one of 16 user-defined true colors (15 colors plus one transparent). They are stored using 4-bits per pixel.

4.15.1 Character Mapped OSD

User-Definable Font Characteristics

Font Location	Font Type	Max Number of Font Colors	Max Character Size in Pixels (horz x vert)	Definable Characters per Table	Max Number of Font Tables
Resident (SRAM)	1-bit / pixel	1 + background	12 x 18	256	1
	1-bit / pixel 90^0 rotated	1+ background	16 x 12	192	1
	2-bits / pixel	3 + background	12 x 18	128< # <=256	1
External (SDRAM)	1-bit/pixel	1+ background	16 x 24	256	4 (+ 1 SRAM) *
	1-bit/pixel 90^0 rotated	1+ background	24 x 16	256	4 (+ 1 SRAM) *
	2-bits / pixel	3+ background	16 x 24	256	4 (+ 1 SRAM) *
	2-bits / pixel 90^0 rotated	3+ background	24 x 16	256	4 (+ 1 SRAM) *

* may be switched on a from row-by-row basis, must be same sized tables

Character Mapped OSD Features:

- Vertical and/or horizontal magnification of OSD image
- Maximum OSD size: 50 characters horizontal x 20 vertical with full character palette defined
- Background Windows Programming support to define an area in the OSD
- 16 levels of blending - suitable for fade effects
- Support for portrait and landscape OSDs (90^0 rotated fonts)
- Pre and post filter merge of OSD into main graphics channel
- Host update of OSD image while OSD is enabled

4.15.1.1. Character Map and On-chip Font Table

The content of the character map specifies the message generated by the OSD.

The character map for the OSD screen is defined by writing into an on-chip character map SRAM (3594 words by 24 bits) by means of the host interface. This on-chip memory is also

used to store programmable font characters, if the fonts are not stored in external frame buffer memory.

In memory, the character map is organized as an array of words, each defining the attributes (which character to display, the foreground and background colors, blinking) of one visible character on the screen (starting from upper left of the visible character array). In addition, there is a row attribute word that appears at the beginning of each row of the array in memory (so that the width of the array in memory is one higher than the width of the visible character array). The format of these words is described below.

Registers CHARMAP_XSZ and CHARMAP_YSZ are used to define the visible area of the OSD image. For example, Figure 20 shows a character map for which CHARMAP_XSZ =25 and CHARMAP_YSZ =10.

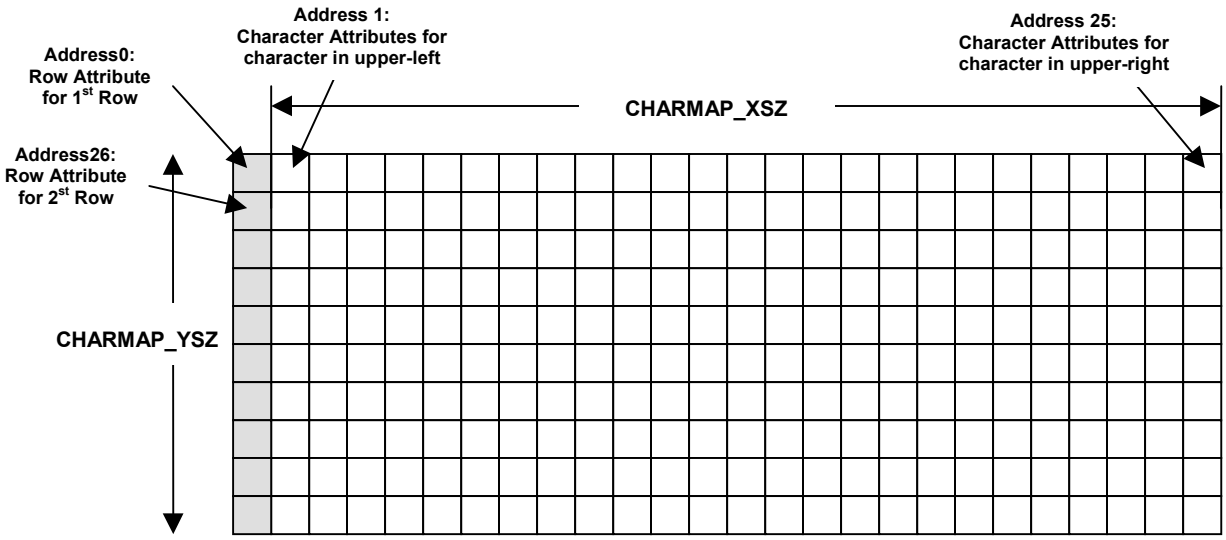


Figure 20. OSD Character Map

Note that when using on-chip programmable fonts, the character map and the font table share the same on-chip RAM. Thus, the size of the character map can be traded off against the number of fonts. For example, in landscape mode the OSD displayed character screen aspect ratio is programmable and is bounded by the equation:

CHARMAP_XSZ * CHARMAP_YSZ + CHARMAP_YSZ + 18 * ROUND(No. of fonts/2) =< 3594 (one bit per pixel)

(The ROUND operation would round 3.5 to 4.)

CHARMAP_XSZ * CHARMAP_YSZ + CHARMAP_YSZ + 18 * (No. of fonts) =< 3594 (two bits per pixel)

No such restrictions apply when fonts are stored in external frame buffer memory.

4.15.1.1.1. Row Attribute Word

The row attribute word at the start of each row in the character array has the following format:

- Bits 23 - 4: Unused
- Bit 3: This bit is used to indicate to the OSD how many colors an SDRAM font uses. If set, the SDRAM font is processed as a two color font. In this mode, the user should use only bit patterns "00" and "11" for describing a font pattern. This mode is useful when WINDOWS BACKGROUND MODE is disabled. SDRAM fonts are processed identically to 1-bit per pixel SRAM fonts – i.e., the SDRAM font will use seven bits (which are independent from the foreground bits) to determine background color.
- Bit 2 [SDRAM_FONT]: If set, characters in this OSD row are retrieved from SDRAM.
- Bit 1 - 0 [SDRAM_FONT_TBL[1:0]]: If SDRAM resident fonts sets are being used, characters in this OSD row use the font table specified by this register.

4.15.1.1.2. Character Attribute Word (One bit-per-pixel mode)

In one bit-per-pixel mode, each character attribute word defines the character index, the background color, the foreground color, and the blink status for a visible character.

- Bits 7 - 0: Character Index
- Bits 23 - 16: Bits 7-0 of foreground color (specified by a "1" in the font map)
- Bits 15 - 9: Bits 7-1 of background color (specified by a "0" in the font map) Note that bit 0 of the background color is always "0". Also note that the background color may be defined using the windowing method as described in Section 4.15.1.3 below. In this case these bits are unused.
- Bit 8: A "1" indicates that this character blinks when blinking is enabled.

When only two bit patterns are used to describe an **SDRAM** font ("11" and "00"), bit 3 of the Character Attribute Row can be set, allowing the background color for fonts to be determined by character index bits 7-1. This feature allows a user who is only using two colors in an SDRAM font (11, 00) to choose the background color independent of the foreground color. The foreground and background colors in this case are chosen the same way as a 1-bit per pixel SRAM font; two bits are used to describe two colors because SDRAM fonts must ALWAYS be defined as 2-bits per pixel.
Also note that the background color may be defined using the windowing method as described in Section 4.15.1.3 below. In this case these bits are unused.

4.15.1.1.3. Character Attribute Word (Two bit-per-pixel mode)

In two bit-per-pixel mode, each character attribute word defines the character index, the background color, three foreground colors, and the blink status for a visible character.

- Bits 7 - 0: Character Index
- Bits 23 - 20: Bits 7-4 of foreground colors
- Bits 19 - 17: Bits 3-0 of foreground color 3 (pixel bit pattern "11")

- Bits 15 - 12: Bits 3-0 of foreground color 2 (pixel bit pattern "10")
- Bits 11 - 9: Bits 3-1 of foreground color 1 (pixel bit pattern "01")
  Note that bit 0 of foreground color 1 is always "0"
- Bit 8: A "1" indicates that this character blinks when blinking is enabled.

Note that the background color (pixel bit pattern "00") can be defined using the window method as described in section in Section 4.15.1.3 below; alternatively it can be the same as foreground color 2.

4.15.1.1.4. Character Map For Rotated OSD

When defining the color and character maps for a rotated OSD image, define the maps from the bottom left hand corner. Note the difference in defining the CHARMAP_XSZ and CHARMAP_YSZ registers for rotated OSD images when compared to non-rotated images.

4.15.1.2. Font Table

Font tables may be defined either in on-chip RAM (same RAM that character map is stored in) or in an external frame buffer. Either way, fonts may be defined using one bit-per-pixel (one foreground color and one background color) or two bits-per-pixel (three foreground colors and one background color).

4.15.1.2.1. One Bit Per Pixel On-chip Programmable SRAM Based Fonts

The gm5060 OSD controller has SRAM available to store up to 256, one bit per pixel character mapped fonts. Figure 21 shows the font definition for a character in the on chip SRAM font table, using one bit per pixel protocol. Each font definition is up to 12 pixels horizontal by 18 pixels vertical.

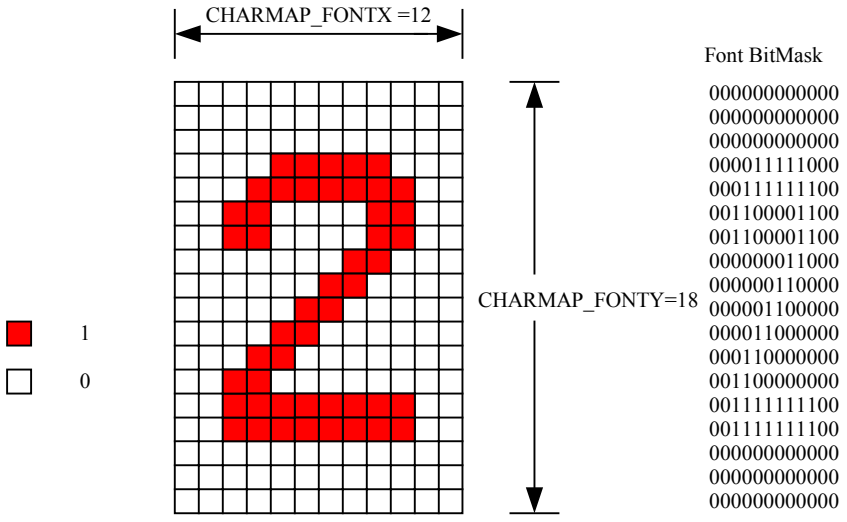


Figure 21. Non-Rotated SRAM Resident Font

Pixels mapped to a "1" are foreground pixels. The foreground index value (FG) programmed into the color index table is then used as the index into the OSD CLUT. Pixels mapped to a "0" are background pixels. The background color for the character is determined by the window region or the background color index value (BG) programmed into the color index table.

Figure 22 shows the font definition for a rotated character in the font SRAM.

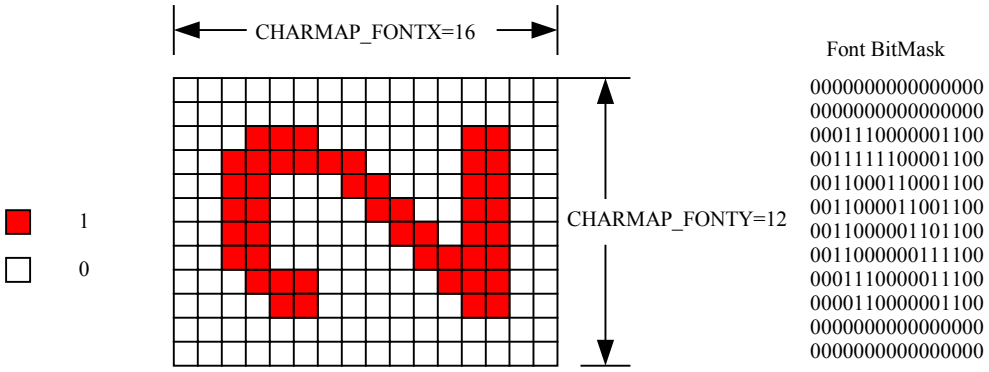


Figure 22. Rotated SRAM Resident Font

4.15.1.2.2. Two Bits Per Pixel SRAM Resident Fonts

Typically there is storage space for 128 or more two bit per pixel SRAM resident fonts.

Two bit per pixel SRAM based fonts support up to three foreground colors per character and one background color per character. Figure 23 shows a two bit per pixel SRAM based font definition for a character.

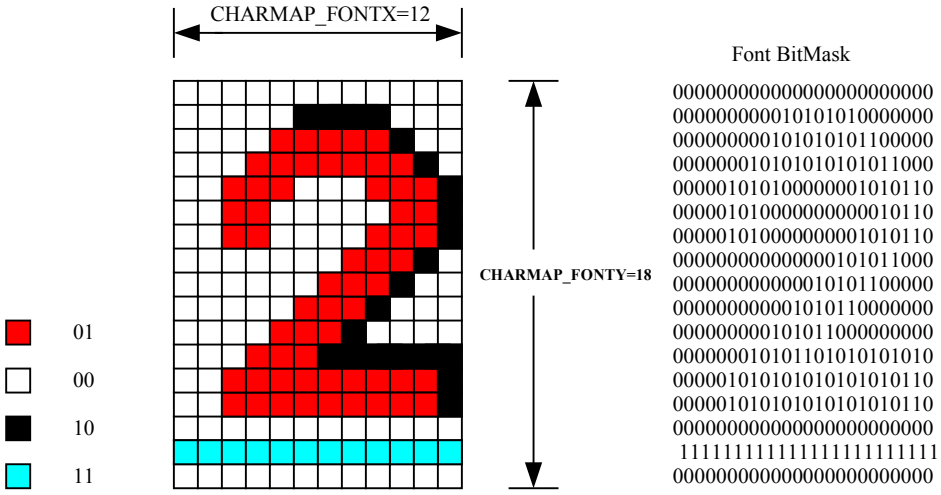


Figure 23. User Define-able SRAM Resident Font

When using 2-bits per pixel SRAM resident fonts, the designer defines each pixel using a 2-bit code. Bit codes “11”, “10”, and “01” are mapped to foreground colors 3, 2 and 1 respectively. Bit code “00” is mapped to the background color using the window region background color or using foreground color 2.

4.15.1.2.3. Frame Buffer Resident Fonts

External frame buffer resident character font tables are supported. The frame buffer interface supplies addresses to fetch character font scan lines via the frame buffer interface port.

The frame buffer based font table supports characters with programmable pixel map organization up to a maximum size of 16 pixels horizontally by 24 pixels vertically. The horizontal character width must be an even number of pixels.

When an external frame buffer is used to store fonts, each character row in the OSD may be programmed to index into one of four user defined font tables. This provides up to 1024 characters in a single character mapped OSD image and is intended to allow multi-language OSD support.

Frame buffer based fonts support up to three foreground colors per character and one background color per character, similar to using two bits per pixel mode using SRAM resident fonts as described 4.15.1.2.2 above.

4.15.1.3. Background Color of Characters

There are two modes of programming the background color of characters within an OSD image. The OSD controller may be programmed such that it is in Background Windows Mode. This mode of operation allows up to four user programmable background windows to be displayed simultaneously. Each background window has a color attribute, in addition to column and row start and stop parameters. Background Windows Mode enables OSD images to be quickly designed with little programming.

With Background Windows Mode disabled, the background color of characters may be programmed such that each character has a unique background color.

4.15.1.3.1. Background Windows Mode Enabled

Up to four background windows are supported. The windows control the background color. Windows may overlap and have a priority sequence. Window sizes are programmable and are defined by host registers. Transparency is achieved by setting the background color for a window to “00”.

4.15.1.3.2. Background Windows Mode Disabled

When background windows are disabled, the background color for each character in the OSD image is user-programmable. In one bit per pixel mode each character has one foreground and one background color defined. In two bit per pixel mode each character has three foreground colors defined, and the background color is the same as foreground color 2.

4.15.1.4. Character Blinking

Character blinking is enabled by setting bit 8 of the character attribute. A global host parameter is set to then make the desired characters blink. Blink frequency and duty cycle is programmable through host registers. When a character is blinking, foreground colors periodically revert to the background color of the character. Blinking frequency is proportional to the display frame rate.

4.15.1.5. Character Spacing

The characters within a character mapped OSD image may have additional spacing added between each character definition. See the register specification for allowed spacing. When spacing is added to a character, background color pixels are inserted around the character to achieve the desired spacing. Character spacing is added before horizontal and vertical stretching causing spaces to be stretched along with the character.

4.15.2 Bitmapped OSD

The OSD block supports bitmapped images stored in SDRAM.

The bitmap is loaded into the external frame buffer by the host. The OSD block fetches the bitmap from the frame buffer and uses the data to define the displayed pixel colors on a pixel by pixel basis. Pixels are represented using either 4-bits per pixel (16 simultaneous colors), 2-bits per pixel (4 colors) or 1-bit per pixel.

The maximum bitmapped image size is 512 horizontal x 512 pixels vertical.

4.15.3 Color Look-up Table (LUT)

Each pixel of a displayed character is resolved to an 8-bit color code. This selected color code is then transformed to a 24-bit value using a 256 x 24-bit look up table. Color index value “00” is reserved for transparent OSD pixels. The LUT is stored in an on-chip SRAM and is loaded via the Host interface.

4.15.4 Multiple OSD Windows

Up to three OSDs may appear on the screen at any given time: two bitmapped OSDs and one character-mapped OSD.

4.15.5 OSD Stretch

The OSD image can be stretched horizontally and/or vertically by a factor of two, three, or four. Pixel and line replication is used to stretch the image.

4.15.6 Blending

16 levels of blending are supported for the character-mapped and bitmapped images. One host register controls the blend levels for pixels with LUT values of 128 and greater, while another host register controls the blend levels for pixels with LUT values of 127 and lower. OSD color LUT value 0 is reserved for transparency and is unaffected by the blend attribute.

Blend levels for binary codes “1111” through “0000” are 6.25%, 12.5%, 18.75%, 25%, 31.25%, 37.5%, 43.75%, 50%, 56.25%, 62.5%, 68.75%, 75%, 81.25%, 87.5%, 93.75%, 100%.

4.15.7 OSD Merge

The OSD data can be merged before or after the scaling engine. Character mapped image would typically be merged after the scaling engine. Merge location is common for all OSD images (bitmapped and character mapped) at any given time.

4.16 On-Chip Microprocessor

The gm5060 incorporates an embedded microprocessor, or OCM (On-Chip Microprocessor). This processor is intended to simplify the gm5060 system software implementation by providing embedded macro functions such as OSD menu configurations. It is not intended to replace the system microprocessor.

An arbitration mechanism handles the register access requests from the OCM and the system micro.

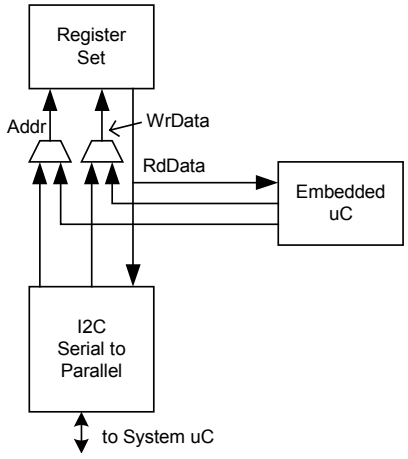


Figure 24. System µC - Embedded µC Communication

4.16.1 Bootstrap Configuration

During reset, the frame store address lines (FSADDR [13:0]) are configured as inputs. On the negating edge of RESETn, the value on the address lines is captured. This value is readable by the system (or embedded) micro. Seven of the bootstrap bits have a fixed, hard-wired function. The value on FSADDR [6:0] specifies the 2-wire host protocol device address.

Table 13. Bootstrap Signals

Name	I/O	Shared With	Description
ADDR(6:0)	I	FSADDR(6:0)	If using 2-wire protocol, this determines the chip address.
USER_BITS(4:0)	I	FSADDR(4:0)	If using 6-wire nibble protocol, these settings are available for reading from a status register but are otherwise unused by the IC.
Reserved	I	FSADDR5	If using 6-wire nibble protocol, bootstrap program this bit to 0.
Reserved	I	FSADDR6	Set to '0'
HOST_PROTOCOL	I	FSADDR7	Selects 6-wire nibble protocol (HOST_PROTOCOL=1) or 2-wire protocol (HOST_PROTOCOL=0).
USER_BITS(7:5)	I	FSADDR(10:8)	These settings are available for reading from a status register but are otherwise unused by the IC
OCM_START	I	FSADDR11	Set to '0'
OCM_EXTCLK	I	FSADDR12	Select EXTCLK as Host Interface and MCU clock. 0 = As selected with OCM_CLK bootstrap. 1 = Override OCM_CLK selection with EXTCLK.
OCM_CLK	I	FSADDR13	Select over-sampling clock source for Host Interface and OCM. 0 = RCLK PLL / 2 [default ~ 100MHz], 1 = TCLK.

4.17 Host Interface

The host microcontroller interface of the gm5060 has two modes of operation: 2-Wire compatible mode, and a 6-wire (nibble wide) interface mode, selected by bootstrapping options.

- The 2-wire compatible connection that consists of a serial clock (SCL) and bi-directional serial data line (SDA). The bus master drives the SCL clock and either the master or slave may drive the SDA line. The gm5060 operates as a slave on the interface. The SDA and SCL lines are shared with the 6-wire communication lines HFSn and HCLK respectively, as illustrated below.
- The 6-wire interface connection features four data lines HDATA[3:0], one clock (HCLK), and one chip select / framing signal (HFSn). Four bits are transferred on each clock edge.

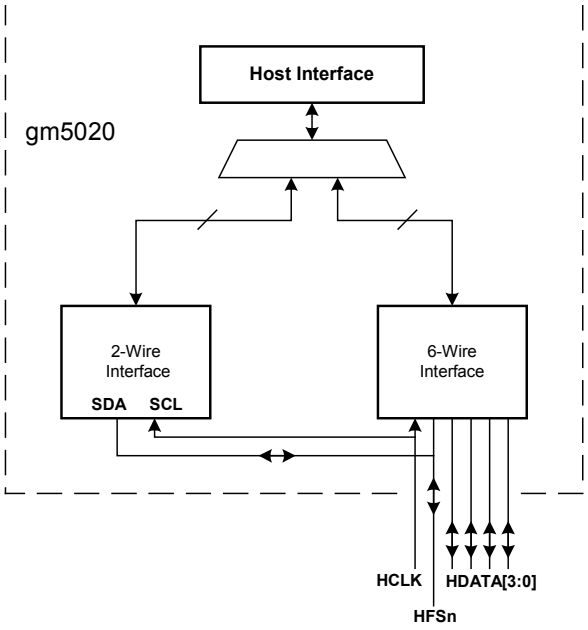


Figure 25. 2-Wire / 6-Wire External Interface

4.17.1 2-wire Communication

The 2-Wire compatible protocol features only a serial clock (SCL) and a bi-directional serial data line (SDA). The bus master, typically a controller, is responsible for generating the SCL clock. Depending on whether the gm5060 is the receiver or sender, it either reads in or sends out data. The gm5060 operates as a slave device when using the 2-wire protocol bus.

4.17.1.1. Mode Configuration

The 2-wire protocol requires each device be addressable by a 7-bit identification number. The gm5060 can be initialized on power-up to 2-wire mode by asserting bootstrap pins (HOST_PROTOCOL=1 and device identification number on ADDR[6:0]) on the rising edge of RESETn. This provides flexibility in system configuration with multiple devices that may have the same address.

4.17.1.2. Serial Protocol

A data transfer consists of a stream of serially transmitted bytes formatted as shown in the figure below. A transfer is initiated (START) by a high-to-low transition on SDA while SCL is held high. A transfer is terminated by a STOP (a low-to-high transition on SDA while SCL is held high) or by a START (to begin another transfer). The SDA signal must be stable when SCL is high, it may only change when SCL is low (to avoid being misinterpreted as START or STOP).

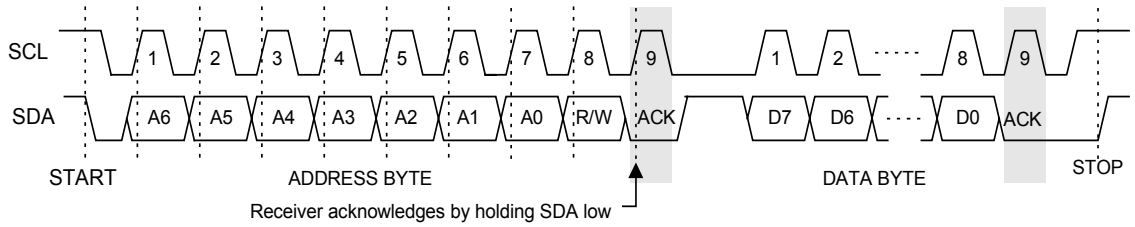


Figure 26. 2-wire Protocol Data Transfer

Each transaction on the SDA is in integer multiples of bytes (8 bits). The number of bytes that can be transmitted per transfer is unrestricted. Each byte is transmitted with the most significant bit (MSB) first. After the eight data bits, the master releases the SDA line and the receiver asserts the SDA line low to acknowledge receipt of the data. The master device generates the SCL pulse during the acknowledge cycle. The addressed receiver is obliged to acknowledge each byte that has been received.

4.17.1.3. Command Format

The serial interface operates in slave mode only. The communication protocol consists of a device select address byte, an instruction byte, a device register address and/or one or more data bytes.

The first byte of each transfer consists of a 7-bit device address that identifies the slave device for the transfer. The 8th bit (LSB) of the device address byte indicates a read or write operation and also determines the direction for successive data byte transfer. This bit is set low or high, respectively, to indicate a write or read transfer.

The second byte of each transfer contains an instruction byte indicating the type of operation to be performed by the gm5060. The table below lists the instruction codes and the type of transfer operation. The content of bytes that follow the instruction byte will vary depending on the instruction chosen. By utilizing these modes effectively, registers can be quickly configured.

'P' in Table 14 below represents the LSB in the instruction code, and is the 9th addressing bit of the internal register address (Register Address [8]). It is set to '0' to select a starting register address of less than 256, or '1' to select an address greater than 255. This bit of the address increments in Address Increment transfers. The unused bits in the instruction byte should be set to '1'.

Table 14. Instruction Byte Map

Value 7 6 5 4 3 2 1 0	Operation Mode	Description
0 0 0 1 x x x P	Write Address Increment	Allows the user to write a single or multiple bytes to a specified starting address location. A Macro operation will cause the internal address pointer to increment after each byte transmission. Termination of the transfer will cause the address pointer to increment to the next address location.
0 0 1 0 x x x P	Write Address No Increment (for table loading)	
1 0 0 1 x x x P	Read Address Increment	Allows the user to read multiple bytes from a specified starting address location. A Macro operation will cause the internal address pointer to increment after each read byte. Termination of the transfer will cause the address pointer to increment to the next address location.
1 0 1 0 x x x P	Read Address No Increment (for table reading)	
0 0 1 1 x x x P 0 1 0 0 x x x P 1 0 0 0 x x x P 1 0 1 1 x x x P 1 1 0 0 x x x P	Reserved	
0 0 0 0 x x x P 0 1 0 1 x x x P 0 1 1 0 x x x P 0 1 1 1 x x x P 1 1 0 1 x x x P 1 1 1 0 x x x P 1 1 1 1 x x x P	Spare	No operation will be performed

4.17.1.3.1. Write Address Increment and Write Address No Increment

The Write Address Increment and the Write Address No Increment mode of operation allows one or multiple registers to be programmed with only sending one start address. In Write Address Increment, the address pointer is automatically incremented after each byte has been sent and written. The transmission data stream for this mode is illustrated below. The highlighted sections of the waveform represent moments when the transmitting device must release the SDA line and wait for an acknowledgement from the gm5060 (the slave receiver).

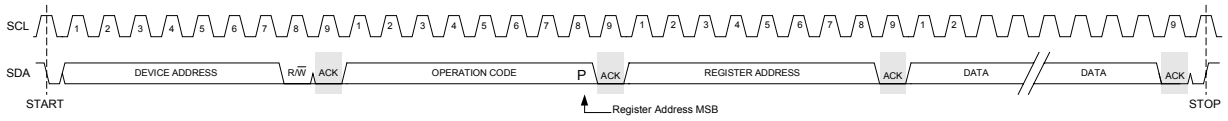


Figure 27. Write Address Increment and Write Address No Inc (0x10 & 0x20)

4.17.1.3.2. Read Address Increment and Read Address No Increment

The Read Address Increment and the Read Address No Increment mode of operation allows one or multiple registers to be read with only sending one start address. In Address Read Increment, the address pointer is automatically incremented after each byte has been sent.

The transmission protocol for this mode is illustrated below. The highlighted sections of the waveform represent moments when the transmitting device must release the SDA line and waits for an acknowledgement from the master receiver.

Note that on the last byte read, no acknowledgement is issued to terminate the transfer.

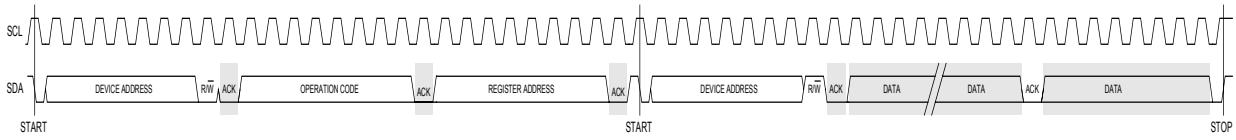


Figure 28. Read Address Increment and Read Address No Inc (0x90 & 0xA0)

4.17.1.4. Read Transfer

It is also possible to perform a read as illustrated below. The internal address will only increment after each byte if the previous operation code was an incremented operation, i.e., the previous operation state is retained.

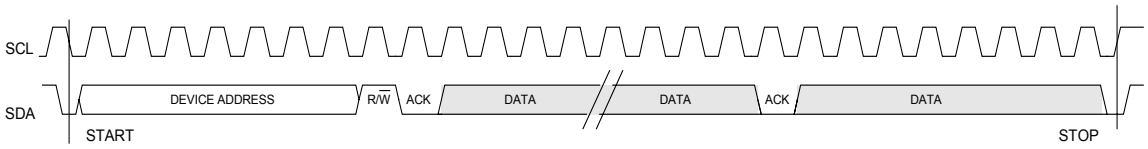


Figure 29. Direct Read

4.17.2 6-Wire Communication Protocol

The 6-Wire interface consists of a device select signal (HFSn), a serial clock (HCLK), and four bi-directional data signals (HDATA[3:0]). Selection of this communication protocol provides the maximum transfer rate.

4.17.2.1. 6-Wire Mode Configuration

Protocol selection is performed during power-up at the rising edge of RESETn input. The 6-Wire protocol is selected via a bootstrap configuration.

The interface can operate at a maximum rate of 1/20th the selected internal OCM_CLK. The OCM_CLK typically operates at 100MHz, thus providing a maximum HCLK frequency of 5 MHz. This would equate to a potential 20 Mbit/second data transfer rate.

4.17.2.2. 6-Wire Control Signals

4.17.2.2.1. HFSn

The host framing signal is a master enable for the host interface. If HFSn is de-asserted (high), then all activity on the remaining signals shall be ignored. If the HFSn is asserted (low), the host interface responds to bus activity. The assertion of HFSn marks the START condition upon which the host interface is initialized, and the de-assertion of HFSn marks the end condition upon which all pending operations are cleared.

4.17.2.2.2. HCLK

HCLK is the clock by which data is loaded into, or read from the host interface. HCLK is active low; the gm5060 captures on the falling edge and transmits on the rising edge of HCLK.

4.17.2.2.3. HDATA[3:0]

HDATA[3:0] contains the data that is written to, and read from the host interface. This is a bi-directional data bus, and thus must be tri-stated by the master device whenever reading from the gm5060. Each line on this bi-directional bus requires a pull-up resistor.

The serial interface port operates as a slave device and is uniquely addressed by the HFSn input. The HFSn signal must be de-asserted during a Hardware Reset (i.e. when RESETn is asserted). A master device initiates a data transfer by asserting HFSn (START) and terminated by de-asserting HFSn (STOP). HCLK must be inactive for no less than ½ HCLK cycle before HFSn is asserted and after HFSn is de-asserting. The HFSn signal must be de-asserted for a minimum of a half cycle between transfers.

A data transfer consists of a number of sequentially transmitted bytes, sent four bits at a time on HDATA[3:0], formatted as shown in the figures below. Bytes are transferred on the HDATA lines with the most significant bit (MSB) first. The number of bytes that can be transmitted per transfer is unrestricted. The protocol supports static operation, and can be halted or started by controlling the HCLK at any time during a transfer.

4.17.2.3. Transfer Modes

The data transfers using the 6-Wire protocol consist of an instruction byte indicating the type of operation to be performed by the gm5060. Table 14 above lists the instruction codes and the type of transfer operation. The content of bytes that follow the instruction byte will vary depending on the instruction chosen.. All operation modes and instruction codes are identical to those of the 2-Wire protocol. See Section 4.17.1.3. No data acknowledge is implemented in the 6-Wire protocol. It is the responsibility of the external controller to verify, via transfer operations, that data is received and transmitted correctly.

The data transfer formats following the instruction byte are identical with the following exceptions:

- The HFSn signal is used for direct addressing, therefore no device address byte is sent. The first byte instead contains the instruction byte indicating the type of operation to be performed. Figure 30 shows and equivalent Write Address Increment operation. ('Increment' Write implies that the register address is incremented after each data byte is read or written, allowing the user to program a block of sequential addresses, stating only a single starting address.)

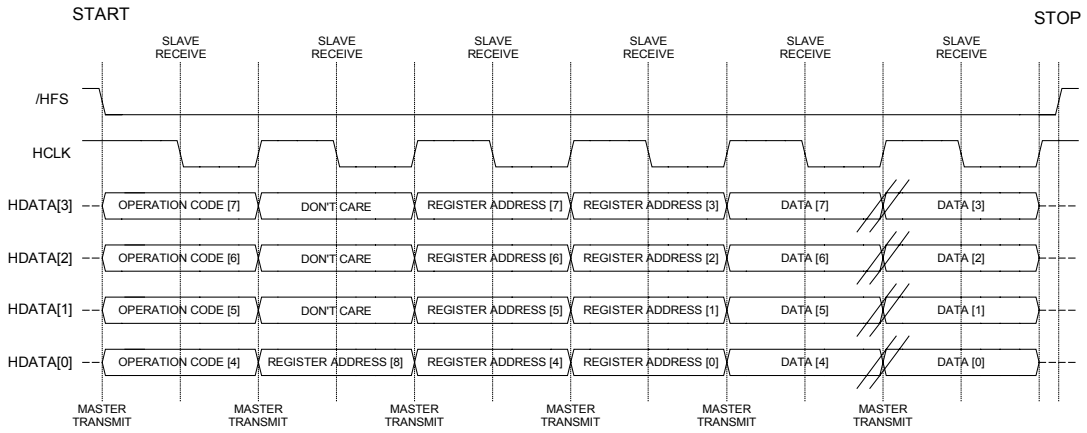


Figure 30. 6-Wire Write Operations (0x1*x* & 0x2*x*)

- Read operations can be performed in one transfer without a re-start cycle and re-send of the device address before data is sent from the slave device. Data is sent in the byte immediately following the instruction or address. Figure 31 shows the equivalent operation for the Read Address Increment transfer.

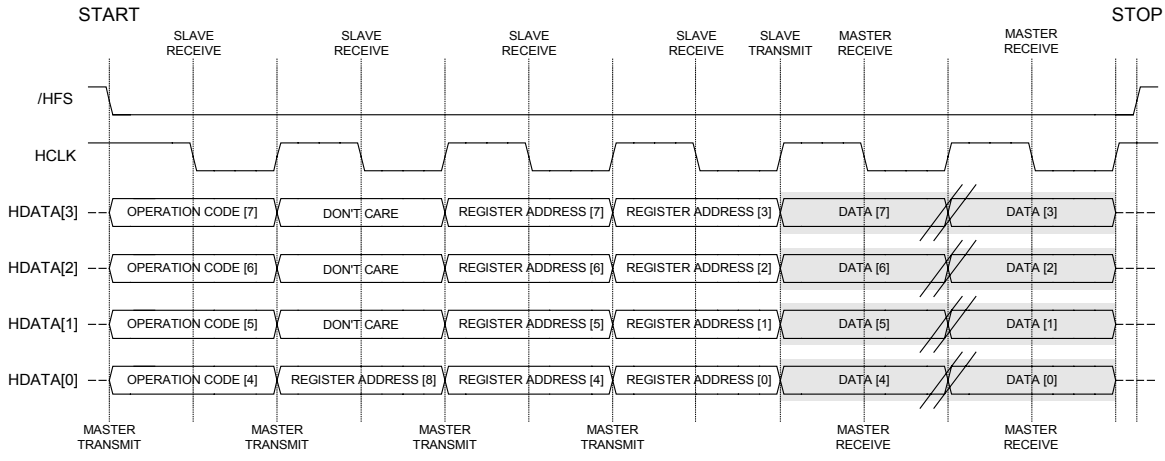


Figure 31. 6-Wire Read Operations (0x9*x* & 0xA*x*)

4.18 Miscellaneous Functions

4.18.1 General Purpose Inputs and Outputs (GPIO's)

The gm5060 has nine general purpose inputs / outputs. These provide the external microcontroller with additional signals to control the various devices in the system. Each GPIO has independent direction control, open drain enable, reading and writing.

Note that GPIO0 and GPIO1 can also serve as PWM back light intensity controls, as described in section 4.18.3 below. Also note that GPIO8 can be configured as an external interrupt source for the on-chip microcontroller.

In addition to nine general-purpose inputs / outputs, pins YUV7 through YUV0 can also serve as general-purpose inputs. YUV7 through YUV0 can be read from the host register, and are always configured as inputs so that no direction control is required.

4.18.2 Low Power State

The gm5060 provides a low power state in which the clocks to selected parts of the chip may be disabled.

4.18.3 Pulse Width Modulation (PWM) Back Light Control

Many of today's LCD back light inverters require both a PWM input and variable DC voltage to minimize flickering (due to the interference between panel timing and inverter's AC timing), and adjust brightness. Most LCD monitor manufactures currently use a microcontroller to provide these control signals. To minimize the burden on the external microcontroller, the gm5060 generates these signals directly.

There are two package pins needed for controlling the back light of TFT LCD panels, PWM0 (GPIO0) and PWM1 (GPIO1). The duty cycle of these signals is programmable. They may be connected to an external RC integrator to generate a variable DC voltage for a LCD back light inverter. Panel HSYNC is used as the clock for a counter generating this output signal.

4.18.4 Product ID and Revision

A read-only register provides a product identification and revision number unique to Genesis products.

5. ELECTRICAL SPECIFICATIONS

The following targeted specifications have been derived by simulation.

5.1 Preliminary DC Characteristics

Table 15. Absolute Maximum Ratings

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Supply Voltage AVDD_3.3 & DVDD_3.3 & PLLVDD_3.3 [1]	$V_{VDD\_3.3}$	-0.3		3.6	V
Supply Voltage AVDD_2.5 & DVDD_2.5 [1]	$V_{VDD\_2.5}$	-0.3		2.75	V
Input Voltage (5V tolerant inputs) [1]	V_{IN}	-0.3		5.0	V
Input Voltage (non 5V tolerant inputs) [1]	V_{IN}	-0.3		3.6	V
Electrostatic Discharge	V_{ESD}			±2.0	kV
Latchup	I_{LA}			±100	mA
Ambient Operating Temperature	T_A	0		70	°C
Storage Temperature	T_{STG}	-40		125	°C
Operating Junction Temp.	T_J	0		125	°C
Thermal Resistance: (Junction to Air) Natural Convection gm5060 292 Pin PBGA Package	θ_{JA}			15.6	°C/W
Thermal Resistance: (Junction to Case) Convection or air flow gm5060	θ_{JC}			5.3	°C/W
Soldering Temperature (30 sec.)	T_{SOL}			220	°C
Vapor Phase Soldering (30 sec.)	T_{VAP}			220	°C

NOTE: All voltages are measured with respect to GND

NOTE 1: Absolute maximum voltage ranges are for transient voltage excursions.

NOTE 2: Package thermal resistance is based on a PCB with one signal and two power planes. Package θ_{JA} is improved with four or more layer PCB.

Table 16. DC Characteristics

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Power Consumption (Source UXGA60 (162MHz), Display UXGA60 (135MHz))	P_{UXGA}			3.3	W
Power Consumption (Low Power Mode*)	P_{LP}		0.5		W
Supply Voltage AVDD_3.3 & DVDD_3.3 & PLLVDD_3.3	$V_{VDD\_3.3}$	3.15	3.3	3.45	V
Supply Voltage AVDD_2.5 & DVDD_2.5	$V_{VDD\_2.5}$	2.35	2.5	2.65	V
Supply Current (Source UXGA60 (162MHz), Display UXGA60 (135MHz))	I_{UXGA}			1100	mA
Supply Current (Low Power Mode*)	I_{LP}		140		MA
INPUTS					
High Voltage	V_{IH}	2.0		V_{DD}	V
Low Voltage	V_{IL}	GND		0.8	V
Clock High Voltage	V_{IHC}	2.4		V_{DD}	V
Clock Low Voltage	V_{ILC}	GND		0.4	V
High Current (V_{IN} = 5.0 V)	I_{IH}	-25		25	µA
Low Current (V_{IN} = 0.8 V)	I_{IL}	-25		25	µA
Capacitance (V_{IN} = 2.4 V)	C_{IN}			8	pF
OUTPUTS					
High Voltage (I_{OH} = Pin drive strength**)	V_{OH}	2.4		V_{DD}	V
Low Voltage (I_{OL} = Pin drive strength**)	V_{OL}	GND		0.4	V
Tri-State Leakage Current	I_{OZ}	-25		25	µA

* Note: Low power figures result from setting the ADC, TMDS, and clock power down bits.

** "Pin drive strength" refers to a source or sink current equal to the maximum current for each output pin as specified in Section 3.

5.2 Preliminary AC Characteristics

The following targeted specifications have been derived by simulation. All timing is measured to a 1.5V logic-switching threshold. The minimum and maximum operating conditions used were: T_{DIE} = 0 to 125 °C, Vdd = 2.25 to 2.75 V, Process = best to worst, C_L = 16 pF for all outputs.

Table 17. Maximum Speed of Operation

Clock Domain	gm5060
Main Input Clock (TCLK)	24 MHz (14.3MHz recommended)
TMDS Clock	165MHz
ADC Clock	162MHz
ITU-R BT656 Clock	75 MHz
SCL Host Interface Clock (2-wire mode)	400kHz
HCLK Host Interface Clock (6-wire mode)	5 MHz
IFM_CLK Input Format Measurement Clock	50MHz (14.3MHz recommended)
R_CLK Reference Clock	216MHz (216MHz recommended)
F_CLK Frame Store Clock	144 MHz
OCM_CLK On-Chip uC	100 MHz
DCLK Display Clock	135 MHz

Table 18. ITU-R BT656 Input Port Timing

Signal	Minimum Setup Requirement (ns)	Minimum Hold Requirement (ns)
YUV [7:0]	4.0	1.0

Table 19. Framestore Output Timing and Adjustments

FSOUT_TIMING ->	Tap 0 (default)		Tap 1		Tap 2		Tap 3	
	Min (ns)	Max (ns)	Min (ns)	Max (ns)	Min (ns)	Max (ns)	Min (ns)	Max (ns)
Propagation delay from FSCLK to FSDATA* (output)	1.0	4.5	0.5	3.5	0.0	2.5	-0.5	1.5
Propagation delay from FSCLK to FSADDR*	1.0	4.5	0.5	3.5	0.0	2.5	-0.5	1.5
Propagation delay from FSCLK to FSRAS	1.0	4.5	0.5	3.5	0.0	2.5	-0.5	1.5
Propagation delay from FSCLK to FSCAS	1.0	4.5	0.5	3.5	0.0	2.5	-0.5	1.5
Propagation delay from FSCLK to FSWE	1.0	4.5	0.5	3.5	0.0	2.5	-0.5	1.5
Propagation delay from FSCLK to FSDQM1	1.0	4.5	0.5	3.5	0.0	2.5	-0.5	1.5
Propagation delay from FSCLK to FSDQM0	1.0	4.5	0.5	3.5	0.0	2.5	-0.5	1.5
Propagation delay from FSCLK to FSCKE	1.0	4.5	0.5	3.5	0.0	2.5	-0.5	1.5

Note: This table lists the amount of adjustment that can be made to the framestore output propagation delays, in order to improve setup margin of DRAM write operations at the expense of Hold margin on write operations and setup margin on read operations. The tap selected is controlled by the FSOUTTIMING parameter in the SYS_TIMING register.

Table 20. Framestore Readback Timing (for all conditions)

FSREAD_TIMING Tap 0	FSOUTTIMING			
	Tap 0	Tap 1	Tap 2	Tap 3
FSDATA* Minimum Setup (ns)	2.5	3.5	4.5	5.5
FSDATA* Minimum Hold (ns)	1.0	0.5	0.0	-0.5

FSREAD_TIMING Tap 1	FSOUTTIMING			
	Tap 0	Tap 1	Tap 2	Tap 3
FSDATA* Minimum Setup (ns)	0.5	1.5	2.5	3.5
FSDATA* Minimum Hold (ns)	2.0	1.5	1.0	0.5

FSREAD_TIMING Tap 2	FSOUTTIMING			
	Tap 0	Tap 1	Tap 2	Tap 3
FSDATA* Minimum Setup (ns)	1.5	2.5	3.5	4.5
FSDATA* Minimum Hold (ns)	1.5	1.0	0.5	0.0

FSREAD_TIMING Tap 3	FSOUTTIMING			
	Tap 0	Tap 1	Tap 2	Tap 3
FSDATA* Minimum Setup (ns)	3.0	4.0	5.0	6.0
FSDATA* Minimum Hold (ns)	0.5	0.0	-0.5	-1.0

Note: FSOUTTIMING and FSREADTIMING are controlled by the SYS_TIMING register.

Table 21. Display Timing and DCLK Adjustments

DP_TIMING ->	Tap 0 (default)		Tap 1		Tap 2		Tap 3	
	Min (ns)	Max (ns)	Min (ns)	Max (ns)	Min (ns)	Max (ns)	Min (ns)	Max (ns)
Propagation delay from DCLK to DA*/DB*	1.0	4.5	0.5	3.5	-0.5	2.5	-1.5	1.5
Propagation delay from DCLK to DHS	1.0	4.5	0.5	3.5	-0.5	2.5	-1.5	1.5
Propagation delay from DCLK to DVS	0.5	4.5	0.0	3.5	-1.0	2.5	-2.0	1.5
Propagation delay from DCLK to DEN	1.0	4.5	0.5	3.5	-0.5	2.5	-1.5	1.5
Propagation delay from DCLK to DOVL	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD

Note: DCLK Clock Adjustments are the amount of additional delay that can be inserted in the DCLK path, in order to reduce the propagation delay between DCLK and its related signals.

Table 22. 2-Wire Host I/F Port Timing

Parameter	Symbol	MIN	TYP	MAX	Units
SCL HIGH time	T_{SHI}	1.25			us
SCL LOW time	T_{SLO}	1.25			us
SDA to SCL Setup	T_{SDIS}	30			ns
SDA from SCL Hold	T_{SDIH}	20			ns
Propagation delay from SCL to SDA	T_{SDO3}	10		150	ns

The above table assumes OCM_CLK = R_CLK / 2 = 100 MHz (default) (ie 10ns / clock)

Table 23. 6-Wire Host I/F Port Timing

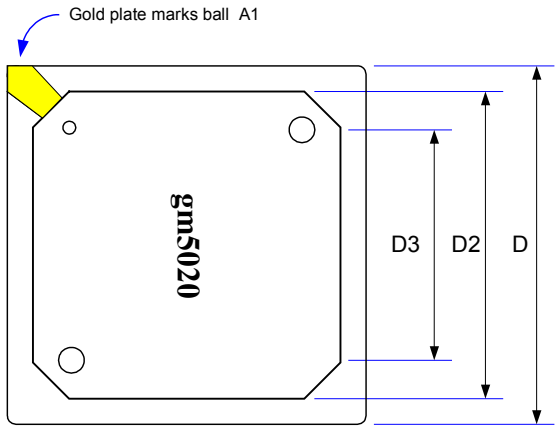
Parameter	Symbol	MIN	TYP	MAX	Units
HCLK HIGH time	T_{SHI}	100	-	-	ns
HCLK LOW time	T_{SLO}	100	-	-	ns
HFSn to HCLK Setup	T_{SDIS}	30	-	-	ns
HFSn from HCLK Hold	T_{SDIH}	20	-	-	ns
HDATA to HCLK Setup		30	-	-	ns
HDATA from HCLK Hold		20	-	-	ns
Propagation delay from HCLK to HDATA	T_{SDO3}	10	-	100	ns

The above table assumes OCM_CLK = R_CLK / 2 = 100 MHz (default)

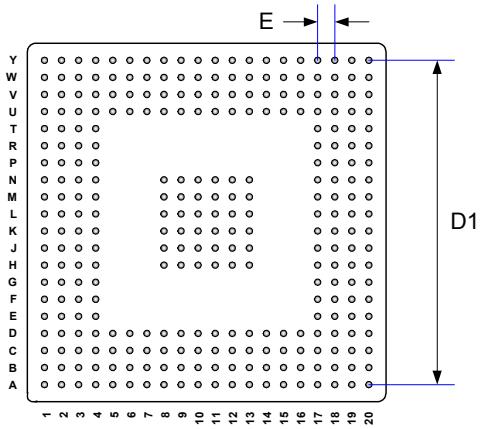
6. ORDERING INFORMATION

Order Code	Application	Package	Speed	Temperature Range
gm5060	UXGA	292-pin PBGA	162MHz	0-70°C

7. MECHANICAL SPECIFICATIONS



Symbol	mm			inches		
	MIN	NOM	MAX	MIN	NOM	MAX
A	2.20	2.33	2.46	0.087	0.092	0.098
A1	0.50	0.60	0.70	-	0.024	-
A2		1.17			0.046	
B	0.60	0.75	0.90	-	0.030	-
C		0.56			0.022	
D	26.80	27.00	27.20	1.055	1.063	1.071
D1	-	24.13	-	-	0.950	-
D2		24.00			0.945	
D3		16			0.63	
E	-	1.27	-	-	0.050	-
F	-	-	0.15	-	-	0.006
G		30^{0}			30^{0}	



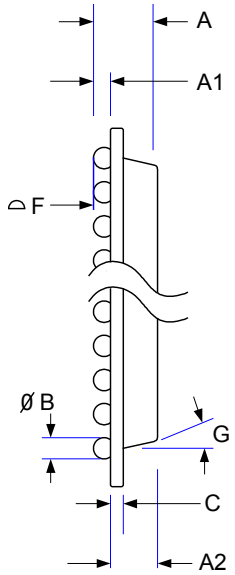


Figure 32. gm5060 292-pin PBGA