DS3133-1.0

MV3506 A-LAW FILTER/CODEC
MV3507 μ-LAW FILTER/CODEC
MV3507A μ-LAW FILTER/CODEC WITH A/B SIGNALLING
MV3508 A-LAW FILTER/CODEC WITH OPTIONAL SQUELCH
MV3509 μ-LAW FILTER/CODEC WITH OPTIONAL SQUELCH

These devices are silicon gate CMOS Companding Encoder/Decoder integrated circuits designed to implement the per channel voice frequency Codecs used in PCM systems. They contain the band-limiting filters and the analog to digital conversion circuits that conform to the desired transfer characteristic. The MV3506 and MV3508 provide the European A-Law companding and the MV3507, MV3507A and MV3509 provide the North American μ-Law companding characteristic. The MV3508 and MV3509 have programmable squelch circuitry to reduce idle channel noise. The MV3507A provides for A/B bit signalling.

These circuits provide the interface between the analog signals of the subscriber loop and digital signals of the PCM highway in a digital telephone switching system. The devices operate from dual power supplies of ±5V.

FEATURES

- Low Power CMOS 80mW (Operating) 10mW (Standby)
- Meets or Exceeds AT & T3, and CCITT G.711, G.712 and G.733 Specifications
- Input Analog Filter Eliminates Need for External Anti-aliasing Prefilter
- Uncommitted Input and Output Op. Amps for Programming Gain
- Output Op. Amp Provides ±3.1V into a 1200 Ohms Load or can be Switched Off for Reduced Power (70mW)
- Encoder has Dual-speed Auto-zero Loop for Fast Acquisition on Power-up
- Low Absolute Group Delay = 410 microseconds at 1kHz

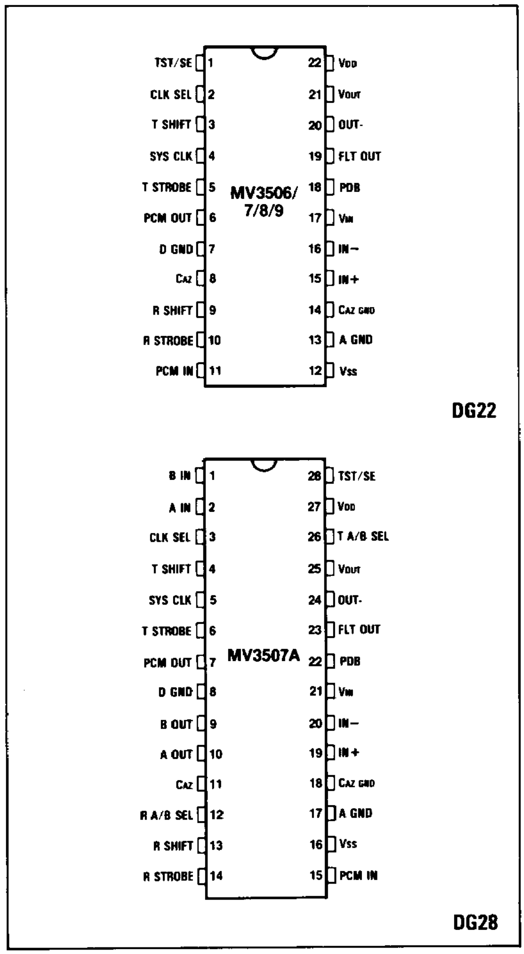

Fig.1 Pin connections - top view

FUNCTIONAL DESCRIPTION

Fig.2 shows the simplified block diagram of the devices. They contain independent circuitry for processing transmit and receive signals. Switched capacitor filters provide the necessary bandwidth limiting of voice signals in both directions. Circuitry for coding and decoding operates on the principle of successive approximation, using charge redistribution in a binary weighted capacitor array to define segments and a resistor chain to define steps.

Transmit Section

Input analog signals first enter the chip at the uncommitted op.amp. terminals (IN + and IN- pins). This allows for the gain in the system to be trimmed. From the V_{IN} pin the signal enters a second-order analog anti-aliasing filter. This filter eliminates the need for any off-chip filtering as it provides attenuation of 34dB (typically) at 256kHz and 44dB (typically) at 512kHz.

The signal next enters the transmit filter, which is a fifth-order low-pass filter clocked at 256kHz, followed by a third-order high-pass filter clocked at 64kHz. The resulting bandpass characteristics meet the CCITT specifications G.711, G.712 and G.733. Some representative attenuations are better than 26dB from 0 to 60Hz and better than 35dB from 4.6kHz to 100kHz.

The output of the transmit filter is sampled at the analog to digital encoder by a capacitor array at the sampling rate of 8kHz. The successive approximation conversion process requires about 72μsec.

The 8-bit PCM data is clocked out by the transmit shift clock which can vary from 64kHz to 2.048MHz in 8kHz steps (see Figs. 3 and 4). A switched capacitor dual-speed, auto-zero loop using a small non-critical external capacitor (0.1μF) provides DC offset cancellation by integrating the sign bit of the PCM data and feeding it back to the non-inverting input of the comparator.

Included in the circuitry of the MV3507 is 'All Zero' code suppression so that negative input signal values between decision values numbers 127 and 128 are encoded as 00000010. This prevents loss of repeater synchronisation by DS1 (T1) line clock recovery circuitry as there are never more than 15 consecutive zeros.

An additional feature of the MV3506/7 and 7A is a special circuit to eliminate any transmitted idle channel noise during quiet periods. When the input of these chips is such that for 250ms the only code words generated were +0, -0, +1 or -1, the output word will be a +0. The steady +0 state prevents alternating sign bits or LSB from toggling and thus results in a quieter signal at the decoder. Upon detection of a different value, the output resumes normal operation resetting the 250ms timer. This feature is a form of idle Channel Noise 'Squelch' or 'Crosstalk Suppression'. It is of particular importance in the MV3506 A-Law version because the A-Law transfer characteristic has 'mid-riser' bias which enhances low level signals from crosstalk.

Receive Section

A receive shift clock, variable between the frequencies of 64kHz and 2.048MHz clocks the PCM data into the input buffer register once every sampling period (see Figs.5 and 6). A charge proportional to the received PCM data word appears on the decoder capacitor array of the digital to analog converter. A sample and hold circuit, initialised to zro by a narrow pulse at the beginning of each sampling period, integrates the charge and holds it for the rest of the sampling period.

The receive filter, consisting of a switched-capacitor fifth-order low-pass filter clocked at 256kHz, smooths the sampled and held signal. It also performs the loss equalisation to compensate for the sin(x)/x distortion due to the sampling.

The filter output (FLT OUT pin) is available for driving electronic hybrids directly as long as the impedance is greater than 20kΩ. When used in this fashion the low impedance output amp can be switched off for a considerable saving in power consumption. When it is required to drive a 600Ω load the output amp allows gain trimming as well as impedance matching.

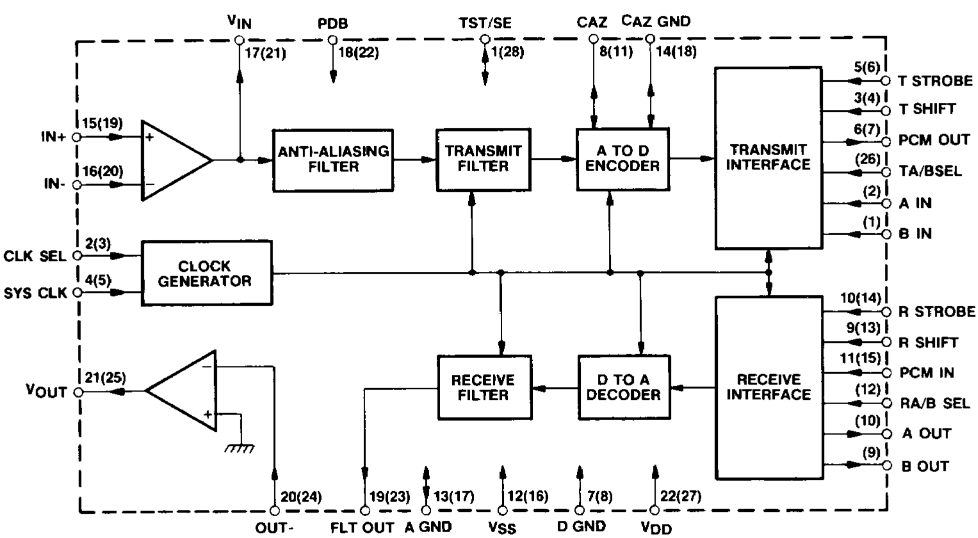

Fig.2 Functional block diagram (pin numbers for the MV3507A are in brackets)

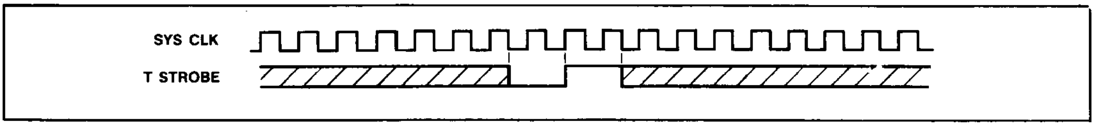

Fig.3 Transmit strobe alignment

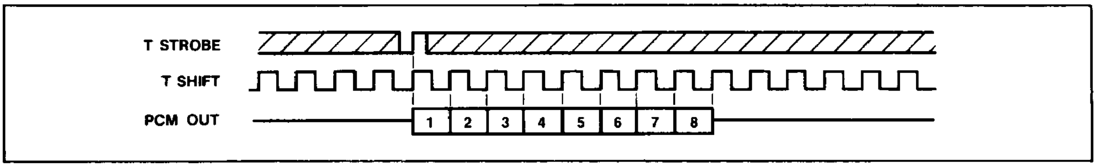

Fig.4 Transmit alignment

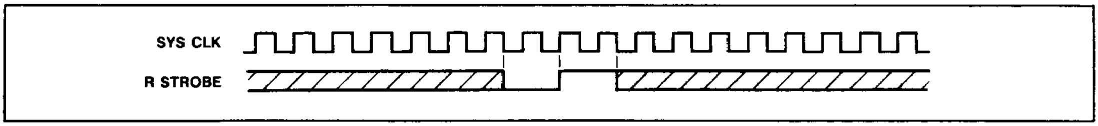

Fig.5 Receive strobe alignment

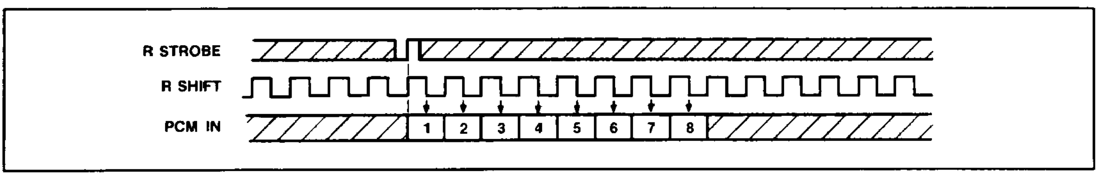

Fig.6 Receive alignment

Timing Requirements

The internal design of the devices paid careful attention to the timing requirements of various systems. In North America, central office and channel bank designs often follow the American Telephone and Telegraph Company's T1 (DS1) Carrier PCM format to multiplex 24 voice channels at a data rate of 1.544Mb/s. PABX designs, on the other hand, may use their own multiplexing formats with different data rates. Nevertheless, in digital telephone designs, Codecs may be used in a non-multiplexed form with data rate as low as 64kbit/s. The μ-Law Codecs fulfil these requirements.

In Europe, telephone exchange and channel bank designs often follow the CCITT carrier PCM format to multiplex 30 telephony channels at a data rate of 2.048Mbit/s. The A-Law Codecs are designed for this market and will also handle PABX and digital telephone applications.

The timing format chosen for the devices allows operation in both multiplexed or non-multiplexed form with data rates variable from 64kbit/s to 2.048Mbit/s. Use of separate internal clocks for filters and for shifting of PCM input/output data allows for this variation.

The devices do not require that the 8kHz transmit and receive sampling strobes be exactly 8 bit periods wide. The device has an internal bit counter that counts the number of data bits shifted. It is reset on the leading (+ve) edges of the strobe, forcing the PCM output into its high impedance state after the 8th bit is shifted out. This allows the width of the strobe signal to vary as long as its repetition rate is 8kHz and the transmit and receive shift clocks are synchronised to it.

System Clock

The basic timing is provided by the system clock which is divided down internally to provide the various filter clocks and the timing for the conversions. The transmit and receive strobes and clocks must be locked to this clock so that the PCM data matches the sample rates.

Signalling in 7-Law Systems

In μ-Law systems there is a requirement for signalling information to be carried in the bit stream with the coded analog data. This coding scheme is sometimes called 7⅞ bit rather than 8 bit because the LSB in every 6th frame is replaced by a signalling bit. This is referred to as A/B signalling and if a signalling frame carries the 'A' bit, then 6 frames later the LSB will carry the 'B' bit. To meet this requirement, the MV3507A is available in a 28-pin package.

Signalling Interface

In the AT&T T1 carrier PCM format (DS1) an A/B signalling method conveys channel information. It might include the on-or-off hook status of the channel, dial pulsing (10 or 20 pulses per second), loop closure, ring ground etc, depending on the application. Two signalling conditions (A and B) per channel, giving four possible signalling states per channel are repeated every 12 frames (1.5msec). The A signalling condition is sent on bit 8 of all 24 channels in frame 6 and the B signalling condition is sent in frame 12. In each frame, the 193rd bit (the S bit) performs the terminal framing function and serves to identify frames 6 and 12.

The MV3507A in a 28-pin package is designed to simplify the signalling interface. For example, the A/B select input pins are transition sensitive. The transmit A/B select pin selects the A signal input on a positive transition and the B signal input on the negative transition. Internally, the device synchronises the A/B select input with the strobe signal. As a result, a common A/B select signal can be used for all 24 transmit channels in the channel bank. The A and B signalling bits are sent in the frame following the frame in which the A/B select input makes the transition. Therefore the A/B select input must go positive in the beginning of frame 5 and negative in the beginning of frame 11.

The decoder uses a similar scheme for receiving the A and B signalling bits, with one difference. They are latched to the respective outputs in the same frame in which A/B select input makes a transition. Therefore, the receive A/B select input must go high at the beginning of frame 6 and go low at the beginning of frame 12. In the T1 (DS1) carrier system, 24 voice channels are multiplexed to form the transmit and receive PCM highway, 8 data bits from each channel plus a framing bit called the S bit form a 193 bit frame. Since each channel is sampled 8000 times per second, the resultant data rate is 1.544Mbit/s. Within the channel bank the transmit and receive channels of a Codec can occupy the same time slot for synchronous operation or they can be independent of each other for asynchronous operation. Asynchronous operation helps minimise switching delays through the system. Since the timing interface for the coder and decoder sections are independent of each other in the MV3507A, it can be operated in either manner.

In the CCITT carrier system 30 voice channels and 2 framing and signalling channels are multiplexed to form the transmit and receive PCM highways, 8 data bits from each channel. Since each channel is sampled 8000 times per second, the resultant data rate is 2.048Mbit/s.

PIN DESCRIPTIONS

Symbol	Pin No.		Pin name and description
	3506/7/8/9	3507A	
TST/SE	1	28	**Test/Squelch Enable (Internal Connection/Digital Input).** This pin is an internal test connection on the MV3506, MV3507 and MV3507A, and it is the squelch enable input on the MV3508 and MV3509. On the MV3506/7/7A it should be left unconnected or connected to the A GND pin via a capacitor for normal operation. On the MV3508/9 it should be tied high to enable the squelch feature and it should be left unconnected otherwise.
CLK SEL	2	3	**Clock Select (Three Level Input).** This pin selects the proper divide ratios for a 256kHz, 1.544MHz or 2.048MHz system clock. The pin is tied to V_{DD} (+5V) for 2.048MHz operation, to D GND (0V) for 256kHz operation, and to V_{SS} (-5V) for 1.544MHz operation.
T SHIFT	3	4	**Transmit Shift Clock (Digital Input).** This TTL compatible input shifts PCM data out of the coder on the positive going edges after receiving a positive edge on the T STROBE input. The clocking rate can vary from 64kHz to 2.048MHz.
SYS CLK	4	5	**System Clock (Digital Input).** This pin is a TTL compatible input for either a 256kHz, 1.544MHz or a 2.048MHz clock that is divided down to provide the filter clocks. The status of the CLK SEL pin must correspond to the provided clock frequency.
T STROBE	5	6	**Transmit Strobe (Digital Input with Pull-up).** This TTL compatible pulse input (typically 8kHz) is used for analog sampling and initiating the PCM output from the coder. It must be synchronised with the T SHIFT and SYS CLK clocks with its positive going edges occurring after the falling edges of these clocks. The width of this signal is not critical. An internal bit counter generates the necessary timing for PCM output.
PCM OUT	6	7	**PCM Out (Pull-down Output).** This is a LS TTL compatible open-drain output. It is active only during transmission of PCM output for 8-bit periods of the T SHIFT clock signal following positive edge on the T STROBE input. Data is clocked out by the positive edge on the T SHIFT clock into one 510Ω pull-up per system plus 2 LS TTL inputs.
D GND	7	8	**Digital Ground (Power Input).** 0V.
C_{AZ}	8	11	**Auto Zero Capacitor (Reference Node).** A capacitor of 0.1μF (±20%) should be connected between this pin and $C_{AZ\,GND}$ for coder auto zero operation. The sign bit of the PCM data is integrated and fed back to the comparator for DC offset cancellation.
R SHIFT	9	13	**Receive Shift Clock (Digital Input).** This TTL compatible input shifts PCM data into the decoder on the negative going edges after receiving a positive edge on the R STROBE input. The clocking rate can vary from 64kHz to 2.048MHz.

PIN DESCRIPTIONS (continued)

Symbol	Pin No. 3506/7/8/9	Pin No. 3507A	Pin name and description
R STROBE	10	14	**Receive Strobe (Digital Input with Pull-up).** This TTL compatible pulse input (typically 8kHz) initiates clocking of PCM input data into the decoder. It must be synchronised with the R SHIFT and SYS CLK clocks with its positive going edges occurring after the falling edges of these clocks. The width of the signal is not critical. An internal bit counter generates necessary timing for PCM input.
PCM IN	11	15	**PCM In (Digital Input).** This is a TTL compatible input for supplying PCM input data to the decoder. Data is clocked in by the negative edge of the R SHIFT clock.
V_{SS}	12	16	**Negative Supply (Power Input).** -5V.
A GND	13	17	**Analog Ground (Reference Node).** This is the ground reference node for analog signals.
$C_{AZ\ GND}$	14	18	**Auto Zero Capacitor Ground (Reference Node).** A capacitor of 0.1μF ($\pm$20%) should be connected between this pin and C_{AZ} for coder auto zero operation. The sign bit of the PCM data is integrated and fed back to the comparator for DC offset cancellation.
IN +, IN-	15,16	19,20	**In Positive and Negative (Analog Voltage Inputs).** These are the differential inputs of a high input impedance op amp whose output is connected to the V_{IN} pin. These three pins allow the user complete control over the input stage so that it can be connected as a fixed gain amplifier, as an amplifier with adjustable gain, or as a differential input amplifier. The adjustable gain configuration will facilitate calibration of the transmit channel.
V_{IN}	17	21	**Input Voltage (Analog High-impedance Voltage Output).** This is the output of a high input impedance op amp whose differential inputs are the IN + and IN- pins. This node feeds the rest of the analog input section.
PDB	18	22	**Power Down Bar (Digital Input with Pull-up).** This TTL compatible input, when held low, puts the chip into the powered down mode regardless of strobes. The chip will also power down if the strobes stop. The strobes can be high, low or floating, but as long as they are static, the powered down mode is in effect.
FLT OUT	19	23	**Filter Out (Analog High-impedance Voltage Output).** This is the output of the low pass filter which represents the recreated analog signal from the received PCM data words. The filter sample frequency of 256kHz is down 37dB at this point. This is a high impedance output which can be used by itself or connected to the output amplifier stage which has a low output impedance. It should not be loaded by less than 20kΩ.
OUT-	20	24	**Out Negative (Analog Voltage Input).** This is the inverting input of the uncommitted output amplifier stage, which has its non-inverting input connected internally to ground and its output connected to V_{OUT}. The signal at the FLT OUT pin can be connected to this pin to realise a low output impedance with unity, increased or reduced gain. This allows easy calibration of the receive channel. If OUT- is connected directly to V_{SS} then the op amp will be powered down, reducing power consumption by 10mW typically.
V_{OUT}	21	25	**Output Voltage (Analog Voltage Output).** This is the output of the uncommitted output amplifier stage, which has its inverting input connected to the OUT- pin and its non-inverting input connected internally to ground. The signal at the FLT OUT pin can be connected to OUT- to realise a low output impedance with unity, increased or reduced gain. This allows easy calibration of the receive channel. The V_{OUT} pin has the capability of driving 0dBm into a 600Ω load (see Fig.4).
V_{DD}	22	27	**Positive Supply (Power Input).** 5V.
B IN, A IN	-	1,2	**B IN and A IN (Digital Inputs with Pull-ups).** These are the TTL compatible inputs for the A and B signalling bits for transmission. The signalling bits are sent in the bit 8 position of the PCM word in the frame following the frame in which the T-A/B SEL input makes a transition.
B OUT,A OUT	-	9,10	**B OUT and A OUT (Digital CMOS Outputs).** These are the outputs for the received A and B signalling bits. The signalling bits received in the PCM input word are latched to the respective outputs in the same frame in which the Receive A/B select (R-A/B SEL) input makes a transition. A-bits are latched on a positive transition and B-bits are latched on a negative transition.

PIN DESCRIPTIONS (continued)

Symbol	Pin No. 3506/7/8/9	Pin No. 3507A	Pin name and description
R-A/B SEL	-	12	**Receive A or B Select (Digital Input with Pull-up).** This is the TTL compatible input which causes A and B signalling bits to b at the A OUT and B OUT pins. The signalling bits received in the PCM input word are latched to the respective outputs in the same frame in which this input makes a transition. A-bits are latched on a positive transition and B-bits are latched on a negative transition. A common select input can be used for all channels in a multiplex operation.
T-A/B SEL	-	26	**Transmit A or B Select (Digital Input with Pull-up).** This is the TTL compatible input which causes the transmission of A and B signalling bits input at the A IN and B IN pins. The signalling bits are sent in the bit 8 position of the PCM word in the frame following the frame in which the T-A/B SEL input makes a transition. A common A/B select input can be used for all channels in a multiplex operation, since it is synchronised to the T STROBE input in each device.

ELECTRICAL CHARACTERISTICS

Test conditions - Voltages are with respect to digital ground (V_{DGND})

Characteristic	Symbol	Value Min.	Value Typ.(1)	Value Max.	Units
Digital supply voltage	V_{DD}	4.75	5	5.25	V
Negative supply voltage	V_{SS}	-5.25	-5	-4.75	V
Analog ground voltage	V_{AGND}	-0.1	0	0.1	V
Ambient temperature	V_{AMB}	0		70	°C
Input low voltage - digital inputs	V_{IL}	0	0.4	0.8	V
Input high voltage - digital inputs	V_{IH}	2.0	2.4	V_{DD}	V
System clock frequency					
CLK SEL tied to V_{DD}	fs	2047.90	2048	2048.10	kHz
CLK SEL tied to D GND		255.99	256	256.01	
CLK SEL tied to V_{SS}		1549.92	1544	1544.08	
Capacitive loading - digital outputs	C_{LD}	0		100	pF
Pull-up resistance for PCM OUT pin	R_{PU}	510			Ω
Analog input voltage	V_{IA}	V_{AGND} -3.1		V_{AGND} +3.1	V
Capacitive loading - analog outputs	C_{LA}			50	pF
Resistive loading - V_{OUT} pin	R_{VOUT}	1200			Ω
Resistive loading - V_{IN} pin	R_{VIN}	10			kΩ
Resistive loading - FLT OUT pin	$R_{RLT\ OUT}$	20			kΩ

Power Supply Requirements - V_{DD} = 5V, V_{SS} = -5V

Characteristic	Symbol	Value Min.	Value Typ.(1)	Value Max.	Units	Conditions
Power dissipation - normal	P_N		80	110	mW	Unloaded
Power dissipation - without output amp.	P_{WA}		70		mW	Unloaded
Power dissipation - standby	P_S		10	20	mW	Unloaded

Static Characteristics - Voltages are with respect to digital ground (V_{DGND})

Characteristic	Symbol	Value Min.	Value Typ.(1)	Value Max.	Units	Conditions
Pin capacitance	C_{PIN}		7	15	pF	
Input leakage current	I_{IL}			1	μA	$0 < V < V_{DD}$
Input source current - inputs with pull-ups	I_{IS}			600	μA	$0 < V < V_{DD}$
Output high voltage	V_{OH}	2.4		V_{DD}	V	I_{OH} (Source) = 40μA
Output low voltage	V_{OL}	0		0.4	V	I_{OL} (Sink) = 1.6mA
Output leakage current	I_{OL}			10	μA	$0 < V < V_{DD}$
Analog input resistance	R_{IA}	100			kΩ	
Analog output voltage	V_{OA}	V_{AGND} -3.1		V_{AGND} +3.1	V	

Digital Switching Characteristics - System Clock (see Fig.7)

Characteristic	Symbol	Value Min.	Value Typ.(1)	Value Max.	Units	Conditions
System clock rise time	t_{SR}		50		ns	
System clock high period	t_{SH}	0.4/fs		0.6/fs	s	
System clock fall time	t_{SF}		50		ns	
System clock low period	t_{SL}	0.4/fs		0.6/fs	s	

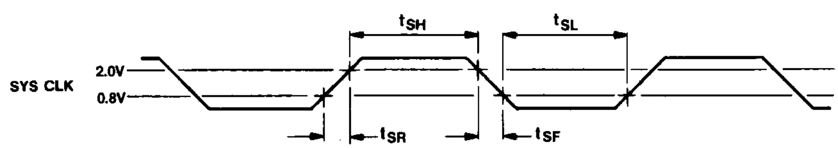

Fig.7 Timing - system clock

Digital Switching Characteristics - Receive Strobe and Clock (see Figs. 8 and 9)

Characteristic	Symbol	Value Min.	Value Typ.(1)	Value Max.	Units	Conditions
Receive strobe frequency	f_{RS}	7.99996	8	8.00004	kHz	Phase-locked with system clock
Receive strobe falling set-up time	t_{RSFS}	120			ns	
Receive strobe early jitter	t_{RSEJ}			200	ns	
Receive strobe late jitter	t_{RSLJ}			100	ns	
Receive strobe falling hold time	t_{RSFH}	220			ns	
Receive clock frequency	f_{RC}	63.9997		2048.01	kHz	Phase-locked with receive strobe
Receive clock rise time	t_{RCR}			100	ns	
Receive clock high period	t_{RCH}	$0.4/f_{RC}$		$0.6/f_{RC}$	s	
Receive clock fall time	t_{RCF}			100	ns	
Receive clock low period	t_{RCL}	$0.4/f_{RC}$		$0.6/f_{RC}$	s	
Receive clock early jitter	t_{RCEJ}			200	ns	
Receive clock late jitter	t_{RSLJ}			100	ns	

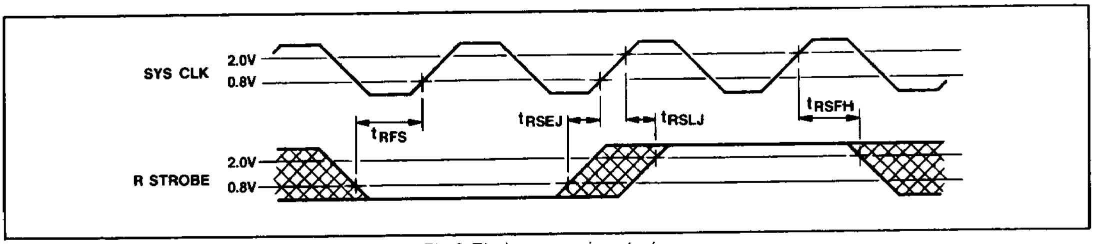

Fig.8 Timing - receive strobe

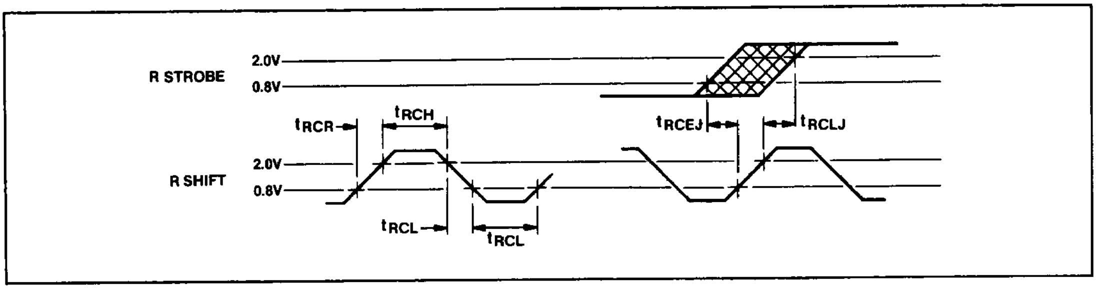

Fig.9 Timing - receive clock

Digital Switching Characteristics - Receive Data (see Fig.10)

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.(1)	Max.		
PCM input set-up time	t_{PIS}	60			ns	
PCM input hold time	t_{PIH}	60			ns	

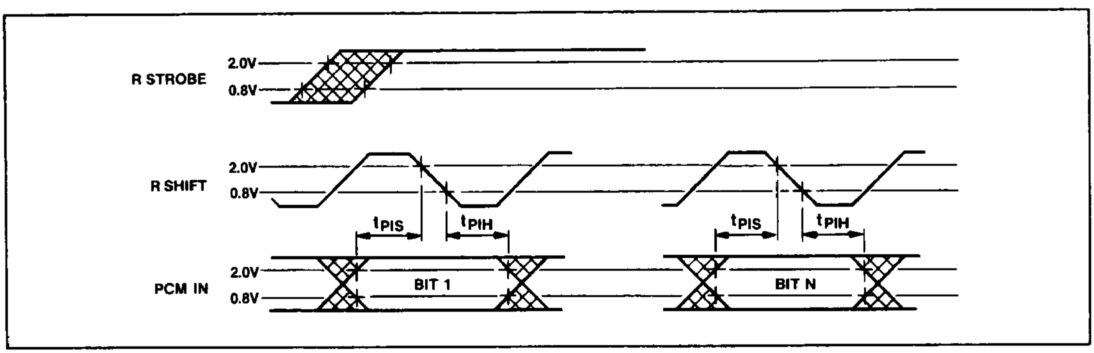

Fig.10 Timing - receive data

Digital Switching Characteristics - Transmit Strobe and Clock (see Figs.11 and 12)

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.(1)	Max.		
Transmit strobe frequency	f_{TS}	7.99996	8	8.00004	kHz	Phase-locked with system clock
Transmit strobe falling set-up time	t_{TSFS}	120			ns	
Transmit strobe early jitter	t_{TSEJ}			200	ns	
Transmit strobe late jitter	t_{TSLJ}			100	ns	
Transmit strobe falling hold time	t_{TSFH}	220			ns	
Transmit clock frequency	f_{TC}	63.9997		2048.01	kHz	Phase-locked with transmit strobe
Transmit clock rise time	t_{TCR}			100	ns	
Transmit clock high period	t_{TCH}	$0.4/f_{TC}$		$0.6/f_{TC}$	s	
Transmit clock fall time	t_{TCF}			100	ns	
Transmit clock low period	t_{TCL}	$0.4/f_{TC}$		$0.6/f_{TC}$	s	
Transmit clock early jitter	t_{TCEJ}			200	ns	
Transmit clock late jitter	t_{TCLJ}			100	ns	

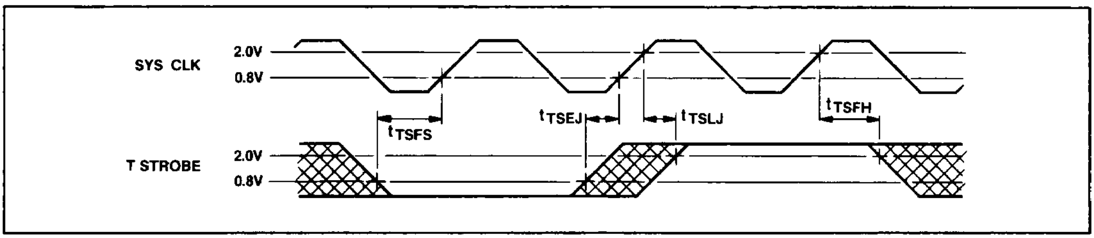

Fig.11 Timing - receive strobe

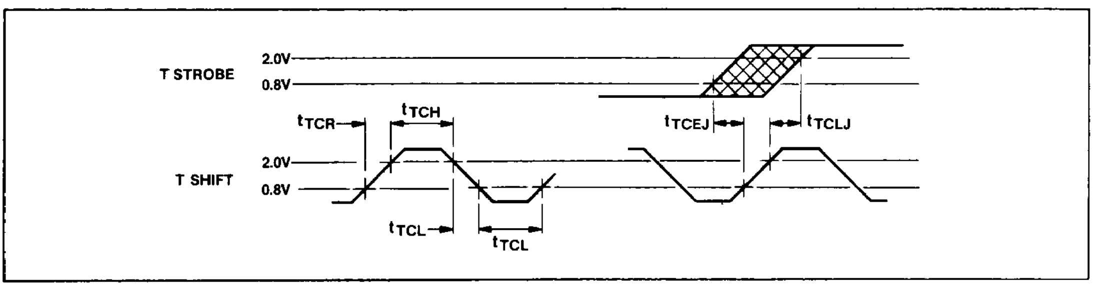

Fig.12 Timing - receive clock

Digital Switching Characteristics - Transmit Data (see Fig.13)

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.(1)	Max.		
PCM output holt time	t_{POH}	0	50		ns	
PCM output delay	t_{POD}		100	150	ns	

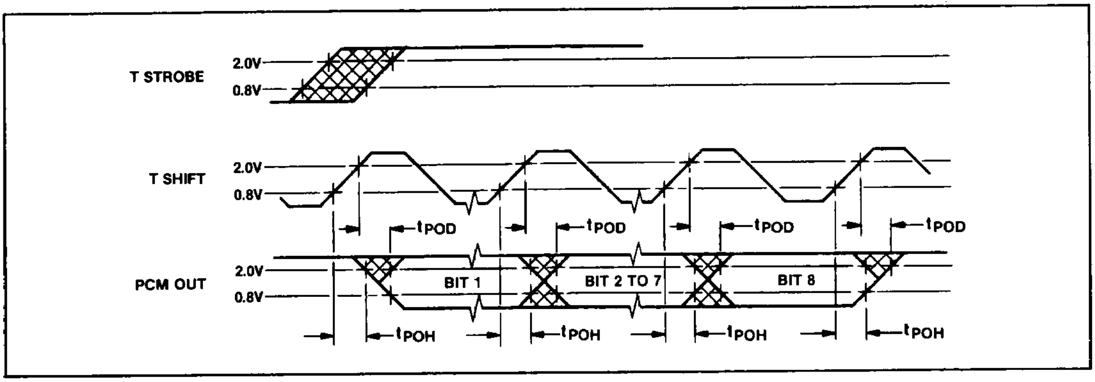

Fig.13 Timing - transmit data

Analog Channel Characteristics - Filter Delays

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.(1)	Max.		
Transmit filter delay	t_{TFD}			182	μs	1kHz
Receive filter delay	t_{RFD}			110	μs	1kHz

Analog Channel Characteristics - A-Law

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.(1)	Max.		
0dBm0 level (see Note 2)	0dBm0	5.3	5.8	6.3	dBm	±5V, 25°C
Variation in 0dBm0 level	Δ_{0dBm0}	-0.3	0	0.3	dB	Over test conditions
Weighted idle channel noise	ICN_W		-85	-73	dBm0p	CCITT G.712, §5.1 (see Note 3)
Single frequency idle channel noise	ICN_{SF}			-60	dBm0	CCITT G.712, §5.2
Weighted receive idle channel noise	ICN_{WR}			-78	dBm0p	CCITT G.712, §5.3
Spurious out-band noise	N_{SOB}			-30	dBm0	CCITT G.712, §7.1
Spurious in-band noise	N_{SIB}			-40	dBm0	CCITT G.712, §10
Two tone interdemodulation	IMD_{2T}			-35	dBm0	CCITT G.712, §8.1
Tone + power inter-demodulation	IMD_{TP}			-49	dBm0	CCITT G.712, §8.2
Crosstalk attenuation between V_{IN} and V_{OUT}	A_X	75	80		dB	CCITT G.712, §12

Analog Channel Characteristics - μ-Law

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.(1)	Max.		
0dBm0 level (see Note 2)	0dBm0	5.3	5.8	6.3	dBm	±5V, 25°C
Variation in 0dBm0 level	Δ_{dBm0}	-0.3	0	0.3	dB	Over test conditions
Weighted idle channel noise	ICN_W		5	17	dBrnc0	AT&T D3 (see Note 3)
Single frequency idle channel noise	ICN_{SF}			-60	dBm0	AT&T D3
Weighted receive idle channel noise	ICN_{WR}			15	dBrnc0	AT&T D3
Spurious out-band noise	N_{SOB}			-28	dBm0	AT&T D3
Spurious in-band noise	N_{SIB}			-40	dBm0	AT&T D3
Two tone interdemodulation	IMD_{2T}			-35	dBm0	AT&T D3
Tone + power inter-demodulation	IMD_{TP}			-49	dBm0	AT&T D3
Crosstalk attenuation between V_{IN} and V_{OUT}	A_X	75	80		dB	AT&T D3

NOTES
1. Typical figures are for design aid only. They are not guaranteed and not subject to production testing.
2. The typical 0dBm0 level of 5.8dBm corresponds to an RMS voltage of 1.51V and a maximum coding level of 3.1V.
3. The maximum value reduces to -68dBm0p without squelch (MV3508 with TST/SE pin unconnected).
4. The maximum value reduces to 22dBrnc0 without squelch (MV3509 with TST/SE pin unconnected).

ABSOLUTE MAXIMUM RATINGS

Exceeding these ratings may cause permanent damage. Functional operation under these conditions is not implied.

Positive supply voltage V_{DD}	-0.5V to +6.0V
Analog ground V_{AGND}	-0.1V to +0.1V
Negative supply voltage V_{SS}	-6.0V to +0.5V
Storage temperature T_S	-65°C to +150°C
Voltage at digital or analog pins V_P	V_{SS}-0.3V to V_{DD} +0.3V
Package power dissipation P	1000mW

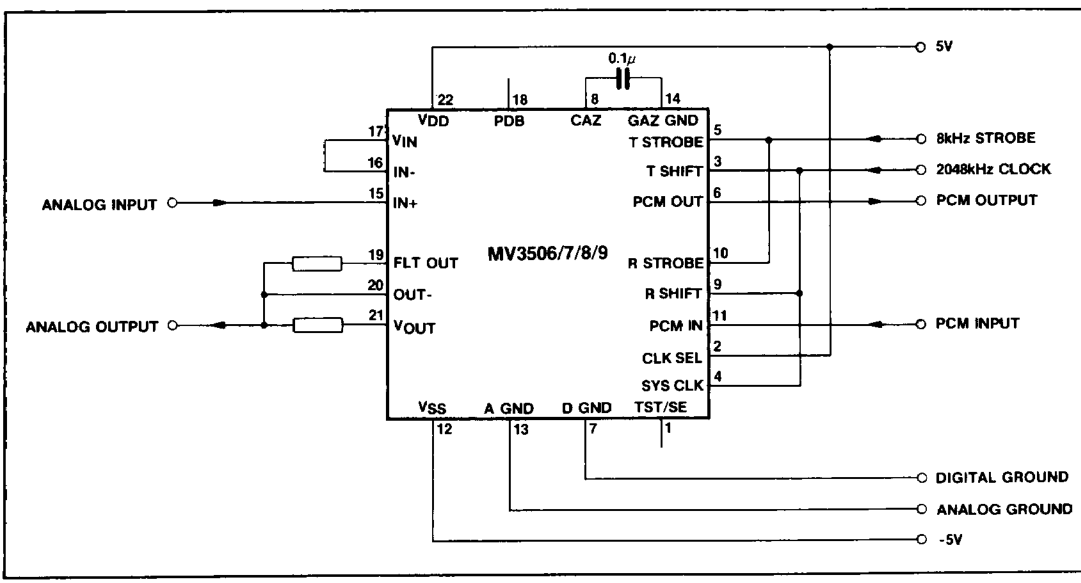

Fig.14 Simple application circuit