

SILICON GATE CMOS

65,536 WORD x 8 BIT CMOS PSEUDO STATIC RAM

Description

The TC51864PL is a 512K bit high speed CMOS pseudo static RAM organized as 65,536 words by 8 bits. The TC51864PL utilizes a one transistor dynamic memory cell with CMOS peripheral circuitry to provide high capacity, high speed and low power storage. The TC51864PL operates from a single 5V power supply. Refreshing is supported by a refresh (RFSH) input which enables two types of refreshing - auto refresh and self refresh. The TC51864PL features a static RAM-like interface with a write cycle in which the input data is written into the memory cell at the rising edge of R/W thus simplifying the microprocessor interface.

The TC51864PL is available in a 32-pin, 0.6 inch width plastic DIP, and a small outline plastic flat package.

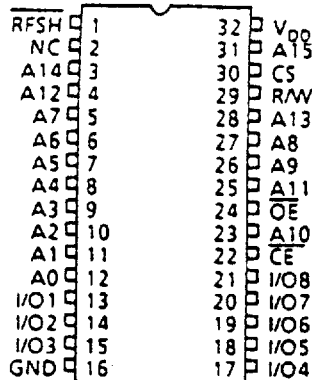
Features

- Organization: 65,536 words x 8 bits
- Single 5V power supply
- Fast access time

	TC51864 Family	
	-85	-10
t _{CEA} CE Access Time	85ns	100ns
t _{OE} OE Access Time	35ns	40ns
t _{RC} Cycle Time	135ns	160ns
Power Dissipation	385mW	330mW
Self Refresh Current	100µA	

- Auto refresh is supported by an internal refresh address counter
- Self refresh is supported by an internal timer
- Inputs and outputs TTL compatible
- Refresh: 256 refresh cycles/4ms
- Package
 - TC51864PL: DIP32-P-600
 - TC51864FL: SOP32-P-525

Pin Connection (Top View)



Pin Names

A0 - A15	Address Inputs
R/W	Read/Write Control Input
OE	Output Enable Input
RFSH	Refresh Input
CE	Chip Enable Input
CS	Chip Select Input
I/O1 ~ I/O8	Data Inputs/Outputs
V _{DD}	Power
GND	Ground
NC	No Connect

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	—	$V_{DD} + 1.0$	V	
V_{IL}	Input Low Voltage	-1.0	—	0.8	V	

DC Characteristics ($T_a = 0 \sim 70^\circ\text{C}$, $V_{DD} = 5V \pm 10\%$)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES	
I_{DDO}	Operating Current (Average) CE, Address cycling: $t_{RC} = t_{RC \text{ min.}}$	85ns version	—	50	70	mA	3, 4
		100ns version	—	40	60		
I_{DDS1}	Standby Current $\overline{CE} = V_{IH}$, $\overline{RFSH} = V_{IH}$	—	—	1	mA		
I_{DDS2}	Standby Current $\overline{CE} = V_{DD} - 0.2V$, $\overline{RFSH} = V_{DD} - 0.2V$	—	—	100	μA		
I_{DDF1}	Self Refresh Current (Average) $\overline{CE} = V_{IH}$, $\overline{RFSH} = V_{IL}$	—	—	1	mA		
I_{DDF2}	Self Refresh Current (Average) $\overline{CE} = V_{DD} - 0.2V$, $\overline{RFSH} = 0.2V$	—	50	100	μA		
$I_{I(L)}$	Input Leakage Current $0V \leq V_{IN} \leq V_{DD}$. All other Inputs not under test = 0V	—	—	± 10	μA		
$I_{O(L)}$	Output Leakage Current Output Disabled ($\overline{CE} = V_{IH}$ or $\overline{OE} = V_{IH}$ or $R/W = V_{IL}$) $0V \leq V_{OUT} \leq V_{DD}$	—	—	± 10	μA		
V_{OH}	Output High Level $I_{OH} = -1\text{mA}$	2.4	—	—	V		
V_{OL}	Output Low Level $I_{OL} = 2.1\text{mA}$	—	—	0.4	V		

Capacitance* ($V_{DD} = 5V$, $T_a = 25^\circ\text{C}$, $f = 1\text{MHz}$)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance (A0 - A15)	—	5	pF
C_{I2}	Input Capacitance (\overline{CE} , CS, \overline{OE} , R/W, \overline{RFSH})	—	7	
C_{IO}	Input/Output Capacitance	—	7	

*This parameter is periodically sampled and is not 100% tested.

AC Characteristics (Ta = 0 ~ 70°C, V_{DD} = 5V±10%) (Notes: 5, 6, 7, 8, 13)

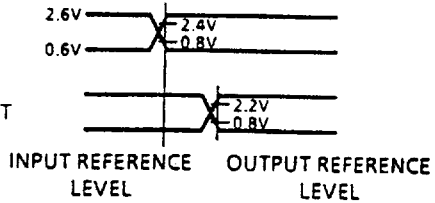
SYMBOL	PARAMETER	-85		-10		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.		
t _{RC}	Random Read, Write Cycle Time	135	—	160	—	ns	
t _{RMW}	Read Modify Write Cycle Time	190	—	220	—		
t _{CE}	\overline{CE} Pulse Width	85	10,000	100	10,000		
t _p	\overline{CE} Precharge Time	40	—	50	—		
t _{CEA}	\overline{CE} Access Time	—	85	—	100		
t _{OEA}	\overline{OE} Access Time	—	35	—	40		
t _{CLZ}	\overline{CE} to Output in Low -Z	20	—	20	—		
t _{OLZ}	\overline{OE} to Output in Low -Z	0	—	0	—		
t _{WLZ}	Output Active from End of Write	0	—	0	—		
t _{CHZ}	Chip Disable to Output in High-Z	0	25	0	30		9
t _{OHZ}	\overline{OE} Disable to Output in High-Z	0	25	0	30		9
t _{WHZ}	Write Enable to Output in High-Z	0	25	0	30		9
t _{ODS}	\overline{OE} Output Disable Setup Time	0	—	0	—		
t _{ODH}	\overline{OE} Output Disable Hold Time	10	—	10	—		
t _{RCS}	Read Command Setup Time	0	—	0	—		
t _{RCH}	Read Command Hold Time	0	—	0	—		
t _{CSS}	Chip Select Setup Time	0	—	0	—		
t _{CSH}	Chip Select Hold Time	20	—	20	—		
t _{WP}	Write Pulse Width	25	—	25	—		
t _{WCH}	Write Command Hold Time	40	—	40	—		
t _{CWL}	Write Command to \overline{CE} Lead Time	25	—	25	—		
t _{DSW}	Data Setup Time from R/W	20	—	20	—		10
t _{DSC}	Data Setup Time from \overline{CE}	20	—	20	—		10
t _{DHW}	Data Hold Time from R/W	0	—	0	—		10
t _{DHC}	Data Hold Time from \overline{CE}	0	—	0	—		10
t _{ASC}	Address Setup Time	0	—	0	—		11
t _{AHC}	Address Hold Time	20	—	20	—		11
t _{RHC}	\overline{RFSH} Command Hold Time	15	—	15	—		
t _{FC}	Auto Refresh Cycle Time	135	—	160	—		
t _{RFD}	\overline{RFSH} Delay Time from \overline{CE}	40	—	50	—		
t _{FAP}	\overline{RFSH} Pulse Width (Auto Refresh)	80	8,000	80	8,000		12
t _{FP}	\overline{RFSH} Precharge Time	30	—	30	—		12
t _{FAS}	\overline{RFSH} Pulse Width (Self Refresh)	8,000	—	8,000	—		12
t _{FRS}	\overline{CE} Delay Time from \overline{RFSH} (Self Refresh)	135	—	160	—	12	
t _{REF}	Refresh Period (256 cycles, A0 ~ A7)	—	4	—	4	ms	
t _T	Transition Time (Rise and Fall)	3	50	3	50	ns	

Notes:

- 1) Stress greater than those listed under "Maximum Ratings" may cause permanent damage to the device.
- 2) All voltages are referenced to GND.
- 3) I_{DDO} depends on the cycle time.
- 4) I_{DDO} depends on the output loading. Specified values are obtained with the outputs open.
- 5) An initial pause of 100 μ s with high \overline{CE} is required after power-up before proper device operation is achieved.
- 6) AC measurements assume $t_f = 5$ ns.

7) Timing reference levels

Input Levels	:	$V_{IH} = 2.6V$ $V_{IL} = 0.6V$	INPUT
Input Reference Levels	:	$V_{IH} = 2.4V$ $V_{IL} = 0.8V$	OUTPUT
Output Reference Levels	:	$V_{OH} = 2.2V$ $V_{OL} = 0.8V$	

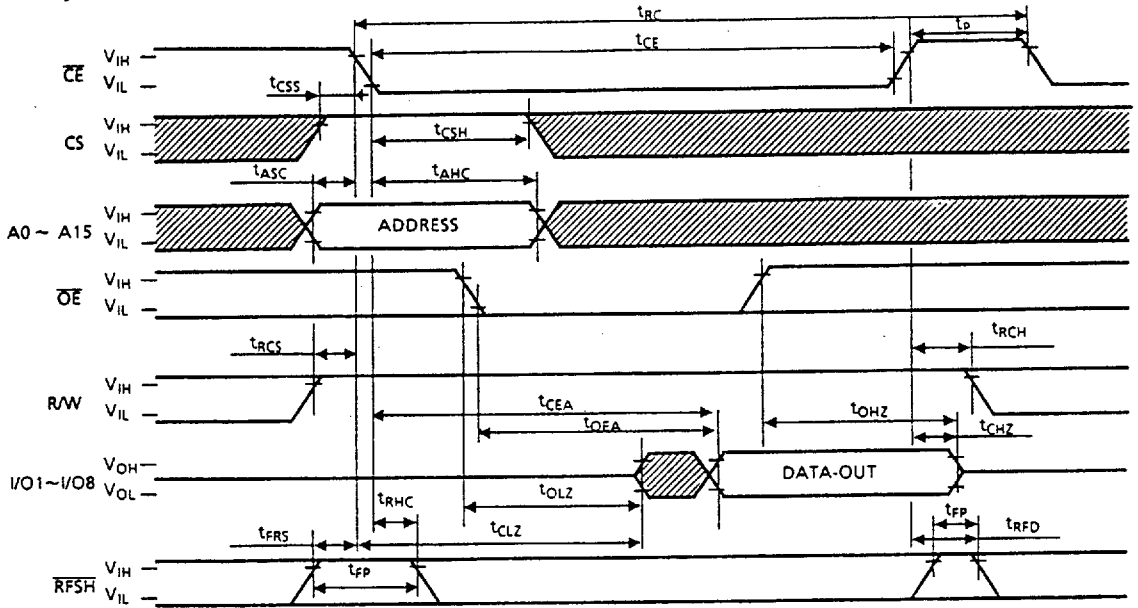


- 8) Measured with a load equivalent to 1 TTL load and 100pF.
- 9) t_{CHZ} , t_{OHZ} , t_{WHZ} define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
- 10) For write cycles, the input data is latched at the earlier of R/W or \overline{CE} rising edge. Therefore, the input data must be valid during the setup time (t_{DSW} or t_{DSC}) and hold time (t_{DHW} or t_{DHC}).
- 11) All address inputs are latched at the falling edge of \overline{CE} . Therefore, all the address inputs must be valid during t_{ASC} and t_{AHC} .
- 12) The two refresh operations, auto refresh and self refresh, are defined by the \overline{RFSH} pulse width under the condition $\overline{CE} = V_{IH}$.
 Auto refresh : \overline{RFSH} pulse width $\leq t_{FAP}$ (max.)
 Self refresh : \overline{RFSH} pulse width $\geq t_{FAS}$ (min.)

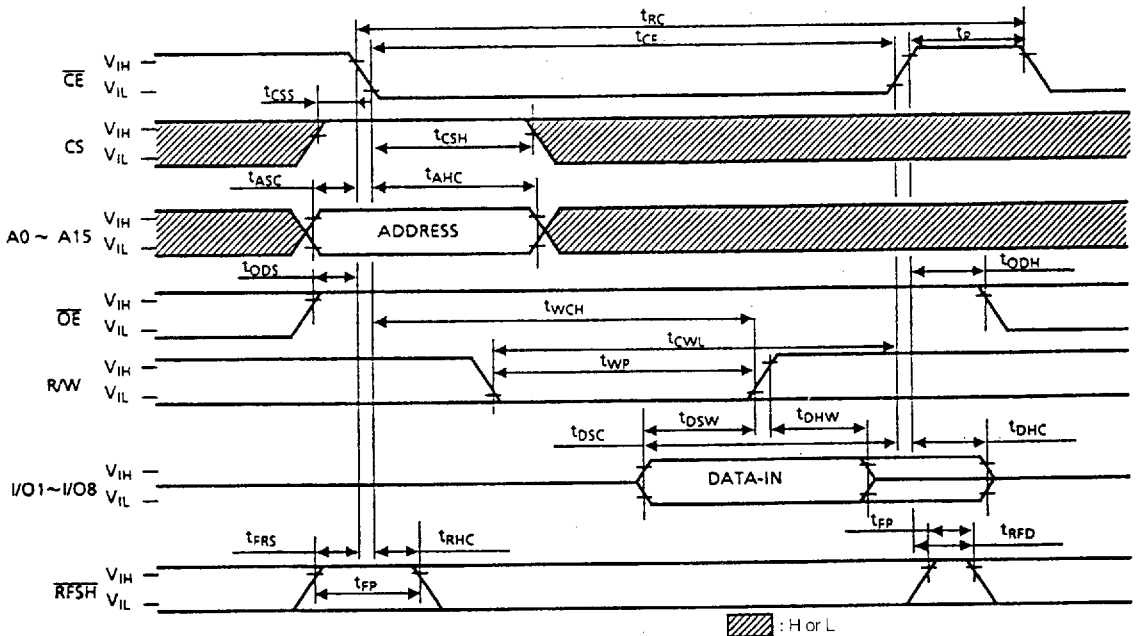
 The timing parameter t_{FRS} must be met for proper device operation under the following conditions:
 - after self refresh
 - if $\overline{RFSH} = "L"$ after power-up
- 13) \overline{CE} only refresh or auto refresh must begin within 15.6 μ s after self refreshing ends.

Timing Waveforms

Read Cycle

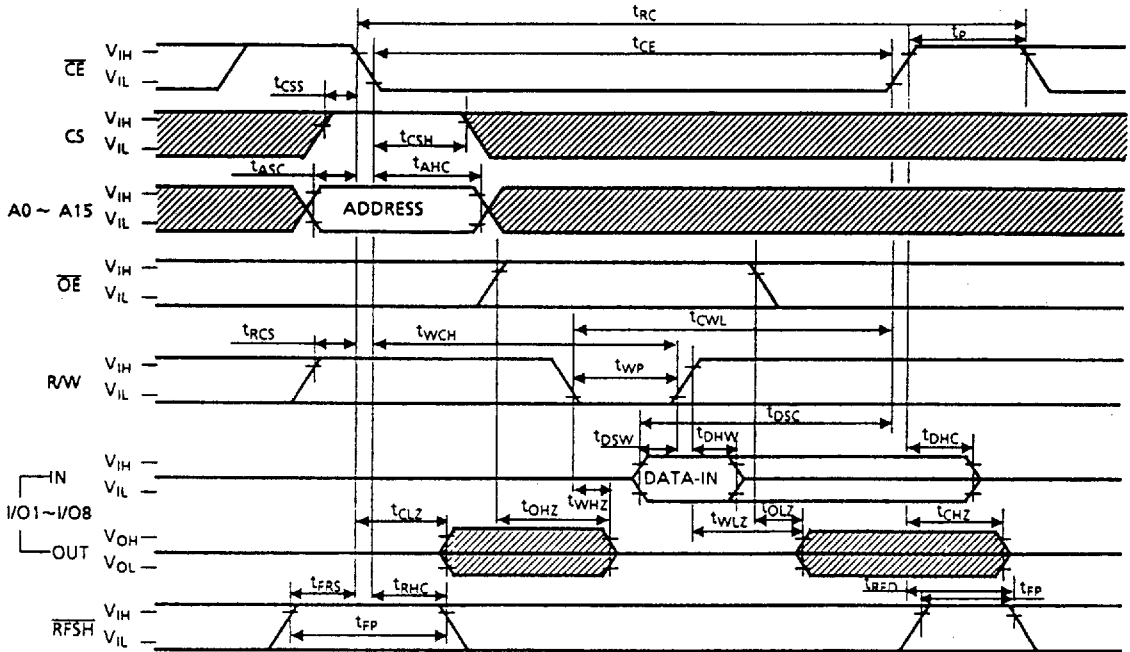


Write Cycle 1 (\overline{OE} Fixed High)

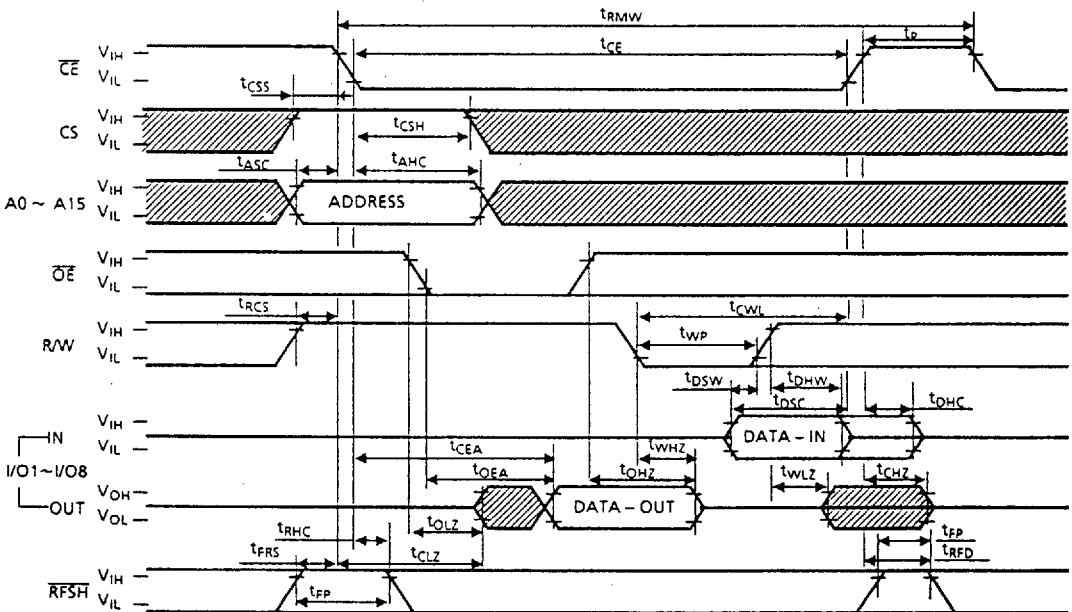


▨ : H or L

Write Cycle 2 (OE Clocked)



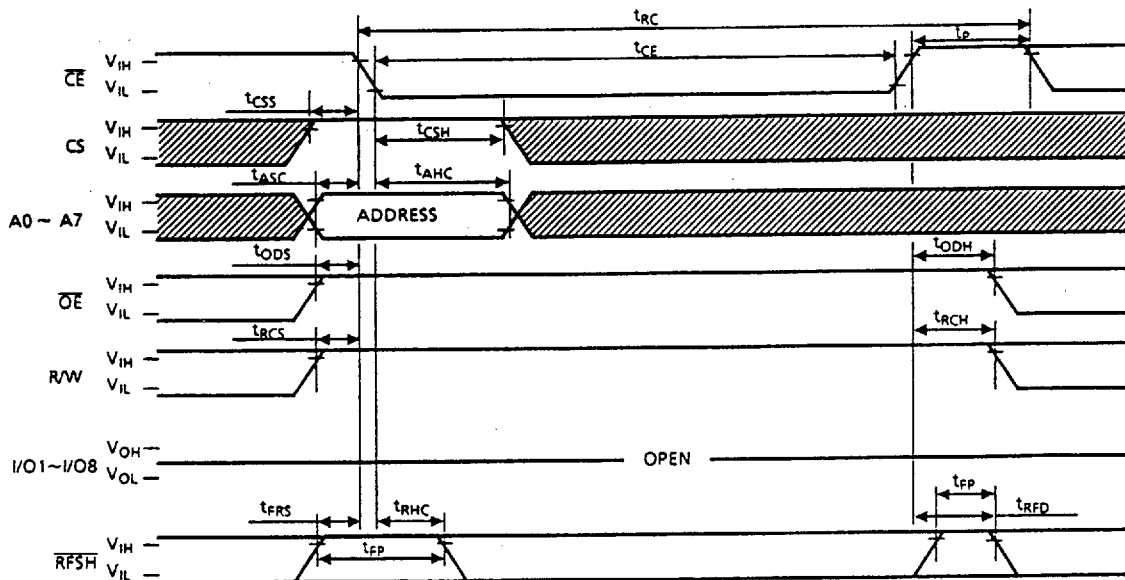
Read Modify Write Cycle



▨ : H or L

9097248 0026479 T10

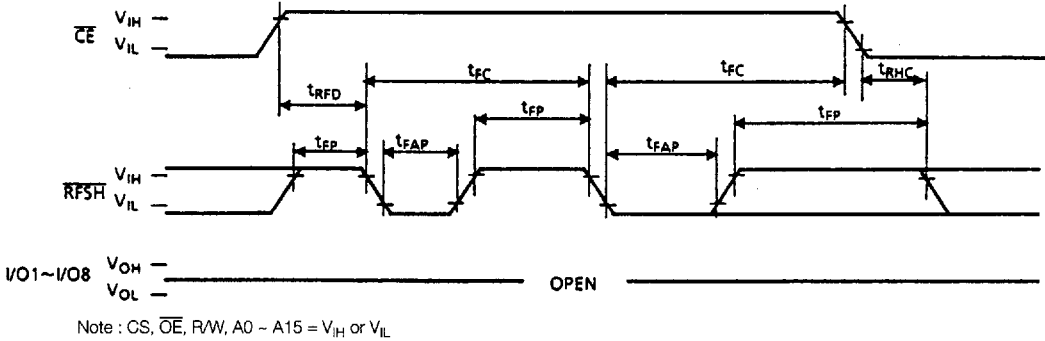
CE Only Refresh



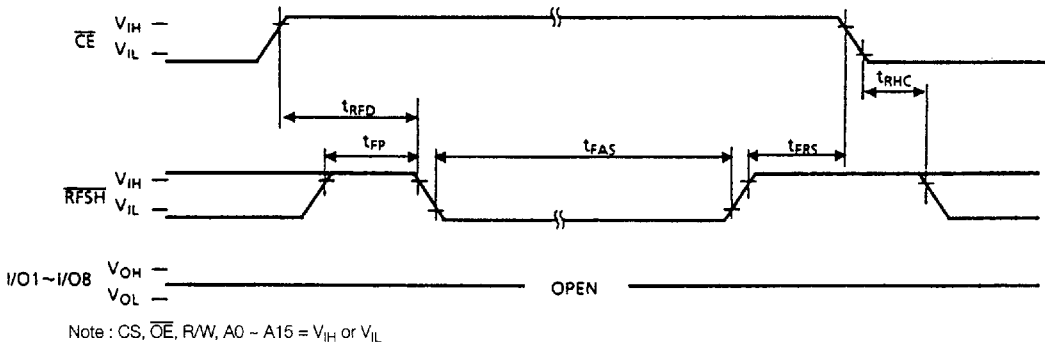
Note: A8 - A15 = V_{IH} or V_{IL}

▨ : H or L

Auto Refresh



Self Refresh



CS Standby Mode

