Preliminary Data Sheet
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microelectronics group

Lucent Technologies
Bell Labs Innovations

FlashDSP®1650 Digital Signal Processor

1 Features

- For 5 V operation:
  — 25 ns instruction cycle time (40 MIPS)
- For 3.3 V operation:
  — 30 ns instruction cycle time (33 MIPS)
- Power-saving features:
  — Low-power 0.6 µm CMOS technology; fully static design
  — Active power: 9.5 mW/MIPS at 5.0 V
    3.3 mW/MIPS at 3.3 V
  — Low-power stopclk: 175 µW at 5.0 V
    66 µW at 3.3 V
- 24 Kwords (maximum) internal flash ROM
- One bank of 1.25 Kwords or two banks of 1 Kword internal RAM
- 16 x 16-bit multiplication and 36-bit accumulation in one instruction cycle
- Two 36-bit accumulators
- Multichannel audio codec, capable of 4 ADC and 3 DAC operations per 16 kHz frame
- Instruction cache for high-speed, program-efficient, zero-overhead looping
- One external vectored interrupt
- Two 64 Kword address spaces with software wait-states for external accesses
- Single-channel serial I/O port; 8-bit data channel
- Programmable phase-locked loop
- Microphone, speaker, and line driver interface circuits
- Four 8-bit and one 4-bit I/O ports for flexible status or control pins
- External memory interface, including DRAM
- Two interrupt timers and one watchdog timer
- 68-pin PLCC, 80-pin MQFP or 100-pin TQFP package
- High- and low-frequency clock options
- Synchronous serial interface unit
- Internal power-loss detection unit
- Object code upward compatible with DSP1600 Digital Signal Processor family
- Supported by DSP165X-ST support tools
- Full-speed in-circuit emulation HDS (HD-supported)

2 Description

The *FlashDSP*1650 is a 16-bit, fixed-point digital signal processor (DSP) based on the DSP1600 core. It is programmable to perform a wide variety of fixed-point signal processing functions. A member of the DSP165X family, the *FlashDSP*1650 includes a mix of peripherals specifically intended to support processing-intensive but cost-sensitive applications. In addition to the core, the *FlashDSP*1650 consists of the following peripheral blocks: external memory interface unit (EMI), synchronous serial interface unit (SSI), five I/O ports (IOPs), two timer units, a watchdog timer, an analog interface, and a JTAG interface; as well as one bank of 1.25 Kwords or two banks of 1 Kword of RAM. The *FlashDSP*1650 is part of a low-cost, high-performance solution for consumer product applications.

The *FlashDSP*1650 is available in the following packages:

- 68-pin PLCC (See Figure 1 on page 13.)
- 80-pin MQFP (See Figure 2 on page 14.)
- 100-pin TQFP (See Figure 3 on page 15.)

The *FlashDSP*1650 achieves high throughput without programming restrictions or latencies due to its parallel pipelined architecture. The processor has an arithmetic unit capable of a 16 x 16-bit multiplication and 36-bit accumulation, or a 32-bit ALU operation in one instruction cycle. Data is accessed from memory through two independent addressing units.

A fully static, low-power, 0.6 µm CMOS design and a low-power standby mode support power-sensitive equipment applications. A single external crystal allows the use of a high-frequency and a low-frequency clock. Under program control, the *FlashDSP*1650 can be switched between the high-frequency and low-frequency clock options. When switched to the low-frequency clock, the power is reduced and can be further reduced using a stop-clock mode.

The *FlashDSP*1650 device is the development platform for the DSP1651/52 and DSP1653. To support full-speed in-circuit emulation, the *FlashDSP*1650 device includes an internal HDS module and an internal flash ROM for program store.

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2 Description (continued)

The DSP1653 is identical to the *FlashDSP*1650 except that it contains mask-programmable internal ROM in place of flash ROM, it does not include an HDS module, and it has only 1.25 Kwords and a single bank of RAM.

The DSP1651 is a subset of the DSP1653. It contains 4 Kwords of internal ROM, 704 words of internal RAM, no external memory interface, and does not include line driver 2, programmable amplifier 2, or AI 5—7.

2.1 Functional Differences Between the DSP1651 and the 80-Pin PLCC *FlashDSP*1650

The DSP1651 is offered only in the 80-pin MQFP package. It is the production version of 80-pin MQFP *FlashDSP* 1650. Table 1 lists the differences between the DSP1651 and the 80-pin MQFP *FlashDSP*1650.

Table 1. Functional Differences Between the DSP1651 and the 80-Pin PLCC *FlashDSP* 1650

Difference	DSP1651	*FlashDSP*1650
ROM	4 Kword (diffusion)	24 Kword, internal flash
RAM	One bank of 700 word only (IR2KEN = 0)*	1 bank of 1.25 Kword (IR2KEN = 0) or 2 banks of 1 Kword (IR2KEN = 1)
Packages	80-pin MQFP only (Pin V_{PP} is tied to V_{DD}.)	68-pin PLCC 80-pin MQFP 100-pin TQFP
Power-loss Detect Settings	**chipo** register bits PLC[2:0] hard-coded with ROM mask	Programmable through **chipo** register bits PLC[2:0]†
Full-speed In-circuit Emulation	JTAG but not HDS‡	HD supported
I/O Ports	8-bit: A, C, E; 6-bit: —; 3-bit: B	8-bit: A, C, E; 6-bit: —; 3-bit: B
Line Drivers	LDOP, LDON	LDOP, LDON
Programmable Gain Amplifier	PGIN, PGOUT	PGIN, PGOUT
Analog Interface (AI–)	I[P, N], 2, 3, 4	I[P, N], 2, 3, 4
External Memory Interface	None	None

* For DSP1651, users should reset IR2KEN, **chipo**[9] = 0. When set, only the memory map in Table 11 applies.
† See Table 45 on page 62 for **chipo** register bits PLC[2:0].
‡ Still supports read/write to registers and internal RAM, and read of internal ROM if the secure bit is not set.

2 Description (continued)

2.2 Functional Differences Between the DSP1653 and the 100-Pin TQFP *FlashDSP*1650

The DSP1653 is offered only in a 100-pin TQFP package. Table 2 lists the differences between the DSP1653 and 100-pin TQFP *FlashDSP*1650.

Table 2. Functional Differences Between the DSP1653 and the 100-Pin TQFP *FlashDSP*1650

Difference	DSP1653	*FlashDSP*1650
ROM	24 Kword (diffusion)	24 Kword, internal flash
RAM	One bank of 1.25 Kword only (IR2KEN = 0)*	1 bank of 1.25 Kword (IR2KEN = 0) or 2 banks of 1 Kword (IR2KEN = 1)
Packages	100-pin TQFP only (Pin V_{PP} is tied to V_{DD}.)	68-pin PLCC 80-pin MQFP 100-pin TQFP
Power-loss Detect Settings	**chipo** register bits PLC[2:0] hard-coded with ROM mask	Programmable through **chipo** register bits PLC[2:0]†
Full-speed In-circuit Emulation	JTAG but not HDS‡	HD supported
I/O Ports	8-bit: A, B, C, E; 4-bit: D	8-bit: A, B, C, D§, E; 4-bit: —

* For DSP1653, users should reset IR2KEN, **chipo**[9] = 0. When set, only the memory map in Table 11 applies.
† See Table 45 on page 62 for **chipo** register bits PLC[2:0].
‡ Still supports read/write to registers and internal RAM, and read of internal ROM if the secure bit is not set.
§ Versions 1, 2, and 3 of *FlashDSP* 1650 provides IOPD[0:3], the same as DSP1653. Version 4 of *FlashDSP* 1650 provides IOPD[0:7].

2.3 Functional Differences Between the DSP1654 and the 100-Pin TQFP *FlashDSP*1650

The DSP1654 is offered only in a 100-pin TQFP package. Table 3 lists the differences between the DSP1654 and 100-pin TQFP *FlashDSP*1650.

Table 3. Functional Differences Between the DSP1654 and the 100-Pin TQFP *FlashDSP*1650

Difference	DSP1654	*FlashDSP*1650
ROM	32 Kword VIA	24 Kword, internal flash
RAM	One bank of 2 Kword only (IR2KEN = 0)*	1 bank of 1.25 Kword (IR2KEN = 0) or 2 banks of 1 Kword (IR2KEN = 1)
Packages	100-pin TQFP only (Pin V_{PP} is tied to V_{DD}.)	68-pin PLCC 80-pin MQFP 100-pin TQFP
Power-loss Detect Settings	**chipo** register bits PLC[2:0] hard-coded with ROM mask	Programmable through **chipo** register bits PLC[2:0]†
I/O Ports	8-bit: A, B, C, D, E	8-bit: A, B, C, D‡, E

* For DSP1654, users should reset IR2KEN, **chipo**[9] = 0. When set, only the memory map in Table 11 applies.
† See Table 45 on page 62 for **chipo** register bits PLC[2:0].
‡ Versions 1, 2, and 3 of *FlashDSP*1650 provides IOPD[0:3]. Version 4 of *FlashDSP*1650 provides IOPD[0:7] the same as DSP1654.

2 Description (continued)

2.4 Functional Differences Between the DSP1655 and the *FlashDSP*1650

Table 4 lists the differences between the DSP1655 and *FlashDSP*1650.

Table 4. Functional Differences Between the DSP1655 and the *FlashDSP*1650

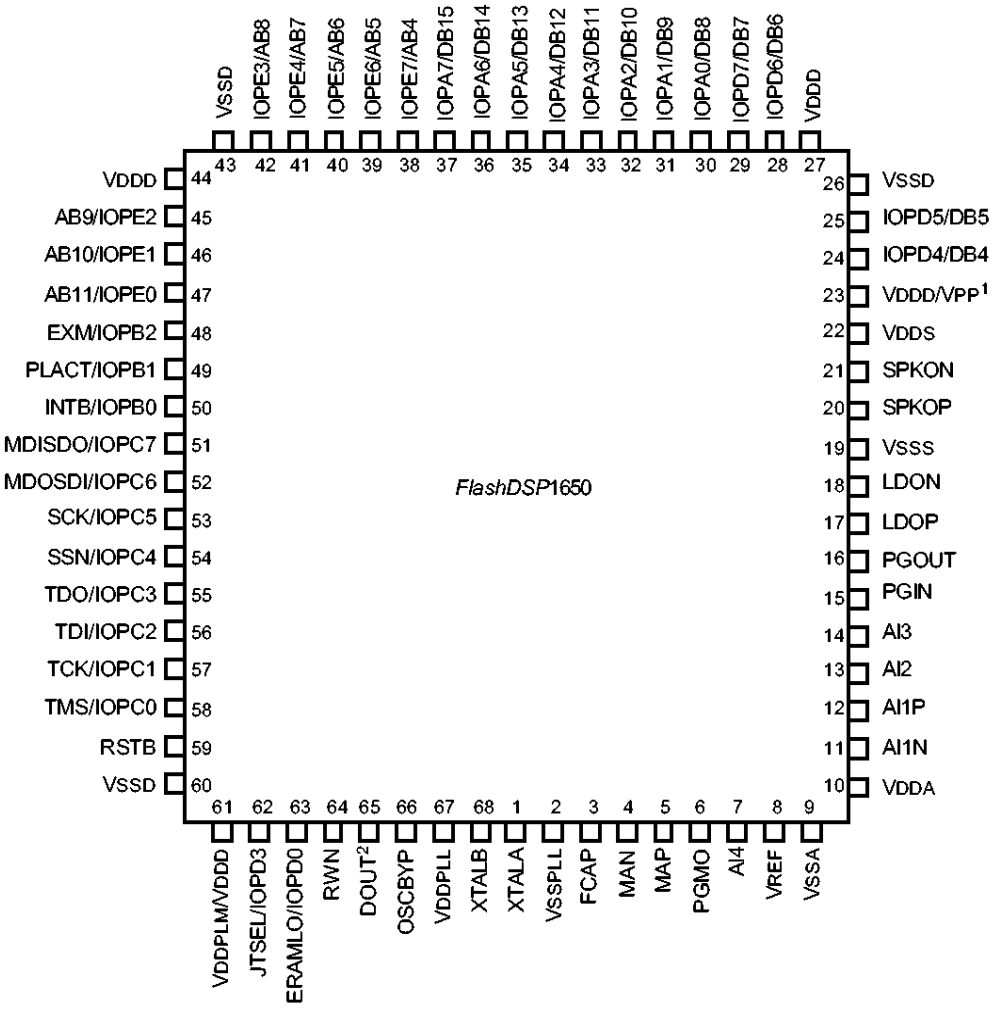
Difference	DSP1655	*FlashDSP*1650
ROM	16 Kword on chip	24 Kword, internal flash
RAM	One bank of 1.25 Kword only (IR2KEN = 0)*	1 bank of 1.25 Kword (IR2KEN = 0) or 2 banks of 1 Kword (IR2KEN = 1)
Packages	68-pin PLCC 100-pin TQFP	68-pin PLCC 80-pin MQFP 100-pin TQFP
Power-loss Detect Settings	**chipo** register bits PLC[2:0] hard-coded with ROM mask	Programmable through **chipo** register bits PLC[2:0]†
Full-speed In-circuit Emulation	JTAG but not HDS‡	HD supported
I/O Ports: 68-pin PLCC 80-pin MQFP 100-pin TQFP	8-bit: 6-bit: 3-bit: A, C, E D B — — — A, B, C, D, E — —	8-bit: 6-bit: 3-bit: A, C, E D B A, C, E — B A, B, C, D§, E — —
Line Drivers: 68-pin PLCC 80-pin MQFP 100-pin TQFP	 LDOP, LDON — LDOP, LDON	 LDOP, LDON LDOP, LDON LDOP, LDON, LDOP2, LDON2
Programmable Gain Amplifier: 68-pin PLCC 80-pin MQFP 100-pin TQFP	 PGIN, PGOUT — PGIN, PGOUT	 PGIN, PGOUT PGIN, PGOUT PGIN, PGOUT, PGIN2, PGOUT2
Analog Interface (AI–): 68-pin PLCC 80-pin MQFP 100-pin TQFP	 I[P, N], 2, 3, 4 — I[P, N], 5[P, N], 2, 3, 4	 I[P, N], 2, 3, 4 I[P, N], 2, 3, 4 I[P, N], 5[P, N], 2, 3, 4, 6, 7
External Memory Interface: 68-pin PLCC 80-pin MQFP 100-pin TQFP	Address Bus: Data Bus: AB[11:4] DB[15:4] — AB[11:0] DB[15:0]	Address Bus: Data Bus: AB[11:4] DB[15:4] — — AB[15:0] DB[15:0]
JTAG Test Mode Interface: JTSEL: 68-pin PLCC 80-pin MQFP 100-pin TQFP TDO, TDI, TCLK, and TMS: 68-pin PLCC 80-pin MQFP 100-pin TQFP	 Multiplexed with IOPD3 — Multiplexed with IOPD3 Multiplexed with IOPC[3:0] — Multiplexed with IOPC[3:0]	 Multiplexed with IOPD3 A dedicated pin Multiplexed with IOPD3 Multiplexed with IOPC[3:0] Multiplexed with IOPC[3:0] Can choose to multiplex with IOPC[3:0] or use dedicated pins

* For DSP1655, users should reset IR2KEN, **chipo**[9] = 0. When set, only the memory map in Table 11 applies.
† See Table 45 on page 62 for **chipo** register bits PLC[2:0].
‡ Still supports read/write to registers and internal RAM, and read of internal ROM if the secure bit is not set.
§ Version 4 of *FlashDSP*1650 provides IOPD[0:7]. Versions 1, 2, and 3 provides only IOPD[0:3].

3 Pin Information

The *FlashDSP*1650 is available in the following packages:

- 68-pin PLCC (See Figure 1.)
- 80-pin MQFP (See Figure 2 on page 14.)
- 100-pin TQFP (See Figure 3 on page 15.)



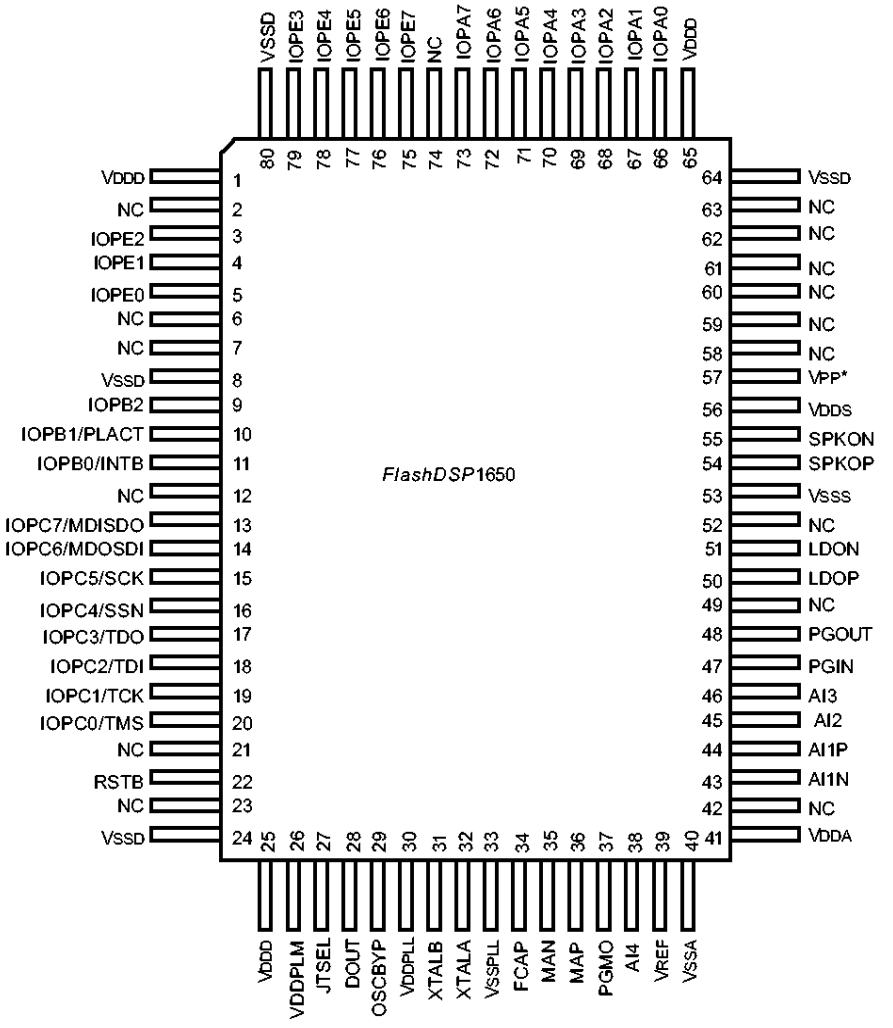
1. VPP becomes VDD for nonflash versions of the device.
2. DOUT is also known as CKO.

Note: VDDPLM and VDDD are connected to the same pin.

5-3995(C).a

Figure 1. *FlashDSP*1650 68-Pin PLCC Pin Diagram

3 Pin Information (continued)

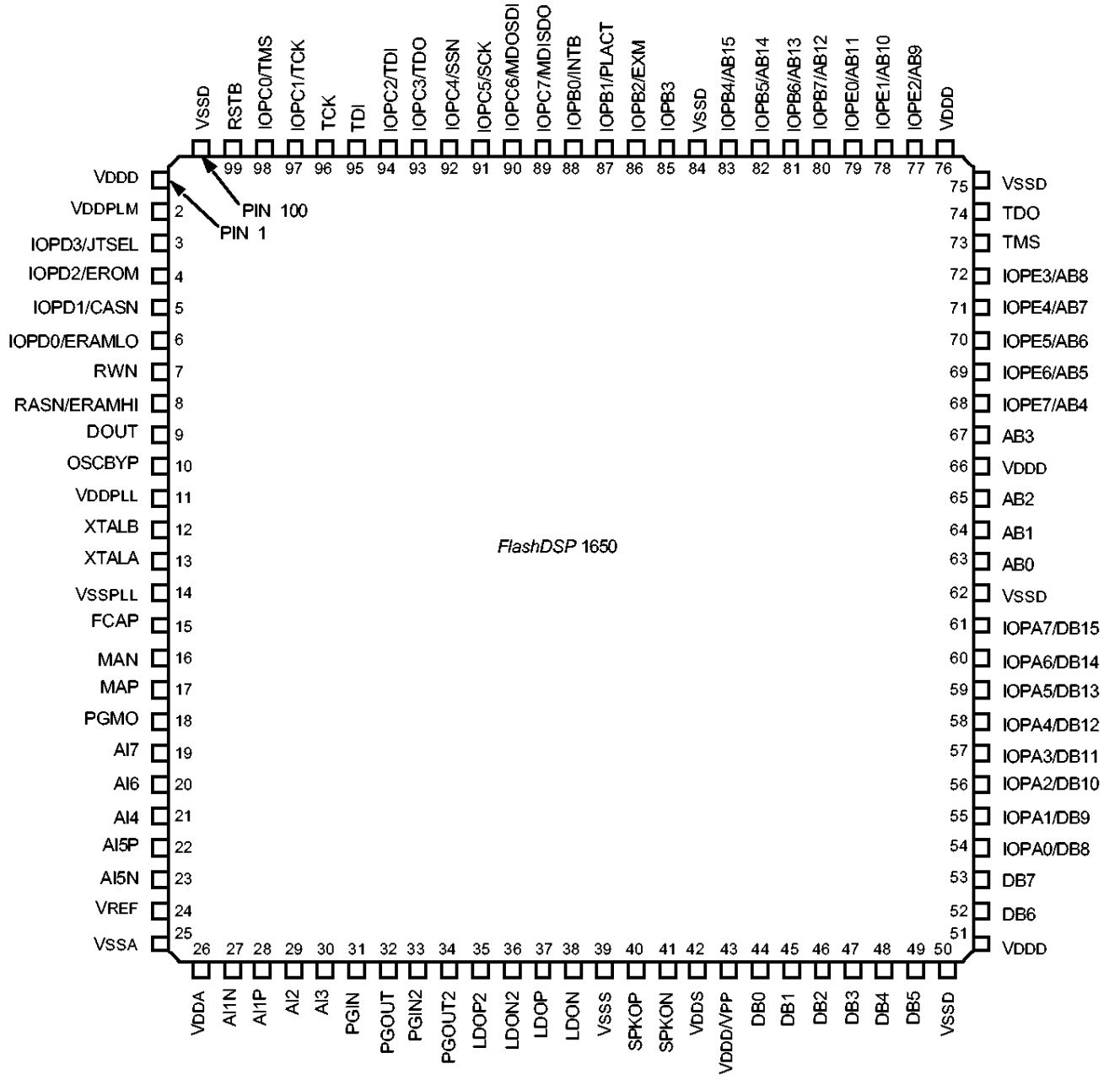


* VPP becomes VDD for nonflash versions of the device, i.e., DSP1651 and DSP1653.

5-4003(C).a

Figure 2. *FlashDSP*1650 80-Pin MQFP Pin Diagram

3 Pin Information (continued)



* VPP becomes VDD for nonflash versions of the device, i.e., DSP1651 and DSP1653.

5-4003(C).a

Figure 3. *FlashDSP*1650 100-Pin TQFP Pin Diagram

3 Pin Information (continued)

Figure 4 shows *FlashDSP*1650 pins organized into their functional groups. Tables 5 and 6 and Sections 3.1 through 3.11 describe these pins.

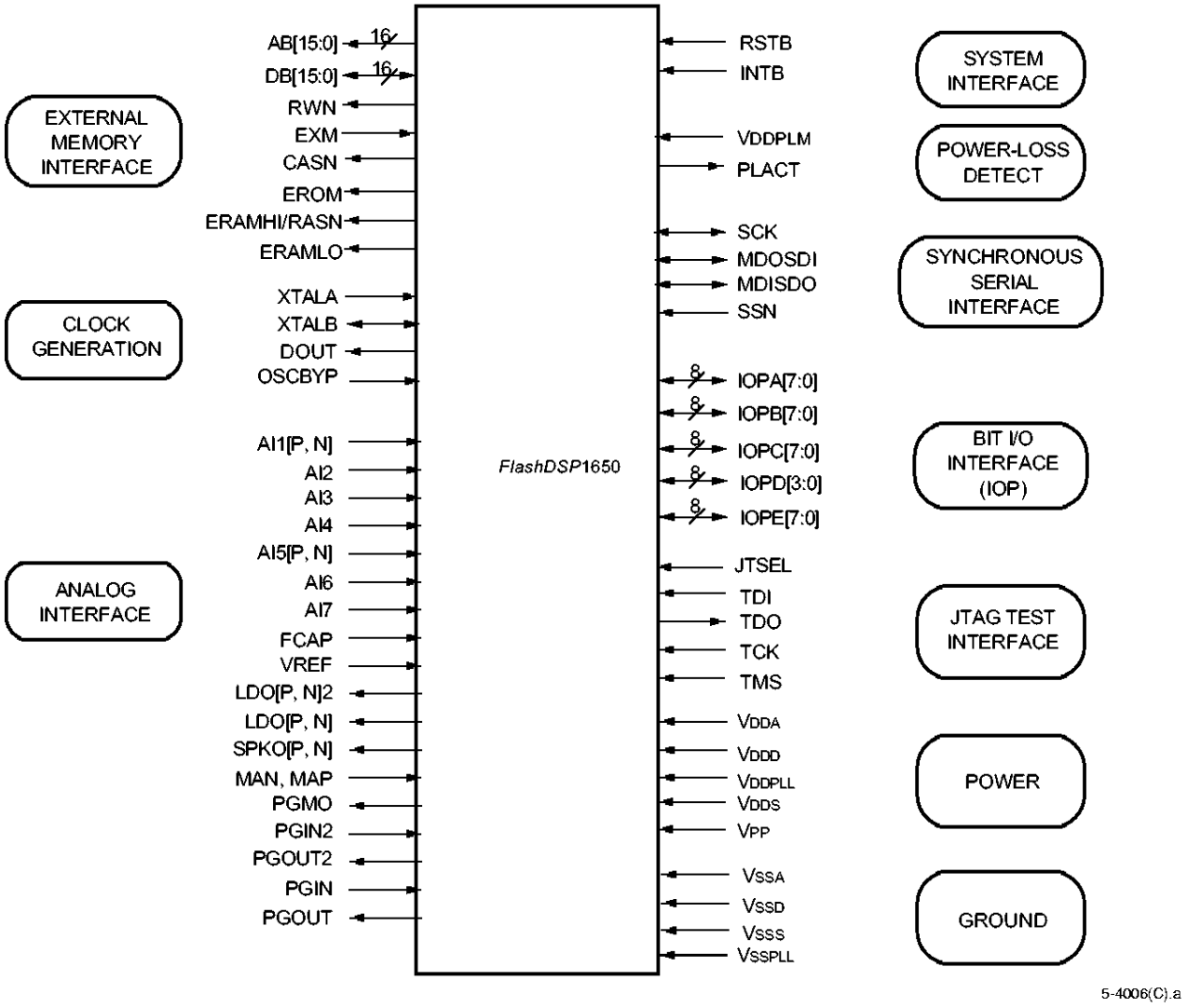


Figure 4. *FlashDSP*1650 Pinout by Group

Note: The *FlashDSP*1650 80-pin MQFP package has no AB[15:0], AI[7:6], AI5N, AI5P, DB[15:0], EXM, IOPB3, IOPD[2:0], EROM, ERAMLO, LDON2, LDOP2, PGIN2, PGOUT2, RASN/ERAMHI, CASN, or RWN pin.

3 Pin Information (continued)

For each *FlashDSP*1650 pin listed in Table 5:

- Each entry in the Type column is one of the following:
  - —I (input)
  - —I/O (input/output)
  - —O (output)
  - —OD (open-drain output)
  - —TO (3-state output)
- Each entry in the Active column is one of the following:
  - —High
  - —Low
  - —Pgm (programmable polarity)
  - —Neg (negative edge triggered)

Table 5. *FlashDSP*1650 Pinout

Symbol	Pin Number		Type	Active	Pin Description
	80-Pin MQFP	100-Pin TQFP			
AB[2:0]	—	63—65	O	High	16-bit external memory address bus, bits 15—0. Pins AB[15:4] are multiplexed with IOPB[4:7] and IOPE[0:7] in the 100-pin TQFP. (The 80-pin MQFP has no AB pins, but does have IOP pins.)
AB[3]	—	67			
AB[8:4]	—	68—72			
AB[15:9]	—	77—83			
AI1N	43	27	I	—	Differential analog pair.
AI1P	44	28			
AI5N	—	23	I	—	Second differential analog pair. (The 80-pin MQFP has no AI5N or AI5P pins.)
AI5P	—	22			
AI[7:6]	—	19—20	I	—	Single-ended analog inputs. (The 80-pin MQFP has no AI[7:6] pins.)
AI4	38	21			
AI[3:2]	46—45	30—29			
CASN	—	5	O	Low	Column address select; multiplexed with IOPD1. (The 80-pin MQFP has no CASN pin.)
DB[5:0]	—	49—44	I/O	High	Data bus for read or write transaction to external memory data bus. DB[15:8] are multiplexed with IOPA[7:0]. (The 80-pin MQFP has no DB pins.)
DB[15:6]	—	61—52			
DOUT	28	9	O	High	Processor clock; digital output/clock output.
ERAMHI/ RASN	—	8	O	Low	External RAM, high select, or row address select. (The 80-pin MQFP has no ERAMHI/RASN pin.)
ERAMLO	—	6	O	Low	External RAM, low select; multiplexed with IOPD0. (The 80-pin MQFP has no ERAMLO pin.)
EROM	—	4	O	Low	External ROM select; multiplexed with IOPD2. (The 80-pin MQFP has no EROM pin.)
EXM	—	86	I	High	External memory enable; multiplexed with IOPB2. (The 80-pin MQFP has no EXM pin.)
FCAP	34	15	O	—	Microphone power supply output.
INTB	11	88	I	Neg	External interrupt, negative edge triggered; multiplexed with IOPB0.
IOPA[7:0]	73—66	61—54	I/O	Pgm	I/O port A (bits 7—0). (In the 100-pin TQFP, pins IOPA[7:0] are multiplexed with pins DB[15:8].)

3 Pin Information (continued)

Table 5. *FlashDSP*1650 Pinout (continued)

Symbol	Pin Number		Type	Active	Pin Description
	80-Pin MQFP	100-Pin TQFP			
IOPB[7:4]	—	80—83	I/O	Pgm	I/O port B (bits 7—0). (The 80-pin MQFP has no IOPB[7:3] pins. In the 100-pin TQFP, pins IOPB[7:4] are multiplexed with pins AB[12:15], and pin IOPB2 is multiplexed with EXM. In both packages, IOPB[1:0] are multiplexed with pins PLACT and INTB, respectively.)
IOPB[3]	—	85			
IOPB[2:0]	9—11	86—88			
IOPC[7:2]	13—18	89—94	I/O	Pgm	I/O port C (bits 7—0); multiplexed with pins MDISDO, MDOSDI, SCK, SSN, TDO, TDI, TCK, and TMS, respectively.
IOPC[1:0]	19—20	97—98			
IOPD[3:0]	—	3—6	I/O	Pgm	I/O port D (bits 3—0); multiplexed with pins JTSEL, EROM, CASN, and ERAMLO, respectively. (The 80-pin MQFP has no IOPD pins.)
IOPE[7:3]	75—79	68—72	I/O	Pgm	I/O port E (bits 7—0). (In the 100-pin TQFP, pins IOPE[7:0] are multiplexed with pins AB[4:11].)
IOPE[2:0]	3—5	77—79			
JTSEL	27	3	I	High	JTAG select. (In the 100-pin TQFP, JTSEL is multiplexed with IOPD3.)
LDOP	50	37	O	—	Differential output for interface to a telephone line.
LDON	51	38			
LDOP2	—	35	O	—	Second differential output to telephone line. (The 80-pin MQFP has no LDOP2 or LDON2 pins.)
LDON2	—	36			
MAN	35	16	I	—	Microphone amplifier positive and negative inputs.
MAP	36	17			
MDISDO	13	89	I/O	—	SSI master data in/slave data out; multiplexed with IOPC7.
MDOSDI	14	90	I/O	—	SSI master data out/slave data in; multiplexed with IOPC6.
OSCBYP	29	10	I	High	Oscillator bypass.
PGIN	47	31	I	—	Programmable gain input.
PGIN2	—	33		—	Programmable gain input for two-line applications. (The 80-pin MQFP has no PGIN2 pin.)
PGMO	37	18	O	—	Programmable gain amplifier output for the microphone amplifier.
PGOUT	48	32	O	—	Programmable gain output.
PGOUT2	—	34	O	—	Programmable gain output for two-line applications. (The 80-pin MQFP has no PGOUT2 pin.)
PLACT	10	87	O	High	Power-loss active; multiplexed with IOPB1.
RSTB	22	99	I/O	Low	Reset.
RWN	—	7	O	—	Read/write not. (The 80-pin MQFP has no RWN pin.)
SCK	15	91	I/O	—	SSI serial clock; multiplexed with IOPC5.
SPKON	55	41	O	—	Speaker differential outputs.
SPKOP	54	40			
SSN	16	92	I	Low	SSI serial slave select; multiplexed with IOPC4.

3 Pin Information (continued)

Table 5. *FlashDSP*1650 Pinout (continued)

Symbol	Pin Number		Type	Active	Pin Description
	80-Pin MQFP	100-Pin TQFP			
TCK	19	96 and 97	I	—	Test clock (JTAG). (In the 100-pin TQFP, TCK is connected to two pins; pin 97 is multiplexed with IOPC1.)
TDI	18	95 and 94	I	High	Test data in (JTAG). (In the 100-pin TQFP, TDI is connected to two pins; pin 94 is multiplexed with IOPC2.)
TDO	17	74 and 93	O	High	Test data in (JTAG). (In the 100-pin TQFP, TDO is connected to two pins; pin 93 is multiplexed with IOPC3.)
TMS	20	73 and 98	I	High	Test mode select (JTAG). (In the 100-pin TQFP, TMS is connected to two pins; pin 98 is multiplexed with IOPC0.)
V_{DDPLM}	26	2	I	High	V_{DD} power-loss monitor.
V_{REF}	39	24	I	—	Voltage reference for the converter.
XTALA	32	13	I/O	—	Crystal oscillator connection.
XTALB	31	12			

Table 6. *FlashDSP*1650 Power Supply, Ground, and Unconnected Pins

Symbol	Pin Number		Pin Description
	80-Pin MQFP	100-Pin TQFP	
V_{DDA}	41	26	Supply for analog circuitry (5 V or 3.3 V).
V_{SSA}	40	25	Ground for analog circuitry.
V_{DDD}	1, 25, 65	1, 51, 66, 76	Supply for digital circuitry (5 V or 3.3 V).
V_{SSD}	8, 24, 64, 80	50, 62, 75, 84, 100	Ground for digital circuitry.
V_{DDPLL}	30	11	Supply for phase-locked loop (should be connected to V_{DDD}).
V_{SSPLL}	33	14	Ground for phase-locked loop (should be connected to V_{SSD}).
V_{DDS}	56	42	Supply for speaker driver.
V_{SSS}	53	39	Ground for speaker driver.
V_{PP}	57	43	Programming supply for flash ROM. V_{PP} becomes a V_{DD} pin for nonflash devices (DSP1651, DSP1652, and DSP1653).
NC	2, 6, 7, 12, 21, 23, 42, 49, 52, 58—63, 74	—	No connection.

3 Pin Information (continued)

3.1 System Interface

3.1.1 XTALA, XTALB

Crystal Oscillator. Input/Output. The external crystal is connected between these two pins, which places the crystal in the feedback loop of the on-chip crystal oscillator. The output of the crystal oscillator is used as a reference for the phase-locked loop (PLL) and codec. The frequency of the oscillator input must be 4.096 MHz.

3.1.2 RSTB

Reset. Bidirectional (Schmitt trigger). Negative assertion. A high-to-low transition on RSTB causes the *FlashDSP*1650 to enter the reset state. Upon deassertion, the *FlashDSP*1650 begins execution from location 0x0000.

Note: This input contains a Schmitt trigger providing a hysteresis between positive- and negative-going transitions. When power-loss detect or watchdog timer is triggered, RSTB is pulled low.

3.1.3 INTB

Interrupt. Input (Schmitt trigger). Negative edge triggered. External interrupt to the *FlashDSP*1650, PLL, and codec. This input contains a Schmitt trigger providing a hysteresis between positive- and negative-going transitions. An interrupt is posted when a negative-going transition is detected. Also, note that there is no acknowledge pin. External hardware must guarantee that the interrupt service routine has completed before issuing another interrupt on INTB.

Any activity on INTB is **not** recognized during the interrupt service routine and must be reissued after the interrupt service routine has completed. This input contains a Schmitt trigger providing a hysteresis between positive- and negative-going transitions.

3.1.4 DOUT

Digital Output. Output. The default of the pin is to output CLKLOW, the internal low-power oscillator clock. DOUT is selectable through the **clkc** register (see Table 44 on page 61). The following options are selectable: internal low-power oscillator, an input crystal clock, a free-running clock, a wait-stated clock, a logic 0, or a logic 1.

3.1.5 PLACT

Power-Loss Active. Output. The power-loss detect is set in the **chipo**[2:0] register. The PLC bit specifies nominal trip and recover voltages. If the supply voltage falls below the minimum required value, the RSTB pin is pulled low. If **chipo**[10] is set to 1 when the power-loss detect circuit is triggered, the PLACT pin is asserted high for the duration of the power-loss condition.

3.1.6 VDDPLM

VDD Power-Loss Monitor. Input. This pin should be connected to VDD to enable the internal power-loss detect circuit. Power loss is set in **chipo**[2:0]. When grounded, the power-loss circuit is disabled.

3.2 External Memory Interface

3.2.1 AB[15:0]

Address Bus. Output. Address bus for read or write transactions to external memory or I/O. Pins AB[15:4] are multiplexed with IOPB[4:7] and IOPE[0:7] in the 100-pin TQFP.

3.2.2 DB[15:0]

Data Bus. Bidirectional. Data bus for read or write transactions to external memory or I/O.

DB[15:8]. DB[15:8] are multiplexed with IOPA[7:0]. See the description of the IOPA in Section 3.4.

DB[7:0]. Lower 8 bits of the data bus. Each pin has an internal pull-down resistor that is typically 68 kΩ.

3.2.3 ERAMLO

External RAM Low Select. Output. Negative assertion. Asserted when the ERAMLO segment in the Y memory space is accessed. The leading edge of ERAMLO may be programmed to be delayed by one-half a clock cycle.

3 Pin Information (continued)

3.2 External Memory Interface (continued)

3.2.4 ERAMHI/RASN

External RAM Hi Select/Row Address Select. Output. Negative assertion. The function of this pin depends on whether the DRAM controller is enabled in the **chipc** register. If the DRAM controller is enabled, this pin functions as RASN. Along with its assertion, the row address is driven on the AB pins. If the DRAM controller is not enabled, this pin functions as ERAMHI and is asserted when the ERAMHI segment in the Y memory (data) space is accessed. The leading edge of ERAMHI may be programmed to be delayed by one-half a clock cycle.

3.2.5 CASN

Column Address Select. Output. Negative assertion. Asserted when the ERAMHI segment in the Y address space is accessed. Along with its assertion, the column address is driven on the AB pins.

3.2.6 RWN

Read/Write Not. Output. When a logic 1, a read access is in progress; when a logic 0, a write access is in progress.

3.2.7 EXM

External Memory Enable. Input. This pin is sampled on the rising edge of RSTB. If sampled high, the DSP boots from external program space and the 16-bit data bus is enabled (using IOPA as a data bus). If sampled low, the DSP boots from internal ROM and the 8-bit data bus is enabled. Note that this pin is multiplexed with IOPB2. See the description of the IOPB in Section 3.4.2.

3.2.8 EROM

External ROM Select. Output. Negative assertion. Asserted when the EROM segment is accessed in the X memory (instruction) space. The leading edge of EROM may be programmed to be delayed by one-half a free-running clock cycle by programming bit 11 of the **chipc** register.

3.3 Synchronous Serial Interface (SSI)

The SSI is configurable for either master mode or slave mode, selectable by the **ssic** register.

3.3.1 SCK

SSI Clock. Bidirectional. If SSI is configured in master mode, this pin is an output providing a clock to the slave devices. If SSI is configured in slave mode, this pin is an input that takes in the serial clock.

3.3.2 MDOSDI

Master Data Out/Slave Data In. Bidirectional. If SSI is configured in master mode, this pin is the serial data output. If SSI is configured in slave mode, this pin is the serial data input. The SSI is either master or slave, according to the **ssic** register MSTR field.

3.3.3 MDISDO

Master Data In/Slave Data Out. Bidirectional. If SSI is configured in master mode, this pin is the serial data input. If SSI is configured in slave mode, this pin is the serial data output. The SSI is either master or slave, according to the **ssic** register MSTR field.

3.3.4 SSN

Serial Select. Input. Negative assertion. When SSI is configured as a slave, the assertion of SSN signals the slave that it is being addressed to transfer data with the master device. If this pin is asserted while SSI is configured as a master, a mode fault is detected by SSI. Alternatively, in master mode, this pin can be configured to act as a general-purpose IOP pin.

3 Pin Information (continued)

3.4 I/O Port Interface (IOP)

3.4.1 IOPA[7:0]

I/O Port A. Bidirectional. These pins may be individually configured to be inputs or outputs. As outputs, each bit may be set, cleared, or toggled under program control. As inputs, they may be read. Note that IOPA pins are multiplexed with the upper 8 bits of the data bus as follows:

- IOPA0/DB8
- IOPA1/DB9
- IOPA2/DB10
- IOPA3/DB11
- IOPA4/DB12
- IOPA5/DB13
- IOPA6/DB14
- IOPA7/DB15

3.4.2 IOPB[7:0]

I/O Port B. Bidirectional. These pins may be individually configured to be inputs or outputs. As outputs, each bit may be set, cleared, or toggled under program control. As inputs, they may be read. Note that IOPB pins are multiplexed as follows:

- IOPB0/INTB
- IOPB1/PLACT
- IOPB2/EXM
- IOPB3
- IOPB4/AB15
- IOPB5/AB14
- IOPB6/AB13
- IOPB7/AB12

The 80-pin MQFP has no IOPB[7:3] pins. In both packages, IOPB[1:0] are multiplexed with pins PLACT and INTB, respectively.

3.4.3 IOPC[7:0]

I/O Port C. Bidirectional. These pins may be individually configured to be inputs or outputs. As outputs, each bit may be set, cleared, or toggled under program control. As inputs, they may be read.

Note that IOPC pins are multiplexed with other pins as follows:

- IOPC0/TMS
- IOPC1/TCK
- IOPC2/TDI
- IOPC3/TDO
- IOPC4/SSN
- IOPC5/SCK
- IOPC6/MDOSDI
- IOPC7/MDISDO

3.4.4 IOPD[3:0]

I/O Port D. Bidirectional. These pins may be individually configured to be inputs or outputs. As outputs, each bit may be set, cleared, or toggled under program control. As inputs, they may be read. Note that IOPD pins are multiplexed with other pins as follows:

- IOPD0/ERAMLO
- IOPD1/CASN
- IOPD2/EROM
- IOPD3/JTSEL

3.4.5 IOPE[7:0]

I/O Port E. Bidirectional. These pins may be individually configured to be inputs or outputs. As outputs, each bit may be set, cleared, or toggled under program control. As inputs, they may be read. Note that in the 100-pin TQFP, IOPE pins are multiplexed with other pins as follows:

- IOPE0/AB11
- IOPE1/AB10
- IOPE2/AB9
- IOPE3/AB8
- IOPE4/AB7
- IOPE5/AB6
- IOPE6/AB5
- IOPE7/AB4

3 Pin Information (continued)

3.5 JTAG Test Mode Interface

3.5.1 TCK

Test Clock. Input. JTAG serial shift clock that clocks data into TDI and out of TDO and controls the JTAG port by latching TMS into the state machine controller.

3.5.2 TMS

Test Mode Select. Input. JTAG mode control signal that controls the state of the JTAG controller. TMS is sampled on the rising edge of TCK. This pin has an internal pull-up resistor that is typically 68 kΩ.

3.5.3 TDI

Test Data Input. Input. JTAG serial input of all serial-scanned data and instructions that is sampled on the rising edge of TCK. This pin has an internal pull-up resistor that is typically 68 kΩ.

3.5.4 TDO

Test Data Output. 3-state Output. JTAG serial output of all serial-scanned data and status bits. TDO changes on the falling edge of TCK.

3.5.5 JTSEL

JTAG Select. Input. JTSEL is multiplexed with IOPD3. This pin is sampled on the rising edge of RSTB. If sampled high, the four multiplexed JTAG pins will be active in place of IOPC[3:0], and the unmultiplexed JTAG pins will be inactive. If sampled low, the unmultiplied JTAG pins will be active and, the IOP[3:0] pins will behave as normal IOP signals.

3.6 Line Drivers

3.6.1 LDOP, LDON

Line Driver Output. Output. LDOP and LDON provide a differential output suitable for directly driving a 1200 Ω to 600 Ω transformer interface to the telephone line. The differential drive allows the creation of a hybrid function to reject the outgoing signal with respect to the incoming signal. The resulting incoming signal connects to PGIN or PGIN2.

3.6.2 LDOP2, LDON2

Line Driver Output. Output. LDOP2 and LDON2 provide a second differential output for use with two line applications.

3.7 Microphone Amplifier and Power Supply

3.7.1 FCAP

Microphone Power Supply Output. Output. Connect a 0.33 µF capacitor from FCAP to V_{SSA} to prevent power supply noise from getting into the microphone supply. For 5 V operation, an internal regulator circuit regulates the 5 V analog (V_{DDA}) with respect to analog ground (V_{SSA}) to 4 V FCAP with respect to V_{SSA}. For 3 V operation, an internal switch connects FCAP to V_{DDA}.

Note: If CMXP = 1 in the **cdc** register, the microphone power must be supplied externally to this pin.

3.7.2 PGMO

Programmable Gain Amplifier Output. Output. Connect PGMO to one of the analog inputs AI2, AI3, AI4, AI6, or AI7 through an antialias filter.

3.7.3 MAP

Microphone Amplifier Positive. Input. The differential input signal is amplified by 16 dB plus the additional gain programmed into its associated programmable gain amplifier.

3.7.4 MAN

Microphone Amplifier Negative. Input. The differential input signal is amplified by 16 dB plus the additional gain programmed into its associated programmable gain amplifier.

3.8 Speaker Amplifier

3.8.1 SPKON, SPKOP

Speaker Outputs. Output. In 5 V operation, an 8 Ω speaker can be connected directly across SPKOP and SPKON. In 3 V operation, a 150 Ω load can be driven differentially. Single-ended operation requires the use of blocking capacitors and has poorer power supply rejection.

3 Pin Information (continued)

3.9 Programmable Gain Amplifiers

3.9.1 PGOUT

Programmable Gain. Output. Typically connected to one of the single-ended analog inputs (AI2, AI3, AI4, AI6, or AI7) through an antialias filter.

3.9.2 PGOUT2

Programmable Gain. Output. PGOUT2 is the output of a second programmable gain amplifier for two line applications. The output has a common mode of VREF.

3.9.3 PGIN

Programmable Gain. Input. PGIN is the input for the received telephone line speech signal after the hybrid to reduce the transmitted signal. A dc blocking capacitor is needed at the input.

3.9.4 PGIN2

Programmable Gain. Input. PGIN2 is the input for the second programmable gain amplifier to support two line applications.

3.10 Analog Utility

3.10.1 VREF

Voltage Reference. A 10 µF capacitor should be connected from VREF to VSSA to provide a solid reference for the converter.

3.11 PWR/GND

3.11.1 VDDA

5.0 V or 3.3 V Analog Supply. VDDA is the positive supply for the analog blocks. Separate bypass capacitors should be connected from VDDA to VSSA.

3.11.2 VSSA

Analog Ground. VSSA is the ground return for the analog blocks.

3.11.3 VSSD

Digital Ground. There are five ground pins.

3.11.4 VDDD

Digital 5.0 V or Digital 3.3 V Supply. There are four power pins.

3.11.5 VDDPLL

Phase-Locked Loop Supply. This pin should be connected to VDDD.

3.11.6 VSSPLL

Phase-Locked Loop Ground. This pin should be connected to VSSD.

3.11.7 VDDS

Speaker Driver Supply. For 5 V, 8 Ω applications, use a separate low-impedance trace to your supply. Separate bypass capacitors should be connected from VDDS to VSSS.

3.11.8 VSSS

Speaker Driver Ground. For 5 V, 8 Ω applications, use a low-impedance connection to supply ground.

3.11.9 VPP

Flash ROM Power. VPP is the high-voltage pin required on the development device used during flash ROM programming supply and should be connected to 12 V when erasing or programming the flash ROM. Otherwise, it should be connected to VDDD.

4 Hardware Architecture

The *FlashDSP*1650 device is a 16-bit, fixed-point digital signal processor (DSP). The *FlashDSP*1650 consists of a DSP1600 core together with internal memory and peripherals.

To minimize pin count, the *FlashDSP*1650 multiplexes the following package pins:

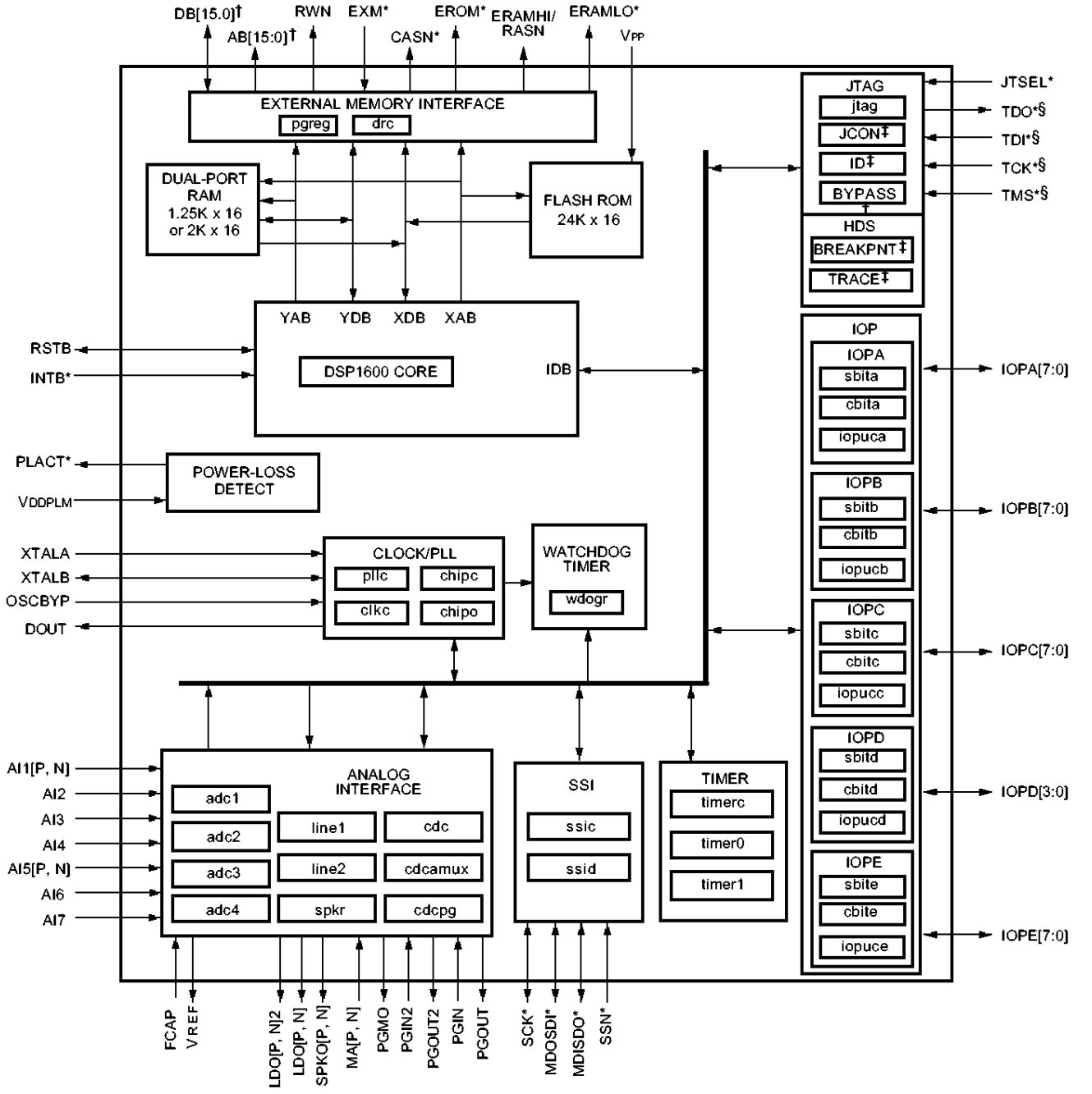
- IOPA0 is multiplexed with DB8.
- IOPA1 is multiplexed with DB9.
- IOPA2 is multiplexed with DB10.
- IOPA3 is multiplexed with DB11.
- IOPA4 is multiplexed with DB12.
- IOPA5 is multiplexed with DB13.
- IOPA6 is multiplexed with DB14.
- IOPA7 is multiplexed with DB15.
- IOPB0 is multiplexed with INTB.
- IOPB1 is multiplexed with PLACT.
- IOPB2 is multiplexed with EXM.
- IOPB4 is multiplexed with AB15.
- IOPB5 is multiplexed with AB14.
- IOPB6 is multiplexed with AB13.
- IOPB7 is multiplexed with AB12.
- IOPC0 is multiplexed with TMS.
- IOPC1 is multiplexed with TCK.
- IOPC2 is multiplexed with TDI.
- IOPC3 is multiplexed with TDO.
- IOPC4 is multiplexed with SSN.
- IOPC5 is multiplexed with SCK.
- IOPC6 is multiplexed with MDOSDI.
- IOPC7 is multiplexed with MDISDO.
- IOPD0 is multiplexed with ERAMLO.
- IOPD1 is multiplexed with CASN.
- IOPD2 is multiplexed with EROM.
- IOPD3 is multiplexed with JTSEL.
- IOPE0 is multiplexed with AB11.
- IOPE1 is multiplexed with AB10.
- IOPE2 is multiplexed with AB9.
- IOPE3 is multiplexed with AB8.
- IOPE4 is multiplexed with AB7.
- IOPE5 is multiplexed with AB6.
- IOPE6 is multiplexed with AB5.
- IOPE7 is multiplexed with AB4.

4.1 *FlashDSP*1650 Architectural Overview

Figure 5 on page 26 shows a block diagram of the *FlashDSP*1650, which consists of the modules described in Sections 4.1.1 through 4.1.12. Table 7, on page 27, shows a legend for the *FlashDSP*1650 block diagram. Certain modules contain internal registers that are illustrated (not to scale) in Figure 5. The DSP has a pair of internal buses (address bus and data bus) for program/coefficient memory (X memory space) and a second independent pair of internal buses for data memory (Y memory space).

4 Hardware Architecture (continued)

4.1 *FlashDSP*1650 Architectural Overview (continued)



5-3792(C).1

* These pins are multiplexed with IOP pins.
† DB[15:8] and AB[15:4] are multiplexed with IOP pins.
‡ These registers are accessible only through the JTAG pins.
§ Only available as multiplexed signals for the DSP1651; available as direct and multiplexed signals for the *FlashDSP*1650 and DSP1653.

Figure 5. *FlashDSP*1650 Block Diagram

4 Hardware Architecture (continued)

4.1 *FlashDSP*1650 Architectural Overview (continued)

Table 7. *FlashDSP*1650 Block Diagram Legend

Symbol	Name
adc<1—4>	Analog-to-digital converter data registers for digital input to *FlashDSP*1650.
BREAKPNT	Four instruction breakpoint registers.
BYPASS	JTAG bypass register.
cbit<a—e>	Control registers for IOP<A—E>.
cdc	Codec control register.
cdcamux	Analog-to-digital converter input multiplexing control.
cdcpg	Amplifier gain control register.
chipc	Chip control register—controls the EMI and other miscellaneous functions.
chipo	Chip option register—configures the watchdog timer, the power-loss detect circuit, and other miscellaneous functions.
clkc	Clock control register.
DPRAM	Internal dual-port random-access memory.
drc	DRAM control register.
flash ROM	Internal flash read-only memory (IFROM).
HDS	Hardware development system module.
ID	JTAG device identification register.
IDB	Internal data bus.
IOP	Input/output port unit.
IOP<A—E>	Input/output port units IOPA, IOPB, IOPC, IOPD, and IOPE.
JCON	JTAG control register.
jtag	16-bit serial/parallel register.
line1	Digital-to-analog converter data register for line driver #1 output.
line2	Digital-to-analog converter data register for line driver #2 output.
pgreg	Page register for row address value.
pllc	Phase-lock loop control register.
ROM	Internal read-only memory.
sbit<a—e>	Status registers for IOP<A—E>.
spkr	Digital-to-analog converter data register for speaker amplifier output.
SSI	Synchronous serial interface unit.
ssic	SSI control register.
ssid	SSI data register.
TIMER	Programmable timer unit.
timer<0—1>	Timer running count registers.
timerc	Timer control register.
TRACE	Program discontinuity trace buffer.

4 Hardware Architecture (continued)

4.1 *FlashDSP*1650 Architectural Overview (continued)

Table 7. *FlashDSP*1650 Block Diagram Legend (continued)

Symbol	Name
wdogr	Watchdog timer register.
XAB	X space (program space) address bus.
XDB	X space data bus.
YAB	Y space (data space) address bus.
YDB	Y space data bus.

4.1.1 DSP1600 Core

The DSP1600 core is the heart of the *FlashDSP*1650 device. The core consists of a data arithmetic unit (DAU), two address arithmetic units (XAAU and YAAU), an instruction cache, and a control section. The core provides support for external memory wait-states and internal dual-port RAM, and features vectored interrupts and a trap mechanism. (For more information, see Section 4.2 on page 31.)

4.1.2 Dual-Port RAM (DPRAM)

This module contains two banks of zero wait-state memory in the *FlashDSP*1650. It consists of one 1.25K 16-bit words or two 1K 16-bit words and has separate address and data ports to the instruction/coefficient and data memory spaces. A program can reference memory from either space at any time, transparently and without restriction. The DSP1600 core automatically performs the required multiplexing. In the event that references to both ports of a single bank of DPRAM are made simultaneously, the DSP1600 core automatically inserts a wait-state and performs the data-port access first, followed by the instruction/coefficient-port access.

A program can be downloaded from slow external memory into DPRAM and then be executed without wait-states. DPRAM is also useful for improving convolution performance in cases where the coefficients are adaptive. Because DPRAM can be downloaded through the JTAG port, full-speed, remote in-circuit emulation is possible. DPRAM can also be used for downloading self-test code through the JTAG port.

4.1.3 Read-Only Memory (ROM)

The *FlashDSP*1650 contains 24K of 16-bit words of zero wait-stated, user-programmable flash ROM for program and fixed coefficients. A mask-programmable secure option that prohibits reading out the ROM contents externally, is available on production chips. This is accomplished by prohibiting the selection of memory map 3.

4.1.4 External Memory Interface (EMI)

The EMI connects the *FlashDSP*1650 to external memory and I/O devices. It supports read operations from instruction/coefficient memory (X memory space) and read/write operations from/to data memory (Y memory space). The DSP1600 core automatically controls the EMI. Instructions can transparently reference external memory from either set of internal buses (i.e., instruction/coefficient and data) simultaneously. Through the EMI, both SRAMs and DRAMs can be interfaced to the DSP. Because the two internal buses are multiplexed to a single external bus, a reference to external data is not allowed in the same cycle that a reference is made to external instruction/coefficient. For more information on the EMI, see Section 4.6. Also see Section 4.4, Memory Maps and Wait-States.

4 Hardware Architecture (continued)

4.1 *FlashDSP*1650 Architectural Overview (continued)

4.1.5 Timers

Two interrupt timers are provided in the *FlashDSP* 1650. They are used to provide an interrupt at the expiration of a programmed interval. The interrupt may be a single interrupt or a repetitive interrupt. TIMER0 counts cycles of the free-running core clock, has a clock prescaler, and supports over nine orders of magnitude of interval selection. TIMER1 counts at the frequency of the low-frequency clock (CLKLOW), has a prescaler, and supports over six orders of magnitude of interval selection. The timers may be stopped and restarted at any time. For more information, see Section 4.9.

4.1.6 Watchdog Timer

A watchdog timer can be used to protect from catastrophic loss of control of the DSP. It can be programmed for one of three time-out intervals. The watchdog timer clock is nominally 32 kHz, selectable as the divided-down input clock or the internal ring oscillator output. For more information, see Section 4.10.

4.1.7 Analog Interface

The analog interface includes an audio codec, a programmable speaker amplifier, a programmable microphone amplifier with power supply, user-selectable single-ended and differential analog inputs, programmable gain amplifier(s), and line driver(s). The audio codec performs up to four analog-to-digital conversions and up to three digital-to-analog conversions in a single 16 kHz frame. For more information, see Section 4.11.

4.1.8 Input/Output Ports (IOP)

Four 8-bit IOP units (IOPA, IOPB, IOPC, IOPE) and one 4-bit IOP unit (IOPD) provide convenient and efficient monitoring and control of 36 individually configurable pins. When configured as outputs, the pins can be individually set, cleared, toggled, or left unchanged. When configured as inputs, the entire port can be read (those configured as inputs as well as those configured as outputs). Note that some of the pins of the IOP units are multiplexed with other functions. See Section 4.8.

4.1.9 JTAG

The JTAG section contains logic that implements the JTAG/*IEEE** P1149.1 standard four-signal test port. No boundary-scan register is included. The JTAG port provides a mechanism for the DSP1600 core to communicate with remote test equipment or a remote hardware development system (DSP1600 HDS or *FlashDSP*1600 HDS). The JTAG port also supports program, memory, and register upload/download, and execution start/stop.

A 4-bit instruction register, a bypass register, and a device identification register have been implemented (see Table 42 on page 59). The instructions for accessing the ID and BYPASS registers are 0xE (1110) and 0xF (1111), respectively. There is no separate TRST input pin.

4.1.10 Synchronous Serial Interface Units (SSI)

One independent SSI unit is compatible with the SPI interface of the *Motorola*† 68HC11 microncontroller. All the features of the 68HC11 SPI interface are supported‡. The DSP core can be interrupted upon completion of an SSI data transfer. The SSI pins are multiplexed with IOPC, under control of a programmable bit in the SSI. For more information, see Section 4.7.

* *IEEE* is a registered trademark of The Institute of Electrical and Electronics Engineers, Inc.
† *Motorola* is a registered trademark of Motorola, Inc.
‡ The open collector mode of operation and slave-initiated transfers are not supported.

4 Hardware Architecture (continued)

4.1 *FlashDSP*1650 Architectural Overview (continued)

4.1.11 Clock Generation

The clock structure for the *FlashDSP*1650 incorporates a wide range of options, including a crystal oscillator, a PLL, a low-frequency divider, and an internal ring oscillator.

The DSP core receives a 2X DSP core clock (two times MIPS rate) that is divided by two inside the core to generate the DSP's non-wait-stated and wait-stated clocks.

It includes one low-power internal oscillator and a crystal oscillator that connects to an external crystal. The **clkc** register bits 7—3 (see Table 44 on page 61) determine which clock is selected to run the core and peripherals.

The *FlashDSP*1650 80-pin MQFP and 100-pin TQFP packages each provide an output clock pin, DOUT. As shown in Table 8, **clkc** register bits 11—8 select one of the DOUT MUX pin output functions.

Table 8. DOUT Pin Output Functions

clkc Register Bits 11—8	DOUT MUX[3:0] Pin Output Function
0000	Ring oscillator (CLKRING) selected to DOUT
0001	Input crystal/clock (CLKIN) selected to DOUT
0010	Low-frequency clock (CLKLOW) selected to DOUT
0011	Wait-stated DSP (CLKWAIT) clock selected to DOUT
0100	Free-running DSP (CLKFREE) clock selected to DOUT
0101	Reserved
0110	Logic 0 selected to DOUT
0111	Logic 1 selected to DOUT
1xxx	Reserved

4.1.12 Power-Loss Detect Circuit

The power-loss detect circuit is enabled by programming the PLC field in the **chipo** register and connecting the V_{DDPLM} pin to the power supply. If the supply voltage falls below the minimum required value, the circuit initiates a device reset. The device does not come out of reset until V_{DDPLM} exceeds the specified recover voltage level specified in the PLC field.

When a power-loss reset occurs, the RSTB pin is driven and held low. Optionally, based on the setting of the PLCKOFF bit in the **chipo** register, the power-loss detect circuit can assert the PLACT pin, which is multiplexed with IOPB1. PLACT is asserted high for the duration of the power-loss condition. When the power-loss detect circuit initiates a device reset, the PLRST bit in the **chipc** register is set, allowing the software to detect such an event.

4 Hardware Architecture (continued)

4.2 DSP1600 Core Architectural Overview

Figure 6 shows a block diagram of the DSP1600 core, which consists of the modules described in Sections 4.2.1 through 4.2.4. Table 9, on page 32, contains a legend for the DSP1600 core block diagram.

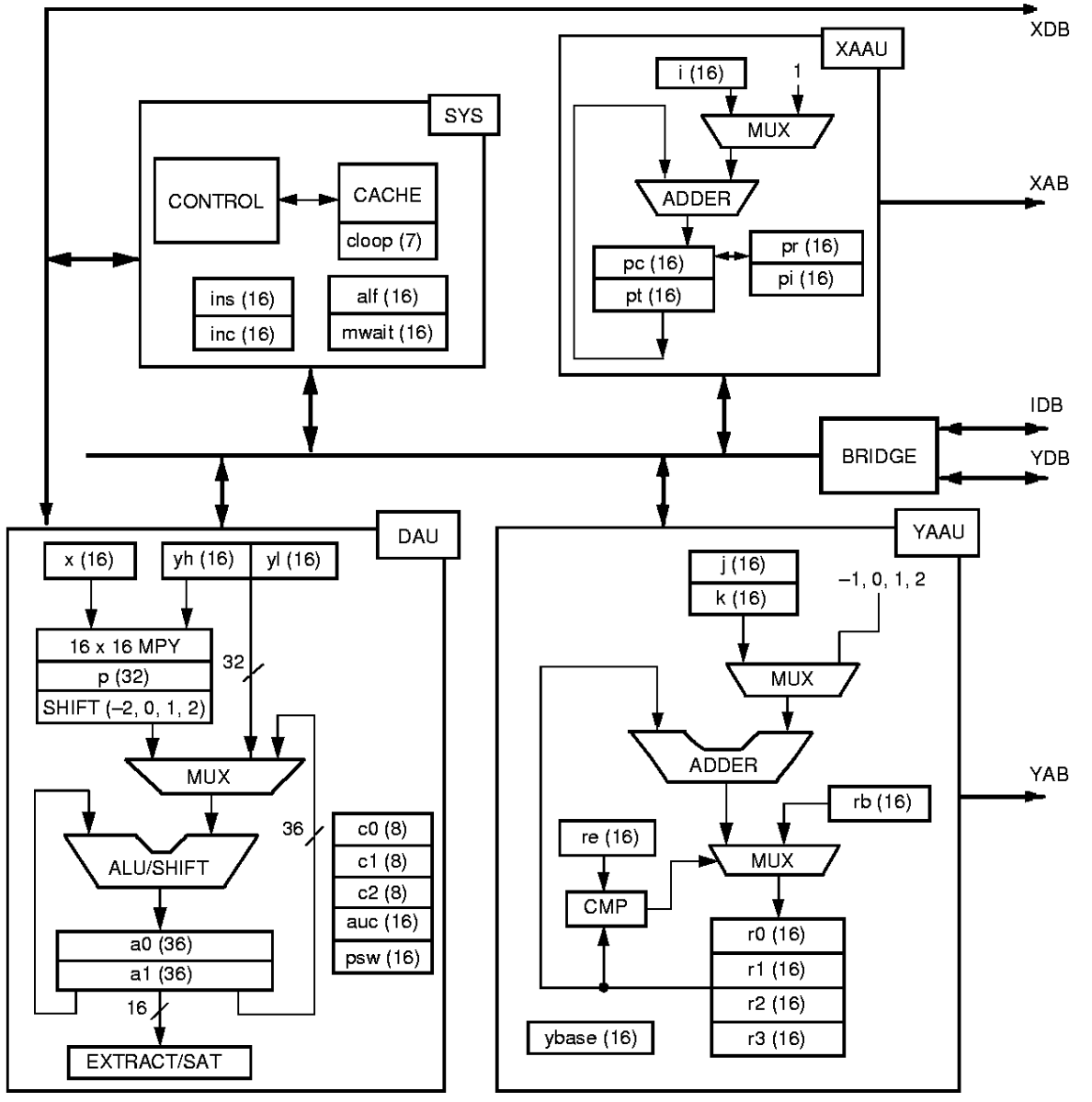


Figure 6. DSP1600 Core Block Diagram

4 Hardware Architecture (continued)

4.2 DSP1600 Core Architectural Overview (continued)

Table 9. DSP1600 Core Block Diagram Legend

Symbol	Name
16 x 16 MPY	16-bit by 16-bit multiplier
a0—a1	Accumulators 0 and 1 (16-bit halves specified as **a0**, **a0l**, **a1**, and **a1l**)*
alf	Low-power standby mode and memory map control
ALU/SHIFT	Arithmetic logic unit/shifter
auc	Arithmetic unit control
c0—c2	Counters 0—2
cloop	Cache loop count
CMP	Comparator
DAU	Digital arithmetic unit
i	Increment register
IDB	Internal data bus
inc	Interrupt control
ins	Interrupt status
j	Increment register
k	Increment register
MUX	Multiplexer
mwait	External memory wait-states control
p	Product register (16-bit halves specified as **p**, **pl**)
PC	Program counter
pi	Program interrupt return register
pr	Program return register
psw	Processor status word
pt	X address space pointer
r0—r3	Y address space pointers
rb	Modulo addressing register (begin address)
re	Modulo addressing register (end address)
SYS	System cache and control section
x	Multiplier input register
XAAU	X space address arithmetic unit
XAB	X space address bus
XDB	X space data bus
YAAU	Y space address arithmetic unit
YAB	Y space address bus
YDB	Y space data bus
ybase	Direct addressing base register
y	DAU register (16-bit halves specified as **y**, **yl**)

* F3 ALU instructions with immediates require specifying the high half of the accumulators as **a0h** and **a1h**.

4 Hardware Architecture (continued)

4.2 DSP1600 Core Architectural Overview (continued)

4.2.1 System Cache and Control Section (SYS)

This section of the core contains a 15-word cache memory and controls the instruction sequencing. It handles vectored interrupts and traps and also provides decoding for registers outside of the DSP1600 core. SYS stretches the processor cycle if wait-states are required (wait-states are programmable for external memory accesses). SYS sequences downloading through JTAG of self-test programs to internal DPRAM.

The cache loop iteration count can be specified at run time under program control as well as at assembly time.

4.2.2 Data Arithmetic Unit (DAU)

The data arithmetic unit (DAU) contains a 16 x 16 parallel multiplier that generates a full 32-bit product in one instruction cycle. The product can be accumulated with one of two 36-bit accumulators. The accumulator data can be directly loaded from, or stored to, memory in two 16-bit words with optional saturation on overflow. The arithmetic logic unit (ALU) supports a full set of arithmetic and logical operations on either 16-bit or 32-bit data. A standard set of flags can be tested for conditional ALU operations, branches, and subroutine calls. This procedure allows the processor to perform as a powerful 16-bit or 32-bit microprocessor for logical and control operations.

The user also has access to two additional DAU registers. The **psw** register contains status information from the DAU. The arithmetic control register, **auc**, is used to configure some of the features of the DAU.

4.2.3 Y Space Address Arithmetic Unit (YAAU)

The YAAU supports high-speed, register-indirect, compound, and direct addressing of data (Y) memory. Four general-purpose 16-bit pointer registers, **r0** to **r3**, are available in the YAAU. These registers can be used to supply the read or write addresses for Y space data.

The YAAU also decodes the 16-bit data memory address and outputs individual memory enables for the data access. The YAAU can address the internal DPRAM or three external memory segments. Up to 48 Kwords of external RAM are addressable.

Two 16-bit registers, **rb** and **re**, allow zero-overhead modulo addressing of data for efficient filter implementations. Two 16-bit signed registers, **j** and **k**, are used to hold user-defined postmodification increments. Fixed increments of +1, –1, and +2 are also available. Four compound addressing modes are provided to make read/write operations more efficient.

The YAAU allows direct (or indexed) addressing of data memory. In direct addressing, the 16-bit base register (**ybase**) supplies the 11 most significant bits of the address. The direct data instruction supplies the remaining 5 bits to form a Y space memory address and also specifies one of 16 registers for source or destination.

4.2.4 X Space Address Arithmetic Unit (XAAU)

The XAAU supports high-speed, register-indirect instruction/coefficient memory addressing with postmodification of the register. The **pt** register is used for addressing coefficients. The signed register **i** holds a user-defined postincrement. A fixed postincrement of +1 is also available. Register PC is the program counter. Registers **pr** and **pi** hold the return address for subroutine calls and interrupts, respectively.

All of the XAAU registers and the adder for increments are 16 bits wide. The XAAU decodes the 16-bit instruction/coefficient address and produces signals for the appropriate X memory segment. The addressable X segments are internal ROM, internal DPRAM, external ROM.

The locations of these memory segments depend upon the memory map selected. A security mode can be selected by mask option. This prevents unauthorized access to the contents of internal ROM.

4.3 Interrupts, Trap, and Low-Power Standby Mode

The *FlashDSP*1650 supports vectored interrupts and a trap. The device has eight internal hardware sources of program interrupt and one external interrupt pin. As shown in Table 10 on page 34, each source of an interrupt and trap has been assigned a unique vector address.

Vectored interrupts are enabled in the **inc** register (see Table 40 on page 59) and monitored in the **ins** register (see Table 41 on page 59).

4 Hardware Architecture (continued)

4.3 Interrupts, Trap, and Low-Power Standby Mode (continued)

Table 10. Interrupt Vectors

Source	Vector	Priority	Issued By
No interrupt	0x0	—	—
Software interrupt	0x2	1 (lowest)	Reserved
SW2	0x1	2	—
JINT	0x42	3	JTAG interrupt
TIME0	0x4	4	TIMER0
IOPD	0x8	5	IOPD interrupt
IOPA	0xc	6	IOPA interrupt
Reserved 6	0x10	7	—
INTB	0x14	8	INTB pin
Reserved 7	0x18	9	—
EMUXBOTH	0x1c	10	External access collision
SSI	0x20	11	SSI
SW4	0x24	12	—
Codec	0x28	13	Internal codec
Reserved 1	0x2c	14	—
Reserved 2	0x30	15	—
TIME1	0x34	16	TIMER1
SW1	0x38	17	—
HDS TRAP	0x3	18 (highest)	HDS/JTAG

4.3.1 Interruptibility

Vectored interrupts are serviced only after an interruptible instruction or the completion of a prior interrupt service routine. If more than one vectored interrupt is asserted at the same time, the interrupts are serviced sequentially according to their assigned priorities. Interrupt service routines, branch and conditional branch instructions, cache loops, and instructions which only decrement one of the RAM pointers, **r0** to **r3** (e.g., ***r3– –**), are not interruptible.

A trap is similar to an interrupt, but it gains control of the processor by branching to the trap service routine even when the current instruction is noninterruptible. It may not be possible to return to normal instruction execution from the trap service routine because the machine state cannot always be saved. In particular, program execution cannot be continued from a trapped cache loop or interrupt service routine. While in a trap service routine, another trap is ignored.

When set to 1, the status bits in the **ins** register indicate that an interrupt has occurred. The processor must reach an interruptible state (completion on an interruptible instruction or a prior interrupt service routine) before an enabled vectored interrupt can be acted on. An interrupt cannot be serviced if it is not enabled. Polled interrupt service can be implemented by disabling the interrupt in the **inc** register and polling the **ins** register for the expected event.

4.3.2 Vectored Interrupts

A logic 1 written to any bit of the **inc** enables (or unmasks) the associated interrupt. If the bit is cleared to a logic 0, the interrupt is disabled (or masked). The occurrence of an interrupt that is not masked causes the program execution to transfer to the memory location pointed to by that interrupt's vector address, assuming no other interrupt is being serviced.

The occurrence on an interrupt that is masked causes no automatic processor action, but it does set the corresponding status bit in the **ins** register. If an interrupt occurs while it is masked, it is latched. Subsequently, unmasking the interrupt causes it to be serviced as soon as the processor reaches an interruptible state. The status of the interrupt sources is readable in the **ins** register even if the interrupt is masked in the **inc** register.

4.3.3 External Interrupt Pin (INTB)

INTB is a negative edge-triggered interrupt pin. External hardware must guarantee that the interrupt service routine has completed before issuing another interrupt on INTB. Any activity on INTB is **not** recognized during the interrupt service routine and must be reissued after the completion of the interrupt service routine. Because there is no interrupt acknowledge pin on the *FlashDSP*1650, the interrupt service routine must communicate with the external hardware through other means. One possible way of performing this task would be through the use of IOP pins.

4 Hardware Architecture (continued)

4.3 Interrupts, Trap, and Low-Power Standby Mode (continued)

4.3.4 Clearing Interrupts

The IOPA interrupt is cleared by reading the **sbita** register. The JTAG interrupt (JINT) is cleared by reading the **jtag** register.

Other interrupts are cleared by either of the following methods:

- After a vectored interrupt has been serviced, it is cleared when the **ireturn** instruction is issued, leaving set any other vectored interrupts that are pending.
- In the **ins** register, writing a 1 to the bit that is associated with the interrupt. Writing a 0 to the **ins** register does nothing.

Once an interrupt is cleared, the corresponding bit in the **ins** register is cleared.

4.3.5 Power-Saving Modes

Three primary power-saving modes are available. These modes are described below in order of increasing power savings:

Low-Frequency Clock Mode—Switching the core clock to the lowest frequency possible for as long as possible is the easiest way to conserve power, since power consumption is directly linked to the instruction cycle rate. The low-frequency clock source to the DSP is controlled by register bits **clkc**[7:4]. The appropriate selection of the low-frequency clock depends on the application requirements. For example, if the DRAM controller is enabled, only the input clock divided by four can be used, since DRAM refresh requirements must be met. If an application requires an accurate real-time clock, the internal ring oscillator probably cannot be used.

Low-Power Standby Mode—Setting the AWAIT bit in the **alf** register causes the processor to go into a standby mode in which program execution is halted and the internal wait-stated DSP clock is turned off. The occurrence of any interrupt which is enabled in the **inc** register is processed and returns the processor to the previous state, allowing program execution to continue.

Stop Clock Mode—Setting the STOPCLK bit in the **clkc** register causes the processor to go into a sleep mode in which program execution is halted and the internal wait-stated and free-running clocks are turned off. An IOPA interrupt, an IOPD interrupt, an INTB pin interrupt, or a Timer1 time-out interrupt clears the STOPCLK condition and allows program execution to continue. The settings of the **inc** register have no effect on the clearing of STOPCLK; however, the desired interrupt must be enabled and selected with the appropriate MUX controls and enables. See IOP MUX controls and IOPA/IOPD interrupt descriptions.

4.4 Memory Maps and Wait-States

The DSP implements a modified Harvard architecture that has separate internal 16-bit address and data buses for the instruction/coefficient (X) and data (Y) memory spaces. The *FlashDSP*1650 contains 24 Kwords of flash ROM and either one bank of 1.25 Kwords of RAM or two banks of 2 Kwords of RAM.

The *FlashDSP*1650 has a multiplexed external bus that accesses external RAM (ERAMHI and ERAMLO), and external ROM (EROM). Programmable wait-states are provided for external memory accesses to ERAMHI, ERAMLO, and EROM.

The instruction/coefficient memory map is configurable to provide application flexibility.

Tables 11 and 12 show the four instruction/coefficient memory maps available for the *FlashDSP*1650.

The data memory maps are divided into segments as shown in Tables 13 and 14. The selection of a segment is automatic depending on the address in the YAAU. When IR2KEN = 1 in **chipo**[9], the segment for the internal RAM is further divided into two banks.

The internal RAM can be accessed by both the Y space and the X space. If the same bank of internal RAM is accessed from both memory spaces simultaneously, one wait-state is added, and the Y space is accessed first.

4 Hardware Architecture (continued)

4.4 Memory Maps and Wait-States (continued)

Table 11. Instruction/Coefficient Memory Map (X Memory Space) for *FlashDSP*1650 (IR2KEN = 0)

<table>
<tr><th>Decimal Address</th><th>Hexadecimal Address in pc, pt, pi, pr</th><th>MAP1 (EXM = 0 LOWPR = 0)</th><th>MAP2 (EXM = 1 LOWPR = 0)</th><th>MAP3 (EXM = 0 LOWPR = 1)</th><th>MAP4 (EXM = 1 LOWPR = 1)</th></tr>
<tr><td>0
1279</td><td>0x0000
0x04FF</td><td rowspan="4">IROM</td><td rowspan="6">EROM</td><td>RAM1</td><td>RAM1</td></tr>
<tr><td>1280
8191</td><td>0x0500
0x1FFF</td><td rowspan="2">Reserved</td><td rowspan="2">Reserved</td></tr>
<tr><td>8192
16,383</td><td>0x2000
0x3FFF</td></tr>
<tr><td>16,384
24,575</td><td>0x4000
0x5FFF</td><td rowspan="3">IROM</td><td rowspan="4">EROM</td></tr>
<tr><td>24,576
32,767</td><td>0x6000
0x7FFF</td><td>Reserved</td></tr>
<tr><td>32,768
40,959</td><td>0x8000
0x9FFF</td><td rowspan="2">EROM</td></tr>
<tr><td>40,960
49,151</td><td>0xA000
0xBFFF</td><td>Reserved</td></tr>
<tr><td>49,152
50,431</td><td>0xC000
0xC4FF</td><td>RAM1</td><td>RAM1</td><td rowspan="3">EROM</td></tr>
<tr><td>50,432
57,343</td><td>0xC500
0xDFFF</td><td rowspan="2">Reserved</td><td rowspan="2">Reserved</td></tr>
<tr><td>57,344
65,535</td><td>0xE000
0xFFFF</td></tr>
</table>

Notes:
Physical memory: 24K IFROM (flash ROM).

MAP1: Automatically selected when the hardware development system trap is in effect. The user-selected map is restored at the end of the HDS trap service routine.

EXM: The external memory control input pin, latched at reset. When the device is reset with EXM = 1, the upper 8 bits of the data bus, pins DB[15:8], are enabled onto pins IOPA[7:0].

LOWPR: The LOWPR bit of the **alf** register, bit 14.

4 Hardware Architecture (continued)

4.4 Memory Maps and Wait-States (continued)

Table 12. Instruction/Coefficient Memory Map (X Memory Space) for *FlashDSP*1650 (IR2KEN = 1)

<table>
<tr><th>Decimal Address</th><th>Hexadecimal Address in pc, pt, pi, pr</th><th>MAP1 (EXM = 0 LOWPR = 0)</th><th>MAP2 (EXM = 1 LOWPR = 0)</th><th>MAP3 (EXM = 0 LOWPR = 1)</th><th>MAP4 (EXM = 1 LOWPR = 1)</th></tr>
<tr><td>0
2047</td><td>0x0000
0x07FF</td><td rowspan="4">IROM</td><td rowspan="6">EROM</td><td>RAM1, 2</td><td>RAM1, 2</td></tr>
<tr><td>2048
8191</td><td>0x0800
0x1FFF</td><td rowspan="2">Reserved</td><td rowspan="2">Reserved</td></tr>
<tr><td>8192
16,383</td><td>0x2000
0x3FFF</td></tr>
<tr><td>16,384
24,575</td><td>0x4000
0x5FFF</td><td rowspan="3">IROM</td><td rowspan="4">EROM</td></tr>
<tr><td>24,576
32,767</td><td>0x6000
0x7FFF</td><td>Reserved</td></tr>
<tr><td>32,768
40,959</td><td>0x8000
0x9FFF</td><td rowspan="2">EROM</td></tr>
<tr><td>40,960
49,151</td><td>0xA000
0xBFFF</td><td>Reserved</td></tr>
<tr><td>49,152
51,199</td><td>0xC000
0xC7FF</td><td>RAM1, 2</td><td>RAM1, 2</td><td rowspan="3">EROM</td><td rowspan="3">EROM</td></tr>
<tr><td>51,200
57,343</td><td>0xC800
0xDFFF</td><td rowspan="2">Reserved</td><td rowspan="2">Reserved</td></tr>
<tr><td>57,344
65,535</td><td>0xE000
0xFFFF</td></tr>
</table>

Notes:
Physical memory: 24K IFROM (flash ROM); two 1K banks of RAM populated (RAM1 and RAM2).

MAP1: Automatically selected when the hardware development system trap is in effect. The user-selected map is restored at the end of the HDS trap service routine.

EXM: The external memory control pin, an input to the device, latched at reset. When the device is reset with EXM = 1, the upper 8 bits of the data bus, pins DB[15:8], are enabled onto pins IOPA[7:0].

LOWPR: The LOWPR bit of the **alf** register, bit 14.

4 Hardware Architecture (continued)

4.4 Memory Maps and Wait-States (continued)

Table 13. *FlashDSP*1650 Data Memory Map (IR2KEN = 0)

Decimal Address	Address in r0, r1, r2, r3	Segment
0 — 1279	0x0000 — 0x04FF	RAM1
1280 — 16K – 1	0x5000 — 0x3FFF	Reserved
16K — 32K – 1	0x4000 — 0x7FFF	ERAMLO
32K — 64K – 1	0x8000 — 0xFFFF	ERAMHI

Table 14. *FlashDSP*1650 Data Memory Map (IR2KEN = 1)

Decimal Address	Address in r0, r1, r2, r3	Segment
0 — 2K – 1	0x0000 — 0x07FF	RAM1, 2
2K — 16K – 1	0x0800 — 0x3FFF	Reserved
16K — 32K – 1	0x4000 — 0x7FFF	ERAMLO
32K — 64K – 1	0x8000 — 0xFFFF	ERAMHI

4.4.1 Instruction/Coefficient Memory Map Selection

In determining which memory map to use, the processor evaluates the state of two parameters. The first is the LOWPR bit (bit 14) of the **alf** register. The LOWPR bit of the **alf** register is initialized to 0 automatically at reset. LOWPR controls the address in memory assigned to the two 1K banks of dual-port RAM (i.e., RAM1 and RAM2). If LOWPR is low, internal dual-port RAM begins at address 0xC000. If LOWPR is high, internal dual-port RAM begins at address 0x0. LOWPR also moves IROM from 0x0 in MAP1 to 0x4000 in MAP3, and EROM from 0x0 in MAP2 to 0x4000 in MAP4.

The second parameter is the value at reset of the EXM pin. EXM determines whether the 24 Kword internal flash ROM (IFROM) is addressable in the memory map. At reset, the EXM pin also selects the 16-bit external data bus. Specifically, if the EXM pin is held high during reset, the upper 8 bits of the data bus DB[15:8] are enabled onto pins IOPA[7:0].

The Lucent development system tools using the JTAG port can independently set the memory map. Specifically, during a trap from JTAG, the memory map is forced to MAP1. The map selection made prior to the JTAG trap is restored when the trap service routine has completed execution.

Whenever the device is reset using the RSTB pin, the default memory map is either MAP1 or MAP2, depending on the state of the EXM pin at reset. A reset through the JTAG port does not reinitialize the **alf** register, so the previous memory map is retained.

4.4.2 Boot from External ROM

After RSTB goes from low to high, the *FlashDSP*1650 comes out of reset and fetches an instruction from address zero of the instruction/coefficient space. The physical location of address zero is determined by the memory map in effect. If EXM is high at the rising edge of RSTB, MAP2 is selected. MAP2 has EROM at location zero; thus, program execution begins from external memory.

4.4.3 Data Memory Map Selection

Tables 13 and 14 show the data memory maps when IR2KEN = 0 and IR2KEN = 1, respectively. RAM1 and RAM2 are each 1 Kword banks of internal dual-port RAM. ERAMLO and ERAMHI are external memory segments for external data RAMs. The ERAMHI segment may contain DRAM, for which the DRAM controller is enabled by setting bit 12 of the **chipc** register (see Table 43 on page 60).

4 Hardware Architecture (continued)

4.5 Clock Generation

There are multiple options for clock generation in the *FlashDSP*1650. The device includes a crystal oscillator to be used with an external crystal, but can also accept a direct-driven input clock. (In either case, the internal codec uses this input clock; therefore, the frequency must be 4.096 MHz.) An internal independently enabled PLL is also provided, allowing the input clock to be multiplied up to provide a high-frequency 2X core clock of up to 80 MHz. If the PLL is not used, then a 2X clock (2 times the MIP rate) must be provided externally. This 2X clock, whether provided externally or generated internally by the PLL, is internally divided by two to generate the DSP core clock. An internal low-power oscillator is also provided which can be used to clock the DSP core for power savings.

4.5.1 Functional Overview

The clock generator for the DSP165X incorporates a wide range of options, including a crystal oscillator, PLL, low-frequency divider, and internal ring oscillator. The clock generates the outputs shown in Table 15.

Table 15. Clock Options

Clock Option	Signal	Generated by/Output
Input Crystal/ Clock	CLKIN	Output of the oscillator. The crystal oscillator circuit provides the device input clock and is controlled by the OSCBYP input pin. CLKIN is also used to clock the codec.
Ring Oscillator	CLKRING	The internal ring oscillator defaults to a minimum of 32 kHz. Even though the internal oscillator frequency is not exact, it may be measured against the crystal oscillator output and coarsely adjusted by setting the ROSP[1:0] bits in the **chipo** register (see Table 45). The **clkc** register (see Table 44) controls most of the configuration settings in the clock generator.
Wait-stated DSP Clock	CLKWAIT	The wait-stated clock generated by the core.
PLL Clock	CLKPLL	The PLL consists of the phase detector, loop filter, voltage-controlled oscillator (VCO), M divider, K divider, and N divider and provides output clock frequencies ranging from 8 MHz to 80 MHz. The value of M, K, and N are set in the **pllc** register (see Table 42 on page 59).
DSP 2X Core Clock	CLKCORE2X	Generated by the PLL, low-frequency clock, input clock, or ring oscillator and output to clock the core.
Stop Clock	STOPCLK	A power-saving mode that completely turns off CLKCORE2X. Any reset (powerup, pin, or JTAG), IOPA interrupt, INTB, or Timer1 interrupt clears STOPCLK.
Low-frequency Clock	CLKLOW	Generated by the internal ring oscillator or input clock and output to Timer1. Timer1 counts cycles of CLKLOW divided by a prescaler that is set in the **timerc** register (see Table 55 on page 67).
Codec Clock	CLKCODEC	Generated by CLKIN (should be set to 4.096 MHz) and output to the codec. It is additionally divided by 256 inside the codec block to generate a 16 kHz sampling rate. An 8 kHz rate can also be set by setting the CDCHFLX bit in the **chipc** register (see Table 43 on page 60).
Free-running DSP Clock	CLKFREE	Generated by the core clock (the 2X core clock divided by two) and output to Timer0 and EMI. Timer0 counts cycles of CLKFREE divided by a prescaler that is set in the **timerc** register (see Table 55 on page 67). CLKFREE is also the MIPS rate of the DSP.
Watchdog Clock	CLKWD	Generated by the input clock or the ring oscillator and output to the watchdog timer. The watchdog timer clock is selectable between CLKIN divided by 128 or CLKRING. Its time-out period is specified by bits WDEN[1:0] in the **chipo** register (see Table 45 on page 62).
DOUT	—	Provides digital output depending on the setting of DOUTMUX[3:0] in the **clkc** register (see Table 44 on page 61).

4 Hardware Architecture (continued)

4.5 Clock Generation (continued)

4.5.1 Functional Overview (continued)

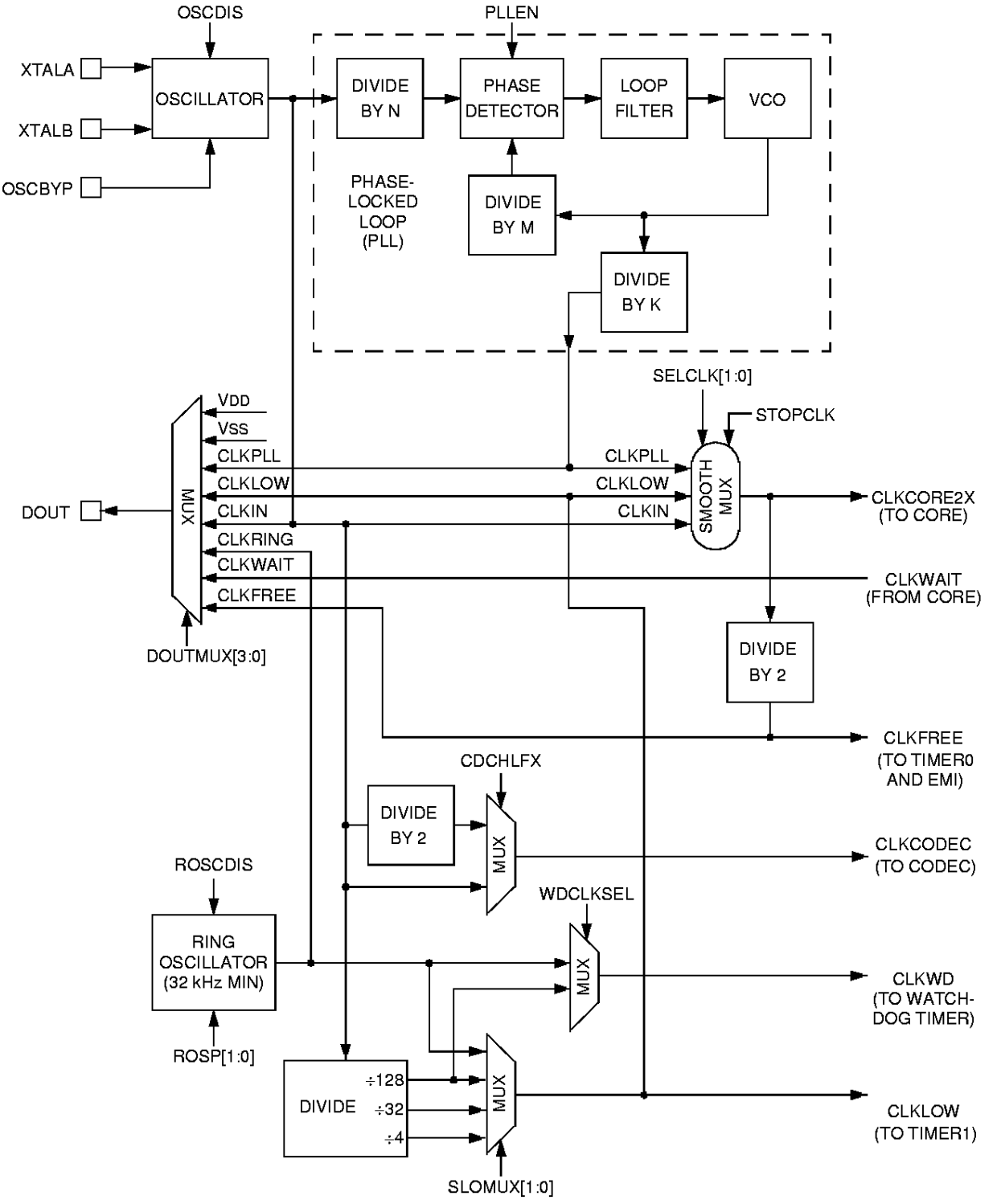


Figure 7. Clock Generation Overview

4 Hardware Architecture (continued)

4.5 Clock Generation (continued)

4.5.2 Core Clock Switching

When any of the smooth MUX control bits are changed, because of synchronization issues, a delay is incurred before the clock switch takes place. Five conditional flags can be checked via software to determine when the clock change actually takes place. These five conditionals are pllon, plloff, slowon, slowoff, stopclk. These five flags indicate that:

- CLKPLL currently is or is not the output of the smooth MUX.
- CLKLOW currently is or is not the output of the smooth MUX.
- STOPCLK has been requested but not yet cleared.

When the SELCLK control bits (**clkc**[5:4]) are changed, resulting in the smooth MUX switching the source for the core clock, there is a maximum time for the clock switch to occur (see Table 16). The latencies are defined in terms of input clock cycles (CLKIN period) and/or low-frequency clock cycles (CLKLOW period). In addition, a stabilization time is required for the entire clock path of the new source clock before that clock is selected via the SELCLK control bits (see Table 17).

Table 16. Clock Switch Latencies

Source Clock Before Switch	Source Clock After Switch	Maximum Clock Cycles for Switch
CLKIN	CLKPLL	[((N + 1) • 2.5) + ((K + 1)/(M + 2)) + 1.5]CLKIN Period
CLKIN	CLKLOW	1.5 CLKLOW Period
CLKIN	CLKCORE2X stopped	1.5 CLKIN Period
CLKLOW	CLKIN	1.5 CLKLOW Period + 1.5 CLKIN Period
CLKLOW	CLKPLL	[((N + 1) • 2.5) + ((K + 1)/(M + 2)) + 1.5]CLKIN Period + 1.5 CLKLOW Period
CLKLOW	CLKCORE2X stopped	1.5 CLKLOW Period
CLKPLL	CLKIN	[((N + 1) • 3) + 0.5](CLKIN Period)
CLKPLL	CLKLOW	1.5 CLKLOW Period
CLKPLL	CLKCORE2X stopped	[((N + 1) • 2.5) + ((K + 1)/(M + 2)) + 1.5]CLKIN Period
CLKCORE2X stopped	CLKIN	1.5 CLKIN Period
CLKCORE2X stopped	CLKLOW	1.5 CLKLOW Period
CLKCORE2X stopped	CLKPLL	[((N + 1) • 2.5) + ((K + 1)/(M + 2)) + 1.5]CLKIN Period

Table 17. Core Clock Stabilization Requirements

Source Clock to be Selected	Condition	Required Stabilization Time Prior to Selecting Source Clock
CLKIN*	Oscillator just enabled	120 ms (preliminary)
CLKRING	Ring oscillator just enabled	100 µs (preliminary)
CLKPLL	PLL just enabled	50 µs (preliminary)
CLKPLL	Any change to **pllc** register bits	50 µs (preliminary)
CLKLOW	Any change to SLOWMUX[1:0] bits	1 instruction cycle

* Assumes that OSCBYP = 0.

4 Hardware Architecture (continued)

4.6 External Memory Interface (EMI)

The external memory interface supports read/write operations from instruction/coefficient memory, data memory, and memory-mapped I/O devices. The *FlashDSP*1650 provides a 16-bit external address bus, AB[15:0], and a 16-bit (or alternatively 8-bit) external data bus, DB[15:0]. These buses are multiplexed between the internal buses for the instruction/coefficient memory and the data memory.

Because the two internal buses are multiplexed to a single external bus, a reference to external data is not allowed in the same cycle that a reference is made to an external instruction/coefficient. If this condition occurs, the internal multiplexer defaults to the instruction/coefficient access, and the data access does not take place. If bit 11, EMUXBOTH, of the **inc** register (see Table 40 on page 59) is a logic 1, a vectored interrupt would then become pending.

4.6.1 Memory Segment Enables

Three external memory enables, ERAMLO, ERAMHI, and EROM, select the external memory segment to be addressed. When an enable is low, the segment associated with that enable is selected. The leading edge of each can be delayed one-half a free-running clock period by programming the **chipc** register (see Table 43 on page 60). This avoids bus contention and allows the mix of fast and slow external memory and/or I/O devices. Note that the ERAMHI signal is multiplexed with the RASN signal onto a common pin. If the DRAM controller has been enabled via the **chipc** register, this pin assumes the RASN function.

The flexibility provided by the programmable options of the external memory interface (see Table 48 on page 63 and Table 43 on page 60) allows the *FlashDSP*1650 to interface gluelessly with a variety of commercial memory devices. Each of the three external memory segments, ERAMLO, ERAMHI, and EROM, has a number of wait-states that is programmable (from 0 to 15) by writing to the **mwait** register. When the program references memory in one of the three external segments, the internal multiplexer is automatically switched to the appropriate set of internal buses, and the associated external enable of ERAMLO, ERAMHI, or EROM, is issued. The external memory cycle is automatically stretched by the number of wait-states in the appropriate field of the **mwait** register.

When writing to external memory, the RWN pin goes low for the external cycle. The external data bus, DB[15:0], is driven by the DSP starting halfway through the cycle. The data driven on the external data bus is automatically held after the cycle unless an external read cycle immediately follows. When an access to internal memory is made, the AB[15:0] bus holds the last valid external memory address. After reset, the AB[15:0] value is undefined.

4.6.2 DRAM Support

The DSP interfaces directly to dynamic RAMs. The DRAM controller is enabled by bit 12 of the **chipc** register. The timing of the row address select (RASN) and column address select (CASN) strobes are programmable for support of slow as well as fast DRAMs. The dynamic RAM control register (**drc**, see Table 39 on page 58) contains fields for programming the CASN delay, the access time, and the precharge time. The DRAM controller also automatically refreshes DRAMs, with a variable refresh interval programmed in the **drc** register. Also supported are CASN before RASN refreshing and the early write cycle on write transactions to DRAM. When the DSP is operating from the low-frequency clock (CLKLOW), the DRAM controller prevents corruption of the DRAM contents by continuously refreshing using the low-frequency clock. During this time, the program must not access external memory. The DRAM controller also continues to refresh the DRAM during a reset, when the RSTB pin is asserted low.

On a DRAM access, the contents of the page register (**pgreg**, see Table 49 on page 64) are first driven onto the address bus as the row address for the DRAM devices. Next, the RASN strobe is asserted. The column address, which comes from the contents of the Y address space register pointer specified in the instruction, is then driven onto the address bus. This is followed by the assertion of the CASN strobe. The RWN signal indicates whether a read or write transaction is to occur. At the end of the programmed access time, both RASN and CASN are deasserted (returned high).

4.6.3 Pin Multiplexing Control

Setting bit eight of the **chipc** register, DB16EN, to 0 enables the upper 8 bits of the data bus, DB[15:8], onto the IOPA[7:0] pins. Note that if the DSP is reset with EXM = 1, the upper 8 bits of the data bus are similarly enabled onto the IOPA[7:0] pins, regardless of the value of bit eight of the **chipc** register.

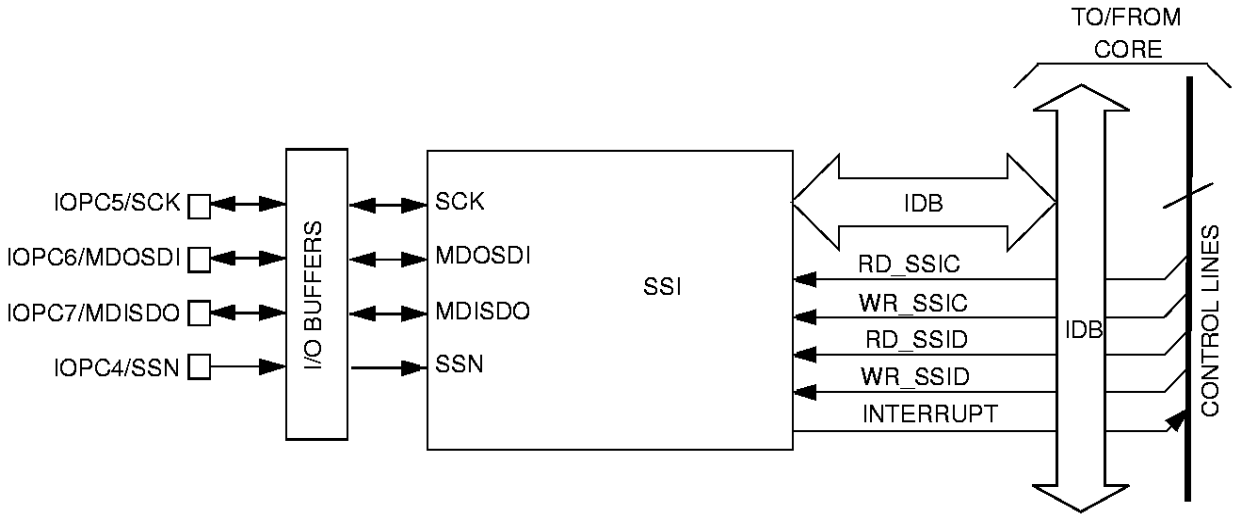
See Table 20 on page 46 for information on multiplexing.

4 Hardware Architecture (continued)

4.7 Synchronous Serial Interface (SSI)

The SSI can be programmed in the master or slave mode. The control word can be written to a 16-bit control register, **ssic**, to configure the SSI. The byte to be transmitted is written into the 8-bit data register, **ssid**. As a master, the SSI initiates serial transmission of a byte. This occurs whenever the master writes a byte to the data register (provided there is no transmission in progress). As a slave, it waits until the master initiates the start of transfer. In either case, transmitting and receiving occur simultaneously at the master and slave.

The byte from the data register of the master is shifted into the data register of the slave and vice versa. The two registers operate as a 16-bit circular shift register wherein the most significant bit (MSB) of the master data register is simultaneously shifted into the least significant bit (LSB) of the slave data register and the MSB of the slave data register is shifted into the LSB of the master data register. The DSP165X reads the received byte as a 16-bit word. The lower byte is the received data, and it is sign-extended into the upper byte. The shift clock is provided by the master. Depending on the polarity of the shift clock and the phase of the transfer relative to the shift clock, the master operates in one of four different modes of transfer. These modes are under program control and must match the mode used by the peripheral device with which the SSI communicates. In addition, there are five different clock rates that the master can choose from as the rate at which the bits are to be shifted out. The status of the transfer is indicated by three status bits, included as read-only bits in the control register. These indicate end of transfer and any errors that may have occurred.



Note: Table 18 on page 44 describes the SSI pins.

5-6147 (F)

Figure 8. SSI Interconnections

4 Hardware Architecture (continued)

4.7 Synchronous Serial Interface (SSI) (continued)

Table 18. SSI Pin Descriptions

Pin	Description
SCK	**SSI Clock**. Bidirectional. If SSI is configured in master mode, this pin is an output providing a clock to the slave devices. If SSI is configured in slave mode, this pin is an input which takes in the serial clock. This pin is multiplexed with IOPC5 (if the **ssic** register disables the SSI (bit 15 = 0), then this pin is used for IOPC5).
MDOSDI	**Master Data Out/Slave Data In**. Bidirectional. If the SSI is configured in master mode, this pin is the serial data output. If the SSI is configured in slave mode, this pin is the serial data input. This pin is multiplexed with IOPC6 (if the **ssic** register disables the SSI (bit 15 = 0), then this pin is used for IOPC6).
MDISDO	**Master Data In/Slave Data Out**. Bidirectional. If SSI is configured in master mode, this pin is an input and samples serial data supplied by the master device. If SSI is configured in slave mode, this pin is the serial data output. This pin is multiplexed with IOPC7 (if the **ssic** register disables the SSI (bit 15 = 0), then this pin is used for IOPC7).
SSN	**Serial Select**. Input. Negative assertion. When SSI is configured as a slave, the assertion of SSN signals the slave that is being addressed to transfer data with the master device. If this pin is asserted while SSI is configured as a master, a mode fault will be detected by SSI. This pin is multiplexed with IOPC4 (if the **ssic** register disables the SSI (bit 15 = 0), **or** if the **ssic** register configures the SSI for master mode (bit 14 = 1) and the SSN input is disabled (bit 10 = 0), then this pin is used for IOPC4).

The SSI has two programmable registers, one 16-bit register for control and one 8-bit register for data. The 16-bit control register, **ssic**, enables and configures the SSI for serial communication in the desired mode. It has control fields (the EN, MSTR, SPOL, SPHA, SDOEN, SSNEN, and SCLK bits of the **ssic** register) and status fields (the SDONE, WCOLL, and MODF bits of the **ssic** register). The 8-bit data register, **ssid**, is used for writing the byte to be transmitted and reading the received byte.

Table 53 on page 66 shows the register structure of the SSI control registers **ssic**. Brief descriptions of the function of each control bit are also given in the tables. Table 54 on page 67 shows the register structure of the SSI data register **ssid**.

4.7.1 SSI Operation

The SPOL and SPHA bits in the SSI control register determine the mode of data transfer. Both of these bits control the type of shift clock (SCK) generated. SPOL controls the polarity of SCK and SPHA determines the phase at which the serial transfer begins. The latter leads to a fundamentally different type of transfer with implications in situations where back-to-back byte transfer is required. The transfer formats may be different for different peripheral devices but remain unchanged during a transfer between the master and the slave device. The SSI is flexible enough to allow any desired configuration that conforms to the HC11 specifications.

The SSI generates an interrupt whenever a byte is successfully shifted in and copied to the read data buffer or when a mode-fault occurs. The interrupts are enabled by the appropriate bits in the **inc** register, and their status is posted in the **ins** register.

The SSI control register includes three bits, SDONE, WCOLL, and MODF, that can only be read by the processor. Their values are written by the SSI. SDONE is a status flag that indicates the end of a transfer. The WCOLL flag indicates a write was attempted to the SSI data register while a transfer was in progress. The MODF bit indicates a mode fault. This occurs when the *FlashDSP*1650 SSI is configured as a master and its SSN line is pulled low. Another error condition occurs when the *FlashDSP*1650 is configured as a slave, and a transfer is aborted by pulling SSN high before the transfer is complete. This error condition is not indicated by the status flags.

4 Hardware Architecture (continued)

4.8 I/O Ports (IOP)

The *FlashDSP*1650 contains four 8-bit IOP units and one 4-bit IOP unit, IOP<A—E>. Each IOP controls the directions of eight bidirectional control I/O pins, IOP<A—E>[7:0]. If a pin is configured as an output, it can be individually set, cleared, or toggled. If a pin is configured as an input, it can be read. See Table 19 for IOP operation.

4.8.1 IOP Operation

The lower half of each **sbit<a—e>** register (see Table 38 on page 57) contains the current value (VALUE[7:0]) of that register's eight bidirectional pins. The upper half of each **sbit<a—e>** register (DIR[7:0]) controls the direction of each pin independently. A logic 1 configures the corresponding pin as an output; a logic 0 configures it as an input. Reset clears the upper half of each **sbit<a—e>**, configuring all IOP<A—E> pins as inputs, except for IOPB1 that is reset as an output driven low.

The **cbit<a—e>** registers (see Table 38 on page 57) each contain two 8-bit fields, MODE[7:0] and DATA[7:0]. Reset clears the values of DATA[7:0]. The meaning of a bit in either field depends on whether it has been configured as an input or an output in the corresponding **sbit<a—e>** register. If a pin has been configured to be an output, the meanings are MODE and DATA. For an input, MODE and DATA are used on some pins as multiplex controls, or for IOPA interrupt control. Table 19 shows the functionality of the MODE and DATA bits based on the direction selected for the associated IOP pin.

Table 19. IOP Operation

DIR[n*]	MODE[n*]	DATA[n*]	Action on IOP[n*]
1 (Output)	0	0	Clear
1 (Output)	0	1	Set
1 (Output)	1	0	No Change
1 (Output)	1	1	Toggle
0 (Input)	Don't Care	Don't Care	Input

* $0 \le n \le 7$.

If an IOP pin is switched from being configured as an output to being configured as an input and then back to being configured as an output, the pin retains the previous output value.

4.8.2 IOPA Interrupt Circuitry

The IOPA port has an interrupt generation capability to help perform functions like a keypad scan. Each IOPA bit can individually be configured to generate the IOPA interrupt or not. To configure a bit for interrupt, it should be set as an input, with its mode bit set to 1. For example, to configure IOPA[1] for interrupt, set (**cbita**[9] = 1) and (**sbita**[9] = 0).

The interrupt generation logic compares the current state of the IOPA pins against a shadowed state which is loaded with the IOPA pins every time the **sbita** register is read. Whenever the current state and the shadowed state differ, an interrupt is generated. Which IOPA pin caused the interrupt can be determined by reading the **sbita** register. Reading sbita is also necessary to clear the interrupt and reload the shadowed state. Before any pins are enabled for interrupt, **sbita** should be read once to set the initial shadowed state to a defined value.

4.8.3 IOPD Interrupt Circuitry

The IOPD port 7 through 4 has an interrupt generation capability intended to help perform such functions as keypad scan. Each IOPD bit can individually be configured to generate the IOPD interrupt. To configure a bit for interrupt, it should be set as an input, with its mode bit set to 1. For example, to configure IOPD[4] for interrupt, set (**cbitd**[12] = 1) and (**sbitd**[12] = 0).

The interrupt generation logic compares the current state of the IOPD pins against a shadowed state which is loaded with the IOPD pin value every time the **sbitd** register is read. Whenever the current state and the shadowed state differ, an interrupt is generated. The **sbitd** register needs to be read to determine which IOPD pin caused the interrupt. Reading **sbitd** is also necessary to clear the interrupt and reload the shadowed state. Before any pins are enabled for interrupt, **sbitd** should be read once to set the initial shadowed state to a defined value.

4 Hardware Architecture (continued)

4.8 I/O Ports (IOP) (continued)

4.8.4 Pin Multiplexing Control

Table 20. IOP Pin Multiplexing

IOP Pin	Multiplexed Signal	Condition for Selection of Multiplexed Signal
IOPA0	DB8	(**chipc**[8] = 1) OR (EXM* = 1)
IOPA1	DB9	(**chipc**[8] = 1) OR (EXM* = 1)
IOPA2	DB10	(**chipc**[8] = 1) OR (EXM* = 1)
IOPA3	DB11	(**chipc**[8] = 1) OR (EXM* = 1)
IOPA4	DB12	(**chipc**[8] = 1) OR (EXM* = 1)
IOPA5	DB13	(**chipc**[8] = 1) OR (EXM* = 1)
IOPA6	DB14	(**chipc**[8] = 1) OR (EXM* = 1)
IOPA7	DB15	(**chipc**[8] = 1) OR (EXM* = 1)
IOPB0	INTB	(**cbitb**[8] = 0) AND (**sbitb**[8] = 0)
IOPB1	PLACT†	**chipo**[10] = 1
IOPB2	EXM	Latched on RSTB rising edge
IOPB3	—	—
IOPB4	AB15	((**cbitb**[12] = 1) AND (**sbitb**[12] = 0)) OR (EXM* = 1)
IOPB5	AB14	((**cbitb**[13] = 1) AND (**sbitb**[13] = 0)) OR (EXM* = 1)
IOPB6	AB13	((**cbitb**[14] = 1) AND (**sbitb**[14] = 0)) OR (EXM* = 1)
IOPB7	AB12	((**cbitb**[15] = 1) AND (**sbitb**[15] = 0)) OR (EXM* = 1)
IOPC0	TMS	JTSEL‡ = 1
IOPC1	TCK	JTSEL‡ = 1
IOPC2	TDI	JTSEL‡ = 1
IOPC3	TDO	JTSEL‡ = 1
IOPC4	SSN	((**ssic**[15] = 1) AND (**ssic**[14] = 0)) OR (**ssic**[10] = 1)
IOPC5	SCK	**ssic**[15] = 1
IOPC6	MDOSDI	**ssic**[15] = 1
IOPC7	MDISDO	**ssic**[15] = 1
IOPD0	ERAMLO	(**cbitd**[8] = 1) AND (**sbitd**[8] = 0)
IOPD1	CASN	((**cbitd**[9] = 1) AND (**sbitd**[9] = 0)) OR (**chipc**[12] = 1)
IOPD2	EROM	((**cbitd**[10] = 1) AND (**sbitd**[10] = 0)) OR (EXM* = 1)
IOPD3	JTSEL	Latched on RSTB rising edge
IOPE0	AB11	((**cbite**[8] = 1) AND (**sbite**[8] = 0)) OR (EXM* = 1)
IOPE1	AB10	((**cbite**[9] = 1) AND (**sbite**[9] = 0)) OR (EXM* = 1)
IOPE2	AB9	((**cbite**[10] = 1) AND (**sbite**[10] = 0)) OR (EXM* = 1)
IOPE3	AB8	((**cbite**[11] = 1) AND (**sbite**[11] = 0)) OR (EXM* = 1)
IOPE4	AB7	((**cbite**[12] = 1) AND (**sbite**[12] = 0)) OR (EXM* = 1)
IOPE5	AB6	((**cbite**[13] = 1) AND (**sbite**[13] = 0)) OR (EXM* = 1)
IOPE6	AB5	((**cbite**[14] = 1) AND (**sbite**[14] = 0)) OR (EXM* = 1)
IOPE7	AB4	((**cbite**[15] = 1) AND (**sbite**[15] = 0)) OR (EXM* = 1)

* EXM refers to the state of the EXM pin during the most recent device reset (RSTB held active-low).
† PLACT only controls the pin during power-loss reset; at all other times, it is always under IOP control.
‡ JTSEL refers to the state of the JTSEL pin during the most recent device reset (RSTB held active-low).

4 Hardware Architecture (continued)

4.9 Timers

The *FlashDSP*1650 contains two timers, TIMER0 and TIMER1. TIMER0 is composed of three main blocks: the timer control register, the prescaler, and the timer itself. The timer control register, **timerc**, (see Table 55 on page 67) sets up the operational state of the timer and prescaler. The prescaler is a programmable divider that can be set to a count of 2 to 65,536. It provides a wide range of time delay. The timer itself is a 16-bit binary counter that can be preloaded with any 16-bit number. If enabled, the timer counts down at the programmed rate and generates an interrupt upon reaching zero.

If the TIME0 interrupt is enabled (see Table 40 on page 59), program control jumps to location 0x0004 where typically a branch to an interrupt service routine should be placed. Writing the **timer0** register sets the initial count into the timer and loads the period register with the same value for repeated count cycles.

The following functions are programmable in the **timerc** register:

- T*n*EN starts TIMER*n* counting when set.
- RELOAD*n* enables repeated counts of TIMER*n* when set. If zero, TIMER*n* counts down once and stops. If one, TIMER*n* automatically reloads the previous starting value from the period register into the **timer*n*** register, and recommences counting down.
- DISABLE0 turns off the TIMER0 clock when set. This is a power-saving feature.
- PRESCALE*n* encodes the value of the divider of the clock going to the counter. For TIMER0, it ranges from CLKFREE/2 to CLKFREE/65,536 (where CLKFREE is the free-running clock). For TIMER1, it ranges from CLKLOW/2 to CLKLOW/16 (where CLKLOW is the low-frequency clock).

The timer interrupt can be individually enabled or disabled through the **inc** register. The timer can be stopped and started by software and can be reloaded with a new delay at any time. Its current value can also be read by software. When the DSP is reset, the timer is guaranteed to be in an inactive state.

The timer is normally run with two data move instructions, one to write the **timer0** register with the initial count, and the second to write the **timerc** register with initial values. Setting T0EN starts the counting of TIMER0.

When the DSP is reset, the control bits of the **timerc** register and the timer itself are initialized to 0. This sets the prescaler to CLKFREE/2, turns off the reload feature, disables timer counting, and initializes the timer value to its inactive state. The act of resetting the device does not cause a timer interrupt. Note that the period register is not initialized on reset. Also, if the timer clocks are turned off by DISABLE0, the period register cannot be written.

TIMER1 is the same as TIMER0, except that it counts at the frequency of the low-frequency clock, has no disable bit, and is automatically powered down when not enabled.

4.10 Watchdog Timer

The watchdog timer allows for protection from catastrophic loss of control of the DSP by the software system. It can be programmed for one of three time-out intervals. The watchdog timer clock is nominally 32 kHz (selectable as the divided-down input clock or the internal ring oscillator output).

When the watchdog timer is enabled, it can be programmed to time-out based on counting out one of three periods. This time period is the watchdog input clock period multiplied by 2^{12}, 2^{14}, or 2^{16}. It is specified by the WDEN[1:0] bits in the **chipo** register (see Table 45 on page 62).

When the watchdog timer is enabled and counting, the current watchdog count value is not viewable; however, the timer can be reset at any time by writing any value to the watchdog reset register, **wdogr**. If the watchdog timer ever counts out the specified time between **wdogr** writes, it initiates a chip reset and asserts the RSTB pin low. The fact that a watchdog chip reset has occurred may be determined by reading the WDRST bit in the **chipc** register (see Table 43 on page 60), which is set after such a reset takes place.

4.11 Analog Interface

The analog interface includes an audio codec, two differential analog inputs, five single-ended analog inputs, two line drivers, one programmable speaker amplifier, two programmable gain amplifiers, and one programmable microphone amplifier.

The audio codec nominally runs at a 16 kHz frame/conversion rate. Within each frame, up to three digital-to-analog conversions (DAC) and four analog-to-digital (ADC) conversions can be performed. Correspondingly, three output data registers and four input data registers are provided to hold the data.

4 Hardware Architecture (continued)

4.11 Analog Interface (continued)

Three control registers may also be written for each frame to control which conversions take place, where the data comes from and goes to, and the amplifier settings.

All control and data registers are double-buffered allowing for maximum interrupt latency. More explicitly, just before the codec interrupt is sent to the *FlashDSP*1650 core, all codec registers are transferred to/from their shadow registers. The *FlashDSP*1650 then has one full 16 kHz period to read out the old data and send in the new data and control. If no new control or data values are given, the previous ones are reused.

Table 21. Analog Interface Registers

Register	Description
cdc	Control register. Stores codec control data (see Table 56 on page 68).
cdcpg	Control register. Stores codec programmable gain data, including microphone and speaker settings (see Table 57 on page 69).
cdcamux	Analog MUX control register. Stores analog-to-digital channel selection for all four input channels (see Table 58 on page 70).
adc1, adc2, adc3	Data register. Stores input data for the three oversampled analog-to-digital conversions (see Table 59 on page 71).
adc4	Data register. Stores input data for a single sample analog-to-digital conversion (see Table 60 on page 71).
spkr, line1, line2	Data register. Stores data for the three digital-to-analog conversions (see Table 61).

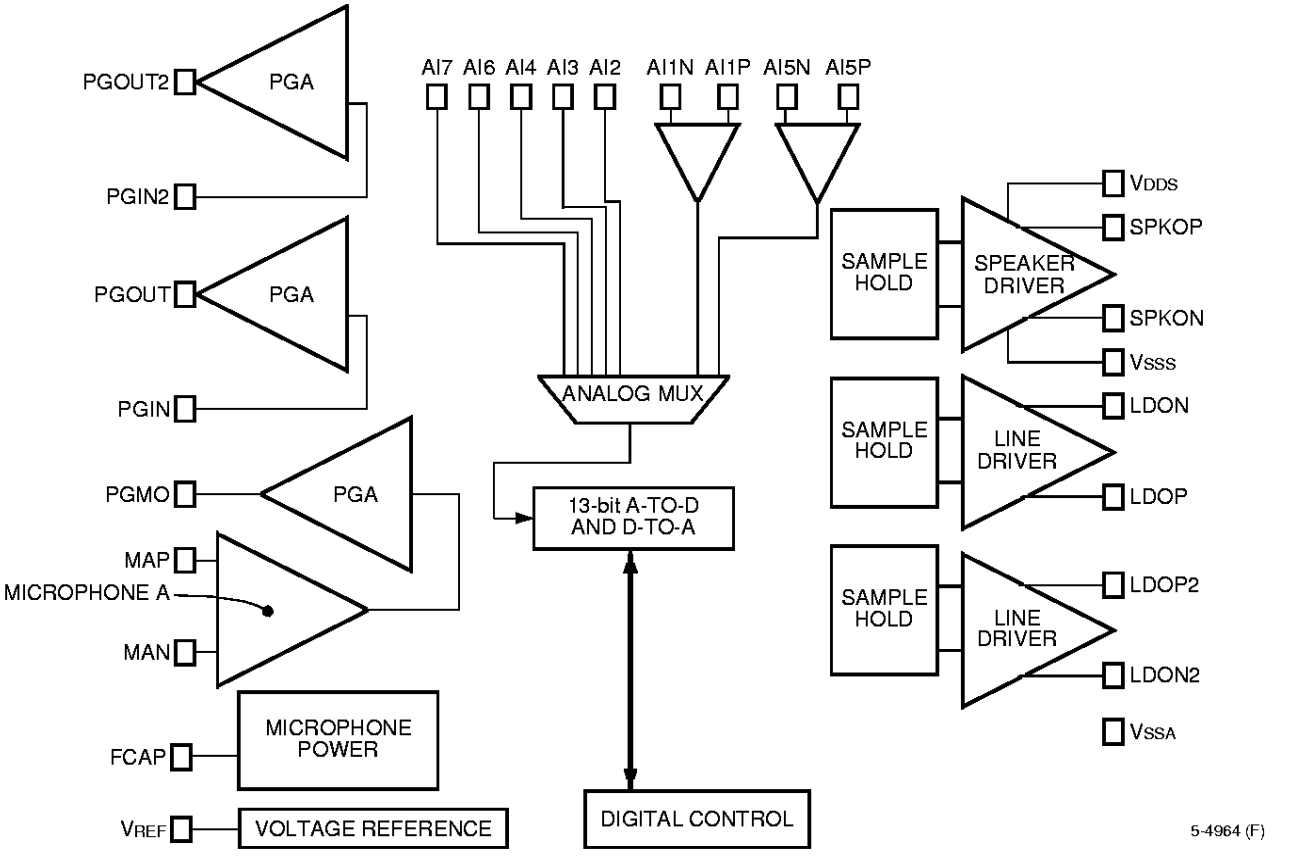


Figure 9. Block Diagram of Analog Circuitry

5 Software Architecture

5.1 Instruction Set

The *FlashDSP*1650 processor has six types of instructions: multiply/ALU, special function, control, F3 ALU, cache, and data move. The multiply/ALU instructions are the primary instructions used to implement signal processing algorithms. Statements from this group can be combined to generate multiply/accumulate, logical, and other ALU functions, and to transfer data between memory and registers in the data arithmetic unit. The special function instructions can be conditionally executed based on flags from the previous ALU operation, the condition of one of the counters, or the value of a pseudorandom bit in the *FlashDSP*1650 device. Special function instructions perform shift, round, and complement functions.

The F3 ALU instructions enrich the operations available on accumulators. The control instructions implement the **goto** and **call** commands. Control instructions can also be executed conditionally. Cache instructions are used to implement low overhead loops, conserve program memory, and decrease the execution time of certain multiply/ALU instructions. Data move instructions are used to transfer data between memory and registers or between accumulators and registers. (For a detailed description of this instruction set, see the *DSP165X Digital Signal Processor* Information Manual.)

The operators in Table 22 are used to describe the instructions in Sections 5.1.1 through 5.1.7.

Table 22. Instruction Set Operators

Symbol	Meaning
*	Denotes any of the following: 16-by-16 multiplication for a 32-bit product. Register-indirect addressing when used as a prefix to an address register. Direct addressing when used as a prefix to an immediate.
+	36-bit addition[1].
–	36-bit subtraction[1].
>>	Arithmetic right shift.
<<	Arithmetic left shift.
|	36-bit bitwise OR[1].
&	36-bit bitwise AND[1].
^	36-bit bitwise EXCLUSIVE OR[1].
:	Compound address swapping, accumulator shuffling.
~	One's complement.

1. These are 36-bit operations. One operand is 36-bit data in an accumulator; the other operand may be 16, 32, or 36 bits.

5.1.1 F1 Multiply/ALU Instructions

Note that the function statements and transfer statements in Table 23 are chosen independently. Any function statement (F1) can be combined with any transfer statement to form a valid multiply/ALU instruction. If either statement is not required, a single statement from either column constitutes a valid instruction. The number of cycles to execute the instruction is a function of the transfer column. (An instruction with no transfer statement executes in one instruction cycle.)

Whenever PC, **pt**, or rM is used in the instruction and points to external memory, the programmed number of wait-states must be added to the instruction cycle count. All multiply/ALU instructions require one word of program memory. The no-operation (**nop**) instruction is a special case encoding of a multiply/ALU instruction and executes in one cycle. The assembly-language representation of a **nop** is either **nop** or a single semicolon.

5 Software Architecture (continued)

5.1 Instruction Set (continued)

5.1.1 F1 Multiply/ALU Instructions (continued)

Table 23. F1 Multiply/ALU Instructions

F1 Function Statement	Transfer Statement[1]	Transfer Statement Cycles[2]	
		Not Using Cache	Using Cache
p = x • y3	y = Y, x = X	2	1
aD = p, p = x • y3	y = aT, x = X	2	1
aD = aS + p, p = x • y3	y[l] = Y	1	1
aD = aS – p, p = x • y3	aT[l] = Y	1	1
aD = p	x = Y	1	1
aD = aS + p	Y	1	1
aD = aS – p	Y = y[l]	2	2
aD = y	Y = aT[l]	2	2
aD = aS + y	Z:y, x = X	2	2
aD = aS – y	Z:y[l]	2	2
aD = aS & y	Z:aT[l]	2	2
aD = aS | y	—	1	1
aD = aS ^ y	—	1	1
aS – y	—	1	1
aS & y	—	1	1

1. The [l] is an optional argument that specifies the low 16 bits of aT or **y**.
2. Add cycles for either of the following:
   - When an external memory access is made in X or Y space and wait-states are programmed, add the number of wait-states.
   - If an X space access and a Y space access are made to the same bank of DPRAM in one instruction, add one cycle.
3. **p = x • y** becomes a single-cycle squaring operation if the **auc** bit 7 is set. With bit 7 set, a transfer statement of the form **y = Y** loads the **x** register and the **y** register with the same number, so **p = x • y** results in the square.

Note: For transfer statements when loading the upper half of an accumulator, the lower half is cleared if the corresponding CLR bit in the **auc** register is zero. **auc** is cleared by reset.

Table 24. Replacement Table for F1 Multiply/ALU Instructions

Replace	Value	Meaning
aD, aS, aT	a0, a1	One of the DAU accumulators.
X	*pt++, *pt++i	X space memory location pointed to by **pt**. **pt** is postmodified by +1 and **i**, respectively.
Y	*rM, *rM++, *rM– –, *rM++j	RAM location pointed to by rM (M = 0, 1, 2, 3). rM is postmodified by 0, +1, –1, or **j**, respectively.
Z	*rMzp, *rMpz, *rMm2, *rMjk	Read/write compound addressing. rM (M = 0, 1, 2, 3) is used twice. First, postmodified by 0, +1, –1, or **j**, respectively; and, second, postmodified by +1, 0, +2, or **k**, respectively.

5 Software Architecture (continued)

5.1 Instruction Set (continued)

5.1.2 F2 Special Function Instructions

All forms of the special function instructions require one word of program memory and execute in one instruction cycle. (If PC points to external memory, add programmed wait-states.)

The special functions in Table 25 can be executed conditionally, as in:

```
if CON instruction
```

and with an event counter

```
ifc CON instruction
```

which means:

```
if CON is true then
    c1 = c1 + 1
    instruction
    c2 = c1
else
    c1 = c1 + 1
```

The preceding special function instructions can be executed unconditionally by writing them directly. For example, **a0 = a1**.

Table 25. F2 Special Function Instructions

Statement	Meaning
aD = aS >> 1	Arithmetic right shift (sign preserved) of the 36-bit accumulators.
aD = aS >> 4	
aD = aS >> 8	
aD = aS >> 16	
aD = aS	Load destination accumulator from source accumulator.
aD = –aS	2's complement.
aD = ~aS	1's complement.
aD = rnd(aS)	Round upper 20 bits of accumulator.
aDh = aSh + 1	Increment upper half of accumulator (lower half cleared).
aD = aS + 1	Increment accumulator.
aD = y	Load accumulator with 32-bit **y** register value with sign extend.
aD = p	Load accumulator with 32-bit **p** register value with sign extend.
aD = aS << 1	Arithmetic left shift (sign not preserved) of the lower 32 bits of accumulators (upper 4 bits are sign-extended from bit 31 at the completion of the shift).
aD = aS << 4	
aD = aS << 8	
aD = aS << 16	

Table 26. Replacement Table for F2 Special Function Instructions

Replace	Value	Meaning
aD, aS	a0, a1	One of the two DAU accumulators.
CON	mi, pl, eq, ne, gt, le, lvs, lvc, mvs, mvc, c0ge, c0lt, c1ge, c1lt, heads, tails, true, false, npint, njint, pllon, plloff, slowon, slowoff, stopclk	See Table 29 for definitions.

5 Software Architecture (continued)

5.1 Instruction Set (continued)

5.1.3 Control Instructions

Table 27 shows control instructions and their required numbers of instruction cycles and program-memory words. Required instruction cycles and program-memory words vary according to whether each instruction is executed unconditionally or conditionally. Control instructions cannot be executed from the cache.

Table 27. Control Instructions

Control Instructions	Executed Unconditionally		Executed Conditionally	
	Number of Cycles	Number of Words	Number of Cycles	Number of Words
goto JA[1] goto pt[2] call JA[1] call pt[2] return (goto pr)[2]	2	1	3	2
ireturn (goto pi)[3]	2	1	—	—

1. The **goto JA** and **call JA** instructions should not be placed in the last or next-to-last instruction before the boundary of a 4 Kword page. If the **goto** or **call** is placed there, the program counter increments to the next page and the jump is to the next page rather than the desired current page.
2. If PC, **pt**, or **pr** point to external memory, add programmed wait-states.
3. The **ireturn** instruction can only be executed unconditionally.

With the exception of **ireturn**, the control instructions in Table 27 can be executed conditionally. For example:

if le goto 0x0345

Table 28. Replacement Table for Control Instructions

Replace	Value	Meaning
CON	mi, pl, eq, ne, gt, le, lvs, lvc, mvs, mvc, c0ge, c0lt, c1ge, c1lt, heads, tails, true, false, npint, njint, plloff, pllon, slowoff, slowon, stopclk	See Table 29 for definitions of mnemonics.
JA	12-bit value	Least significant 12 bits of absolute address within the same 4 Kword memory section.

5 Software Architecture (continued)

5.1 Instruction Set (continued)

5.1.4 Conditional Mnemonics (Flags)

Please note the following:

- Testing the state of the counter (**c0** or **c1**) automatically increments the counter by one.
- The pseudorandom sequence generator (PSG) may be reset by writing any value to the **pi** register, except during an interrupt service routine. While in an interrupt service routine, writing to the **pi** register updates the register and does not reset the PSG. If not in an interrupt service routine, writing to the **pi** register resets the PSG. (The **pi** register is updated, but written with the contents of the PC on the next instruction.) Interrupts must be disabled when writing to the **pi** register. If an interrupt is taken after the **pi** write, but before **pi** is updated with the PC value, the **ireturn** instruction does not return to the correct location. However, if the RAND bit in the **auc** register is set, writing the **pi** register never resets the PSG. A random rounding function can be implemented with either heads or tails.

Table 29. *FlashDSP*1650 Conditional Mnemonics

Test	Meaning	Test	Meaning
pl	Result is nonnegative (sign bit is bit 35).	mi	Result is negative.
eq	Result is equal to 0.	ne	Result is not equal to 0.
gt	Result is greater than 0.	le	Result is less than or equal to 0.
lvs	Logical overflow set.[1]	lvc	Logical overflow clear.
mvs	Mathematical overflow set.[2]	mvc	Mathematical overflow clear.
c0ge	Counter 0 greater than or equal to 0.	c0lt	Counter 0 less than 0.
c1ge	Counter 1 greater than or equal to 0.	c1lt	Counter 1 less than 0.
heads	Pseudorandom sequence bit set.	tails	Pseudorandom sequence bit clear.
true	The condition is always satisfied in an if instruction.	false	The condition is never satisfied in an if instruction.
npint	Not PINT (used by JTAG).	njint	Not JINT (used by JTAG).
pllon	DSP core clock is currently phase-locked loop (CLKPLL).	plloff	DSP core clock is not currently the phase-locked loop (CLKPLL).
slowon	DSP core clock is currently the low-frequency clock (CLKLOW).	slowoff	DSP core clock is not currently the low-frequency clock (CLKLOW).
stopclk	STOPCLK is set but the 2X core clock (CLKCORE2X) has not yet stopped.	—	—

1. Result is not representable in the 36-bit accumulators (36-bit overflow).
2. Bits 35:31 are not the same (32-bit overflow).

5 Software Architecture (continued)

5.1 Instruction Set (continued)

5.1.5 F3 ALU Instructions

These instructions, shown in Table 30, are implemented in the DSP1600 core. F3 ALU instructions allow accumulator two-operand operations with either another accumulator, the **p** register, or a 16-bit immediate operand. The result is placed in a destination accumulator that can be independently specified. All operations are done with the full 36 bits. For the accumulator with accumulator operations, both inputs are 36 bits. For the accumulator high with immediate operations, the immediate is sign-extended into bits 35:32 and the lower bits 15:0 are filled with zeros, except for the AND operation, for which they are filled with ones. These conventions allow the user to do operations with 32-bit immediates by programming two consecutive 16-bit immediate operations.

Table 30. F3 ALU Instructions

Cachable[1] (1 cycle)	Not Cachable[1] (2 cycle)
aD = aS + aT	aD = aSh + IM16
aD = aS – aT	aD = aSh – IM16
aD = aS & aT	aD = aSh & IM16
aD = aS | aT	aD = aSh | IM16
aD = aS ^ aT	aD = aSh ^ IM16
aS – aT	aSh – IM16
aS & aT	aSh & IM16
aD = aS + p	aD = aSl + IM16
aD = aS – p	aD = aSl – IM16
aD = aS & p	aD = aSl & IM16
aD = aS | p	aD = aSl | IM16
aD = aS ^ p	aD = aSl ^ IM16
aS – p	aSl – IM16
aS & p	aSl & IM16

1. If PC points to external memory, add programmed wait-states.

Table 31. Replacement Table for F3 ALU Instructions

Replace	Value	Meaning
aD, aT, aS	a0 or a1	One of the two accumulators.
IM16	16-bit value	Long immediate data: sign-, zero-, or one-extended as appropriate.
aSh	a0h or a1h	Upper half of the accumulator.
aSl	a0l or a1l	Lower half of the accumulator.

5.1.6 Cache Instructions

Each cache instruction requires one program-memory word. Table 32 shows cache instructions and their required numbers of instruction cycles. Control instructions and long immediate values cannot be stored inside the cache.

Table 32. Cache Instructions

Cache Instructions	Number of Cycles[1]
do	1
redo	2

1. If PC points to external memory, add programmed wait-states.

Cache instruction formats are as follows:

```
do K {
INSTR_1
INSTR_2
.
.
.
INSTR_NI
}

redo K
```

5 Software Architecture (continued)

5.1 Instruction Set (continued)

5.1.6 Cache Instructions (continued)

Table 33. Replacement Table for Cache Instructions

Replace	Instruction Encoding	Meaning
K	cloop[1]	Number of times the instructions are to be executed taken from bits 6:0 of the **cloop** register.
	1 to 127	Number of times the instructions are to be executed is encoded in the instruction.
NI	1 to 15	1 to 15 instructions can be included.

1. The assembly-language statement, **do cloop** (or **redo cloop**) is used to specify that the number of iterations is to be taken from the **cloop** register. K is encoded as 0 in the instruction encoding to select **cloop**.

When the cache is used to execute a block of instructions, the cycle timings of the instructions are as follows:

- In the first pass, the instructions are fetched from program memory and the cycle times are the normal out-of-cache values, except for the last instruction in the block of NI instructions. This instruction executes in two cycles.
- During pass two through pass K – 1, each instruction is fetched from cache and the in-cache timings apply.
- During the last (Kth) pass, the block of instructions is fetched from cache and the in-cache timings apply, except that the timing of the last instruction is the same as if it were out-of-cache.
- If any of the instructions access external memory, programmed wait-states must be added to the cycle.

The **redo** instruction treats the instructions currently in the cache memory as another loop to be executed K times. Using the **redo** instruction, instructions are re-executed from the cache without reloading the cache.

The number of iterations, K, for a **do** or **redo** can be set at run time by first moving the number of iterations into the **cloop** register (7 bits unsigned), then issuing the **do cloop** or **redo cloop**. At the completion of the loop, the value of **cloop** is decremented to 0; hence, **cloop** needs to be written before each **do cloop** or **redo cloop**.

5.1.7 Data Move Instructions

Table 34 shows data move instructions and their required numbers of program-memory words and instruction cycles. Required instruction cycles vary according to whether either PC or rM points to external memory. All data move instructions, except those doing long immediate loads, can be executed from within the cache. A direct data addressing mode has been added to the DSP1600 core.

Table 34. Data Move Instructions

Data Move Instructions	Number of Words	Number of Cycles[1]
R = IM16	2	2
SR = IM9	1	1
aT[l] = R R = aS[l] Y = R R = Y Z:R DR = *(OFFSET) *(OFFSET) = DR	1	2

1. If either **PC** or rM point to external memory, add any programmed wait-state. If both **PC** and rM point to same bank of DPRAM, add one cycle.

When signed registers less than 16 bits wide (**c0**, **c1**, **c2**) are read, their contents are sign-extended to 16 bits. When unsigned registers less than 16 bits wide are read, their contents are zero-extended to 16 bits.

Loading an accumulator with a data move instruction does not affect the flags.

5 Software Architecture (continued)

5.1 Instruction Set (continued)

5.1.7 Data Move Instructions (continued)

Table 35. Replacement Table for Data Move Instructions

Replace	Value	Meaning
R	Any of the registers in Table 87 on page 77[1]	—
DR	**r<0—3>**, **a0**[l], **a1**[l], **y**[l], **p**[l], **x**, **pt**, **pr**, **psw**	Subset of registers accessible with direct addressing.
aS, aT	**a0**, **a1**	High half of accumulator.
Y	*rM, *rM++, *rM– –, *rM++j	Same as in multiply/ALU instructions.
Z	*rMzp, *rMpz, *rMm2, *rMjk	Same as in multiply/ALU instructions.
IM16	16-bit value	Long immediate data.
IM9	9-bit value	Short immediate data for YAAU registers.
OFFSET	5-bit value from instruction 11-bit value from base register	Value in bits 15:5 of **ybase** register form the 11 most significant bits of the base address. The 5-bit offset is concatenated to this to form a 16-bit address.
SR	**r<0—3>**, **rb**, **re**, **j**, **k**	Subset of registers for short immediate data.

1. Some registers are write only or read only.

5.2 Register Settings

The following tables, listed alphabetically, describe the programmable registers of the *FlashDSP*1650.

Note: Some tables in this section use the following abbreviations:
X = don't care
W = write only

Table 36. alf (Standby and Memory Map) Register

Bit	15	14	13—0
Field	AWAIT	LOWPR	Res

Bit	Field	Description
15	AWAIT	Set to 1 to enter low-power standby mode.
14	LOWPR	Memory map selection[1]: 0 = select memory MAP1 or MAP2. 1 = select memory MAP3 or MAP4.
13—0	Res	Reserved—read as zero, write as zero.

1. Selects the memory map in conjunction with the value of the EXM pin at reset.

5 Software Architecture (continued)

5.2 Register Settings (continued)

Table 37. auc (Arithmetic Unit Control) Register

Bit	15—9	8	7	6—4	3—2	1—0
Field	Res	RAND	X = Y =	CLR	SAT	ALIGN

Bit	Field	Value	Description
15—9	Res	—	Reserved—read as zero, write as zero.
8	RAND	0	Pseudorandom number generator (PNG) reset by writing the **pi** register only outside an interrupt service routine.
		1	PNG never reset by writing the **pi** register.
7	X = Y =	0	Normal operation.
		1	Transfer statements **y = Y** load both the **x** and the **y** registers. All instructions that load the high half of the **y** register also load the **x** register. This allows single-cycle squaring (**p = x • y**).
6—4	CLR	1XX	Clearing **yl** is disabled (enabled when 0).
		X1X	Clearing **a1l** is disabled (enabled when 0).
		XX1	Clearing **a0l** is disabled (enabled when 0).
3—2	SAT	1X	**a1** saturation on overflow is disabled (enabled when 0).
		X1	**a0** saturation on overflow is disabled (enabled when 0).
1—0	ALIGN	00	**a0**, **a1** ← **p**.
		01	**a0**, **a1** ← **p**/4.
		10	**a0**, **a1** ← **p** x 4 (and zeros written to the two LSBs).
		11	**a0**, **a1** ← **p** x 2 (and zeros written to the LSB).

Table 38. cbit<a—e> (IOP Control Bit) and sbit<a—e> (IOP Status Bit) Registers

cbit<a—e> Registers

Bit	15—8	7—0
Field	MODE[7:0]	DATA[7:0]

sbit<a—e> Registers

Bit	15—8	7—0
Field	DIR[7:0]	VALUE[7:0]*

cbit<a—e> and sbit<a—e> Register Fields

DIR[n]†	MODE[n]†	DATA[n]†	Action on IOP[n]†
1 (Output)	0	0	Clear
1 (Output)	0	1	Set
1 (Output)	1	0	No change
1 (Output)	1	1	Toggle
0 (Input)	x‡	x‡	Input

* Read-only. Any value written to this field is ignored.
† $0 \le n \le 7$.
‡ See Table 20, IOP Pin Multiplexing, on page 46 and Section 4.8.2, IOPA Interrupt Circuitry, on page 45.

Note: Because the **cbit** and **sbit** registers have interrelated fields, Table 38 duplicates the information in Table 51.

5 Software Architecture (continued)

5.2 Register Settings (continued)

Table 39. drc (DRAM Control) Register

Bit	15	14	13—10	9—7	6—0
Field	REXT	CADLY	ACC	PRCH	RFSH

Bit	Field	Description
15	REXT	Refresh extend. When set, REXT causes the DRAM refresh signals to be extended to allow for interface to slower DRAMs when operating the DSP at higher frequencies. When set, the high-speed clock refresh access will be extended a total of three cycles, with the CAS low to RAS low time being lengthened one cycle and the pulse width of RAS low being lengthened two cycles.
14	CADLY	Column address delay. 0 = do not delay. 1 = delay one free-running clock cycle. When set, this bit will extend the hold time of the row address one extra cycle before switching to the column address. Normally, this bit should be set to 1.
13—10	ACC	Access time = ACC + 2. This field sets the length of a DRAM access. ACC + 2 cycles are counted from when the row address is driven to when RAS and CAS are negated.
9—7	PRCH	Precharge. 000 = 0 clock cycles. 100 = 4 clock cycles. 001 = 1 clock cycle. 101 = 5 clock cycles. 010 = 2 clock cycles. 110 = 6 clock cycles. 011 = 3 clock cycles. 111 = 7 clock cycles. This field programs the number of free-running clock (CLKFREE) cycles to allow for precharge. The next access is not allowed to occur until the precharge time is satisfied.
6—0	RFSH	Refresh cycle count. RFSH is a 7-bit positive integer which sets the interval between DRAM refresh cycles when the high-speed clock (PLL) is selected. Expressed in terms of the period of the DSP free-running clock, it is: (RefreshPeriod = 64 • RFSH • FreeRunningPeriod)

5 Software Architecture (continued)

5.2 Register Settings (continued)

Table 40. inc (Interrupt Control) Register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Field	JINT[1]	Codec	SW4[2]	SSI	EMUX BOTH	Res 7	INTB	Res 6	IOPA	IOPD	TIME0	SW2[2]	TIME1	SW1[2]	Res 2	Res 1

1. JINT is a JTAG interrupt and is controlled by the HDS. It may be made unmaskable by the Lucent development system tools.
2. SW1, SW2, and SW4 are user-controlled software interrupts.

Encoding: A zero in a bit of **inc** disables an interrupt; a one enables the interrupt. For more information about the fields in Table 40, see Table 10 on page 34.

Table 41. ins (Interrupt Status) Register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Field	JINT	Codec	SW4	SSI	EMUX BOTH	Res 7	INT B	Res 6	IOPA	IOPD	TIME0	SW 2	TIME1	SW 1	Res 2	Res 1

Encoding: A zero in a bit of **ins** indicates no interrupt. A one indicates an interrupt has been recognized and is pending or being serviced. If a one is written to bits 3, 5, 9, 11, 12, or 14 of **ins**, the corresponding interrupt is cleared. To clear IOPA, the **sbita** register must be read. For more information about the fields in Table 41, see Table 10 on page 34.

Table 42. pllc Register Fields

Bit	15—14	13—11	10—9	8—6	5—0
Field	LF	ICP	N	K	M

Bit	Field	Description
15—14	LF[1:0][1]	PLL Loop Filter Control. See Table 99 on page 85.
13—11	ICP[2:0][1]	PLL Charge Pump Control. See Table 99 on page 85.
10—9	N[1:0][1]	PLL Input Clock Divider. 2-bit positive integer from 0 to 3.
8—6	K[2:0][1]	PLL Output Divider. 3-bit positive integer from 0 to 7.
5—0	M[5:0][1]	PLL Multiplier. 6-bit positive integer from 0 to 63.

1. $VCO(FREQUENCY) = \frac{CLKIN(M+2)}{(N+1)}$

Note: Operation is not guaranteed for the following MIPS rates: VCO(frequency) > 80 MHz at 5 V, or for VCO(frequency) > 66 MHz at 3.3 V.

5 Software Architecture (continued)

5.2 Register Settings (continued)

Table 43. chipc Register Fields

Bit	15—14	13	12	11	10	9	8	7	6	5	4—2	1	0
Field	Res	WEROM	DRCEN	DEROM	DHI	DLO	DB16EN	IOPDEN	CDCLHFX	WIOPUR	Res	PLRST	WDRST

Bit	Field	Description
15—14	Reserved	Reserved; write with zeros, read as zeros.
13	WEROM	Allows writing to the EROM segment for development purposes. 0 = normal operation. 1 = on accesses to the ERAMHI memory segment, activate the EROM strobe instead of the ERAMHI strobe, and also pull RWN low for write operations to this segment.
12	DRCEN	Enable DRAM controller: 0 = disable DRAM controller. 1 = enable DRAM controller.
11	DEROM	Delay EROM strobe: 0 = EROM not delayed. 1 = EROM delayed one phase of CLKFREE.
10	DHI	Delay ERAMHI strobe: 0 = ERAMHI not delayed. 1 = ERAMHI delayed one phase of CLKFREE.
9	DLO	Delay ERAMLO strobe: 0 = ERAMLO not delayed. 1 = ERAMLO delayed one phase of CLKFREE.
8	DB16EN	Enable 16-bit data bus DB[15:0][1]: 0 = 8-bit data bus (DB[15:8] disabled). 1 = 16-bit data bus (IOPA[7:0] disabled).
7	IOPDEN	Enable IOPD[7:4]: 0 = DB[7:4] enabled (IOPD[7:4] disabled). 1 = IOPD[7:4] enabled (DB[7:4] disabled).
6	CDCHLFX	Codec input clock rate: 0 = codec clock is input clock. 1 = codec clock is input clock/2.
5	WIOPUR	Enable write of IOP pull-up resistor control registers: 0 = write **cbit<a—e>** registers as normal. 1 = write **IOPUC<A—E>** registers in place of **cbit<a—e>**.
4—2	Reserved	Reserved; write with zeros, read as zeros.
1	PLRST	Power-loss reset status: 0 = no power-loss reset has occurred. 1 = power-loss reset has occurred.
0	WDRST	Watchdog reset status: 0 = no watchdog reset has occurred. 1 = watchdog reset has occurred.

1. The state of this bit is ignored if the EXM pin is logic one at the time of reset, which enables the 16-bit data bus.

5 Software Architecture (continued)

5.2 Register Settings (continued)

Table 44. clkc Register Fields

Bit	15—13	12	11—8	7—6	5—4	3	2	1	0
Field	Res	PFIVOLT	DOUT MUX	SLOMUX	SELCLK	STOPCLK	ROSCDIS	OSCDIS	PLLEN

Bit	Field	Description
15—13	Reserved	Write with 0, read as 0.
12	PFIVOLT	Phase-locked loop voltage: 0 = PLL in 3 V mode. 1 = PLL in 5 V mode.
11—8	DOUT MUX[3:0]	DOUT source selection: 0000 = ring oscillator (CLKRING) selected to DOUT. 0001 = input crystal/clock (CLKIN) selected to DOUT. 0010 = low-frequency clock (CLKLOW) selected to DOUT. 0011 = wait-stated DSP clock (CLKWAIT) selected to DOUT. 0100 = free-running DSP clock (CLKFREE) selected to DOUT. 0101 = reserved. 0110 = logic 0 selected to DOUT. 0111 = logic 1 selected to DOUT. 1xxx = reserved.
7—6	SLOMUX[1:0][1]	Low-frequency clock source selection (CLKLOW): 00 = chip input clock (CLKIN) divided by 4. 01 = chip input clock (CLKIN) divided by 32. 10 = chip input clock (CLKIN) divided by 128. 11 = internal ring oscillator (CLKRING).
5—4	SELCLK[1:0][2]	Select the 2X core clock (CLKCORE2X) (as long as STOPCLK = 0): 00 = select input clock (CLKIN). X1 = select PLL output (CLKPLL). 10 = select low-frequency clock (CLKLOW) as selected by SLOMUX[1:0].
3	STOPCLK	Stop DSP core clock (CLKCORE2X): 0 = clock runs as normal. 1 = disable 2X DSP input core clock.
2	ROSCDIS	Ring oscillator disable: 0 = enable the internal ring oscillator clock (CLKRING). 1 = disable the internal ring oscillator clock (CLKRING).
1	OSCDIS[3]	Oscillator disable: 0 = enable the crystal oscillator clock. 1 = disable the crystal oscillator clock.
0	PLLEN[4]	Phase-locked loop enable: 0 = disable PLL circuitry. 1 = enable PLL to operate.

1. If the DRAM controller is used, SLOMUX[1:0] should be set to 00.
2. It is recommended that the 2 bits of the SELCLK field be changed one at a time to prevent the possibility of an intermediate clock switch before switching to the desired destination clock. For example, to switch the clock selection back and forth between the low-frequency clock (CLKLOW) and the high-frequency PLL output (CLKPLL), the more significant bit of SELCLK (**clkc**[5]) should be set to one, allowing the less significant bit of SELCLK (**clkc**[4]) to be toggled on and off without the possibility of an intermediate clock switch.
3. This bit should not be set if the internal crystal oscillator is bypassed, i.e., OSCBYP pin = 1. Also note that when this bit is set, it will not take effect until after CLKRING is selected and is sourcing CLKCORE2X.
4. This bit is overridden if it is cleared to zero and if the PLL output (CLKPLL) is selected as the 2X core clock (if SELCLK[0] = 1).

5 Software Architecture (continued)

5.2 Register Settings (continued)

Table 45. chipo Register Fields

Bit	15—12	11	10	9	8—7	6	5—4	3	2—0
Field	Res	LOCK	PLCKOFF	IR2KEN	ROSP	LOCKOSCON	WDEN	WDCLKSEL	PLC

Bit	Field	Description
15—12	Reserved	Write with 0.
11	LOCK[1]	Lock all bits in the **chipo** register: 0 = **chipo** register contents may be changed. 1 = **chipo** register contents may not be modified until after next powerup or reset.
10	PLCKOFF	Clocks off during power-loss reset: 0 = clocks on during power-loss reset. 1 = force all DSP clocks off during power-loss reset, and assert PLACT pin high during power-loss reset.
9	IR2KEN[2]	Configure banks of internal RAM: 0 = a single 1.25 Kword bank of RAM. 1 = two 1 Kword banks of RAM.
8—7	ROSP[1:0]	Ring oscillator speed: 00 = minimum of 32 kHz. 01 = increase default speed approximately 36%. 10 = decrease default speed approximately 28%. 11 = decrease default speed approximately 50%.
6	LOCKOSCON	Lock oscillator ON, crystal oscillator override: 0 = allows the OSCDIS bit (**clkc**[1]) to control oscillator. 1 = forces the oscillator to produce a clock; takes precedence over the OSCDIS bit (**clkc**[1]).
5—4	WDEN[1:0]	Watchdog timer enable bits: 00 = watchdog timer disabled. 01 = time-out after 2^{12} watchdog clock cycles. 10 = time-out after 2^{14} watchdog clock cycles. 11 = time-out after 2^{16} watchdog clock cycles.
3	WDCLKSEL	Watchdog clock select: 0 = select (CLKIN/128) as watchdog clock source. 1 = select internal ring oscillator (CLKRING) as watchdog clock source; also prevent ROSCDIS (**clkc**[2]) from disabling ring oscillator.
2—0	PLC[2:0]	Power-loss reset control bits, specify nominal trip and recover voltages: 000 = power-loss circuit disabled. 001 = trip at 4.3 V and recover at 4.6 V. 01x = trip at 3.9 V and recover at 4.2 V. 100 = trip at 3.05 V and recover at 3.25 V. 101 = trip at 3.05 V and recover at 3.75 V. 110 = trip at 2.6 V and recover at 2.8 V. 111 = trip at 2.6 V and recover at 3.3 V.

1. The **chipo** register should be initialized once immediately after reset and can be locked to prevent any further changes to its contents by setting the LOCK bit. Once LOCK bit has been set, the **chipo** register cannot be modified until a reset sequence occurs.
2. The IR2KEN field is used only for the *FlashDSP*1650. This field is reserved in the DSP1651 and DSP1652/53.

5 Software Architecture (continued)

5.2 Register Settings (continued)

Table 46. JTAG ID Register (32-bit)

Bit	31	30	29—28	27—19	18—12	11—0
Field	SLEWR	SECURE	BOPT	ROMCODE	DEVICE	$03B_{16}$

Bit	Field	Mask-Programmable Features
31	SLEWR	Slew rate control: Specifies the slew rate for the output buffers for all IOP pins, DB[7:0], AB[3:0], ERAMHI, and RWN. 0 = slow buffers. 1 = standard buffers.
30	SECURE	Security: 0 = unsecured (always unsecured for the *FlashDSP*1650). 1 = secured.
29—28	BOPT	Buffer options: Specifies what value of series resistance is placed in all IOP pins, DB[7:0], AB[3:0], ERAMHI, and RWN. 00 = no resistance with output buffers. 01 = 100 Ω of resistance in output buffers. 10 = 300 Ω of resistance in output buffers. 11 = 500 Ω of resistance in output buffers.
27—19	ROMCODE	The user's ROMCODE ID (in hexadecimal), as calculated by the following formula, using the letter codes from Table 47: ROMCODE ID = 0x[(20 x first letter) + second letter] Hard coded to YY for the *FlashDSP*1650.
18—12	DEVICE	Device code: 50 = *FlashDSP*1650.
11—0	$03B_{16}$	Fixed constant of $03B_{16}$.

Table 47. JTAG ROMCODE Letter Values

ROMCODE Letter	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	S	T	U	W	Y
Value	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19

Table 48. mwait (External Memory Wait-States Control) Register

Bit	15—12	11—8	7—4	3—0
Field	EROM[3:0]	ERAMHI[3:0]	Res	ERAMLO[3:0]

Bit	Field	Value	Description
15—12	EROM[3:0]	From 0000 to 1111	From zero to 15 EROM wait-states.
11—8	ERAMHI[3:0]	From 0000 to 1111	From zero to 15 ERAMHI wait-states.
7—4	Reserved	—	Reserved.
3—0	ERAMLO[3:0]	From 0000 to 1111	From zero to 15 ERAMLO wait-states.

5 Software Architecture (continued)

5.2 Register Settings (continued)

Table 49. pgreg (Page Address) Register

Bit	15—0
Field	PAGE

Bit	Field	Description
15—0	PAGE	16-bit page address.

Table 50. psw (Processor Status Word) Register

Bit	15—12	11—10	9	8—5	4	3—0
Field	DAU Flags	Res	a1[V]	a1[35:32]	a0[V]	a0[35:32]

Bit	Field	Value	Description
15—12	DAU Flags[1]	WXXX	LMI—logical minus when set (bit 35 = 1).
		XWXX	LEQ—logical equal when set (bit 35:0 = 0).
		XXWX	LLV—logical overflow when set.
		XXXW	LMV—mathematical overflow when set.
11—10	Res	—	Reserved—read as zero, write as zero.
9	a1[V]	W	Accumulator 1 (**a1**) overflow when set.
8—5	a1[35:32]	WXXX	Accumulator 1 (**a1**) bit 35.
		XWXX	Accumulator 1 (**a1**) bit 34.
		XXWX	Accumulator 1 (**a1**) bit 33.
		XXXW	Accumulator 1 (**a1**) bit 32.
4	a0[V]	W	Accumulator 0 (**a0**) overflow when set.
3—0	a0[35:32]	WXXX	Accumulator 0 (**a0**) bit 35.
		XWXX	Accumulator 0 (**a0**) bit 34.
		XXWX	Accumulator 0 (**a0**) bit 33.
		XXXW	Accumulator 0 (**a0**) bit 32.

1. The DAU flags are set by multiply/ALU (F1), conditionals (F2), or ALU (F3) operations involving the accumulators.

5 Software Architecture (continued)

5.2 Register Settings (continued)

Table 51. sbit<a—e> (IOP Status Bit) and cbit<a—e> (IOP Control Bit) Registers

sbit<a—c> Registers

Bit	15—8	7—0
Field	DIR[7:0]	VALUE[7:0]*

cbit<a—c> Registers

Bit	15—8	7—0
Field	MODE[7:0]	DATA[7:0]

sbit<a—c> and cbit<a—c> Register Fields

DIR[n]†	MODE[n]†	DATA[n]†	Action on IOP[n]†
1 (Output)	0	0	Clear
1 (Output)	0	1	Set
1 (Output)	1	0	No change
1 (Output)	1	1	Toggle
0 (Input)	x	x	Input

* Read-only. Any value written to this field is ignored.
† $0 \le n \le 7$ in version 4.0 and higher; all other versions bits 4 through 7 are not used for IOPD.
Notes:
For the IOPA port, when IOPU[n] = 1 and IOPL[n] = 1, this results in a strong pull-up.
Pull-up/pull-down is disabled for DIR[n] = 1 (output).

Note: Because the **sbit** and **cbit** registers have interrelated fields, Table 51 duplicates the information in Table 38.

Table 52. IOPUC<a—e> Register Fields

Bit	15—8	7—0
Field	IOPU[7:0]	IOPL[7:0]

Bit	Field	Description
15—8	IOPU[7:0]	IOPU[7:0] pull-up control: 0 = no pull-up resistor. 1 = pull-up IOP pin when configured as an input.
7—0	IOPL[7:0]	IOPL[7:0] pull-down control: 0 = no pull-down resistor. 1 = pull-down IOP pin when configured as an input.

Notes:
For the IOPA port, when IPU[n] = 1 and IOPL[n] = 1, this results in a strong pull-up.
Pull-up/pull-down is disabled for DIR[n] = 1 (output).
IOPB2 and IOPD3 have no internal pull-up or pull-down capability.

5 Software Architecture (continued)

5.2 Register Settings (continued)

Table 53. SSI Control Register (SSIC) Fields

Bit	15	14	13	12	11	10	9—8	7	6	5	4—3	2—0
Field	EN	MSTR	SPOL	SPHA	SDOEN	SSNEN	Res	SDONE	WCOLL	MODF	Res	SCLK

Bit	Field	Description
15	EN	Enable SSI: 0 = disable SSI. 1 = enable SSI.
14	MSTR	SSI master/slave: 0 = configure SSI as a slave. 1 = configure SSI as a master.
13	SPOL	SCK polarity: 0 = SSI clock is idle at a logic 0. 1 = SSI clock is idle at a logic 1.
12	SPHA	SCK phase: 0 = data transmitted on SCK idle level. 1 = data transmitted on SCK active level.
11	SDOEN	SSI slave data out enable: 0 = MDISDO disabled in slave mode. 1 = MDISDO enabled in slave mode.
10	SSNEN	SSN input enable: 0 = SSN input disabled in master mode. 1 = SSN input enabled in master mode.
9—8	Res	Reserved—must be written with logic 0.
7	SDONE[1]	SSI transfer done: 0 = SSI transfer not completed. 1 = SSI transfer completed.
6	WCOLL[1]	Write collision error: 0 = no error. 1 = write to SSI data register (ssid) during a transaction.
5	MODF[1]	Mode fault error: 0 = no error. 1 = SSN asserted while SSI is in master mode.
4—3	Res	Reserved—must be written with logic 0.
2—0	SCLK	SSI clock frequency is master mode: 000 = $f_{FREERUNNINGCLOCK}/2$. 001 = $f_{FREERUNNINGCLOCK}/4$. 010 = $f_{FREERUNNINGCLOCK}/8$. 011 = $f_{FREERUNNINGCLOCK}/16$. 100 = $f_{FREERUNNINGCLOCK}/32$. 101 = reserved. 110 = reserved. 111 = reserved.

1. These fields are read only.

5 Software Architecture (continued)

5.2 Register Settings (continued)

Table 54. SSI Data Register (SSID) Fields

Bit	15—8	7—0
Field	Sign extension of SSI data[1]	SSI data

1. For a read operation, these bits are a sign extension of the data, i.e., the same as bit 7. For a write operation, these bits are ignored.

Table 55. timerc (Timer Control) Register (TIMER0 and TIMER1)

Bit	15—14	13	12	11—10	9—8	7	6	5	4	3—0
Field	Res	RELOAD1	T1EN	Res	PRESCALE1	Res	DISABLE0	RELOAD0	T0EN	PRESCALE0

Bit	Field	Description
15—14	Reserved	Reserved—read as zero, write as zero.
13	RELOAD1	Repeat counts of Timer1 enable: 0 = Timer1—count down and stop. 1 = Timer1—repeat count cycle.
12	T1EN	Timer 1 enable: 0 = Timer1—hold current count. 1 = Timer1—count toward zero.
11—10	Reserved	Reserved—read as zero, write as zero.
9—8	PRESCALE1	Timer 1 prescaler frequency divider (CLKLOW is the low-frequency clock): 00 = CLKLOW/2 01 = CLKLOW/4 10 = CLKLOW/8 11 = CLKLOW/16
7	Res	Reserved—read as zero, write as zero.
6	DISABLE0	Disable timer to conserve power: 0 = Timer0 clocks enabled. 1 = Timer0 clocks off (period register cannot be written with the clock off).
5	RELOAD0	0 = Timer0—count down and stop. 1 = Timer0—repeat count cycle.
4	T0EN	Timer 0 enable: 0 = Timer0—hold current count. 1 = Timer0—count toward zero.
3—0	PRESCALE0	Timer 0 prescaler frequency divider (CLKFREE is the free-running DSP clock): 0000 = CLKFREE/2 1000 = CLKFREE/512 0001 = CLKFREE/4 1001 = CLKFREE/1024 0010 = CLKFREE/8 1010 = CLKFREE/2048 0011 = CLKFREE/16 1011 = CLKFREE/4096 0100 = CLKFREE/32 1100 = CLKFREE/8192 0101 = CLKFREE/64 1101 = CLKFREE/16384 0110 = CLKFREE/128 1110 = CLKFREE/32768 0111 = CLKFREE/256 1111 = CLKFREE/65536

5 Software Architecture (continued)

5.2 Register Settings (continued)

Table 56. cdc Register Fields

Bit	15—14	13	12	11	10—7	6	5	4	3	2	1	0
Field	Res	CFIVOLT	CMXP	CALSTR	CDCCNT	Res	Res	CDC44X	CDCEN	LINE2EN	LINE1EN	SPKREN

Bit	Field	Description
15—14	Reserved	Write with 0.
13	CFIVOLT[1]	5 V mode: 0 = codec is in 3 V mode. 1 = codec is in 5 V mode.
12	CMXP[1]	Enable microphone power external: 0 = microphone power is supplied internally to FCAP. 1 = microphone power must be supplied externally to FCAP.
11	CALTSR[1]	Codec alternate sampling rate; enables the extension of the codec frame: 0 = do not extend the codec frame. 1 = extend the codec frame using CDCCNT.
10—7	CDCCNT[1]	Frame extension count, 4-bit positive integer. If frame extension is enabled by CALTSR, extend the codec frame according to: Frame Cycles = $256 + [(CDCCNT + 1) \times 4]$
6	Reserved	Write with 0.
5	Reserved	Write with 0.
4	CDC4X[1]	Codec interrupt 4 times the normal rate, allows direct access to oversampled data: 0 = codec interrupt every 256 codec clock cycles. 1 = codec interrupt every 64 codec clock cycles.
3	CDCEN[2]	Codec enable: 0 = disable the codec. 1 = enable the codec for any and all operations.
2	LINE2EN	Line 2 output driver enable: 0 = output disabled. 1 = output enabled.
1	LINE1EN	Line 1 output driver enable: 0 = output disabled. 1 = output enabled.
0	SPKREN	Speaker output driver enable: 0 = output disabled. 1 = output enabled.

1. These bits should not be changed when the codec is running, i.e., CDCEN = 1.
2. When CDCEN = 0, all analog outputs and amplifiers are disabled.

5 Software Architecture (continued)

5.2 Register Settings (continued)

Table 57. cdcpg Register Fields

Bit	15—12	11—8	7—4	3	2—0
Field	PGA2	PGMO	PGA1	Res	SPKG

Bit	Field	Description
15—12	PGA2[3:0]	Programmable gain amplifier two (PGA2), settings: 0000 = off, powerdown 0001 = 0 dB 0010 = 2 dB 0011 = 4 dB 0100 = 6 dB 0101 = 8 dB 0110 = 10 dB 0111 = 12 dB 1000 = 14 dB 1001 = 16 dB 1010 = 18 dB 1011 = 20 dB 1100 = 22 dB 1101 = 24 dB 1110 = 26 dB 1111 = 28 dB
11—8	PGMO[3:0]	Programmable microphone amplifier (PGMO), settings: 0000 = off, powerdown 0001 = 16 dB 0010 = 18 dB 0011 = 20 dB 0100 = 22 dB 0101 = 24 dB 0110 = 26 dB 0111 = 28 dB 1000 = 30 dB 1001 = 32 dB 1010 = 34 dB 1011 = 36 dB 1100 = 38 dB 1101 = 40 dB 1110 = 42 dB 1111 = 44 dB
7—4	PGA1[3:0]	Programmable gain amplifier one (PGA1), settings. (See definition above for PGA2[3:0].)
3	Reserved	Write with 0.
2—0	SPKG[2:0]	Speaker amplifier (SPKO), gain settings: 000 = silent 001 = –10 dB 010 = –6 dB 011 = –2 dB 100 = 2 dB 101 = 6 dB 110 = 10 dB 111 = 14 dB

5 Software Architecture (continued)

5.2 Register Settings (continued)

Table 58. cdcamux Register (Codec Analog MUX) Fields

Bit	15—13	12	11—9	8	7—5	4	3—1	0
Field	ADC4MX	ADC4REF	ADC3MX	ADC3REF	ADC2MX	ADC2REF	ADC1MX	ADC1REF

Bit	Field	Description
15—13	ADC4MX	adc4 conversion channel source selection: 000 = convert signal on AI1P and AI1N pins. 001 = convert signal on AI2 pin. 010 = convert signal on AI3 pin. 011 = convert signal on AI4 pin. 100 = convert signal on AI5P and AI5N pins. 101 = convert signal on AI6 pin. 110 = convert signal on AI7 pin. 111 = reserved.
12	ADC4REF	adc4 conversion reference mode: 0 = common-mode reference conversion. 1 = ground-mode reference conversion.
11—9	ADC3MX	adc3 conversion channel source selection. (See definition above for ADC4MX.)
8	ADC3REF	adc3 conversion reference mode. (See definition above for ADC4REF.)
7—5	ADC2MX	adc2 conversion channel source selection. (See definition above for ADC4MX.)
4	ADC2REF	adc2 conversion reference mode. (See definition above for ADC4REF.)
3—1	ADC1MX	adc1 conversion channel source selection. (See definition above for ADC4MX.)
0	ADC1REF	adc1 conversion reference mode. (See definition above for ADC4REF.)

5 Software Architecture (continued)

5.2 Register Settings (continued)

Table 59. adc1, adc2, adc3 Register Fields

Bit	Field	Description
15—1	data	2's complement input data.
0	not used	Filled with 0.

Table 60. adc4 Register Fields

Bit	Field	Description
15—3	data	2's complement input data.
2—0	not used	Filled with 0s.

Table 61. spkr, line1, and line2 Register Fields

Bit	Field	Description
15—3	data	2's complement output data.
2—0	not used	Don't care.

5 Software Architecture (continued)

5.3 Reset States

Table 62. Register States After Reset

Register	Bits 15—0	Register	Bits 15—0	Register	Bits 15—0
a0	•••• •••• •••• ••••	cloop	•••• •••• •••• ••••	psw	•••• 00•• •••• ••••
a0l	•••• •••• •••• ••••	drc	MMMM MMMM MMMM MMMM	pt	•••• •••• •••• ••••
a1	•••• •••• •••• ••••	flashc	0000 0000 0000 0000	r0	•••• •••• •••• ••••
a1l	•••• •••• •••• ••••	IOPUCA[1]	CCCC CCCC CCCC CCCC	r1	•••• •••• •••• ••••
alf	00•• •••• •••• ••••	IOPUCB[1]	CCCC CCCC CCCC CCCC	r2	•••• •••• •••• ••••
auc	0000 0000 0000 0000	IOPUCC[1]	CCCC CCCC CCCC CCCC	r3	•••• •••• •••• ••••
adc1	•••• •••• •••• ••••	IOPUCD[1]	CCCC CCCC CCCC CCCC	rb	0000 0000 0000 0000
adc2	•••• •••• •••• ••••	IOPUCE[1]	CCCC CCCC CCCC CCCC	re	0000 0000 0000 0000
adc3	•••• •••• •••• ••••	inc	0000 0000 0000 0000	sbita	0000 0000 PPPP PPPP
adc4	•••• •••• •••• ••••	ins	0010 0101 0101 0111	sbitb	0000 0010 PPPP PP0P
c0	•••• •••• •••• ••••	i	•••• •••• •••• ••••	sbitc	0000 0000 PPPP PPPP
c1	•••• •••• •••• ••••	j	•••• •••• •••• ••••	sbitd	0000 0000 0000 PPPP
c2	•••• •••• •••• ••••	jtag	•••• •••• •••• ••••	sbite	0000 0000 PPPP PPPP
cbita	0000 0000 •••• ••••	k	•••• •••• •••• ••••	spkr	•••• •••• •••• ••••
cbitb	EEEE 0000 •••• ••••	line1	•••• •••• •••• ••••	ssic	0100 0000 0000 0000
cbitc	•••• •••• •••• ••••	line2	•••• •••• •••• ••••	ssid	•••• •••• •••• ••••
cbitd	XXXX 0000 XXXX ••••	mwait	1111 1111 1111 1111	timer0	0000 0000 0000 0000
cbite	EEEE EEEE •••• ••••	p	•••• •••• •••• ••••	timer1	0000 0000 0000 0000
cdc	0000 0000 0000 0000	PC	0000 0000 0000 0000	timerc	0000 0000 0000 0000
cdcamux	0000 0000 0000 0000	pgreg	•••• •••• •••• ••••	wdogr	•••• •••• •••• ••••
cdcpg	0000 0000 0000 0000	pi	SSSS SSSS SSSS SSSS	x	•••• •••• •••• ••••
chipc	000M 0000 0000 00CC	pl	•••• •••• •••• ••••	y	•••• •••• •••• ••••
chipo	CCCC 0CCC CCCC CCCC	pllc	•••• •••• •••• ••••	ybase	•••• •••• •••• ••••
clkc	0000 0000 DDDD 000D	pr	•••• •••• •••• ••••	yl	•••• •••• •••• ••••

1. These registers are shown as upper-case because they are not directly program-accessible. They are accessed indirectly via write operations to the **cbit<a—e>** registers.

Bit code: Indicates that this bit:

- • is unknown on powerup reset and unaffected by all other resets.
- 0 is set to logic zero by all types of resets.
- 1 is set to logic one by all types of resets.
- C is not affected by a pin (RSTB) reset, watchdog reset or power-loss reset; however, powerup reset and JTAG reset clear the bit to zero.
- D setting depends on the value of DRCEN (**chipc**[12]) bit. If DRCEN is 0, it is cleared to logic 0 by all resets. If DRCEN is 1, the bit retains its state following a pin (RSTB), but is cleared to zero by all other resets—watchdog, power-loss, or powerup reset.
- E setting is dependent on the value of the EXM pin during an external pin reset. If EXM is zero, the value is cleared to zero. If EXM is one, the same bit is preset to one.
- M is not changed following an external pin (RSTB) reset; however, watchdog, power-loss, powerup, and JTAG reset clears the bit to zero.
- P reflects the value on its corresponding input pin.
- S shadows the program counter (PC).
- X may not be written and is read as zero.

5 Software Architecture (continued)

5.4 Instruction Set Formats

This section defines the hardware-level encoding of the *FlashDSP*1650 instructions.

5.4.1 Multiply/ALU Instructions

Table 63. Format 1: Multiply/ALU Read/Write Group

Field	T					D	S	F1				X	Y			
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Table 64. Format 1a: Multiply ALU Read/Write Group

Field	T					$\overline{aT}$	S	F1				X	Y			
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Table 65. Format 2: Multiply/ALU Read/Write Group

Field	T					D	S	F1				X	Z			
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Table 66. Format 2a: Multiply/ALU Read/Write Group

Field	T					$\overline{aT}$	S	F1				X	Z			
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

5.4.2 Special Function Instructions

Table 67. Format 3: F2 ALU Special Functions

Field	T					D	S	F2				CON				
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Table 68. Format 3a: F3 ALU Operations

Field	T					D	S	F3				SRC2		$\overline{aT}$	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

5.4.3 Control Instructions

Table 69. Format 4: Branch Direct Group

Field	T				JA											
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

5 Software Architecture (continued)

5.4 Instruction Set Formats (continued)

5.4.3 Control Instructions (continued)

Table 70. Format 5: Branch Indirect Group

Field	T					B			Reserved							0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Table 71. Format 6: Conditional Branch Qualifier

Field	T					SI	Reserved				CON					
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Note: A branch instruction immediately follows the qualifier.

5.4.4 Data Move Instructions

Table 72. Format 7: Data Move Group

Field	T					$\overline{aT}$	R						Y/Z			
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Table 73. Format 8: Data Move (16-Bit Immediate Operand—2 Words)

Field	T					D	R						Reserved			
	16-bit Immediate Operand (IM16)															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Table 74. Format 9: Short Immediate Group

Field	T					I	9-bit Short Immediate Operand (IM9)								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Table 75. Format 9a: Direct Addressing

Field	T					R/W	DR[3:0]				1	OFFSET				
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

5.4.5 Cache Instructions

Table 76. Format 10: Do/Redo

Field	T					NI			K							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

5 Software Architecture (continued)

5.4 Instruction Set Formats (continued)

5.4.6 Field Descriptions

T Field: Specifies the type of instruction.

Table 77. T Field

T	Operation	ALU Type	Format
0000x	goto JA		4
00010	short IM9 j, k, rb, re		9
00011	short IM9 r0, r1, r2, r3		9
00100	Y = a1[l]	F1[1]	1
00101	Z:aT[l]	F1	2a
00110	Y	F1	1
00111	aT[l] = Y	F1	1a
01000	Bit 0 = 0, aT = R		7
01000	Bit 0 = 1, aTl = R		7
01001	Bit 10 = 0, R = a0	—	7
01001	Bit 10 = 1, R = a0l		7
01010	R = IM16		8
01011	Bit 10 = 0, R = a1		7
01011	Bit 10 = 1, R = a1l		7
01100	Y = R		7
01101	Z:R	—	7
01110	Do, Redo		10
01111	R = Y		7
1000x	call JA		4
10010	ifc CON	F2[2]	3
10011	if CON	F2	3
10100	Y = y[l]	F1	1
10101	Z:y[l]	F1	2
10110	x = Y	F1	1
10111	y[l] = Y	F1	1
11000	Bit 0 = 0, branch indirect		5
11000	Bit 0 = 1	F3[3]	3a
11001	y = a0, x = X		1
11010	Conditional branch qualifier		6
11011	y = a1, x = X	F1	1
11100	Y = a0[l]	F1	1
11101	Z:y, x = X	F1	2
11110	Bit 5 = 0, reserved		9a
11110	Bit 5 = 1, direct addressing		9a
11111	y = Y, x = X	F1	1

1. See Table 83 on page 76.
2. See Table 84 on page 76.
3. See Table 85 on page 76.

$\overline{aT}$ Field: Specifies a transfer accumulator.

Table 78. $\overline{aT}$ Field

$\overline{aT}$	Register
0	Accumulator 1
1	Accumulator 0

B Field: Specifies the type of branch instruction.

Table 79. B Field

B	Operation
000	return
001	ireturn
010	goto pt
011	call pt
1XX	Reserved

CON Field: Specifies the condition for special functions and conditional control instructions.

Table 80. CON Field

CON	Condition	CON	Condition
00000	mi	10000	gt
00001	pl	10001	le
00010	eq	10010	pllon
00011	ne	10011	slowon
00100	lvs	10100	plloff
00101	lvc	10101	slowoff
00110	mvs	10110	stopclk
00111	mvc	10111	Reserved
01000	heads	11000	Reserved
01001	tails	11001	Reserved
01010	c0ge	11010	npint
01011	c0lt	11011	njint
01100	c1ge	11100	Reserved
01101	c1lt	11101	Reserved
01110	true	11110	Reserved
01111	false	11111	Reserved

D Field: Specifies a destination register.

Table 81. D Field

D	Register
0	Accumulator 0
1	Accumulator 1

5 Software Architecture (continued)

5.4 Instruction Set Formats (continued)

5.4.6 Field Descriptions (continued)

DR Field: Specifies the data register.

Table 82. DR Field

DR Value	Register
0000	r0
0001	r1
0010	r2
0011	r3
0100	a0
0101	a0l
0110	a1
0111	a1l
1000	y
1001	yl
1010	p
1011	pl
1100	x
1101	pt
1110	pr
1111	psw

F1 Field: Specifies the multiply/ALU function.

Table 83. F1 Field

F1	Operation	
0000	aD = p	p = x * y
0001	aD = aS + p	p = x * y
0010		p = x * y
0011	aD = aS – p	p = x * y
0100	aD = p	
0101	aD = aS + p	
0110	nop	
0111	aD = aS – p	
1000	aD = aS | y	
1001	aD = aS ^ y	
1010	aS & y	
1011	aS – y	
1100	aD = y	
1101	aD = aS + y	
1110	aD = aS & y	
1111	aD = aS – y	

F2 Field: Specifies the special function to be performed.

Table 84. F2 Field

F2	Operation
0000	aD = aS >> 1
0001	aD = aS << 1
0010	aD = aS >> 4
0011	aD = aS << 4
0100	aD = aS >> 8
0101	aD = aS << 8
0110	aD = aS >> 16
0111	aD = aS << 16
1000	aD = p
1001	aDh = aSh + 1
1010	aD = ~aS
1011	aD = rnd(aS)
1100	aD = y
1101	aD = aS + 1
1110	aD = aS
1111	aD = –aS

F3 Field: Specifies the operation in an F3 ALU instruction.

Table 85. F3 Field

F3	Operation
1000	aD = aS[h, l] | (aT, IM16, p)
1001	aD = aS[h, l] ^ (aT, IM16, p)
1010	aS[h, l] & (aT, IM16, p)
1011	aS[h, l] – (aT, IM16, p)
1101	aD = aS[h, l] + (aT, IM16, p)
1110	aD = aS[h, l] & (aT, IM16, p)
1111	aD = aS[h, l] – (aT, IM16, p)

I Field: Specifies a register for short immediate data move instructions.

Table 86. I Field

I	Register
00	r0/j
01	r1/k
10	r2/rb
11	r3/re

5 Software Architecture (continued)

5.4 Instruction Set Formats (continued)

5.4.6 Field Descriptions (continued)

JA Field: 12-bit jump address.

K Field: Number of times the NI instructions in cache are to be executed. Zero specifies use of value in **cloop** register.

NI Field: Number of instructions to be loaded into the cache. Zero implies **redo** operation.

R Field: Specifies the register for data move instructions.

Table 87. R Field

R	Condition	R	Condition
000000	r0	100000	inc
000001	r1	100001	ins
000010	r2	100010	pllc
000011	r3	100011	clkc
000100	j	100100	cloop
000101	k	100101	mwait
000110	rb	100110	drc
000111	re	100111	wdogr
001000	pt	101000	cbita, iopuca[1]
001001	pr	101001	sbita
001010	pi	101010	chipo
001011	i	101011	jtag
001100	p	101100	cbite, iopuce[1]
001101	pl	101101	sbite
001110	Reserved	101110	cbitd, iopucd[1]
001111	sbitd	101111	flashc
010000	x	110000	a0
010001	y	110001	a0l
010010	yl	110010	a1
010011	auc	110011	a1l
010100	psw	110100	timerc
010101	c0	110101	timer0
010110	c1	110110	cbitb
010111	c2	110111	sbitb
011000	cdcpg	111000	cbitc, iopucc[1]
011001	cdcamux	111001	sbitc
011010	adc1/spkr	111010	timer1
011011	pgreg	111011	line1, adc2[2]
011100	ssid	111100	line2, adc3[2]
011101	ssic	111101	adc4
011110	chipc	111110	cdc
011111	ybase	111111	alf

1. These registers are double-mapped and accessed based on the value of the WIOPUR bit in the **chipc** register.
2. One is read only and the other is write only.

R/W Field: A 1 specifies a read, DR = *(OFFSET). A 0 specifies a write, *(OFFSET) = DR.

S Field: Specifies a source accumulator.

Table 88. S Field

S	Register
0	Accumulator 0
1	Accumulator 1

SI Field: Specifies when the conditional branch qualifier instruction should be interpreted as a software interrupt instruction. (Reserved for Lucent hardware development system use.)

Table 89. SI Field

SI	Operation
0	Not a software interrupt
1	Software interrupt

SRC2 Field: Specifies operands in an F3 ALU instruction.

Table 90. SRC2 Field

SRC2	Operands
00	aSl, IM16
01	aSh, IM16
10	aS, aT
11	aS, p

X Field: Specifies the addressing of ROM data in the two-operand multiply/ALU instructions. Specifies the high or low half of an accumulator or the **y** register in one-operand multiply/ALU instructions.

Table 91. X Field

X	Operation
Two-Operand Multiply/ALU	
0	*pt++
1	*pt++i
One-Operand Multiply/ALU	
0	aTl, yl
1	aTh, yh

5 Software Architecture (continued)

5.4 Instruction Set Formats (continued)

5.4.6 Field Descriptions (continued)

Y Field: Specifies the form of register-indirect addressing with postmodification.

Table 92. Y Field

Y	Operation
0000	*r0
0001	*r0++
0010	*r0– –
0011	*r0++j
0100	*r1
0101	*r1++
0110	*r1– –
0111	*r1++j
1000	*r2
1001	*r2++
1010	*r2– –
1011	*r2++j
1100	*r3
1101	*r3++
1110	*r3– –
1111	*r3++j

Z Field: Specifies the form of register-indirect compound addressing with postmodification.

Table 93. Z Field

Z	Operation
0000	*r0zp
0001	*r0pz
0010	*r0m2
0011	*r0jk
0100	*r1zp
0101	*r1pz
0110	*r1m2
0111	*r1jk
1000	*r2zp
1001	*r2pz
1010	*r2m2
1011	*r2jk
1100	*r3zp
1101	*r3pz
1110	*r3m2
1111	*r3jk

6 Device Requirements and Characteristics

This section describes *FlashDSP*1650 device requirements and characteristics.

6.1 Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability.

Absolute maximum ratings are the limiting conditions that can be applied to all variations of circuit and environmental conditions without the occurrence of permanent damage.

External leads can be bonded and soldered safely at temperatures of up to 300 °C.

Table 94. Maximum Package Rating Parameters and Values

Parameter	Min	Max	Unit
Voltage on Any Pin with Respect to Ground	V_{SS} – 0.5	V_{DD} + 0.5	V
Power Dissipation	—	1	W
Ambient Temperature	–40	85	°C
Storage Temperature	–65	150	°C

6.2 Handling Precautions

All MOS devices must be handled with certain precautions to avoid damage due to the accumulation of static charge. Although input protection circuitry has been incorporated into the devices to minimize the effect of this static buildup, proper precautions should be taken to avoid exposure to electrostatic discharge during handling and mounting.

Lucent employs a human-body model for ESD-susceptibility testing. Because the failure voltage of electronic devices is dependent on the current, voltage, and hence, the resistance and capacitance, it is important that standard values be employed to establish a reference by which to compare test data. Values of 100 pF and 1500 V are the most common and are the values used in the Lucent human-body model test circuit. The breakdown voltage for the *FlashDSP*1650 is greater than 2000 V.

6 Device Requirements and Characteristics (continued)

6.3 Recommended Operating Conditions

Table 95. Recommended Voltage and Temperature

Minimum Instruction Cycle Time (T_{MIN})	Temperature Class	Supply Voltage V_{DD} (V)		Ambient Temperature T_A (°C)	
		Min	Max	Min	Max
25 ns	Commercial	4.5	5.5	0	70
30 ns	Industrial	4.5	5.5	–40	85
31.25 ns	Industrial	3.0	3.6	–40	85

6.4 Decoupling Requirements

Install a high-quality ceramic 0.01 pF capacitor between each V_{DD} pin and ground. Install each capacitor as close as possible to the *FlashDSP* 1650 package. Also, install an additional 0.47 µF—1.0 µF capacitor at only one of the V_{DD} pins.

6.5 Package Thermal Considerations

The recommended operating temperature specified in Table 95 is based on the maximum power, package type, and maximum junction temperature. The following equations describe the relationship between these parameters. If the application's maximum power is less than the worst-case value; this relationship determines a higher maximum ambient temperature or the maximum temperature measured at top dead center of the package.

$T_A = T_J - P \times \Theta_{JA}$

$T_{TDC} = T_J - P \times \Theta_{J-TDC}$

where T_A is the still-air ambient temperature and T_{TDC} is the temperature measured by a thermocouple at the top dead center of the package.

Maximum Junction Temperature (T_J) in 80-pin MQFP . . . . . .125 °C

80-pin MQFP Maximum Thermal Resistance in Still-air-ambient (Θ_{JA}) . . . . . 55 °C/W

80-pin MQFP Maximum Thermal Resistance, Junction to Top Dead Center (Θ_{J-TDC}) . . . . . 12 °C/W

Maximum Junction Temperature (T_J) in 100-pin TQFP . . . . . .125 °C

100-pin TQFP Maximum Thermal Resistance in Still-air-ambient (Θ_{JA}). . . . . 64 °C/W

100-pin TQFP Maximum Thermal Resistance, Junction to Top Dead Center (Θ_{J-TDC}) . . . . . 6 °C/W

WARNING: Due to package thermal constraints, proper precautions in the user's application should be taken to avoid exceeding the maximum junction temperature of 125 °C. Otherwise, the device will be affected adversely.

7 Electrical Requirements and Characteristics

The following electrical requirements and characteristics are preliminary and subject to change. Electrical requirements refer to conditions imposed on the user for proper operation of the device. Electrical characteristics refer to the behavior of the device under conditions specified in Section 6, Device Requirements and Characteristics. Tables 96, 97, and 98 describe the valid electrical parameters of these conditions.

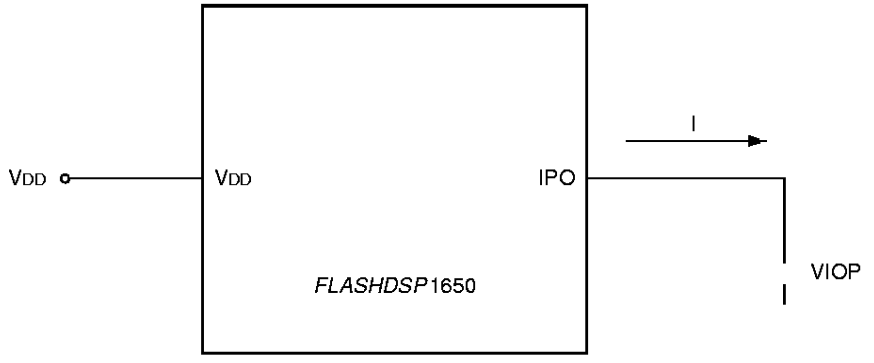
Table 96. Electrical Requirements

Parameter	Symbol	V_{DD} = 4.5 V to 5.5 V			V_{DD} = 3.0 V to 3.6 V			Unit
		T_{MIN} = 25 ns or 30 ns			T_{MIN} = 31.25 ns			
		Min	Typ	Max	Min	Typ	Max	
Input Voltage (except clocks, INTB, RSTB):								
Low	V_{IL}	—	—	0.8	—	—	0.8	V
High	V_{IH}	2.0	—	—	2.0	—	—	V
Input Voltage (INTB):								
Low	V_{IL}	—	—	0.6	—	—	0.6	V
High	V_{IH}	V_{DD} – 0.5	—	—	V_{DD} – 0.3	—	—	V
Input Voltage (RSTB) and XTALB[1]:								
Low	V_{IL}	—	—	0.5	—	—	0.5	V
High	V_{IH}	V_{DD} – 0.5	—	—	V_{DD} – 0.3	—	—	V
Pull-Up Resistance (strong pull, for IOPA only): DIR[n] = 0 (Input) IOPUA[n] = 1 and IOPLA[n] = 1	R_{up}	—	18	—	—	32	—	kΩ
Pull-Up Resistance: DIR[n] = 0 (Input) IOPU[n] = 1 and IOPL[n] = 0	R_{up}	—	87	—	—	157	—	kΩ
Pull-Down Resistance: DIR[n] = 0 (Input) IOPU[n] = 0 and IOPL[n] = 1	R_{dn}	—	39	—	—	53	—	kΩ

1. Internal crystal oscillator bypass mode only.

Note: For information about input buffer power dissipation, see Section 7.2.

Figure 10 shows how the pull-up/pull-down can be measured. The detailed settings of registers are specified in Table 96. Subcircuits containing an I/O port are used to simulate the pull-up/pull-down characteristics. Voltage VIOP is varied and the current through it is monitored. The result is shown in Figures 11, 12, and 13.



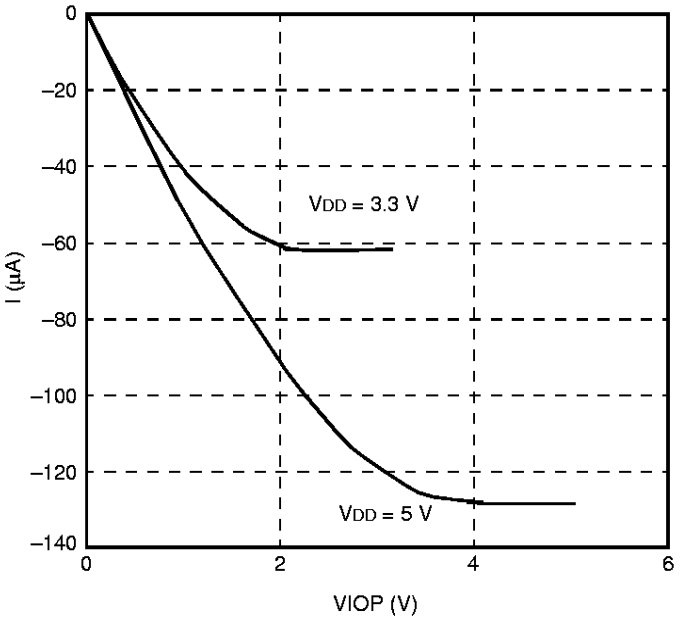
Note: Maximum current occurs when: VIOP = V_{DD} for pull-down; 0 V for pull-up.

5-6208 (F)

Figure 10. Pull-Up and Pull-Down Measurements

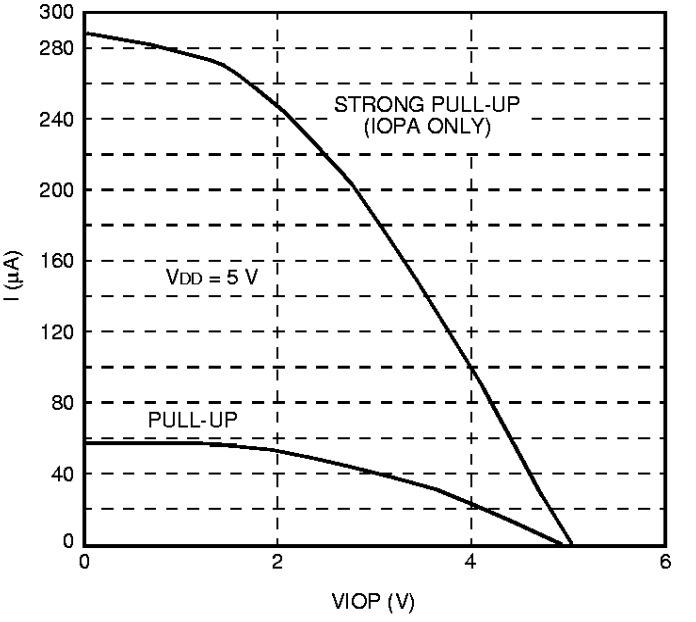
7 Electrical Requirements and Characteristics (continued)

Figures 11, 12, and 13 show that the current during pull-up or pull-down are not resistive since MOS transistors are used. In Table 96, R_{up} is measured with the IOP pad shorted to ground while R_{dn} is measured with the IOP pad shorted to V_{DD}. In either case, the current through the short, I, is measured to calculate the resistance $R_{up} = V_{DD}/I$ or $R_{dn} = V_{DD}/I$. The resistance gives highest value during pull-up/pull-down as the I – V characteristics in Figures 11, 12, and 13 show.



5-611 (F)

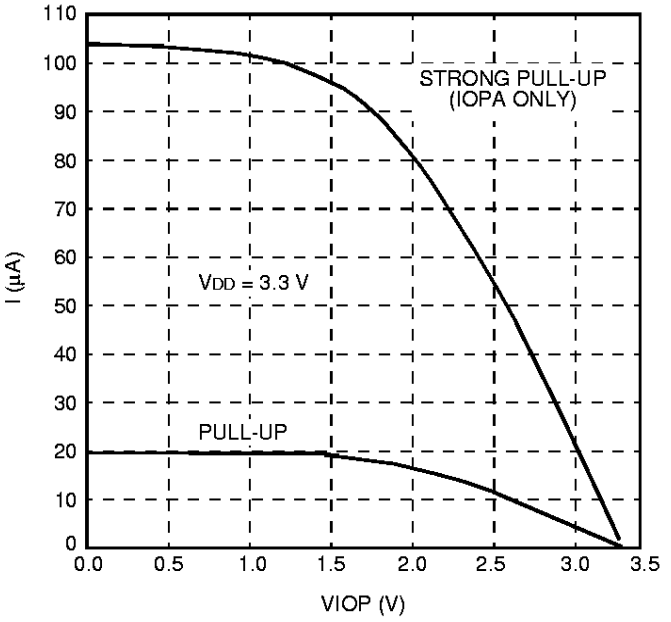
Figure 11. Pull-Down Characteristics of an I/O Port



5-6209 (F)

Figure 12. Pull-Up Characteristics of an I/O Port at V_{DD} = 5 V

7 Electrical Requirements and Characteristics (continued)



5-6210 (F)

Figure 13. Pull-Up Characteristics of an I/O Port at V_{DD} = 3.3 V

Table 97. Electrical Characteristics

Parameter	Symbol	V_{DD} = 4.5 V to 5.5 V		V_{DD} = 3.0 V to 3.6 V		Unit
		T_{MIN} = 25 ns or 30 ns		T_{MIN} = 31.25 ns		
		Min	Max	Min	Max	
Output Low Voltage:						
Low (I_{OL} = 2.0 mA)	V_{OL}	—	0.4	—	0.4	V
Low (I_{OL} = 50 µA)	V_{OL}	—	0.2	—	0.2	V
Output High Voltage:						
High (I_{OH} = –2.0 mA)	V_{OH}	V_{DD} – 0.7	—	V_{DD} – 0.7	—	V
High (I_{OH} = –50 µA)	V_{OH}	V_{DD} – 0.2	—	V_{DD} – 0.2	—	V
Output 3-state Current, V_{DD} = V_{DD} (max):						
Low (V_{IL} = 0 V)	I_{OZL}	–10	—	–10	—	µA
High [V_{IH} = V_{DD} (max)]	I_{OZH}	—	10	—	10	µA
Schmitt Trigger Hysteresis:						
INTB	V_{IHL}	300	600	300	600	mV
RSTB	V_{IHL}	1.8	2.2	1.8	2.2	V
V_{DDPLM}	V_{IHL}	150	160	280	320	mV
Input Capacitance	C_I	—	10	—	10	pF
Power-loss Detect Circuit:						
Upper Threshold—V_{DDPLM}	V_{REC}	3.9	4.5	2.7	3.0	V
Lower Threshold—V_{DDPLM}	V_{TRIP}	3.6	4.2	2.5	2.8	V
Slew Rate:						
V_{DDPLM} Rise	—	—	1	—	1	V/ms
V_{DDPLM} Fall	—	—	1	—	1	V/ms
Input Current:						
V_{DDPLM}	I_{PU}	200	320	200	320	µA

7 Electrical Requirements and Characteristics (continued)

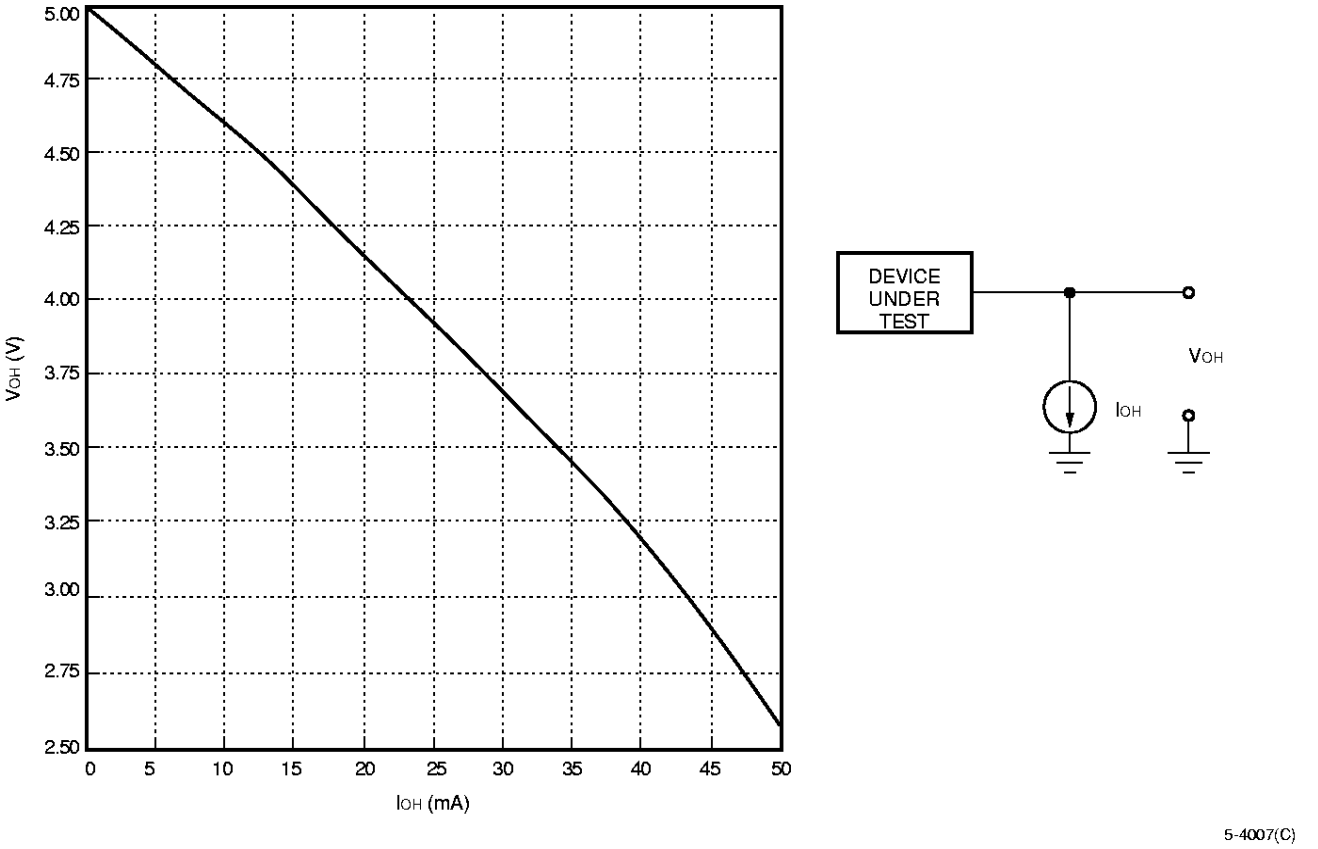


Figure 14. Plot of V_{OH} vs. I_{OH} Under Typical Operating Conditions

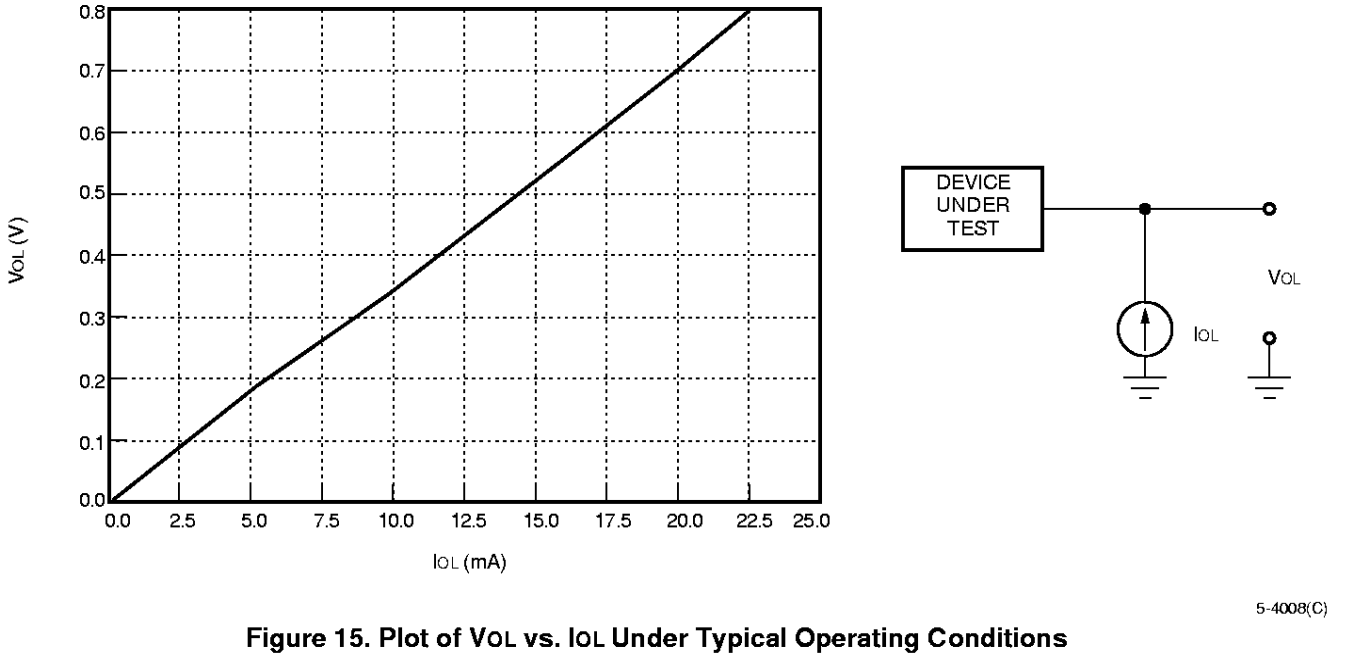


Figure 15. Plot of V_{OL} vs. I_{OL} Under Typical Operating Conditions

7 Electrical Requirements and Characteristics (continued)

Table 98. PLL Electrical Specifications, VCO Frequency Ranges

Parameter	Symbol	Min	Max	Unit
VCO Frequency Range[1] (V_{DD} = 3 V ± 10%)	fVCO	30	60	MHz
VCO Frequency Range[1] (V_{DD} = 5 V ± 5%)	fVCO	40	80	MHz
Input Jitter at CKI	—	—	200	ps-rms

1. The M and N counter values in the **pllc** register must be set so that the VCO will operate in the appropriate range,

where $VCOfreq = CLKINfreq \times \frac{(m+2)}{(N+1)}$.

Choose the lowest value of N and then the appropriate value of M for internal MIPS rate = $\frac{(InputClock(m+2))}{2((K+1)(N+1))}$

Table 99. PLL Electrical Specifications and Register Settings

Voltage (Volts)	M pllc[5:0]	K pllc[8:6]	N pllc[10:9]	ICP pllc[13:11]	LF pllc[15:14]	PFIVOLT clkc[12]	Typical Lock Time (µs) (See Note.)
3.0—3.6	18—26	0—7	0	110	11	0	12
3.0—3.6	10—17	0—7	0	110	10	0	12
3.0—3.6	1—9	0—7	0	111	00	0	12
4.5—5.5	18—26	0—7	0	110	11	1	12
4.5—5.5	10—17	0—7	0	110	10	1	12
4.5—5.5	1—9	0—7	0	111	00	1	12

Note: Lock-in time represents the time following assertion of the PLLEN bit of the **pllc** register during which the PLL output clock is unstable. The DSP must operate from the CLKIN input clock or from CLKLOW while the PLL is locking.

7.1 Typical Power Dissipation

Power dissipation is highly dependent on program activity and the frequency of operation. Table 100 lists typical power dissipation on a module-by-module basis and consists of preliminary data that is subject to change. For analog modules, this data assumes the recommended external circuitry is being used. For digital modules, it refers to internal power only, i.e., Table 100 does not account for activity on digital I/O pins. The total analog and internal digital power can be calculated by adding the sum of the modules that have been enabled. For example, the lowest power dissipation can be achieved by turning everything off except for the internal low-power oscillator and setting the stop clock bit. In this case, the total power would be 62 µW at 3.1 V.

As another example, with the PLL on and driving the DSP at 40 MIPS, and with the analog codec, microphone amp, and line1 driver enabled, and with TIMER1 counting at 32 kHz and TIMER0 running, the total analog and internal digital power at 5 V is 1.65 + (0.092 • 80) + (9.4 • 40) + (0.1 • 40) + 0.02 + 9.5 + 5.3 + 12.13 = 415.96 µW.

7 Electrical Requirements and Characteristics (continued)

7.1 Typical Power Dissipation (continued)

Table 100. Internal Module Power Dissipation

DSP Module	Enabled When	Instruction Rate (CLKFREE)	Typical Module Power Dissipation	
			5.0 V (mW)	3.1 V (mW)
Internal Low Power Oscillator	**clkc**[2] = 0	NA	0.175	0.062
4 MHz Crystal Oscillator	**clkc**[1] = 0 and OSCBYP pin = GND	NA	6	0.83
4 MHz Direct Clock Input (internal oscillator bypassed)	OSCBYP pin = V_{DD}	NA	2.5	0.52
Power-loss Circuit	VDDPLM pin = V_{DD} and **chipo**[2:0] ≠ 000	NA	1.37	0.53
Analog On (speaker, line drivers, and PG amps off)	**cdc**[3] = 1	NA	9.5	3.5
PGA2 Amplifier	**cdcpg**[15:12] ≠ 0000	NA	2.65	0.76
PGA1 Amplifier	**cdcpg**[7:4] ≠ 0000	NA	2.65	0.76
Microphone Amplifier	**cdcpg**[11:8] ≠ 0000	NA	5.30	1.62
Speaker Driver (8 Ω load)[1]	**cdc**[3] = 1 and **cdc**[0] = 1	NA	330.0	89.6
Speaker Drvier (150 Ω load)[1]	**cdc**[3] = 1 and **cdc**[0] = 1		82.75	8.37
Line1 Driver (1.2 kΩ load)	**cdc**[3] = 1 and **cdc**[1] = 1	NA	12.13	3.72
Line2 Driver (1.2 kΩ load)	**cdc**[3] = 1 and **cdc**[2] = 1	NA	12.13	3.72
SSI Enabled	**ssic**[15] = 1	NA	0.032 • $F_{CLKFREE}^2$	0.012 • $F_{CLKFREE}^2$
PLL Enabled	**clkc**[0] = 1	NA	1.65 + (0.092 • F_{VCO}^2)	0.75 + (0.036 • F_{VCO}^2)
Timer1 Enabled (32 kHz)	**timerc**[12] = 1	NA	<0.020	<0.005
Timer1 Enabled (1 MHz)	**timerc**[12] = 1	NA	0.150	0.046
Timer0 Enabled	**timerc**[6] = 0 and **timerc**[4] = 1	16 kHz	<0.020	<0.005
		512 kHz	0.030	0.012
		2 MHz	0.230	0.080
		>4 MHz	0.100 • $F_{CLKFREE}^2$	0.031 • $F_{CLKFREE}^2$
Nonstopclock Sleep Mode	**alf**[15] = 1 and **clkc**[3] = 0	16 kHz	<0.020	<0.005
		512 kHz	0.37	0.127
		2 MHz	0.795	0.493
		>4 MHz	0.678 • $F_{CLKFREE}^2$	0.244 • $F_{CLKFREE}^2$
Active[3]	**alf**[15] = 1 and **clkc**[3] = 0	16 kHz	0.21	0.071
		512 kHz	5.71	2.21
		2 MHz	25.2	8.74
		>4 MHz	9.4 • $F_{CLKFREE}^2$	3.7 • $F_{CLKFREE}^2$
Flash ROM (*FlashDSP*1650 only)	Always	NA	111.50	29.15

1. Speaker driver power was measured at maximum gain using a 1/3 scale 1 kHz sine wave. This power will vary significantly depending on gain setting, signal level, and load impedance.
2. $F_{CLKFREE}$ and F_{VCO} refer to the frequency of the free-running clock and the frequency of the PLL VCO, both in units of megahertz (MHz).
3. Active power is measured while the DSP is executing a single-cycle, double memory fetch FIR filter from cache.

7 Electrical Requirements and Characteristics (continued)

7.2 Input and I/O Buffer Power Dissipation

Power dissipation due to the input and I/O buffers is highly dependent on the input voltage level. At full CMOS levels, essentially no dc current is drawn. However, for levels near the threshold of 1.4 V, high current can flow. Therefore, all unused input pins should be tied inactive to V_{DD} or V_{SS}, and all unused I/O pins should be tied inactive through a 10 kΩ resistor to V_{DD} or V_{SS}. Tables 101 and 102 show the input buffer power dissipation for 43 inputs biased at dc level, V_{IN}, with V_{DD} at 5.0 V.

Table 101. Input Buffer Maximum Power Dissipation

V_{IN} (V)	5.0	3.6	2.8	2.4	2.0	1.4	0.8	0.4	0
PD (mW)	<1.0	13.5	140	180	180	High	80	7.5	<1.0

WARNING: The device needs to be clocked for at least twelve f_{XTALB} cycles during reset after powerup; otherwise, high current may flow.

Table 102. Schmitt Trigger Input Buffer Maximum Power Dissipation

V_{IN} (V)	5.0	3.6	2.8	2.4	2.0	1.4	0.8	0.4	0
PD (mW)	<1.0	13.5	140	180	180	180	80	7.5	<1.0

7.3 Analog Interface

7.3.1 A-to-D and D-to-A Converter

The analog-to-digital converter uses a resistor string of 8191 series connected metal film resistors made from the METAL1 interconnect metallization. A reference voltage is applied to one end of the string while the other end is tied to ground. Digital-to-analog conversion logic selects taps on the resistor representing the digital word. The converted value is then stored in a sample hold.

Analog-to-digital conversion is accomplished using a successive approximation algorithm to the resistor string D to A. The input voltage is sampled and held while a comparator determines if the resistor string tap is higher or lower than the held value of the input.

Table 103. D-to-A and A-to-D Specifications

Parameter	CFIVOLT = 1 Value	CFIVOLT = 0 Value	Unit
Reference Voltage (V_{REF})	~2	~1	V
Conversion Gain	$2^{15} - 1 = V_{REF}$	$2^{15} - 1 = V_{REF}$	V
	$-2^{15} - 1 = 0$	$-2^{15} - 1 = 0$	V
Gain Accuracy	5	5	%
Signal to Noise Ratio (differential)	72	67	dB
Signal to Dist. Ratio: –0.8 Vp-p	60	55	dB
–8 mVp-p	27[1]	27[1]	dB
Number of Bits	>12	>12	—
Center Value Error (1/2 V_{REF})	±25	±25	mV

1. The design goal is 30 dB.

7 Electrical Requirements and Characteristics (continued)

7.3 Analog Interface (continued)

7.3.2 A-to-D Inputs

The A-to-D inputs consist of two differential input pairs and five single-ended inputs. The five single-ended inputs are identical and can be used in either a ground-referenced manner, or a common-mode referenced manner by programming the cdcamux control register.

Common-mode reference is the default mode for the converter and means the input ac signal will be centered about VREF for a common-mode (dc offset) value. Programming the associated control bit for an input to be common-mode referenced causes the sampled value to be compared to VREF. Single-ended input range is approximately 1/2 VREF to 3/2 VREF.

Ground referenced means the input signal to be converted should be between GROUND (VSSA) and reference voltage VREF. The converted value is a 13-bit digital word in two's complement coding. If the input is higher than VREF, the digital word will be near the most positive two's complement value. If the input is below VSSA, the digital word will be near the most negative value.

The differential input compares the difference of the input pins to a differential DAC output in the comparator.

No internal antialias filters are included, so the user must provide these filters externally as needed. A suggested filter from PGMO (PGOUT, PGOUT2) to any single-ended analog input AI(n) is shown in Figure 16.

Figure 17 illustrates the architecture of the 165X successive approximation A/D converter. It consists of a comparator, D/A converter, and codec control logic. The function of the codec control logic is to determine the value of each bit in sequence based on the output of the comparator using a standard successive approximation algorithm. Normally, conversions ADC1, ADC2, and ADC3 operate in the oversampling-averaged mode, which means four samples are converted and averaged for each digital word per 16 kHz frame. In conversion ADC4, only one sample is converted into a 13-bit digital word per frame. In the 4X sampling mode, however, an interrupt is issued every 64 codec clock cycles so the ADC values are available after each conversion. No averaging is done. 4X mode does not affect the DAC operation.

To illustrate the conversion process, assume the reference voltage is VREF/2 (ground reference mode). An analog input (AI1 to AI7) is selected by setting the **cdcamux** register which closes the corresponding select switch (SEL1 to SEL7). The conversion cycle, say of ADC1, begins by closing the sampling switches (SAMP2P and SAMP2N) to sample the analog input signal to be converted. The analog sample is then held by opening the sampling switches and closing the HOLD switch. Next, the codec control logic sets the MSB bit to 1 and all other bits to zero in the output ADC1 register. This 13-bit digital word is applied to the D/A converter, which generates an analog signal equal to 0.5 VREF. This is then compared to the held analog sample. If the comparator output is high, the codec logic keeps the MSB as 1. If the comparator output is low, the codec logic sets the MSB to 0. This completes the first step in the approximation. The value of the MSB is known at this point. The process repeats, and the codec logic sets the next bit to 1 and all other lesser bits to 0. The process continues in this way until all 13 bits in the digital word are determined.

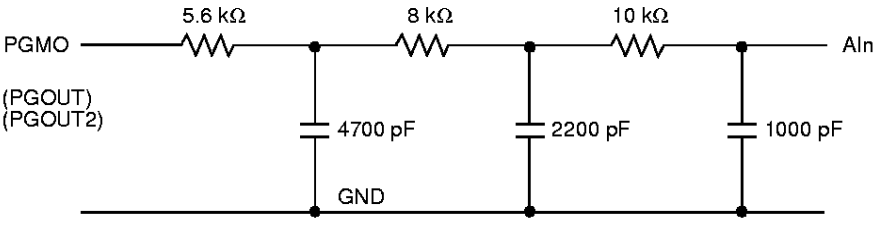


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Figure 16. Antialias Filter from PGMO

7 Electrical Requirements and Characteristics (continued)

7.3 Analog Interface (continued)

7.3.2 A-to-D Inputs (continued)

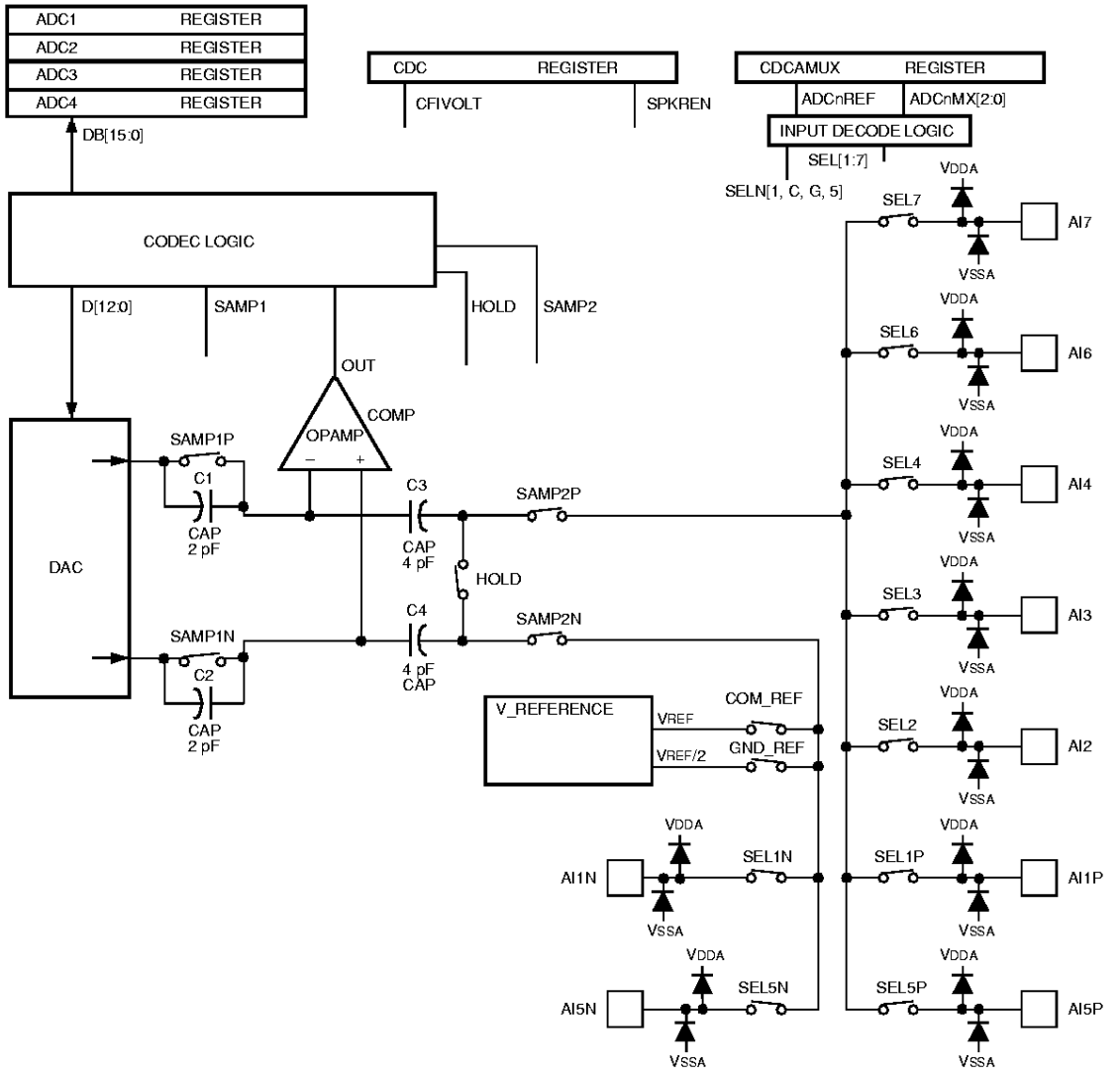

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Figure 17. ADC Functional Block Diagram

7 Electrical Requirements and Characteristics (continued)

7.3 Analog Interface (continued)

7.3.2 A-to-D Inputs (continued)

Table 104. Analog-to-Digital Converter (A/D) Electrical Characteristics (T_A = 25 °C)

Parameter Dynamic Performance	CFIVOLT = 1 Value	CFIVOLT = 0 Value	Unit	Test Conditions/ Comments
Signal to Noise Ratio, at 90% Input Drive Differential Input 0—8 kHz FLAT	75	71	dB	Vin = 1 kHz sine wave fsample = 16 kHz
Signal to Noise Ratio, at 90% Input Drive Single-ended Input 0—8 kHz FLAT	59 (using AI3 input) 67 (using AI1P input, with AI1N connected to V_{REF})	58 (AI3) 62 (AI1P)	dB	Vin = 1 kHz sine wave fsample = 16 kHz
Signal to Distortion Ratio, 90% Drive, Differential Input	82	71	dB	Vin = 1 kHz sine wave fsample = 16 kHz
Signal to Distortion Ratio, 90% Drive, Single-ended Input	69 (AI3) 80 (AI1P)	66 (AI3) 71 (AI1P)	dB	Vin = 1 kHz sine wave fsample = 16 kHz
Gain Mismatch Between Inputs	<0.1	<0.1	dB	—
Analog Input				
Internal Reference V_{REF}	2.0 typ	1.0 typ	V	—
Input Voltage Ranges	0 to V_{REF} 1/2 V_{REF}— 3/2 V_{REF}	0 to V_{REF} 1/2 V_{REF}— 3/2 V_{REF}	V V	Ground-mode reference Common-mode reference
Leakage Current	100 max	100 max	nA	—
Input Capacitance	20 typ	20 typ	pF	—
Logic Outputs				
Output High Voltage, V_{OH}	2.0 typ	1.0 typ	V	—
Output Low Voltage, V_{OL}	0.4 max	0.4 max	V	—
Output Coding	2's complement	2's complement	—	—

Note: The A/D has been modified so that all single-ended inputs (such as AI3 in Table 104) are actually treated internally as if they were differential, with the negative side automatically connected to V_{REF} as was done for the AI1P/N tests above. The higher performance reported when AI1P/N inputs are used should therefore be realized for all inputs.

7 Electrical Requirements and Characteristics (continued)

7.3 Analog Interface (continued)

7.3.2 A-to-D Inputs (continued)

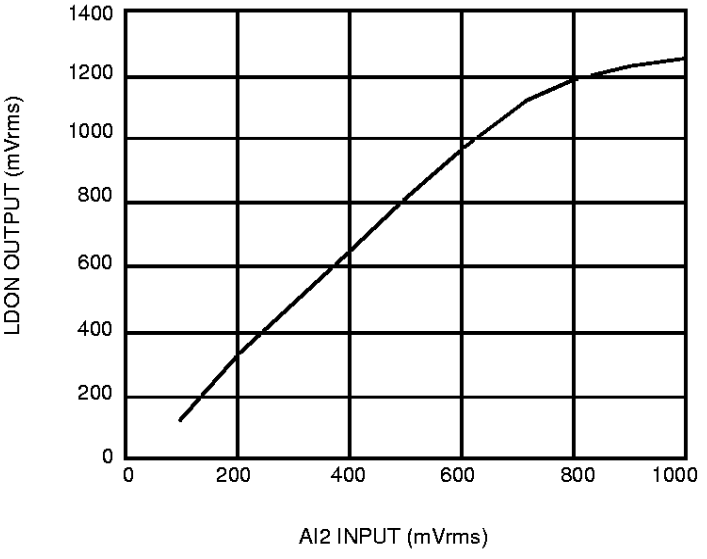

Figure 18. Overload Compression (5 V Supply)

7.3.3 Speaker Driver

The speaker driver is a differential drive requiring no dc blocking capacitor for driving a speaker between the two output terminals. It can drive 8 Ω or larger impedance speakers when in high-voltage mode. The gain controls are shown in Table 105.

Table 105. Speaker Gain Control

SPKG[2:0]	Gain
111	14 dB
110	10 dB
101	6 dB
100	2 dB
011	–2 dB
010	–6 dB
001	–10 dB
000	Silent
Gain Error	±1 dB

An internal digital signal of 0.8 * (2^{15} – 1) * sin(2π1000t) should translate to a differential output signal of approximately 2 * 0.8 * V_{REF} * sin(2π1000t) for the 6 dB gain control setting.

A separate control bit, SPKEN, turns the speaker power off. Separate V_{DDS} and V_{SSS} pins provide power for the speaker driver. The speaker driver specifications are shown in Table 106.

7 Electrical Requirements and Characteristics (continued)

7.3 Analog Interface (continued)

7.3.3 Speaker Driver (continued)

Table 106. Speaker Driver Specifications

Parameter	CFIVOLT = 1 (High Volt.)			CFIVOLT = 0 (Low Volt.)			Unit
	Min	Typ	Max	Min	Typ	Max	
Speaker Impedance	8	—	—	150	—	—	Ω
Total Harmonic Distortion— Differential Output							
5 V Peak-to-peak into 8 Ω	—	—	2	—	—	—	%
0.5 V Peak-to-peak into 150 Ω	—	—	—	—	—	2	%
Gain Accuracy	–1.5	—	1.5	–1.5	—	1.5	dB
Common-mode Voltage	—	2.1	—	—	1.6	—	V
Power Supply Rejection Ratio	30	38	—	30	38	—	dB
Single-ended Output Distortion ac Coupled, High Impedance	—	—	5	—	—	5	%

Table 107. Speaker Driver Electrical Characteristics (T_A = 25 °C)

Parameter	CFIVOLT = 1 Value	CFIVOLT = 0 Value	Unit
Output Impedance	1.2	no data	Ω
THD Differential Output:			
5 Vp-p into 8 Ω	2% maximum	—	—
0.5 Vp-p into 150 Ω	—	2% maximum	—
THD Single-ended Output ac Coupled, High Impedance	2.5% maximum	2.5% maximum	—
Gain Accuracy:			
No load	±1	±1	dB
Load = 8 Ω	–2.5/–0.5	—	dB
Load = 150 Ω	—	±1	dB
Common-mode Voltage	2.1	1.6	V
Common-mode Offset between Differential Outputs	<50	<50	mV
PSRR (differential single-ended):			
Gain = Maximum 1 kHz	51/46	no data	dB
Gain = Maximum 10 kHz	33/24	—	dB

7 Electrical Requirements and Characteristics (continued)

7.3 Analog Interface (continued)

7.3.3 Speaker Driver (continued)

Figure 19 shows the functional view of the D/A converter and the speaker driver. The D/A converter is a resistive string converter and consists of a 2**13 resistor string. The output register **spkr** presents a digital word coded in two's complement to the DAC for conversion. The conversion logic selects taps on the resistor string representing the digital word. The differential outputs of the DAC are then sampled and held by the line driver by closing and opening the switches SAMPLEP and SAMPLEN. The sampling frequency can be 16 kHz or 32 kHz depending on the selected mode. The analog values are stored on 5 pF sampling capacitors and are unity-gain buffered and level-shifted before getting gained up by the programmable gain amplifier section. The speaker gain (silent to 14 dB) is selected by setting the **cdcpg** register. The gain decode logic then closes the corresponding switches in the feed-forward and feedback paths to set the proper resistor ratio for gain. The differential speaker outputs, SPKP and SPKN, are capable of driving an 8 Ω load in the 5 V mode and 150 Ω in the 3 V mode.

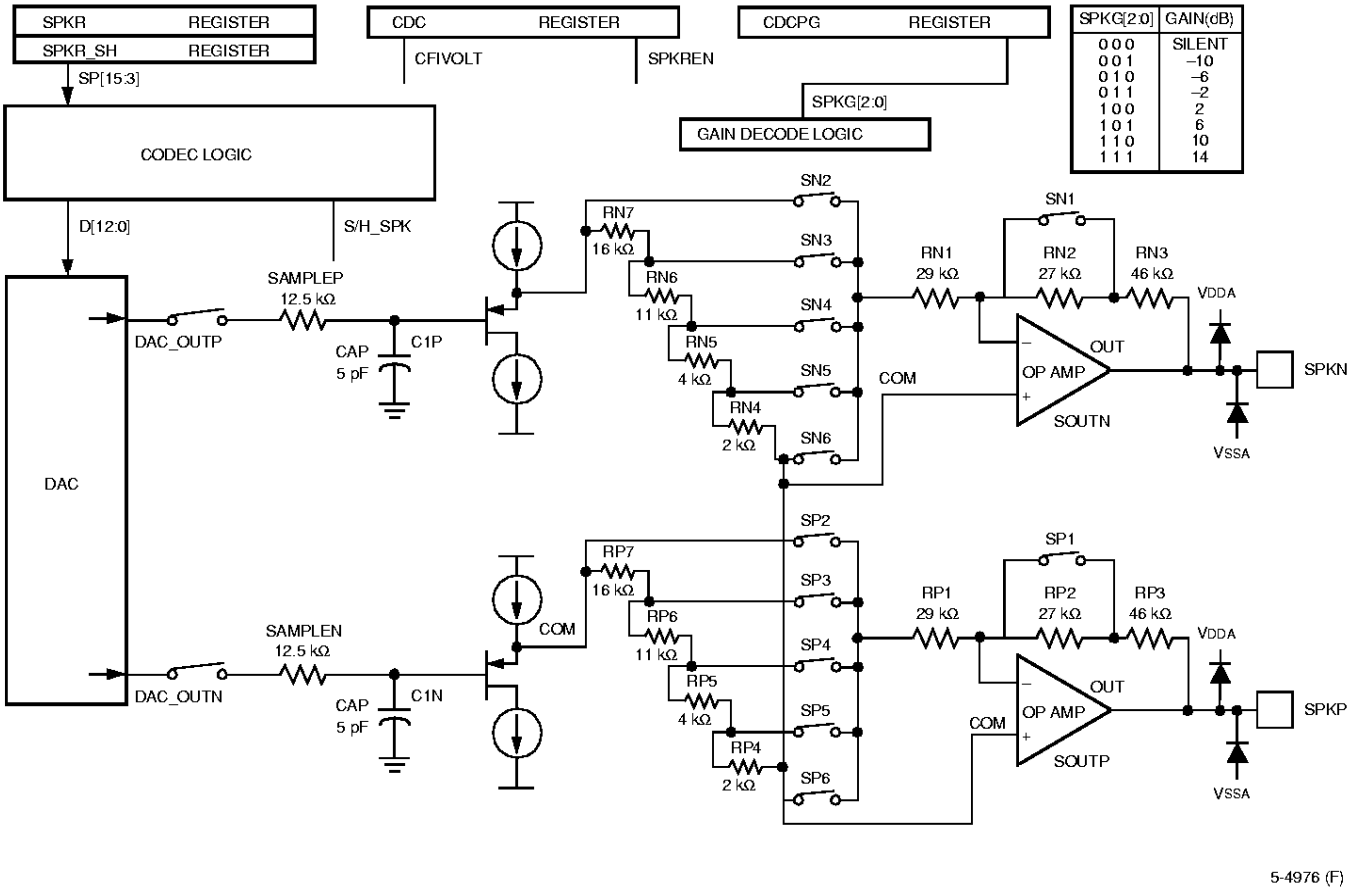

Figure 19. Speaker Driver Functional Block Diagram

7 Electrical Requirements and Characteristics (continued)

7.3 Analog Interface (continued)

7.3.4 Line Driver

The line driver differentially drives a 1200 Ω to 600 Ω transformer with direct coupling. Driving a 600 Ω to 600 Ω transformer single-ended to ground requires a dc blocking capacitor. A reconstruction filter may be needed to smooth the steps of the 16 kilosample conversion rate to prevent unwanted out-of-band tones. Table 108 shows the line driver specifications.

Table 108. Line Driver Specifications

Parameter	CFIVOLT = 1 (High Volt.)			CFIVOLT = 0 (Low Volt.)			Unit
	Min	Typ	Max	Min	Typ	Max	
Output Load	600	—	—	600	—	—	Ω
Gain Accuracy	–1.5	—	1.5	–1.5	—	1.5	dB
Gain	—	12	—	—	12	—	dB
Common-mode Voltage	—	2.4	—	0.7	0.85	1.0	V
Differential Output:	—	—	2	—	—	3	%
Distortion	7 Vp-p into 1200 Ω			3 Vp-p into 1200 Ω			—
Single-ended ac Coupled 600 Ω Impedance:	—			—			—
PSRR	30	38	—	25	33	—	dB
Distortion	—	—	3	—	—	5	%

An internal digital signal of 0.8 * ($2^{15} - 1$) * sin(2π1000t) should provide a differential output swing of approximately sqrt(2) * 2 * 0.8 * V_{REF} * sin(2π1000t).

Figure 20 shows the functional view of the D/A converter and the line driver. The D/A converter is a resistive string converter and consists of a 2**13 resistor string. The output register line1 presents a digital word coded in two's complement to the DAC for conversion. The conversion logic selects taps on the resistor string representing the digital word. The differential outputs of the DAC are then sampled and held by the line driver by closing and opening the switches SAMPLEP and SAMPLEN. The sampling frequency can be 16 kHz or 32 kHz, depending on the selected mode. The analog values are stored on 5 pF sampling capacitors before getting gained up by 12 dB at the outputs, LDOP and LDON (LDOP2 and LDON2). The differential outputs drive a 600 Ω transformer with a low-pass section (see Figure 24 on page 101) to remove out-of-band noise.

7 Electrical Requirements and Characteristics (continued)

7.3 Analog Interface (continued)

7.3.4 Line Driver (continued)

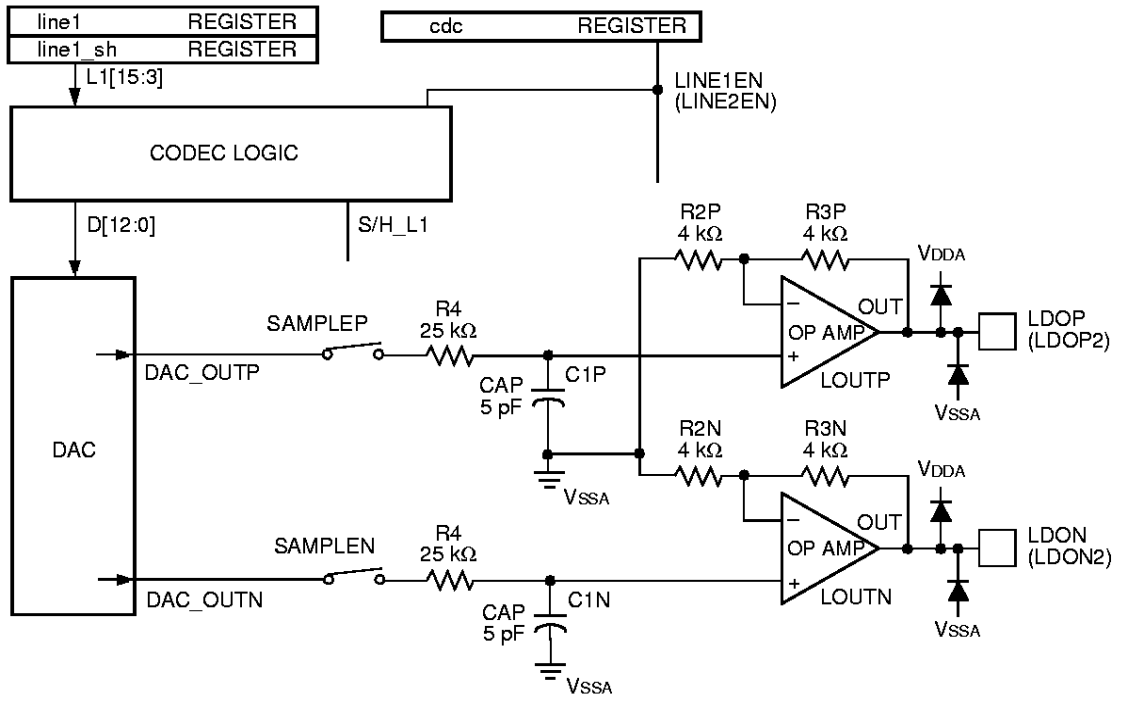

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Figure 20. Line Drivers Functional Block Diagram

Table 109. Line Driver (Analog Test Mode, No A/D/A) Electrical Characteristics (T_A = 25 °C)

Parameter	CFIVOLT = 1 Value	CFIVOLT = 0 Value	Unit
Output Load	1200	1200	Ω
Output Impedance	100	100	Ω
Gain: Open Circuit Load 1200 Ω Load	 4.7 4.0	 not directly testable (test mode is 5 V only)	 dB dB
Common-mode Voltage	2	1	V
Distortion, at Maximum D/A Drive: Differential Output Single-ended Output	 0.04% (6.4 Vp-p out) 1.0%	 not directly testable	 — —
Signal to Noise Ratio, at Maximum D/A Drive: Differential Output Single-ended Output	 85 82	 not directly testable	 dB dB

7 Electrical Requirements and Characteristics (continued)

7.3 Analog Interface (continued)

7.3.5 Programmable Gain Amplifiers

The two independent programmable gain amplifiers provides 2 dB gain steps from 0 dB to 28 dB, as shown in Table 110.

Table 110. Programmable Gain Amplifier Control

PGA[3:0]	Gain
1111	28 dB
1110	26 dB
1101	24 dB
1100	22 dB
1011	20 dB
1010	18 dB
1001	16 dB
1000	14 dB
0111	12 dB
0110	10 dB
0101	8 dB
0100	6 dB
0011	4 dB
0010	2 dB
0001	0 dB
0000	Off (no power)
Gain Error	±1 dB

Table 111. Programmable Gain Amplifier Specifications

Parameter	CFIVOLT = 1 (High Volt.)			CFIVOLT = 0 (Low Volt.)			Unit
	Min	Typ	Max	Min	Typ	Max	
Output Load	10000	—	—	10000	—	—	Ω
Gain Accuracy	–1.5	—	1.5	–1.5	—	1.5	dB
Common-mode Voltage	1.7	2.0	2.3	0.85	1.0	1.15	V
PSRR:							
28 dB Gain	30	—	—	25	—	—	dB
10 dB Gain	47	—	—	42	—	—	dB
0 dB Gain	56	—	—	51	—	—	dB
SNR at Max Signal Output:							
28 dB Gain	55	—	—	50	—	—	dB
0 dB Gain	75	—	—	70	—	—	dB
Output Distribution—ac Coupled 10 kΩ Impedance	—	—	3	—	—	5	%

Note: PGIN is the input and PGOUT is the output for programmable gain amplifier 1. PGIN2 and PGOUT2 are the input and output of programmable gain amplifier 2. The output of the programmable gain amplifier can be connected to one of the AI2, AI3, AI4, AI6, or AI7 inputs through a suitable antialias filter.

7 Electrical Requirements and Characteristics (continued)

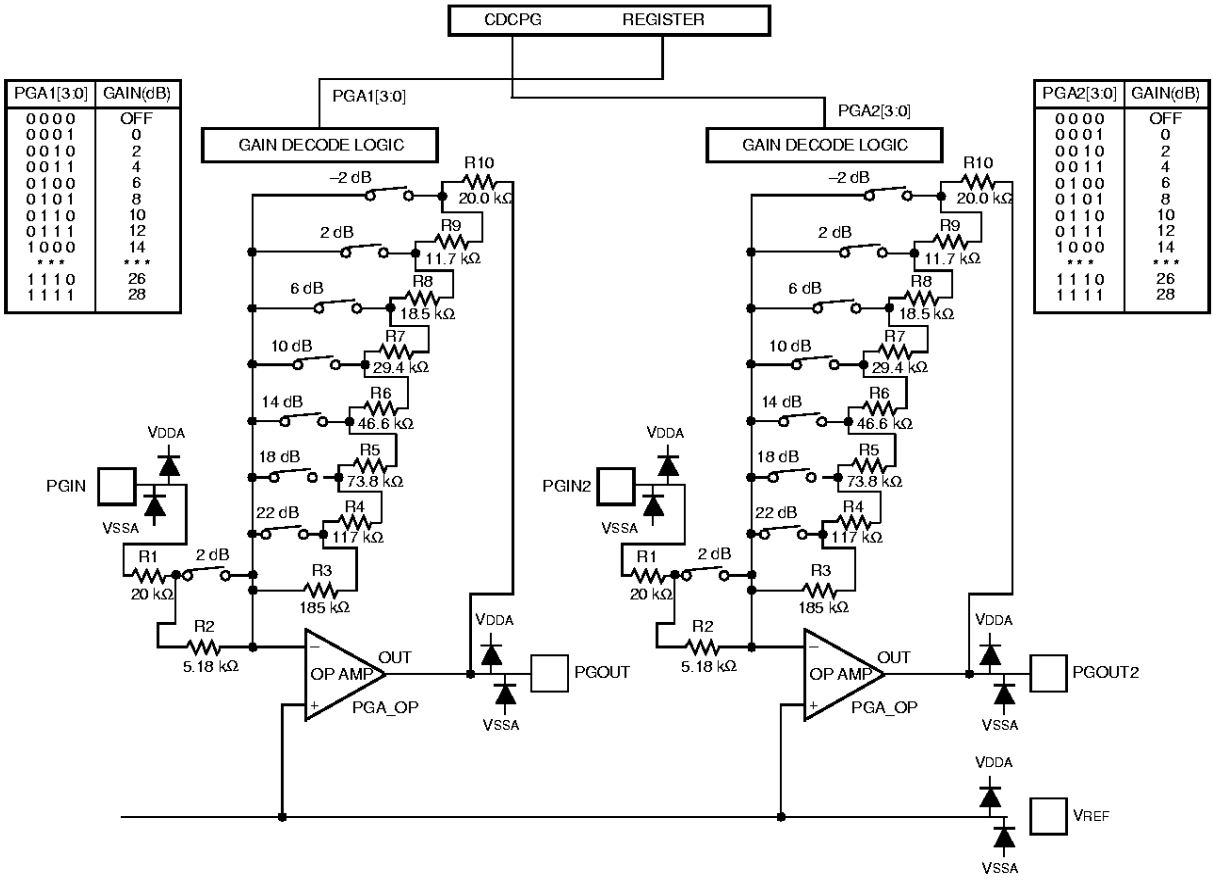
7.3 Analog Interface (continued)

7.3.5 Programmable Gain Amplifiers (continued)

Figure 21 shows the functional block diagram for the programmable gain amplifiers PGA1 and PGA2. These are inverting amplifiers with VREF as the reference voltage at the positive terminal. The programmable gain is achieved by switching in different resistors in the feedforward and feedback paths. A programmable gain setting from 0 dB to 28 dB is selected by setting the **cdcpg** register. The gain decode logic then closes the corresponding switches to provide the proper resistor ratio for gain. The closed-loop frequency response is shown in Table 112.

Table 112. Closed-Loop Frequency Response

Gain	–3 dB Frequency (Small Signal) Measured in the 5 V Mode, Loaded by the Antialias Filter
0 dB	≈ 5.5 MHz
14 dB	≈ 750 kHz
28 dB	≈ 170 kHz



5-4980 (F)

Figure 21. Programmable Gain Amplifiers Functional Block Diagram

7 Electrical Requirements and Characteristics (continued)

7.3 Analog Interface (continued)

7.3.5 Programmable Gain Amplifier (continued)

Table 113. Programmable Gain Amplifier Electrical Characteristics (T_A = 25 °C)

Parameter	CFIVOLT = 1 Value	CFIVOLT = 0 Value	Unit
Output Load	10,000	10,000	Ω
Gain Accuracy	±0.2	±0.2	dB
Common-mode Voltage	V_{REF}	V_{REF}	—
THD at Maximum Usable A/D Drive:			
28 dB Gain	1.0%	1.6%	—
0 dB Gain	1.8%	1.2%	—
PSRR at 1 kHz:			
28 dB Gain	50	52	dB
10 dB Gain	64	63	dB
0 dB Gain	68	70	dB
PSRR at 8 kHz:			
28 dB Gain	38	34	dB
10 dB Gain	49	49	dB
0 dB Gain	51	53	dB
Signal to Noise Ratio at 3% THD Output:			
28 dB Gain	72	64	dB
0 dB Gain	93	98	dB
Signal to Noise Ratio at Maximum Usable Drive to A/D:			
28 dB Gain	67	60	dB
0 dB Gain	89	83	dB

7 Electrical Requirements and Characteristics (continued)

7.3 Analog Interface (continued)

7.3.6 Microphone Power Supply and Amplifier

This input amplifier provides 16 dB of gain to the ac signal from the microphone. The microphone power supply provides a 4 V dc bias supply for the microphone. The 2-pin amplifier interface, MAP and MAN, connect through off-chip capacitors to an electronic microphone. Connecting a 0.33 µF capacitor from FCAP to V_{SSA} and an 800 Ω to 2200 Ω resistor from FCAP to the microphone positive terminal provides dc bias for the microphone. The input amplifier output is attached to an additional programmable gain amplifier providing overall gain settings from 16 dB to 44 dB in 2 dB steps. The output of the programmable gain amplifier can be connected to one of the AI2, AI3, AI4, AI6, or AI7 inputs through a suitable antialias filter.

Table 114. Microphone Gain Control (Includes Associated Programmable Gain Amplifier)

PGMO[3:0]	Gain
1111	44 dB
1110	42 dB
1101	40 dB
1100	38 dB
1011	36 dB
1010	34 dB
1001	32 dB
1000	30 dB
0111	28 dB
0110	26 dB
0101	24 dB
0100	22 dB
0011	20 dB
0010	18 dB
0001	16 dB
0000	Off (no power)
Gain Error	±1 dB

Table 115. Microphone Preamp and Power Supply Specifications

Parameter	CFIVOLT = 1 (High Volt.)			CFIVOLT = 0 (Low Volt.)			Unit
	Min	Typ	Max	Min	Typ	Max	
ac Input Impedance	—	20	—	—	20	—	kΩ
dc Bias Impedance	—	—	20	—	—	100	Ω
dc Output Bias with 1 MΩ Load	3.6	4.0	4.2	—	V_{DD}	—	V
Input Signal Level (differential)	—	10	50	—	10	50	mVp-p
Input Refered Noise: Below 15 mVp-p Over 3 kHz	 — —	 — —	 48.5[1] 56.3	 — —	 — —	 48[1] 56	 dB µVp-p
Signal to Dist. 15 mVp-p/1000 Hz Input Level	—	—	39	—	—	39	dB

1. The design goal is 54 dB below 15 mVp-p.

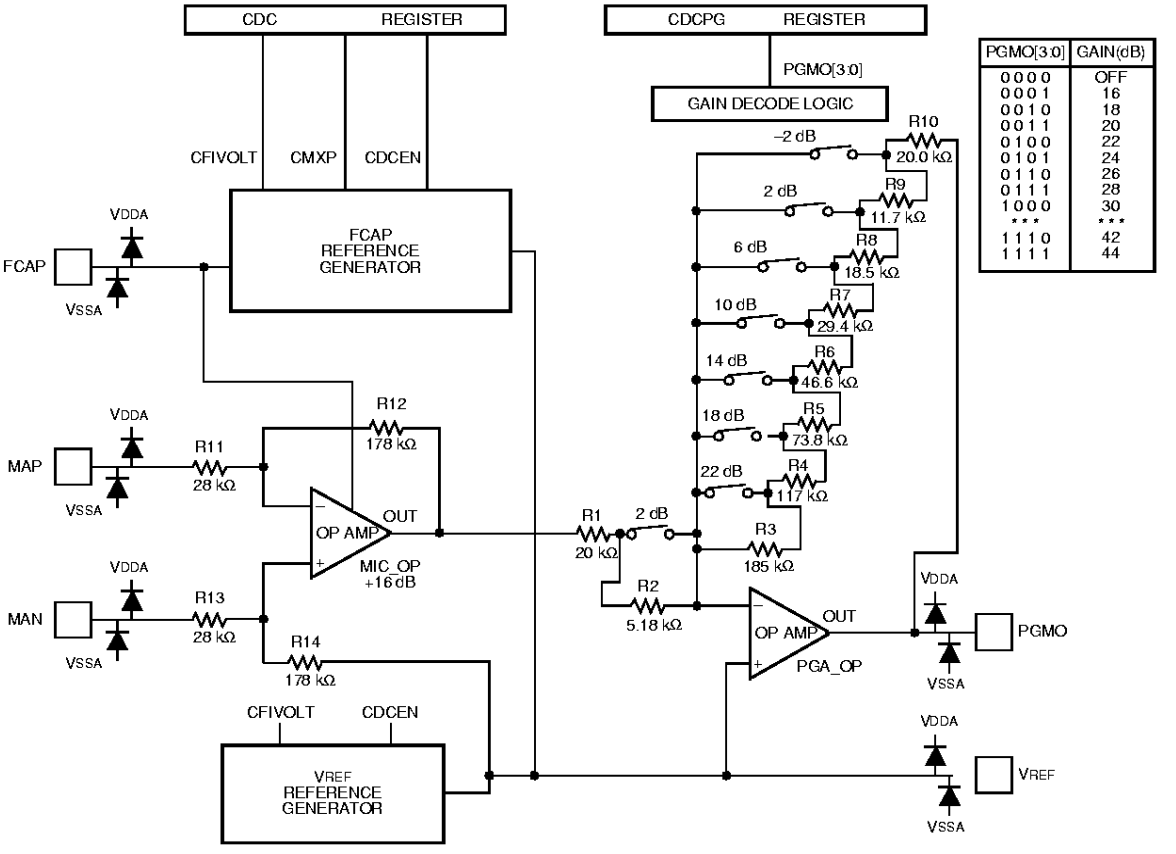
7 Electrical Requirements and Characteristics (continued)

7.3 Analog Interface (continued)

7.3.6 Microphone Power Supply and Amplifier (continued)

Table 116. Microphone Preamp Electrical Characteristics (T_A = 25 °C)

Parameter Dynamic Performance	CFIVOLT = 1 Value	CFIVOLT = 0 Value	Unit	Test Conditions/ Comments
dc Bias Impedance	42	no data	Ω	—
dc Output Bias with 1 MΩ Load	3.7	V_{DD}	V	—
Max Input Signal Level	50 mVp-p (yields 1.3% THD)	50 mVp-p (yields 1.3% THD)	—	—
Input Referred Noise: 300 Hz—4 kHz FLAT	6	8.4	µVrms	—
THD (15 mVp-p, 1 kHz Input) Level:				
PGMO Gain = 44 dB	1.3%	<0.9%	—	—
PGMO Gain = 30 dB	0.94%	<0.9%	—	—
PGMO Gain = 16 dB	0.18%	<0.9%	—	—
PSRR at Max Gain (44 dB)	50	46	dB	—
Differential Input Voltage Range for Max A/D Drive	0—12.6 0—316	0—6.3 0—158	mVp-p mVp-p	@ max gain 44 dB @ min gain 16 dB



5-4982 (F)

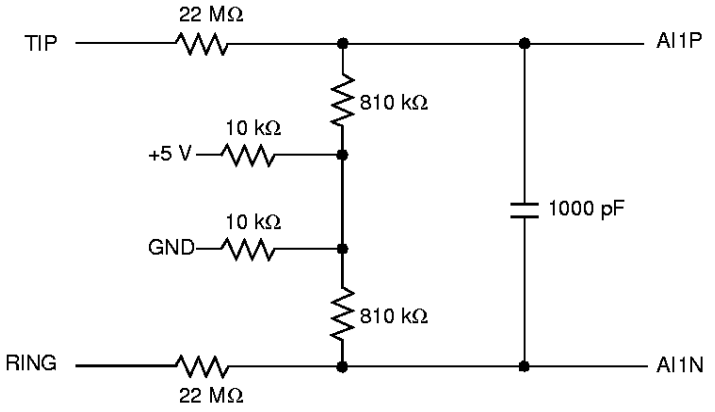
Figure 22. Microphone Power Supply and Amplifier Functional Block Diagram

7 Electrical Requirements and Characteristics (continued)

7.3 Analog Interface (continued)

7.3.7 Reference Designs

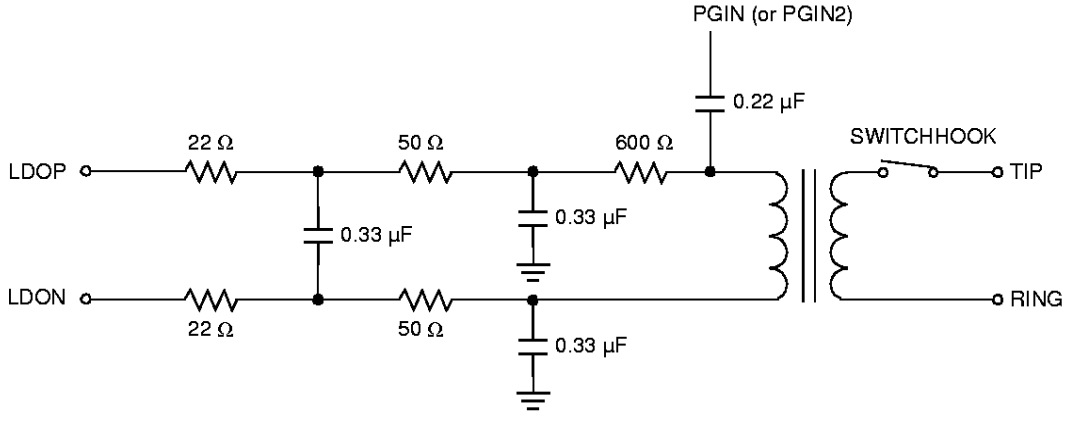
The ring detection/parallel set detection can be performed by the DSP165X with a software routine. The TIP/RING signal could be sensed at the analog differential inputs, AI1P and AI1N, with a low-pass section as shown in Figure 23. This filter provides about a 25:1 attenuation ratio and 3 dB corner frequency at about 1 kHz. Upon detection, the software could use an IOP to control the switchhook relay.



5-4981 (F)

Figure 23. Ring Detection/Parallel Set Detection

A line transmit filter can be configured with external components as shown in Figure 24. The filter presents a 600 Ω matching load impedance to the transformer and a 13 dB line attenuation at 16 kHz. If the sampling frequency is 8 kHz, the filter should be reconfigured to have a lower corner frequency. The TIP/RING receive signal is ac coupled into PGIN (or PGIN2) with an external 0.22 µF capacitor.



5-4983 (F)

Figure 24. Line Interface/Smoothing Filter

7 Electrical Requirements and Characteristics (continued)

7.3 Analog Interface (continued)

7.3.8 System Characteristics

Transmit Path

The transmit path is defined as microphone input to line driver output. For the following tests, no antialiasing nor output smoothing filters were used, PGMO gain = 30 dB, and the input was applied differentially between MAP and MAN. For the intermodulation distortion test, the signals were 2.33 kHz and 500 Hz of equal amplitude, appearing as 1 Vp-p each at the output. For the gain tracking test, the input amplitude was 20 mVrms, which appeared at AI2 as 2 Vp-p, and at LDOP/N as 6 Vp-p.

Table 117. System Characteristics Transmit Path, Electrical Characteristics (T_A = 25 °C)

Parameter	CFIVOLT = 1 Value	CFIVOLT = 0 Value	Unit
Intermodulation Distortion (IMD):			
Spurious Free Range	38	48	dB
Total IMD	1.3%	0.5%	—
Gain Relative to Gain at 1 kHz (with zero order hold correction)	±0.1	±0.1	dB
PSRR, Differential PGMO Gain:			
Min = 0—4 kHz	33	—	dB
Min = 0—50 kHz	31	—	dB
Max = 0—4 kHz	22	—	dB
Max = 0—50 kHz	20	—	dB
PSRR, Single-ended PGMO Gain:			
Min = 0—4 kHz	30	—	dB
Min = 0—50 kHz	25	—	dB
Max = 0—4 kHz	26	—	dB
Max = 0—50 kHz	22	—	dB

Receive Path

The receive path is defined as programmable gain amplifier input to speaker output. For the following tests, the PGA and speaker amplifier gains were maximum. Antialiasing was applied between the PGA and the A/D input (AI2).

For the intermodulation distortion test, the input signals were:

(a) CFIVOLT = 1 2.33 kHz and 500 Hz at 25 mVp-p at the output.

(a) CFIVOLT = 0 2.33 kHz and 500 Hz at 12.5 mVp-p each, appearing as 1 Vp-p at the output.

For the gain tracking test, the input amplitudes were 50 mVp-p (CFIVOLT = 1) and 25 mVp-p (CFIVOLT = 0).

Table 118. System Characteristics Receive Path, Electrical Characteristics (T_A = 25 °C)

Parameter	CFIVOLT = 1 Value	CFIVOLT = 0 Value	Unit
Intermodulation Distortion (IMD):			
Spurious Free Range	46	55	dB
Total IMD	1.2%	0.6%	—
Gain Relative to Gain at 1 kHz (with zero order hold correction)	±0.1	±0.1	dB

8 Timing Requirements and Characteristics

Requirements are restrictions on the external device connected to the *FlashDSP*1650. Characteristics are properties of the *FlashDSP*1650. For details, see Section 6, Device Requirements and Characteristics, and Section 7, Electrical Requirements and Characteristics.

The characteristics listed are valid under the following conditions:

- V_{SS} = 0 V, V_{DD} = 5.0 V ± 0.5 V, T_A = 0 °C to 70 °C, C_{LOAD} = 50 pF, T_{MIN} = 25 ns
- V_{SS} = 0 V, V_{DD} = 3.3 V ± 0.3 V, T_A = –40 °C to +85 °C, C_{LOAD} = 50 pF, T_{MIN} = 31.25 ns

Output characteristics can be derated as a function of load capacitance (C_L):

- For all rising edge outputs, $dt/dC_L \leq 0.06$ ns/pF for $0 \leq C_L \leq 100$ pF at 2.0 V
- For all falling edge outputs, $dt/dC_L \leq 0.05$ ns/pF for $0 \leq C_L \leq 100$ pF at 0.8 V

For example, the derating for a time delay that includes a rising edge with an external load of 20 pF is as follows:

$$\Delta t = (C_L - C_{LOAD})\ dt/dC_L = (20 - 50)\ 0.06 = -1.8 \text{ ns}$$

Output characteristics assume standard slew rate buffers. See Table 46 on page 63 for information on mask options; for slow buffers option, all the output times should be increased by the additional time given by the equation:

$$\Delta t = 0.4 \bullet CL$$

Where CL is the load capacitance in picofarads, and Δt is the additional output delay in nanoseconds. For example, for load capacitance of 50 pF, with slow buffers option, all output timing characteristics should be increased by 20 ns.

Table 119. Test Conditions

Test Conditions for Inputs	Test Conditions for Outputs
Rise and fall times of 4 ns or less.	C_{LOAD} = 50 pF.
Timing reference levels for delays = V_{IH}, V_{IL}.	Timing reference levels for delays = V_{OH}, V_{OL}. 3-state delays are measured to the high-impedance state of the output driver.

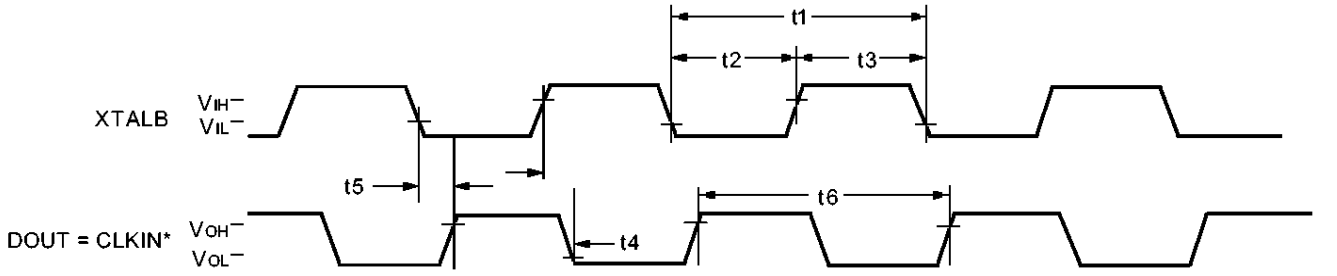
For definitions of the V_{IH}, V_{IL}, V_{OH}, and V_{OL} labels, see Table 96 on page 81. In this section's timing diagrams, these labels distinguish inputs and outputs.

8.1 Input Clock Options

The input clocks to the *FlashDSP*1650 allow for the use of either CMOS level input signals or an internal crystal oscillator with an external crystal. This allows the user to select either both clock inputs to use the internal crystal oscillator or XTALB may be driven with a CMOS level signal. In the latter case, the OSCBYP pin should be pulled high externally, while XTALA will be internally pulled low.

8 Timing Requirements and Characteristics (continued)

8.2 DSP Clock Generation



* Input clock; the DOUT pin may be selected to be the input clock, see the **clkc** register.

Figure 25. I/O Clock Timing Diagram

Note: For Tables 120 to 150, TMIN is the minimum instruction cycle time (see Section 8.1 on page 103).

Table 120. Timing Requirements for Input Clock

Ref	Parameter	VDD = 4.5 V to 5.5 V		VDD = 3.0 V to 3.6 V		Unit
		TMIN = 25 ns		TMIN = 31.25 ns		
		Min	Max	Min	Max	
t1*	Clock In Period (low to low)	25	—†	31.25	—†	ns
t2	Clock In Low Time (low to high)	11	—	14	—	ns
t3	Clock In High Time (high to low)	11	—	14	—	ns

* The clock input frequency should normally be set to 4.096 MHz for proper PLL and codec operation.
† Device is fully static; t1 is tested at 125 ns, and memory hold time is tested at 0.1 s.

Table 121. Timing Requirements for Input Clock and Output Clock

Ref	Parameter	VDD = 4.5 V to 5.5 V		VDD = 3.0 V to 3.6 V		Unit
		TMIN = 25 ns		TMIN = 31.25 ns		
		Min	Max	Min	Max	
t4	Clock Out High Delay (high to high)	—	21	—	25	ns
t5	Clock Out Low Delay (low to low)	—	21	—	25	ns
t6	Clock Out Period (high to low)	25	—	31.25	—	ns

8 Timing Requirements and Characteristics (continued)

8.3 Powerup Reset (Assuming VDDPLM Is Disabled)

The *FlashDSP*1650 has a powerup reset circuit that automatically clears the JTAG controller upon powerup. If the supply voltage falls below the VDD minimum value, a reset is required—the JTAG controller must be reset with another powerup reset, followed by the usual RSTB and XTALB reset sequence (see the Warning in Section 7.2). Figure 26 shows two separate events: an initial powerup and a powerup following a drop in the power supply.

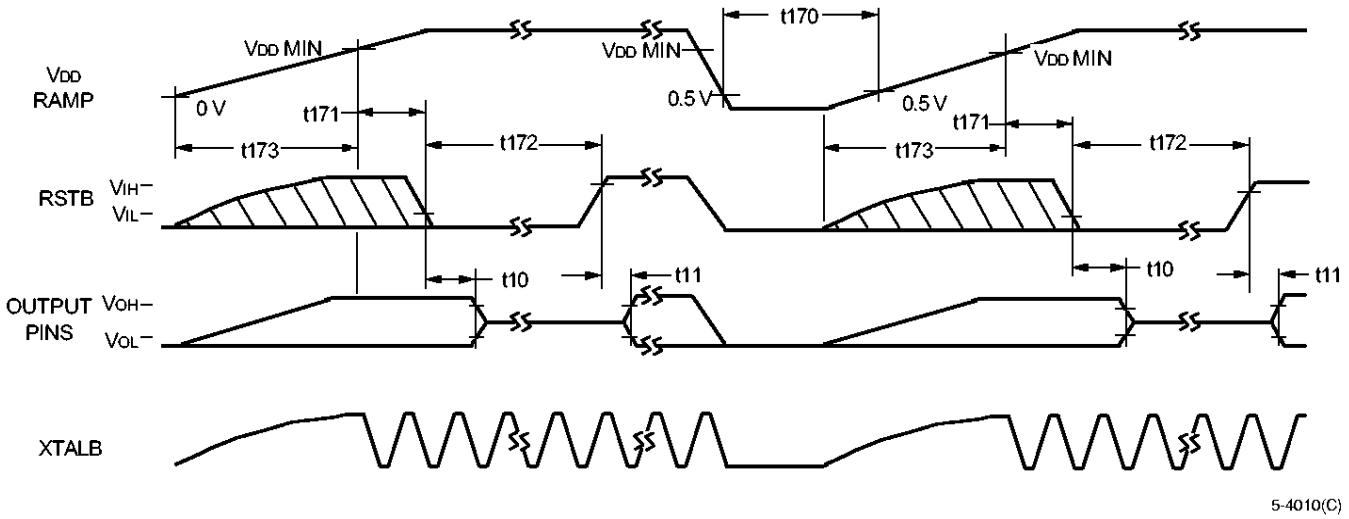


Figure 26. Powerup Reset and Device Reset Timing Diagram

Note: In Table 122, T = the period of CLKFREE which on powerup is the period CLKIN • 2.

Table 122. Timing Requirements for Powerup Reset and Device Reset

Ref	Parameter	VDD = 4.5 V to 5.5 V, TMIN = 25 ns		VDD = 3.0 V to 3.6 V, TMIN = 31.25 ns		Unit
		Min	Max	Min	Max	
t172	Reset Pulse (low to high)	6T	—	6T	—	ns
t173	VDD Ramp	—	40	—	40	ms
t170	VDD Low*	3	—	3	—	s
t171	VDD MIN to RSTB Low (with input clock driven externally)	0	—	0	—	ms
t171	VDD MIN to RSTB Low (with crystal oscillator input clock option†)	120	—	120	—	ms

* Time below 0.5 V required to activate the internal powerup reset circuit that resets the JTAG controller. Following a reset of the JTAG controller, the device must also be reset with the usual RSTB and XTALB sequence.
† With external components as specified in Section 9.

8 Timing Requirements and Characteristics (continued)

8.3 Powerup Reset (Assuming V_{DDPLM} Is Disabled) (continued)

Table 123. Timing Characteristics for Powerup Reset and Device Reset

Ref	Parameter	V_{DD} = 4.5 V to 5.5 V		V_{DD} = 3.0 V to 3.6 V		Unit
		T_{MIN} = 25 ns		T_{MIN} = 31.25 ns		
		Min	Max	Min	Max	
t10	RSTB Disable Time (low to 3-state)	—	100	—	100	ns
t11	RSTB Enable Time (high to valid)	—	100	—	100	ns

WARNING: The device needs to be clocked for at least twelve f_{XTALB} cycles during reset after powerup; otherwise, high current may flow.

8.4 Reset Synchronization

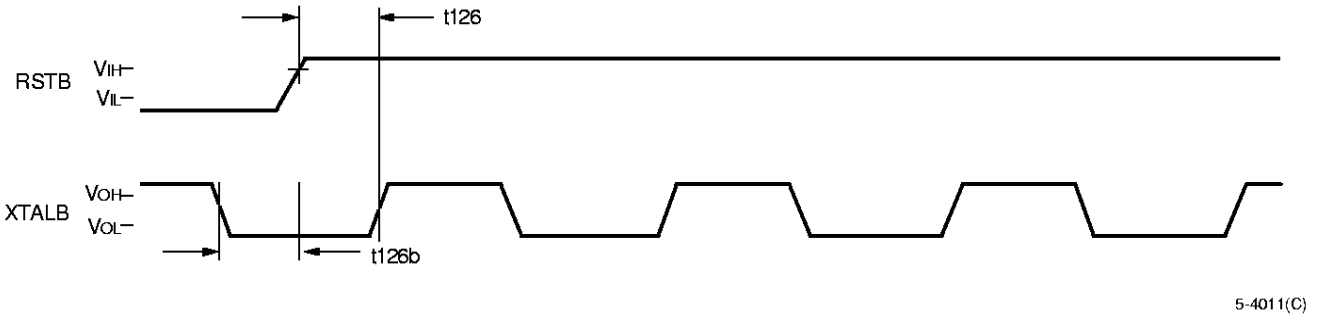


Figure 27. Reset Synchronization Timing

Table 124. Timing Requirements and Characteristics for Reset Synchronization Timing

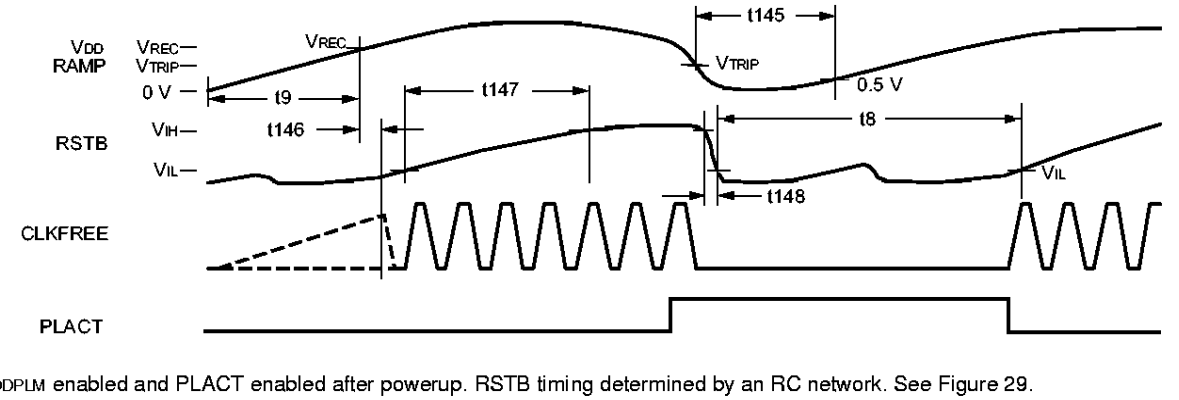
Ref	Parameter	V_{DD} = 4.5 V to 5.5 V				V_{DD} = 3.0 V to 3.6 V		Unit
		T_{MIN} = 25 ns		T_{MIN} = 30 ns		T_{MIN} = 31.25 ns		
		Min	Max	Min	Max	Min	Max	
t126	Reset Setup (high to high)	50	—	50	—	10	—	ns
t126b	Clock Low to Reset High	50	—	50	—	50	—	ns

8 Timing Requirements and Characteristics (continued)

8.5 Powerup and Power-Loss Detect Circuit Reset

The *FlashDSP*1650 has an alternate powerup reset and power-loss detect circuit that automatically clears the JTAG and DRAM controllers, the DSP1600 core, and the remaining internal peripherals. This circuit functions properly with fast power supply ramps and quick power supply drops and recoveries. A powerup reset is considered the condition that the DSP power supply ramps from 0 V to its operating voltage. A power-loss detect reset is considered the condition in which the DSP is operating at a proper voltage and then DSP power supply drops below maximum VTRIP (see Table 127). The DSP stays in full-device reset until the DSP power supply rises above the VREC point. An output pin, PLACT, signals when the DSP has detected a power-loss condition on the DSP power lines. RSTB is also pulled low by the *FlashDSP*1650 for the duration of the power-loss condition. Figure 29 shows an RC network configuration that fulfills all the necessary RSTB timing requirements.

8.5.1 Powerup Reset Specifications (VDDPLM Connected to VDD)



Note: VDDPLM enabled and PLACT enabled after powerup. RSTB timing determined by an RC network. See Figure 29.

Figure 28. Powerup Reset

Table 125. Timing Requirements for Powerup Reset with VDDPLM Enabled

Ref	Parameter	VDD = 4.5 V to 5.5 V		VDD = 3.0 V to 3.6 V		Unit
		TMIN = 25 ns		TMIN = 31.25 ns		
		Min	Max	Min	Max	
t8	Powerup Reset Pulse	120	—	120	—	ms
t9	VDD Ramp	500	—	500	—	µs
t145	VDD Low	200	—	200	—	µs

Table 126. Timing Characteristics for Powerup Reset with VDDPLM Enabled

Ref	Parameter	VDD = 4.5 V to 5.5 V		VDD = 3.0 V to 3.6 V		Unit
		TMIN = 25 ns		TMIN = 31.25 ns		
		Min	Max	Min	Max	
t146	VREC to RSTB High (internal)	0	20	0	20	ns
t147	RSTB Ramp (low to high)	—	500	—	500	ms
t148	RSTB Ramp (high to low)	—	500	—	500	µs

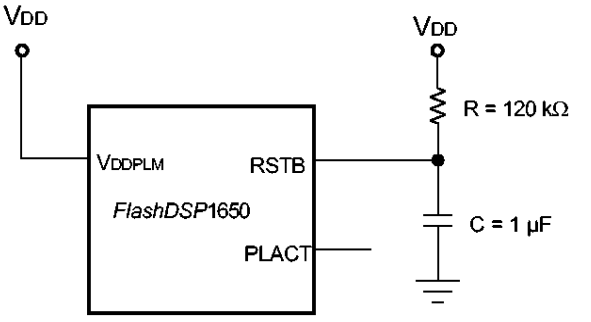
8 Timing Requirements and Characteristics (continued)

8.5 Powerup and Power-Loss Detect Circuit Reset (continued)

8.5.1 Powerup Reset Specifications (V_{DDPLM} Connected to V_{DD}) (continued)

Table 127. Power-Loss Detect Voltage Levels

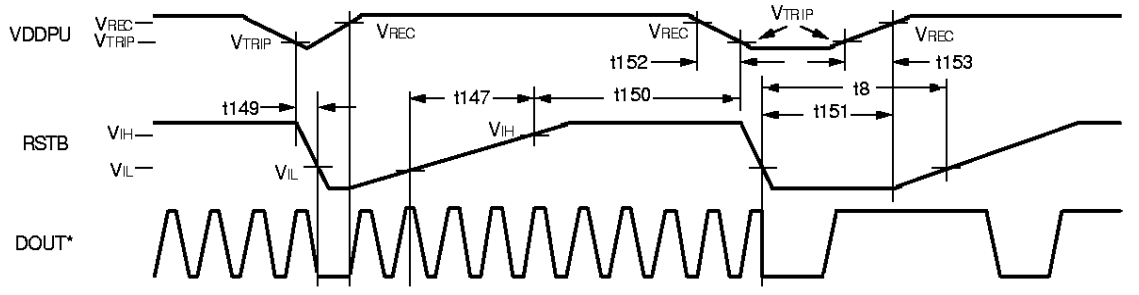
Settings	V_{TRIP}		V_{REC}		Hysteresis		Unit
	Min	Max	Min	Max	Min	Max	
PLC = 001	4.01	4.71	4.27	5.02	0.26	0.32	V
PLC = 01x	3.61	4.22	3.88	4.53	0.26	0.32	V
PLC = 100	2.86	3.33	3.04	3.54	0.18	0.21	V
PLC = 101	2.86	3.33	3.48	4.06	0.62	0.74	V
PLC = 110	2.43	2.81	2.62	3.03	0.18	0.22	V
PLC = 111	2.42	2.81	3.10	3.61	0.67	0.80	V



5-4013(C).b

Figure 29. Example of Power-Loss Detect External Component Configuration

8.5.2 Power-Loss Detect Specifications (V_{DDPLM} Connected to a Separate V_{DD})



* DOUT by default will be the internal ring oscillator during any reset condition. This clock will be turned off during power loss, provided the PLCKOFF bit is set in the **chipo** register; otherwise, it will continue to run.

Note: In Figure 30, V_{DDPLM} is enabled (connected to V_{DD} from a separate, independent supply). RSTB timing is determined by an RC network. See Figure 29.

5-4014(C)

Figure 30. Power-Loss Detect Reset

8 Timing Requirements and Characteristics (continued)

8.5 Powerup and Power-Loss Detect Circuit Reset (continued)

8.5.2 Power-Loss Detect Specifications (V_{DDPLM} Connected to V_{DD}) (continued)

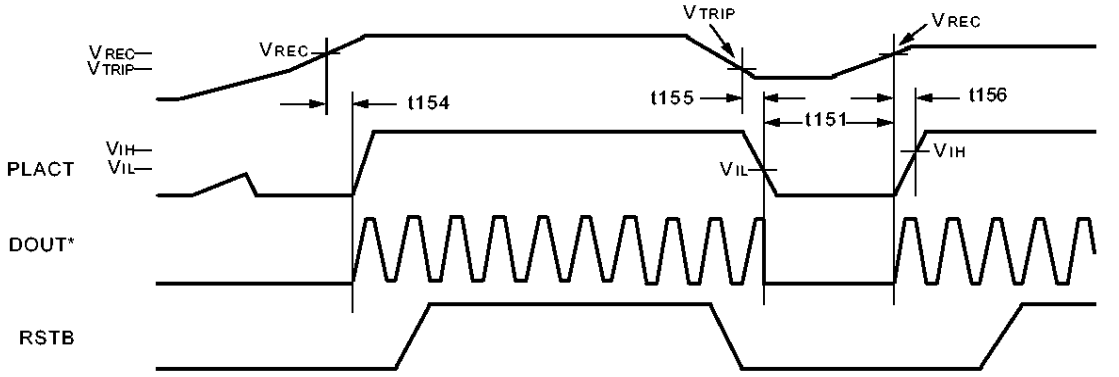
Table 128. Timing Requirements for Power-Loss Reset with V_{DDPLM} Enabled

Ref	Parameter	V_{DD} = 4.5 V to 5.5 V		V_{DD} = 3.0 V to 3.6 V		Unit
		T_{MIN} = 25 ns		T_{MIN} = 31.25 ns		
		Min	Max	Min	Max	
t8	Reset Pulse	120	—	120	—	ms
t150	RSTB High to V_{TRIP} Setup	0	—	0	—	ns
t151	RSTB Low to V_{REC} Setup	20	—	20	—	ns
t152	V_{DDPLM} Fall Rate	200	—	200	—	µs/V
t153	V_{DDPLM} Rise Rate	200	—	200	—	µs/V
t147	RSTB Ramp (low to high)	—	500	—	500	ms
t149	V_{TRIP} to RSTB (low)	2	25	2	25	ns

8 Timing Requirements and Characteristics (continued)

8.5 Powerup and Power-Loss Detect Circuit Reset (continued)

8.5.3 PLACT Pin Specifications



* DOUT is reset to the internal ring oscillator by any reset condition.

5-4015(C)

Figure 31. PLACT Functionality with V_{DDPLM} Enabled and PLCKOFF Bit Set in chipo Register

Table 129. Timing Characteristics for PLACT Response to Power-Loss Reset with V_{DDPLM} Enabled

Ref	Parameter	V_{DD} = 4.5 V to 5.5 V		V_{DD} = 3.0 V to 3.6 V		Unit
		T_{MIN} = 25 ns		T_{MIN} = 31.25 ns		
		Min	Max	Min	Max	
t151	PLACT High Duration	20	—	20	—	ns
t154	V_{REC} to DOUT Start	0	25	0	25	ns
t155	V_{TRIP} to PLACT (high)	2	25	2	25	ns
t156	V_{REC} to PLACT (low)	2	25	2	25	ns

8 Timing Requirements and Characteristics (continued)

8.6 JTAG I/O Specifications

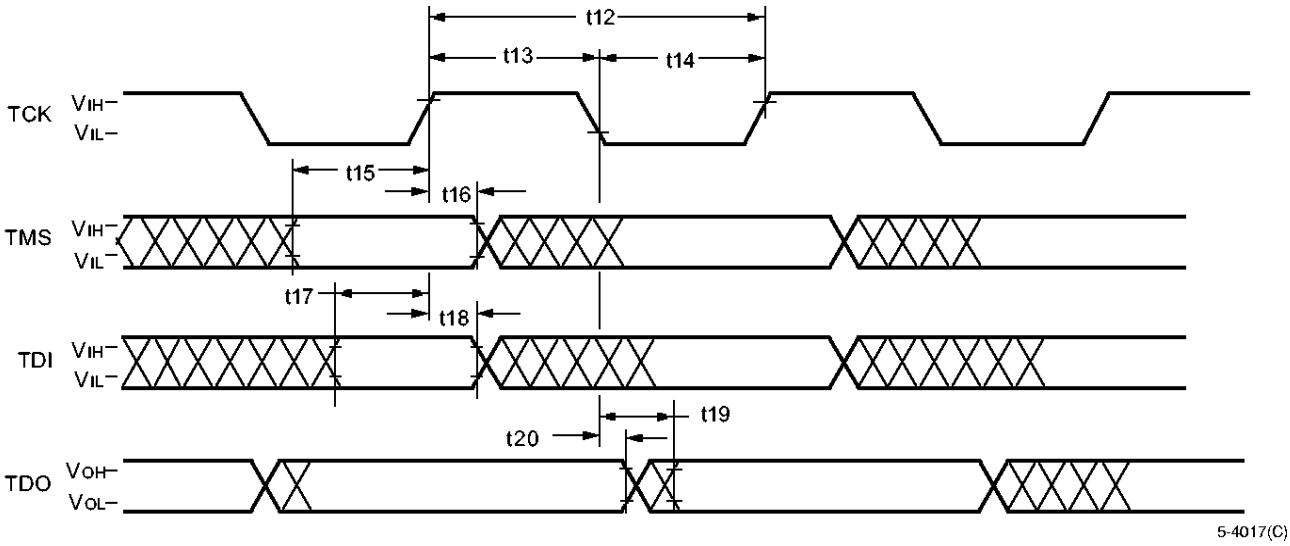


Figure 32. JTAG Timing Diagram

Table 130. Timing Requirements for JTAG Input

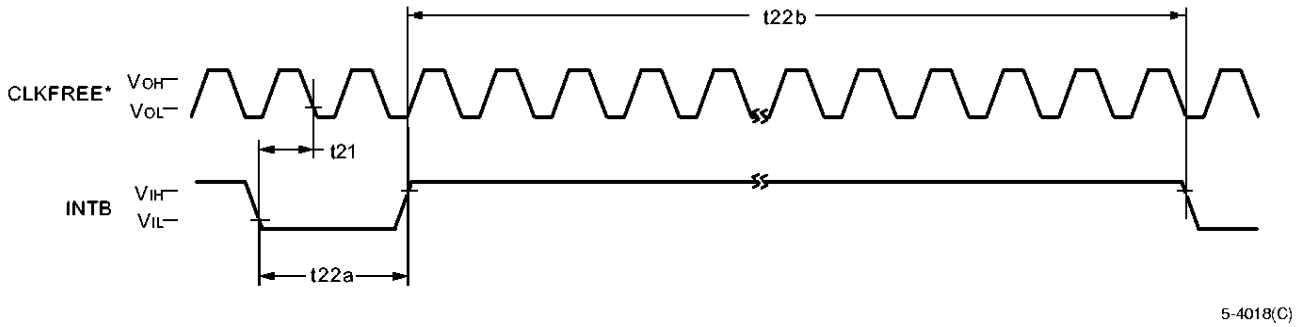
Ref	Parameter	V_{DD} = 4.5 V to 5.5 V		V_{DD} = 3.0 V to 3.6 V		Unit
		T_{MIN} = 25 ns		T_{MIN} = 31.25 ns		
		Min	Max	Min	Max	
t12	TCK Period (high to high)	50	—	62.5	—	ns
t13	TCK High Time (high to low)	22	—	28	—	ns
t14	TCK Low Time (low to high)	22	—	28	—	ns
t15	TMS Setup Time (valid to high)	7	—	11	—	ns
t16	TMS Hold Time (high to invalid)	0	—	0	—	ns
t17	TDI Setup Time (valid to high)	7	—	11	—	ns
t18	TDI Hold Time (high to invalid)	0	—	0	—	ns

Table 131. Timing Characteristics for JTAG Output

Ref	Parameter	V_{DD} = 4.5 V to 5.5 V		V_{DD} = 3.0 V to 3.6 V		Unit
		T_{MIN} = 25 ns		T_{MIN} = 31.25 ns		
		Min	Max	Min	Max	
t19	TDO Delay (low to valid)	—	22	—	26	ns
t20	TDO Hold (low to invalid)	0	—	0	—	ns

8 Timing Requirements and Characteristics (continued)

8.7 Interrupt



* CLKFREE is the free-running clock sourced to DOUT.

Figure 33. Interrupt Timing Diagram

Note: Interrupt is asserted during an interruptible instruction and no other pending interrupts.

Table 132. Timing Requirements for Interrupt

Ref	Parameter	V_{DD} = 4.5 V to 5.5 V		V_{DD} = 3.0 V to 3.6 V		Unit
		T_{MIN} = 25 ns		T_{MIN} = 31.25 ns		
		Min	Max	Min	Max	
t21*	Interrupt Setup (low to low)	17	—	20	—	ns
t22a	INTB Assertion Time (low to high)	2T	—	2T	—	ns
t22b†	INTB Deassertion Time (high to low)	2T	—	2T	—	ns

* Only necessary for synchronized timing, no requirement for asynchronous assertion.
† In general, INTB deassertion time should be long enough to allow for the interrupt service routine to be completed.

Note: T = the period of the free-running clock, CLKFREE.

8 Timing Requirements and Characteristics (continued)

8.8 Input/Output Ports (IOP)

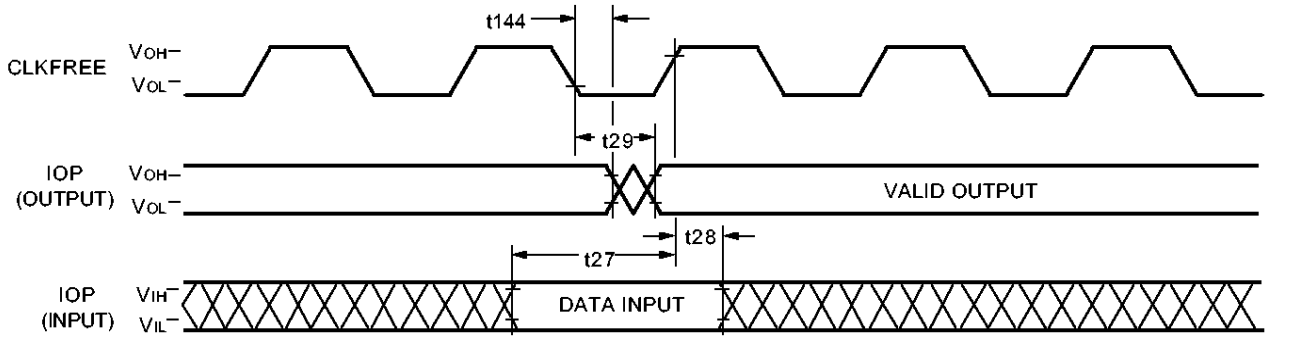


Figure 34. Write Outputs Followed by Read Inputs (cbit = Immediate; a1 = sbit)

Table 133. Timing Requirements for IOP Input Read

Ref	Parameter	V_{DD} = 4.5 V to 5.5 V		V_{DD} = 3.0 V to 3.6 V		Unit
		T_{MIN} = 25 ns		T_{MIN} = 31.25 ns		
		Min	Max	Min	Max	
t27	IOP Input Setup Time (valid to high)	20	—	20	—	ns
t28	IOP Input Hold Time (high to invalid)	—	0	—	0	ns

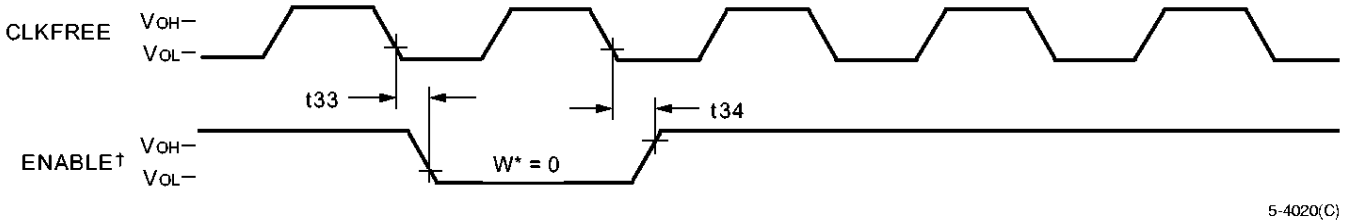
Table 134. Timing Characteristics for IOP Output

Ref	Parameter	V_{DD} = 4.5 V to 5.5 V		V_{DD} = 3.0 V to 3.6 V		Unit
		T_{MIN} = 25 ns		T_{MIN} = 31.25 ns		
		Min	Max	Min	Max	
t29	IOP Output Valid Time (low to valid)	—	4	—	6	ns
t144	IOP Output Hold Time (low to invalid)	–4	—	–6	—	ns

8 Timing Requirements and Characteristics (continued)

8.9 External Memory Interface

The following timing diagrams, characteristics, and specifications do not apply to interactions with delayed external memory enables unless otherwise stated. See the *DSP165X Digital Signal Processor Information Manual* for a more detailed description of the external memory interface, including complete functional diagrams.



* W = number of wait-states selected through the **mwait** register.
† ENABLE is any one of the memory segment enable signals, EROM, ERAMHI, or ERAMLO.

Figure 35. Enable Transition Timing

Table 135. Timing Characteristics for External Memory Enables (EROM, ERAMHI, ERAMLO)

Ref	Parameter	V_{DD} = 4.5 V to 5.5 V		V_{DD} = 3.0 V to 3.6 V		Unit
		T_{MIN} = 25 ns		T_{MIN} = 31.25 ns		
		Min	Max	Min	Max	
t33	Enable Assert (low to low)	0	4	0	6	ns
t34	Enable Deassert (low to high)	0	4	0	6	ns

Table 136. Timing Characteristics for Device Enable

Ref	Parameter	V_{DD} = 4.5 V to 5.5 V		V_{DD} = 3.0 V to 3.6 V		Unit
		T_{MIN} = 25 ns		T_{MIN} = 31.25 ns		
		Min	Max	Min	Max	
t33	Enable Assert Time (low to low)	0	5	0	7	ns
t34	Enable Deassert Time (low to high)	0	5	0	7	ns

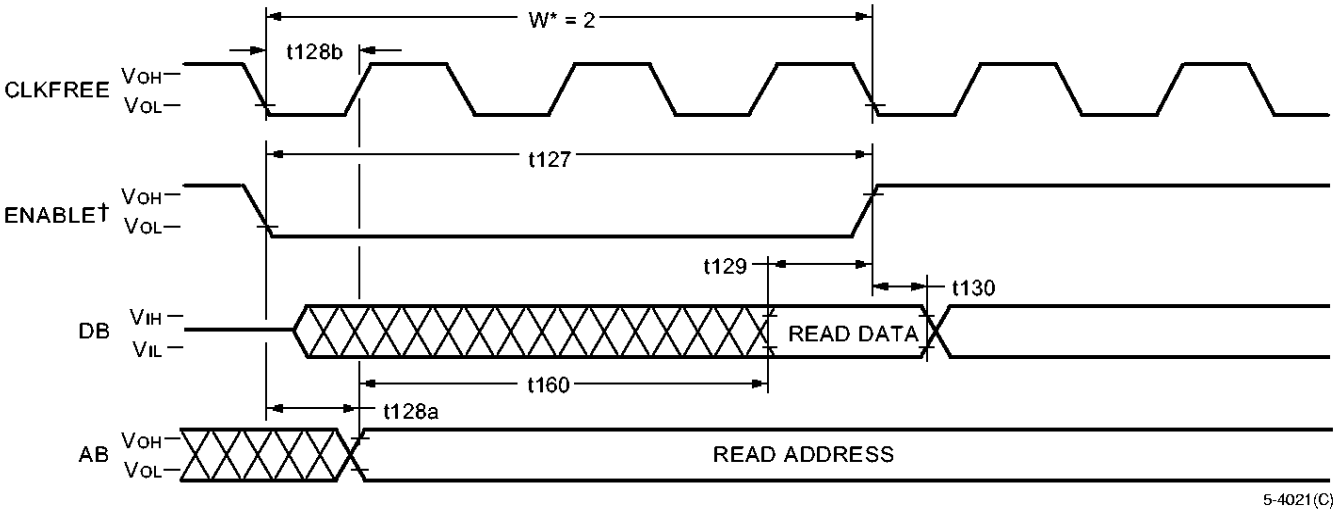
Table 137. Timing Characteristics for Delayed External Memory Enables

Ref	Parameter	V_{DD} = 4.5 V to 5.5 V		V_{DD} = 3.0 V to 3.6 V		Unit
		T_{MIN} = 25 ns		T_{MIN} = 31.25 ns		
		Min	Max	Min	Max	
t33	Delayed Enable Assert Time	T/2	T/2 + 9	T/2	T/2 + 9	ns

Note: T = the period of the free-running clock, CLKFREE.

8 Timing Requirements and Characteristics (continued)

8.9 External Memory Interface (continued)



* W = number of wait-states selected through the **mwait** register.
† ENABLE indicates any one of the memory segment enable signals, EROM, ERAMHI, or ERAMLO.

Figure 36. External Memory Data Read Timing Diagram

Table 138. Timing Characteristics for External Memory Access

Ref	Parameter	V_{DD} = 4.5 V to 5.5 V		V_{DD} = 3.0 V to 3.6 V		Unit
		T_{MIN} = 25 ns		T_{MIN} = 31.25 ns		
		Min	Max	Min	Max	
t127	Enable Width (low to high)	T(1 + W) – 1	—	T(1 + W) – 1	—	ns
t128a	Address Valid (enable low to valid)	—	1	—	1	ns
t128b	Address Valid (CLKFREE low to valid)	—	1	—	1	ns

Note: T = the period of the free-running clock, CLKFREE. W = the number of wait-states selected through the **mwait** register.

8 Timing Requirements and Characteristics (continued)

8.9 External Memory Interface (continued)

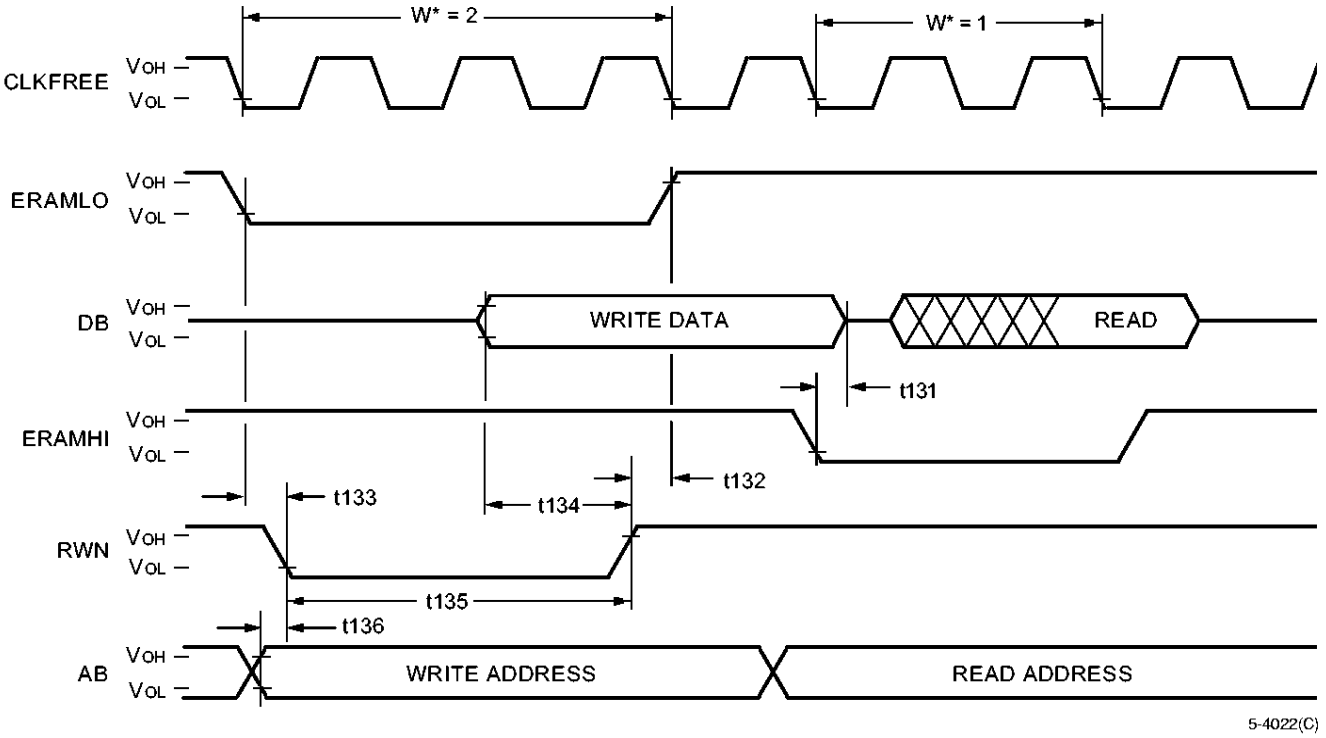
Table 139. Timing Requirements for External Memory Read (EROM, ERAMHI, ERAMLO)

Ref	Parameter	V_{DD} = 4.5 V to 5.5 V		V_{DD} = 3.0 V to 3.6 V		Unit
		T_{MIN} = 25 ns		T_{MIN} = 31.25 ns		
		Min	Max	Min	Max	
t129	Read Data Setup (valid to enable high)	17	—	17	—	ns
t130	Read Data Hold (enable high to hold)	0	—	0	—	ns
t160	External Memory Access Time (valid to valid)	—	T(1 + W) – 17	—	T(1 + W) – 17	ns

Note: T = the period of the free-running clock, CLKFREE. W = the number of wait-states selected through the **mwait** register.

8 Timing Requirements and Characteristics (continued)

8.9 External Memory Interface (continued)



* W = number of wait-states selected through the **mwait** register. In this example, ERAMLO is programmed for two wait-states and ERAMHI is programmed for one wait-state (**mwait** = 0x0102).

Figure 37. External Memory Data Write, Read Timing Diagram

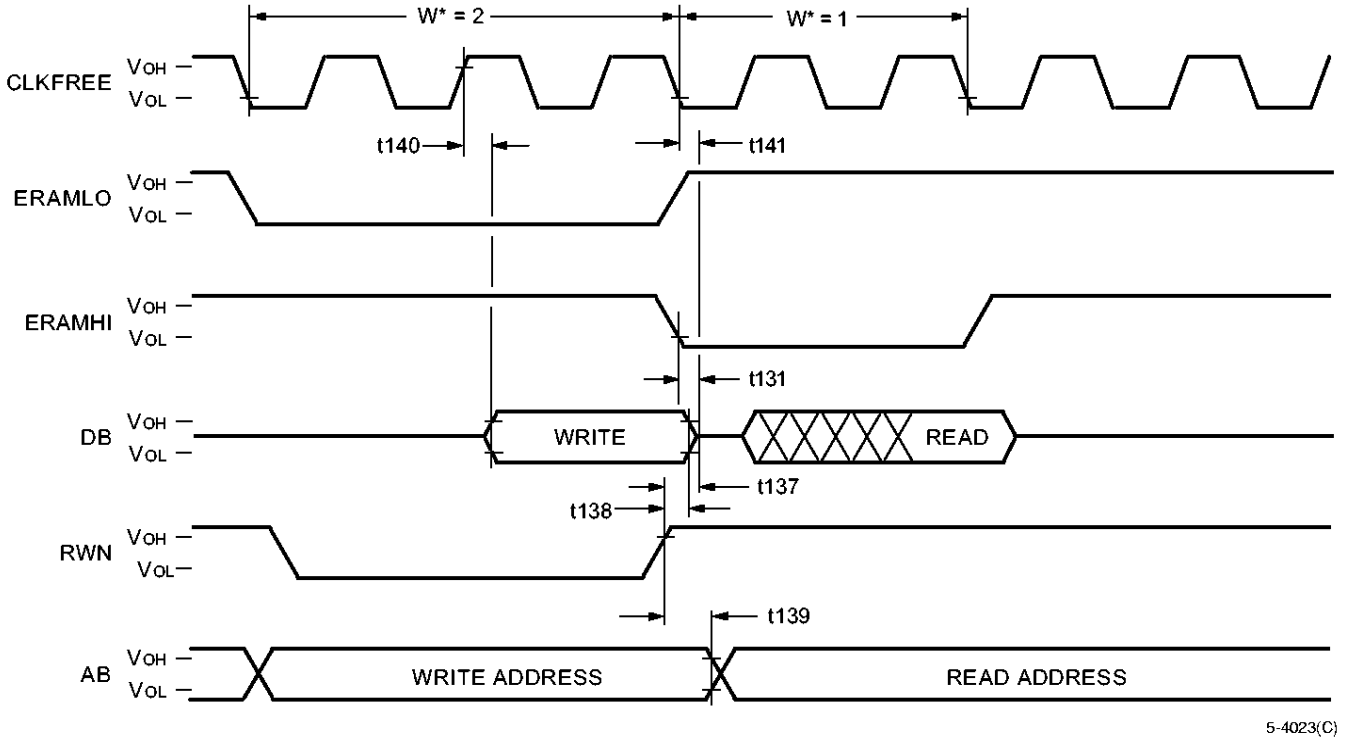
Table 140. Timing Characteristics for External Memory Data Write (All Enables)

Ref	Parameter	V_{DD} = 4.5 V to 5.5 V		V_{DD} = 3.0 V to 3.6 V		Unit
		T_{MIN} = 25 ns		T_{MIN} = 31.25 ns		
		Min	Max	Min	Max	
t131	Write Overlap (enable low to 3-state)	—	0	—	0	ns
t132	RWN Advance (RWN high to enable high)	0	—	0	—	ns
t133	RWN Delay (enable low to RWN low)	0	—	0	—	ns
t134	Write Data Setup (data valid to RWN high)	T(1 + W)/2 – 10	—	T(1 + W)/2 – 10	—	ns
t135	RWN Width (low to high)	T(1 + W) – 8	—	T(1 + W) – 8	—	ns
t136	Write Address Setup (address valid to RWN low)	0	—	0	—	ns

Note: T = the period of the free-running clock, CLKFREE. W = the number of wait-states selected through the **mwait** register.

8 Timing Requirements and Characteristics (continued)

8.9 External Memory Interface (continued)



* W = number of wait-states selected through the **mwait** register. In this example, ERAMLO is programmed for two wait-states and ERAMHI is programmed for one wait-state (**mwait** = 0x0102).

Figure 38. Write Cycle Followed by Read Cycle

Table 141. Timing Characteristics for Write Cycle Followed by Read Cycle

Ref	Parameter	V_{DD} = 4.5 V to 5.5 V		V_{DD} = 3.0 V to 3.6 V		Unit
		T_{MIN} = 25 ns		T_{MIN} = 31.25 ns		
		Min	Max	Min	Max	
t137	Write Data 3-state (RWN high to 3-stated)	—	2	—	2	ns
t138	Write Data Hold (RWN high to data hold)	0	—	0	—	ns
t139	Write Address Hold (RWN high to address hold)	0	—	0	—	ns
t140	Write Data Valid (CLKFREE high to valid)	0	—	0	—	ns
t141	Write Data 3-state (CLKFREE low to 3-state)	0	—	0	—	ns

8 Timing Requirements and Characteristics (continued)

8.9 External Memory Interface (continued)

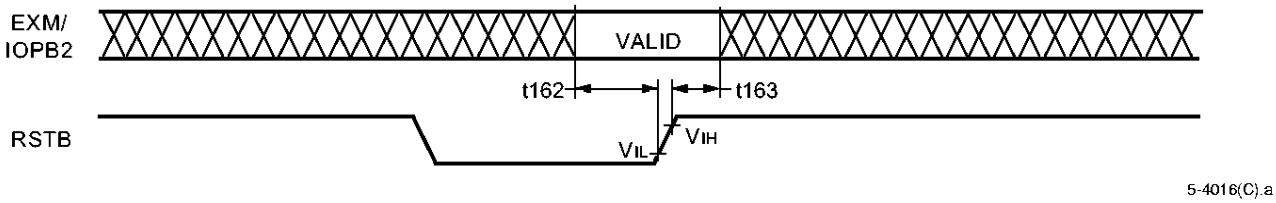


Figure 39. EXM Timing Diagram

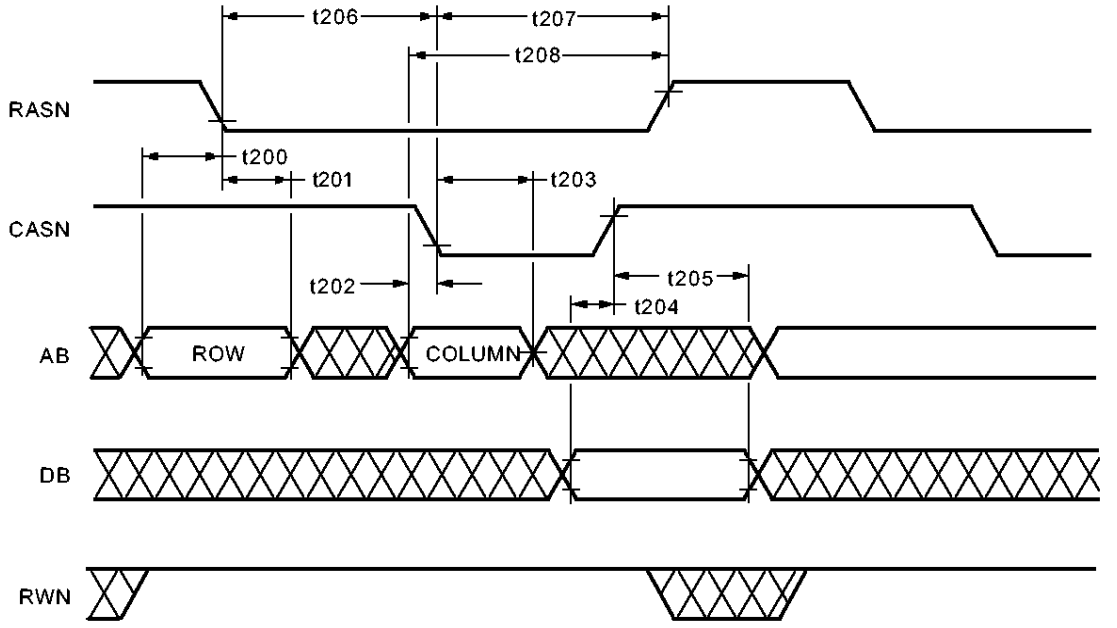
Note: In Figure 39, after the reset transition during which the EXM input is sampled, the EXM/IOPB2 reverts to the IOPB2 function. (See Section 3.2.7 on page 21.)

Table 142. Timing Requirements for EXM with Respect to RSTB

Ref	Parameter	V_{DD} = 4.5 V to 5.5 V		V_{DD} = 3.0 V to 3.6 V		Unit
		T_{MIN} = 25 ns		T_{MIN} = 31.25 ns		
		Min	Max	Min	Max	
t162	EXM Setup with Respect to RSTB	15	—	15	—	ns
t163	EXM Hold with Respect to RSTB	15	—	15	—	ns

8 Timing Requirements and Characteristics (continued)

8.10 External DRAM Interface



5-4024(C)

Figure 40. Read Cycle Timing (Relative) Diagram

Table 143. Timing Specification for a DRAM Read Cycle

Ref	Parameter	V_{DD} = 4.5 V to 5.5 V		V_{DD} = 3.0 V to 3.6 V		Unit
		T_{MIN} = 25 ns		T_{MIN} = 31.25 ns		
		Min	Max	Min	Max	
t200	Address Setup to RASN Low	0.5T – 3	—	0.5T – 3	—	ns
t201	Address Hold to RASN Low	(C + 0.5)T – 3	—	(C + 0.5)T – 3	—	ns
t202	Address Setup to CASN Low	0.5T – 3	—	0.5T – 3	—	ns
t203	Address Hold to CASN Low	(0.5 + P + A)T	—	(0.5 + P + A)T	—	ns
t204	DATA Setup to CASN High	20	—	20	—	ns
t205	DATA Hold to CASN High	0	—	0	—	ns
t206	RASN Low to CASN Low	(C + 1)T – 3	—	(C + 1)T – 3	—	ns
t207	CASN Low to RASN High	(0.5 + A – C)T – 1	—	(0.5 + A – C)T – 1	—	ns
t208	Column Address Valid to RASN High	(A + 1 – C)T – 3	—	(A + 1 – C)T – 3	—	ns

Note: The following definitions apply to the T_{MIN} columns. For more information, see Table 39 on page 58.
C = CADLY, column address delay, 0 or 1 CLKFREE cycle.
A = ACC, access time, 0 to 15 CLKFREE cycles.
P = PRCH, precharge time, 0 to 7 CLKFREE cycles.
T = the period of the free-running clock, CLKFREE.

8 Timing Requirements and Characteristics (continued)

8.10 External DRAM Interface (continued)

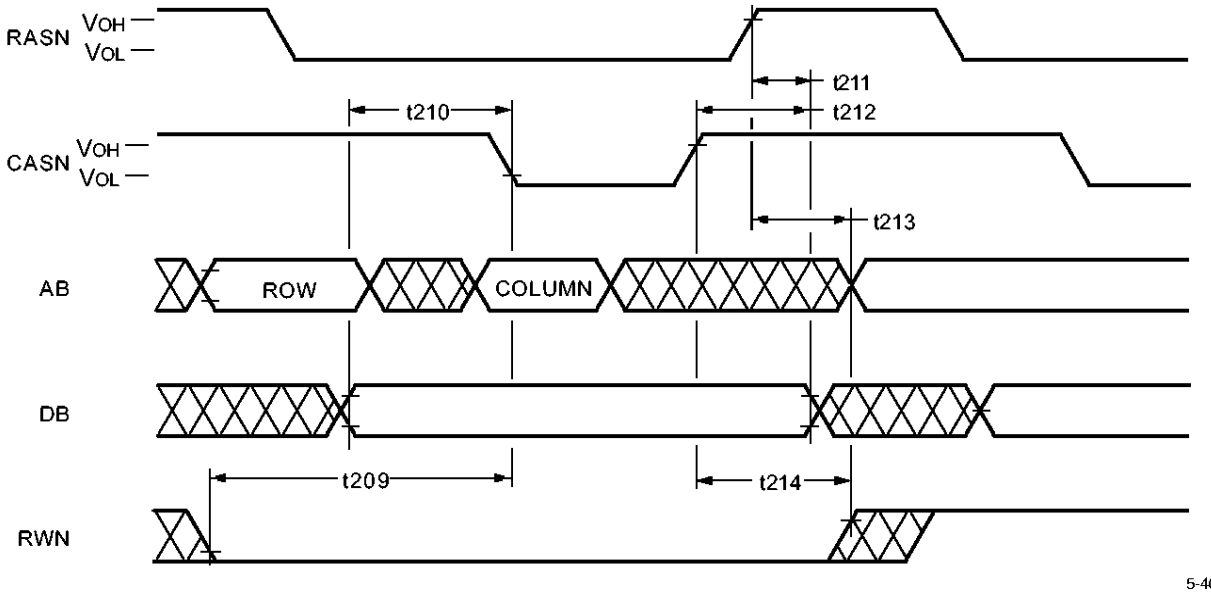


Figure 41. Early Write Cycle Timing (Relative) Diagram

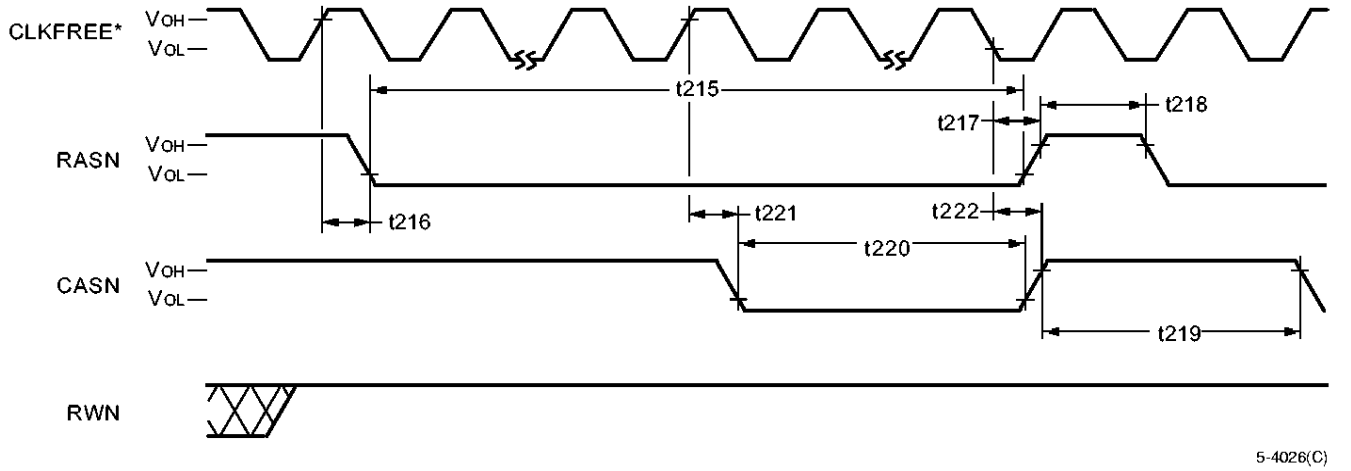
Table 144. Timing Specification for a DRAM Write Cycle

Ref	Parameter	V_{DD} = 4.5 V to 5.5 V		V_{DD} = 3.0 V to 3.6 V		Unit
		T_{MIN} = 25 ns		T_{MIN} = 31.25 ns		
		Min	Max	Min	Max	
t209	RWN Low to CASN Low	(1.5 + C)T – 1	—	(1.5 + C)T – 1	—	ns
t210	DB Valid to CASN Low	(0.5 + C)T – 3	—	(0.5 + C)T – 3	—	ns
t211	RASN High to DB Invalid	0	—	0	—	ns
t212	CASN High to DB Invalid	0	—	0	—	ns
t213	RASN High to RWN High	0	—	0	—	ns
t214	CASN High to RWN High	0	—	0	—	ns

Note: The following definitions apply to the T_{MIN} columns. For more information, see Table 39 on page 58.
C = CADLY, column address delay, 0 or 1 CLKFREE cycle.
T = the period of the free-running clock, CLKFREE.

8 Timing Requirements and Characteristics (continued)

8.10 External DRAM Interface (continued)



* CLKFREE is a free-running clock.

Figure 42. Synchronous Delay DRAM Interface Timing Diagram

Table 145. Timing Specification for DRAM Control Signals

Ref	Parameter	V_{DD} = 4.5 V to 5.5 V		V_{DD} = 3.0 V to 3.6 V		Unit
		T_{MIN} = 25 ns		T_{MIN} = 31.25 ns		
		Min	Max	Min	Max	
t215	Pulse RASN Low	(A + 1.5)T – 1	—	(A + 1.5)T – 1	—	ns
t216	CLKFREE High to RASN Low	—	5	—	5	ns
t217	CLKFREE Low to RASN High	—	5	—	5	ns
t218	Pulse RASN High	(P + 0.5)T – 1	—	(P + 0.5)T – 1	—	ns
t219	Pulse CASN High	(P + 1.5 + C)T – 1	—	(P + 1.5 + C)T – 1	—	ns
t220	Pulse CASN Low	(A + 0.5 – C)T – 1	—	(A + 0.5 – C)T – 1	—	ns
t221	CLKFREE High to CASN Low	—	5	—	5	ns
t222	CLKFREE Low to CASN High	—	5	—	5	ns

Note: The following definitions apply to the T_{MIN} columns. For more information, see Table 39 on page 58.
C = CADLY, column address delay, 0 or 1 CLKFREE cycle.
A = ACC, access time, 0 to 15 CLKFREE cycles.
P = PRCH, precharge time, 0 to 7 CLKFREE cycles.
T = the period of the free-running clock, CLKFREE.

8 Timing Requirements and Characteristics (continued)

8.10 External DRAM Interface (continued)

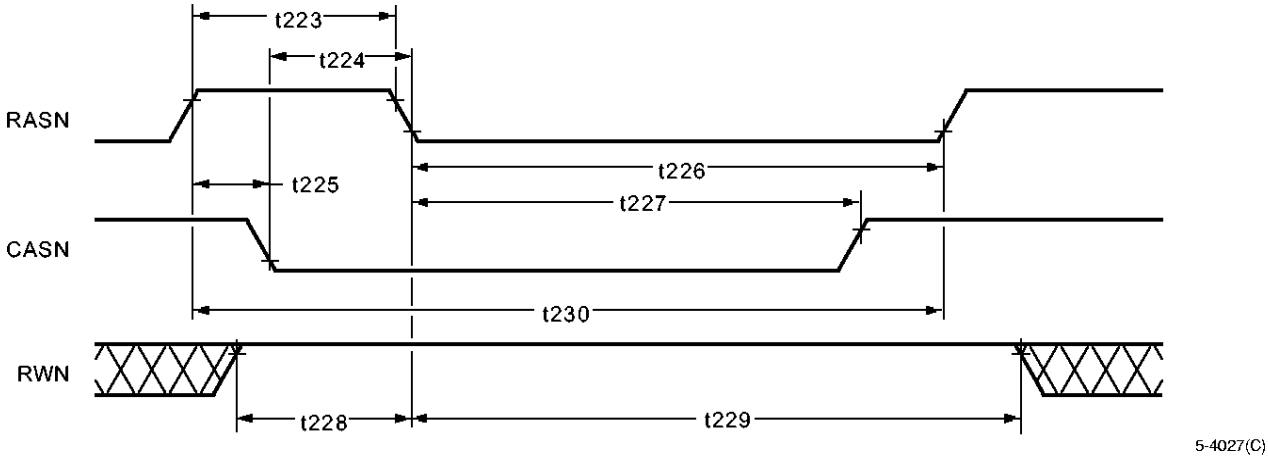


Figure 43. CASN Before RASN Refresh Cycle Timing Diagram

Table 146. Timing Specification for Refresh with High-Speed* Clock

Ref	Parameter	V_{DD} = 4.5 V to 5.5 V		V_{DD} = 3.0 V to 3.6 V		Unit
		T_{MIN} = 25 ns		T_{MIN} = 31.25 ns		
		Min	Max	Min	Max	
t223	Pulse RASN High (precharge)	5T – 1	—	5T – 1	—	ns
t224	CASN Low to RASN Low	T(R† + 1) – 1	—	T(R + 1) – 1	—	ns
t225	RASN High to CASN Low	(5.5)T – 1	—	(5.5)T – 1	—	ns
t226	Pulse RASN Low (refresh)	(5.5 + 2R)T – 1	—	(5.5 + 2R)T – 1	—	ns
t227	RASN Low to CASN High	(5.5 + 2R)T – 1	—	(5.5 + 2R)T – 1	—	ns
t228	RWN Setup with Respect to RASN Low	(1.5 + R)T – 1	—	(1.5 + R)T – 1	—	ns
t229	RWN Hold with Respect to Low	(10.5 + 2R)T – 1	—	(10.5 + 2R)T – 1	—	ns

* That is, not the low-frequency clock chosen as the DSP core clock.
† R = the value of the REXT bit; either 0 or 1.

Note: T = the period of the free-running clock, CLKFREE.

Table 147. Timing Specification for Refresh Under Low-Frequency* Clock

Ref	Parameter	V_{DD} = 4.5 V to 5.5 V		V_{DD} = 3.0 V to 3.6 V		Unit
		T_{MIN} = 25 ns		T_{MIN} = 31.25 ns		
		Min	Max	Min	Max	
t223	Pulse RASN High (precharge)	$2T_2 - 1$	—	$2T_2 - 1$	—	ns
t224	CASN Low to RASN Low	$T_2 - 1$	—	$T_2 - 1$	—	ns
t225	RASN High to CASN Low	$T_2 - 1$	—	$T_2 - 1$	—	ns
t226	Pulse RASN Low (refresh)	$2T_2 - 1$	—	$2T_2 - 1$	—	ns
t227	RASN Low to CASN High	$T_2 - 1$	—	$T_2 - 1$	—	ns
t230	Refresh Cycle	$4T_2 - 1$	—	$4T_2 - 1$	—	ns

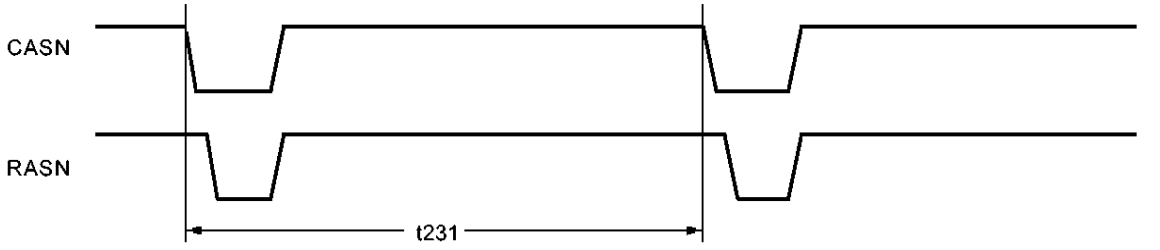
* When using the DRAM controller, the only allowed setting for CLKLOW is the input clock (CLKIN) divided by four.

Note: T_2 = 512 kHz = CLKIN/8.

8 Timing Requirements and Characteristics (continued)

8.10 External DRAM Interface (continued)

The refresh interval is programmed by the RFSH field in the **drc** control register. The refresh period is the period of the free-running clock (CLKFREE) × 64 × RFSH.



5-4028(C)

Figure 44. Refresh Interval Timing with High-Speed Clocking

Table 148. Timing Specifications for Refresh Interval Under High-Speed Clocking

Ref	Parameter	V_{DD} = 4.5 V to 5.5 V		V_{DD} = 3.0 V to 3.6 V		Unit
		T_{MIN} = 25 ns		T_{MIN} = 31.25 ns		
		Min	Max	Min	Max	
t231	Refresh Interval with CLKPLL	—	CLKFREE × 64 × RFSH	—	CLKFREE × 64 × RFSH	ns

The refresh interval is set by the low-frequency clock (CLKLOW)* when clocking has switched to CLKLOW.

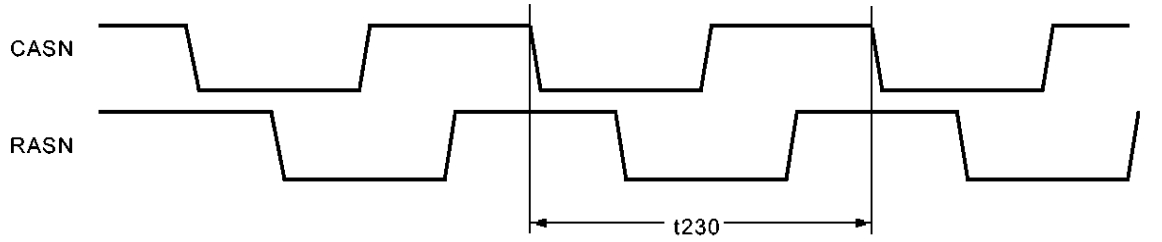


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Figure 45. Refresh Interval Timing with CLKLOW Clocking DSP Core

Table 149. Timing Specifications for Refresh Interval with CLKLOW Clocking DSP Core

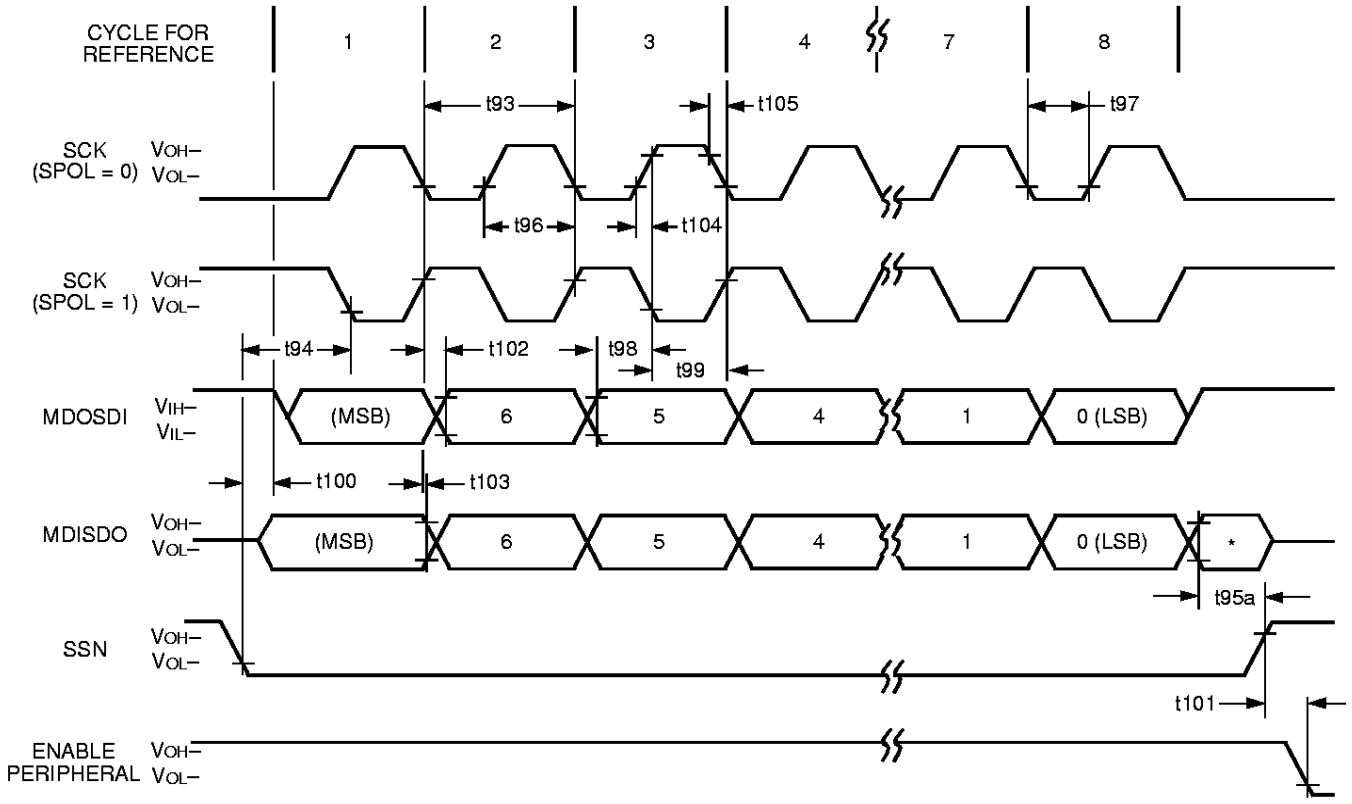
Ref	Parameter	V_{DD} = 4.5 V to 5.5 V		V_{DD} = 3.0 V to 3.6 V		Unit
		T_{MIN} = 25 ns		T_{MIN} = 31.25 ns		
		Min	Max	Min	Max	
t230	Refresh Interval with CLKLOW	—	4 × T_2	—	4 × T_2	ns

Note: T_2 = CLKIN/8 = 512 kHz (1.95 µs), assuming SLOMUX[1:0] = 00.

* CLKLOW should be set to CLKIN/4 for most DRAMs.

8 Timing Requirements and Characteristics (continued)

8.11 Synchronous Serial Interface (SSI) Specifications



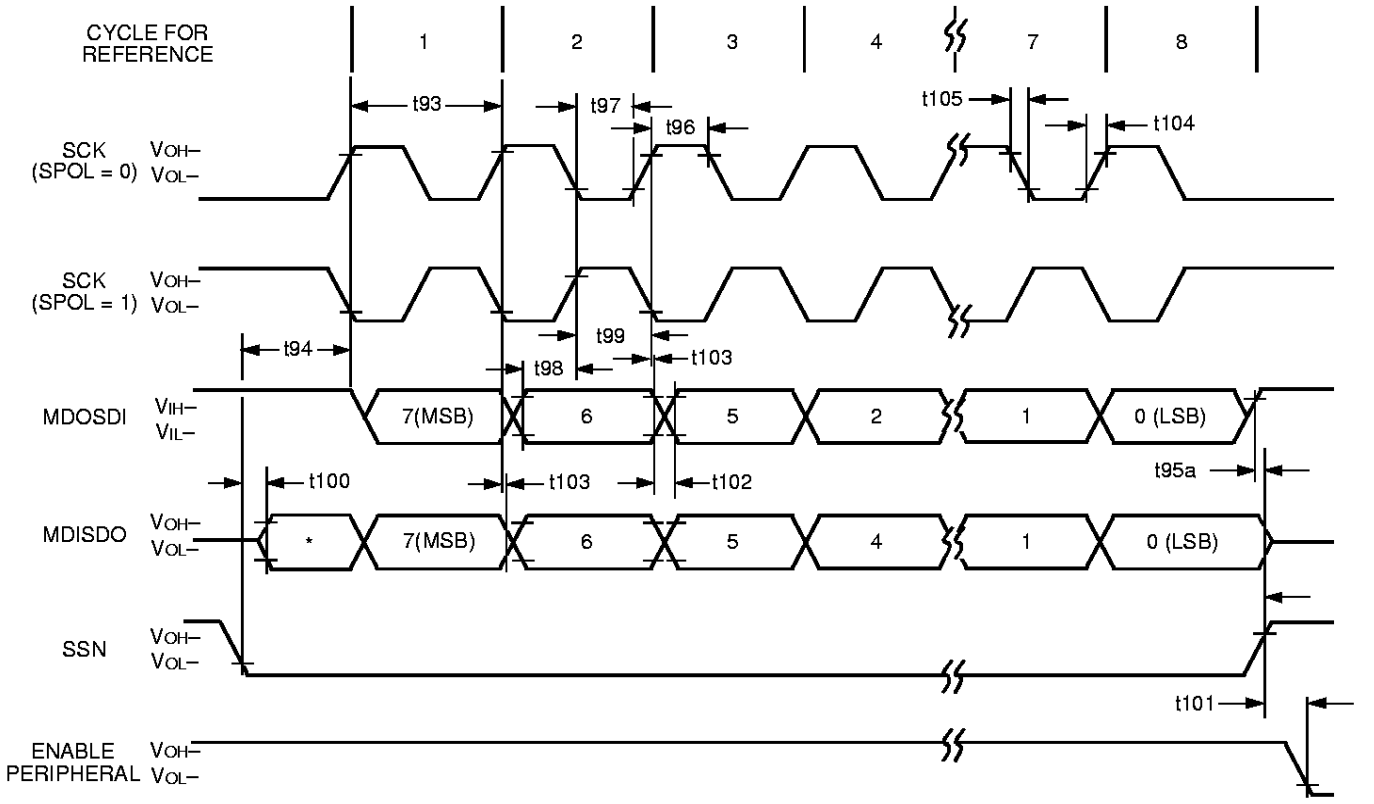
* Not defined, but normally LSB of previously transmitted character.

12-3357 (F)

Figure 46. SSI Transfer Timing (SPHA = 0)

8 Timing Requirements and Characteristics (continued)

8.11 Synchronous Serial Interface (SSI) Specifications (continued)



* Not defined, but normally LSB of previously transmitted character. If SSN remains low, then a back-to-back transfer may take place, in which case the LSB of the previously transmitted character immediately precedes the MSB. That is, there are no undefined states on MDISDO. As long as SSN remains low, MDISDO is not 3-stated between transfers.

12-3358 (F)

Figure 47. SSI Transfer Timing (SPHA = 1)

8 Timing Requirements and Characteristics (continued)

8.11 Synchronous Serial Interface (SSI) Specifications (continued)

Table 150. Timing Characteristics for SSI*

Ref	Parameter	V_{DD} = 4.5 V to 5.5 V		V_{DD} = 3.0 V to 3.6 V		Unit
		T_{MIN} = 25 ns		T_{MIN} = 31.25 ns		
		Min	Max	Min	Max	
t93	Master Cycle Time	2T†	—	2T†	—	ns
	Slave Cycle Time	80	—	80	—	ns
t94	Master Enable Lead Time	Not Applicable				
	Slave Enable Lead Time	5	—	5	—	ns
t95	Master Enable Lag Time	Not Applicable				
	Slave Enable Lag Time	15	—	15	—	ns
t95a	Slave Disable Idle Time	5	—	5	—	ns
t96	Master Clock High Time	T – 25	—	T – 25	—	ns
	Slave Clock High Time	40	—	40	—	ns
t97	Master Clock Low Time	T – 20	—	T – 20	—	ns
	Slave Clock Low Time	40	—	40	—	ns
t98‡	Input Data Setup Time (slave mode)	12	—	12	—	ns
t99‡	Input Data Hold Time (slave mode)	0	—	0	—	ns
t100	Slave Data Out Access Time	0	60	0	60	ns
t101	Slave Data Out Disable Time	0	12	0	12	ns
t102	Output Data Valid After Clock	—	80	—	80	ns
t103	Output Data Hold Time After Clock	0	—	0	—	ns
t104	Output Rise Time	1	25	1	25	ns
	Input Rise Time	—	100	—	100	ns
t105	Output Fall Time	1	25	1	25	ns
	Input Fall Time	—	100	—	100	ns

* These specifications are derived from the 68HC11 specification. Some of the timing definitions may change later to be compatible with the other timing definitions in this document.
† T is the period of CLKFREE.
‡ t98 and t99 are given for slave operation. For master mode, input data setup time is 20 ns minimum and input data hold time is still 0 ns.

9 Crystal Oscillator Electrical Requirements and Characteristics

This section describes electrical requirements and characteristics for high- and low-frequency crystal oscillator circuits.

9.1 Crystal Oscillator

If the option for using the external crystal is chosen, the electrical requirements and characteristics described in this section apply.

9.1.1 Crystal Oscillator Power Dissipation

The typical power dissipation at 4.096 MHz of the internal high-frequency crystal oscillator circuit below is 6 mW at 5 V and 0.82 mW at 3 V.

9.1.2 Crystal Oscillator External Components

The crystal oscillator is enabled by connecting a crystal across XTALA and XTALB, along with one external capacitor from each of these pins to ground (see Figure 48). For most applications, 30 pF external capacitors are recommended; however, larger values may be necessary if precise frequency tolerance is required (see Section 9.2, Frequency Accuracy Considerations). The crystal should be either fundamental or overtone mode, parallel resonant, with a power dissipation of at least 1 mW, and be specified at a load capacitance equal to the total capacitance seen by the crystal (including external capacitors and strays).

The series resistance of the crystal should be specified to be less than half the absolute value of the negative resistance shown in Figures 49 and 50 for the crystal frequency.

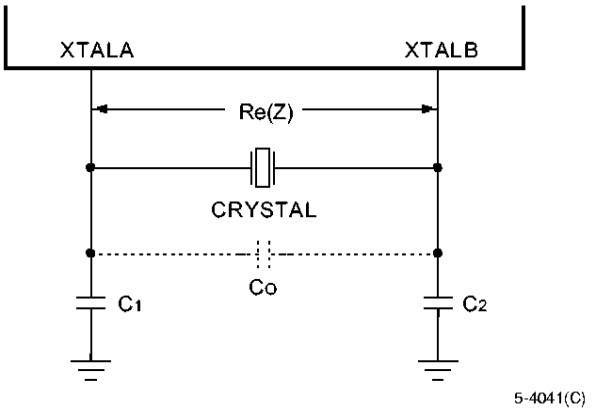


Figure 48. Fundamental Crystal Configuration

The following guidelines should be followed when designing the printed-circuit board layout for a crystal-based application:

- Keep crystal and external capacitors as close to XTALA and XTALB pins as possible to minimize board stray capacitance.
- Keep high-frequency digital signals such as DOUT away from XTALA and XTALB traces to avoid coupling.

9 Crystal Oscillator Electrical Requirements and Characteristics (continued)

9.1 Crystal Oscillator (continued)

9.1.3 Crystal Oscillator Negative Resistance Curves

Figure 49 shows worst-case negative resistance curves for a high-frequency crystal oscillator operating with a 5 V power supply (V_{DD} = 4.5 V to 5.5 V). These worst-case conditions are as follows:

- Maximum Temperature = 120 °C
- Minimum V_{DD} = 4.5 V
- Maximum C_O = 7 pF

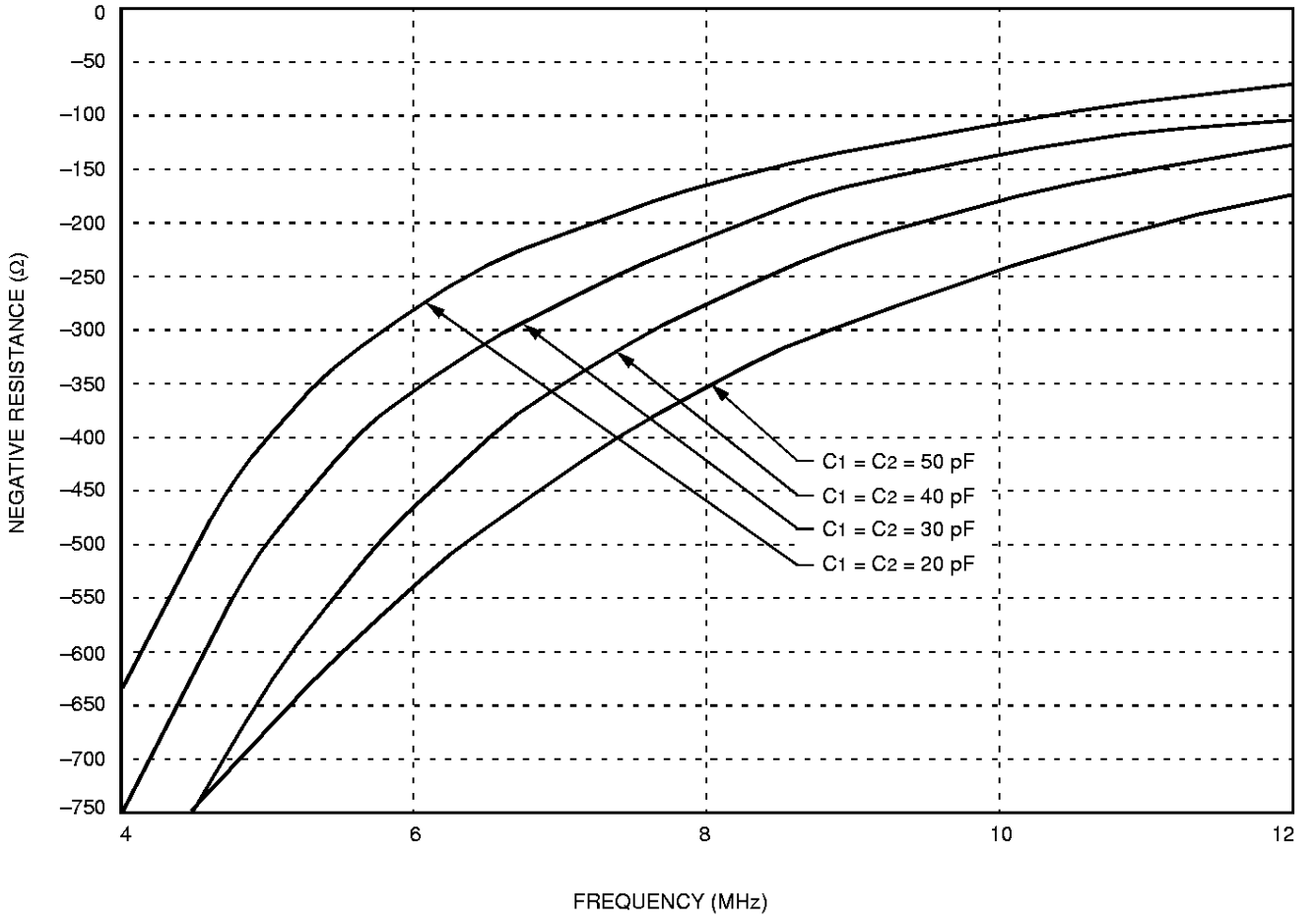


Figure 49. 5 V Crystal Oscillator Negative Resistance Curves

9 Crystal Oscillator Electrical Requirements and Characteristics (continued)

9.1 Crystal Oscillator (continued)

9.1.3 Crystal Oscillator Negative Resistance Curves (continued)

Figure 50 shows worst-case negative resistance curves for a crystal oscillator operating with a 3.3 V power supply (V_{DD} = 3.0 V to 3.6 V). These worst-case conditions are as follows:

- Maximum Temperature = 120 °C
- Minimum V_{DD} = 3.0 V
- Maximum C_O = 7 pF

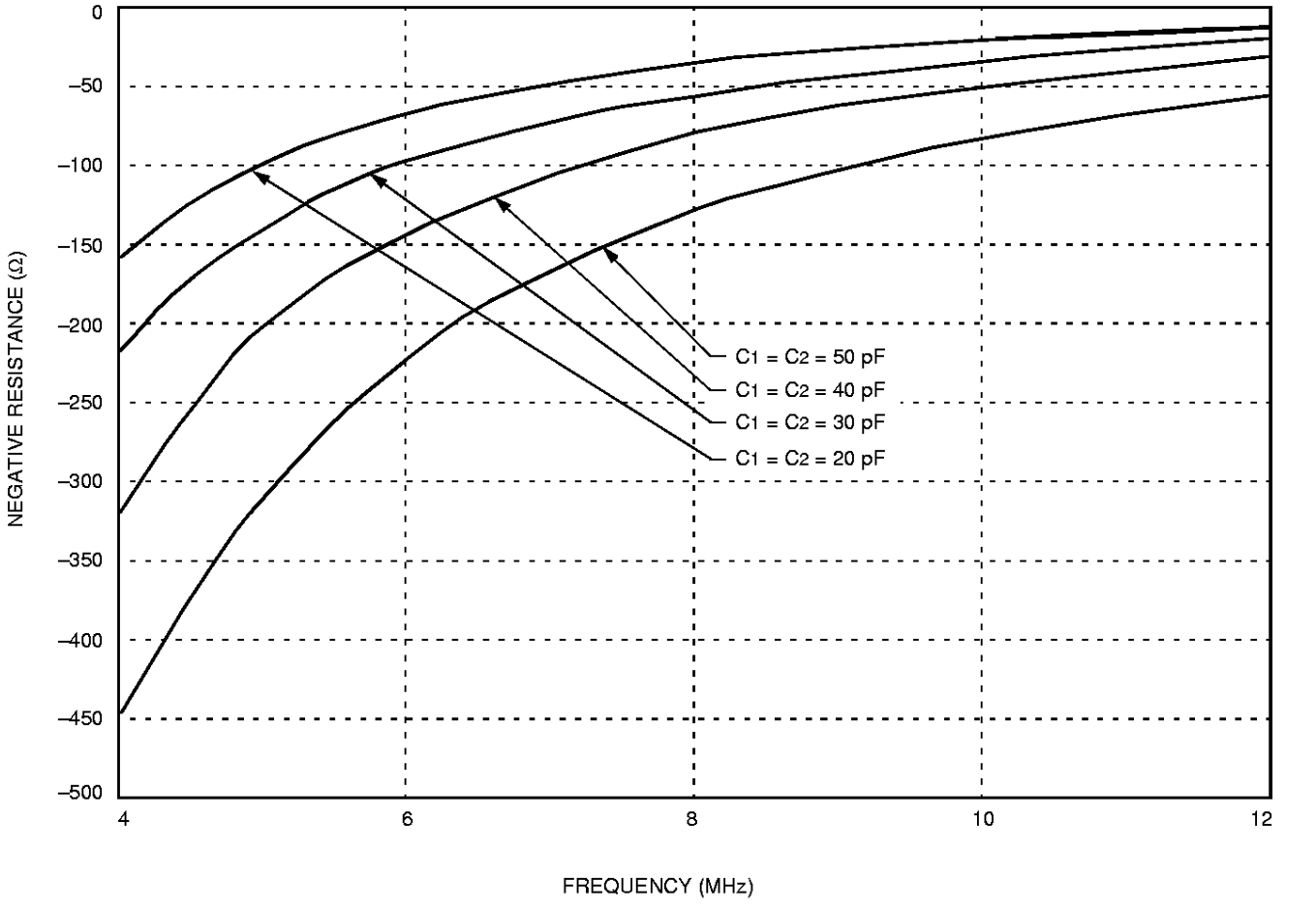


Figure 50. 3.3 V Crystal Oscillator Negative Resistance Curves

9 Crystal Oscillator Electrical Requirements and Characteristics (continued)

9.2 Frequency Accuracy Considerations

For most applications, clock frequency errors in the hundreds of parts per million (ppm) can be tolerated with no adverse effect. However, for applications where precise frequency tolerance on the order of 100 ppm is required, care must be taken in the choice of external components (crystal and capacitors) as well as in the layout of the printed-circuit board. Several factors determine the frequency accuracy of a crystal-based oscillator circuit. Some of these factors are determined by the properties of the crystal itself. Generally, a low-cost, standard crystal is not sufficient for a high-accuracy application, and a custom crystal must be specified. Most crystal manufacturers provide extensive information concerning the accuracy of their crystals, and an applications engineer from the crystal vendor should be consulted prior to specifying a crystal for a given application.

In addition to absolute, temperature, and aging tolerances of a crystal, the operating frequency of a crystal is also determined by the total load capacitance seen by the crystal. When ordering a crystal from a vendor, it is necessary to specify a load capacitance at which crystal operating frequency is measured. Variations in this load capacitance due to temperature and manufacturing variations cause variations in the operating frequency of the oscillator. Figure 51 illustrates some of the sources of this variation.

C_{EXT} = External load capacitor (one each required for XTALA and XTALB)
C_D = Parasitic capacitance of the *FlashDSP*1650 itself
C_B = Parasitic capacitance of the printed-wiring board
C_O = Parasitic capacitance of crystal (not part of C_L, but still a source of frequency variation)

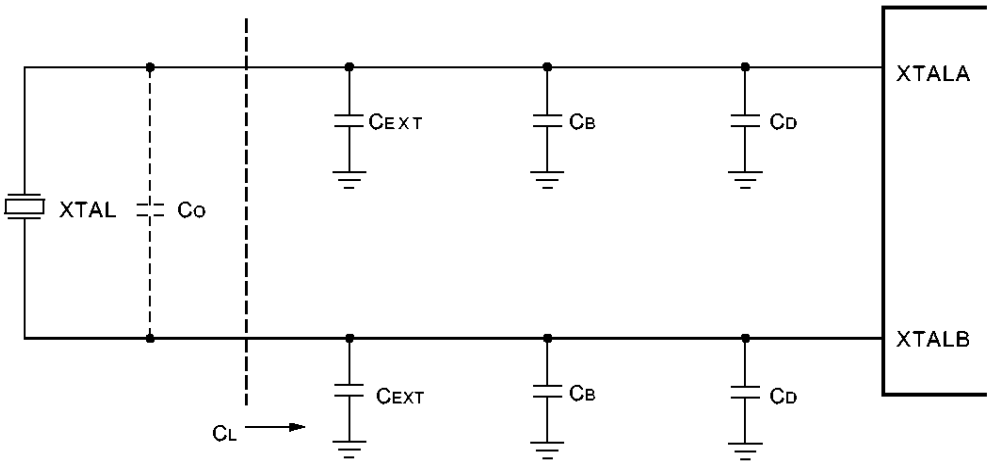


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Figure 51. Components of Load Capacitance for Crystal Oscillator

The load capacitance, C_L, must be specified to the crystal vendor. The crystal manufacturer cuts the crystal so that the frequency of oscillation is correct when the crystal sees this load capacitance. Note that C_L refers to a capacitance seen across the crystal leads, meaning that for the circuit shown in Figure 51, C_L is the series combination of the two external capacitors ($C_{EXT}/2$) plus the equivalent board and device strays ($C_B/2 + C_D/2$). For example, if 10 pF external capacitors were used and parasitic capacitance is neglected, the crystal should be specified for a load capacitance of 5 pF. If the load capacitance deviates from this value due to the tolerance on the external capacitors or the presence of parasitic capacitance, the frequency also deviates. This change in frequency as a function of load capacitance is known as pullability, which is expressed in units of ppm/pF.

9 Crystal Oscillator Electrical Requirements and Characteristics (continued)

9.2 Frequency Accuracy Considerations (continued)

For small deviations of a few pF, pullability can be determined by the following equation.

$$\text{pullability(ppm/pF)} = \frac{(C_1)(10^6)}{2(C_O + C_L)^2}$$

where: C_O = parasitic capacitance of crystal
C_1 = motional capacitance of crystal (usually around 1 fF—25 fF, value can be obtained from crystal vendor)
C_L = total load capacitance seen by crystal

Note: For a given crystal, making C_L as large as possible can reduce pullability and improve frequency stability, while still maintaining sufficient negative resistance to ensure start-up according to the curves shown in Figures 49 and 50.

Because the exact values of the parasitic capacitance in a crystal-based oscillator system are unknown, the external capacitors are usually selected empirically to null out the frequency offset on a typical prototype board. Thus, if a crystal is specified to operate with a load capacitance of 15 pF, each external capacitor would have to be slightly less than 30 pF to account for parasitic capacitance. Suppose, for instance, that a crystal for which C_L = 15 pF is specified is plugged into the system and it is determined empirically that the best frequency accuracy occurs with C_{EXT} = 28 pF. This would mean that the equivalent board and device parasitic capacitance from each lead to ground would be 2 pF.

As an example, suppose it is desired to design a 4.096 MHz, 5.0 V system with ±100 ppm frequency accuracy. The parameters for a typical high-accuracy, custom, 4.096 MHz fundamental mode crystal are as follows:

Initial Tolerance	10 ppm
Temperature Tolerance	25 ppm
Aging Tolerance	6 ppm
Series Resistance	20 Ω max.
Motional Capacitance (C_1)	15 fF max.
Parasitic Capacitance (C_O)	7 pF max.

To ensure oscillator start-up, the negative resistance of the oscillator with load and parasitic capacitance must be at least twice the series resistance of the crystal, or 40 Ω. Interpolating from Figure 49 on page 129, external capacitors plus strays can be made as large as 30 pF while still achieving 40 Ω of negative resistance. Assume for this example that external capacitors are chosen so that the total load capacitance including strays is 30 pF per lead, or 40 pF total. Thus, a load capacitance, C_L = 15 pF would be specified to the crystal manufacturer.

From the preceding equation, the pullability would be calculated as follows:

$$\text{pullability (ppm/pF)} = \frac{(C_1)(10^6)}{2(C_O + C_L)^2} = \frac{(0.015)(10^6)}{2(7 + 15)^2} = 15.5 \text{ ppm/pF}$$

If 2% external capacitors are used, the frequency deviation due to this variation is equal to:

(0.02)(15 pF)(15.5 ppm/pF) = 4.7 ppm

Note: To simplify analysis, C_{EXT} is considered to be 40 pF. In practice, it would be slightly less than this value to account for strays. Also, temperature and aging tolerance on the capacitors has been neglected.

9 Crystal Oscillator Electrical Requirements and Characteristics (continued)

9.2 Frequency Accuracy Considerations (continued)

Typical capacitance variation of oscillator circuit in the *FlashDSP*1650 itself across process, temperature, and supply voltage is ±1 pF. Thus, the expected frequency variation due to the *FlashDSP*1650 is:

(1 pF)(3.4 ppm/pF) = 3.4 ppm

Other frequency accuracy considerations include the following:

- Approximate variation in parasitic capacitance of crystal = ±0.5 pF
- Frequency shift due to variation in C_O = (0.5 pF)(3.4 ppm/pF) = 1.7 ppm
- Approximate variation in parasitic capacitance of printed-circuit board = ±1.5 pF
- Frequency shift due to variation in board capacitance = (1.5 pF)(3.4 ppm/pF) = 5.1 ppm

Therefore, the contributions to frequency variation add up as follows:

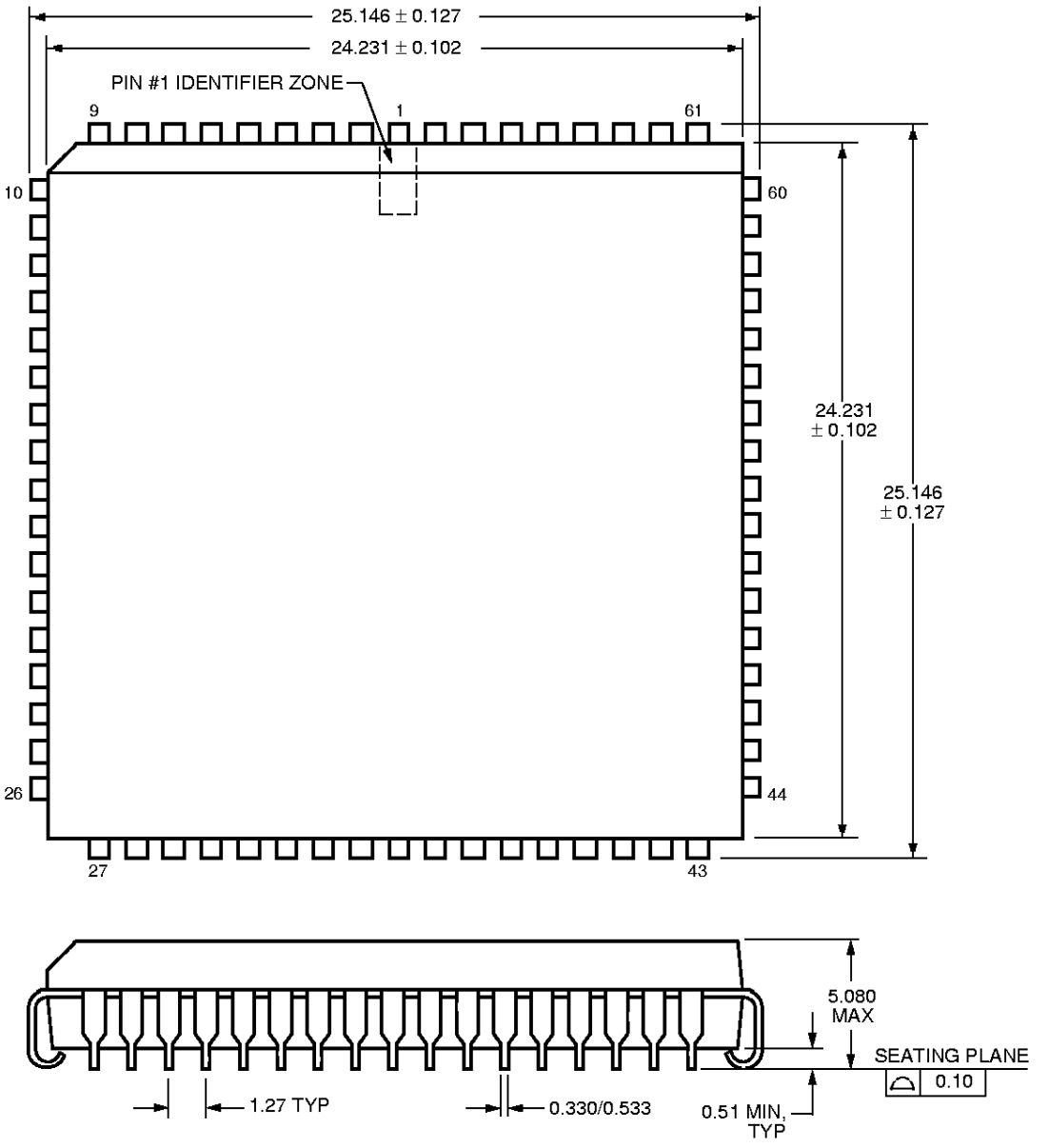
Initial Tolerance of Crystal =	10.0 ppm
Temperature Tolerance of Crystal =	25.0 ppm
Aging Tolerance of Crystal =	6.0 ppm
Load Capacitor Variation =	2.8 ppm
*FlashDSP*1650 Circuit Variation =	3.4 ppm
C_O Variation =	1.7 ppm
Board Variation =	5.1 ppm
Total =	54.0 ppm

This type of detailed analysis should be performed for any crystal-based application where frequency accuracy is critical.

10 Outline Diagrams

10.1 68-Pin PLCC Outline Diagram

Dimensions are in millimeters.



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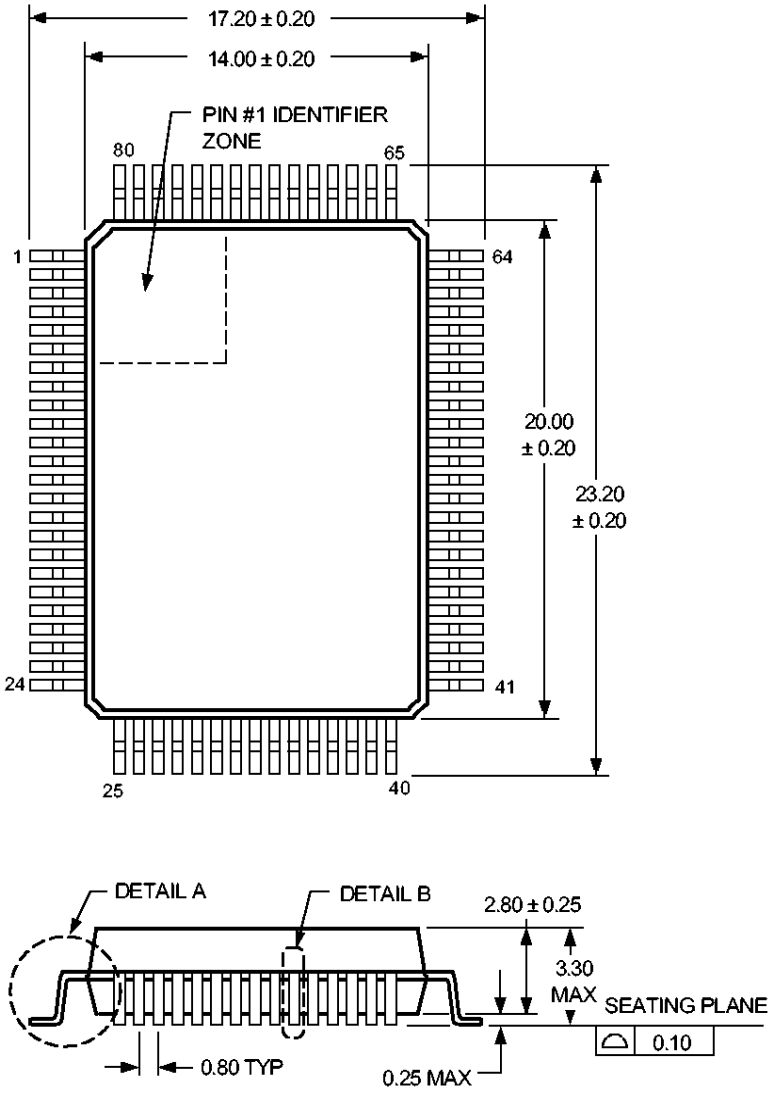
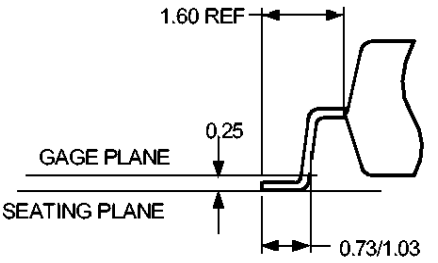
10 Outline Diagrams (continued)

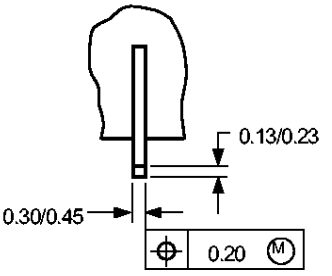
10.2 80-Pin MQFP Outline Diagram

Dimensions are in millimeters.





DETAIL A



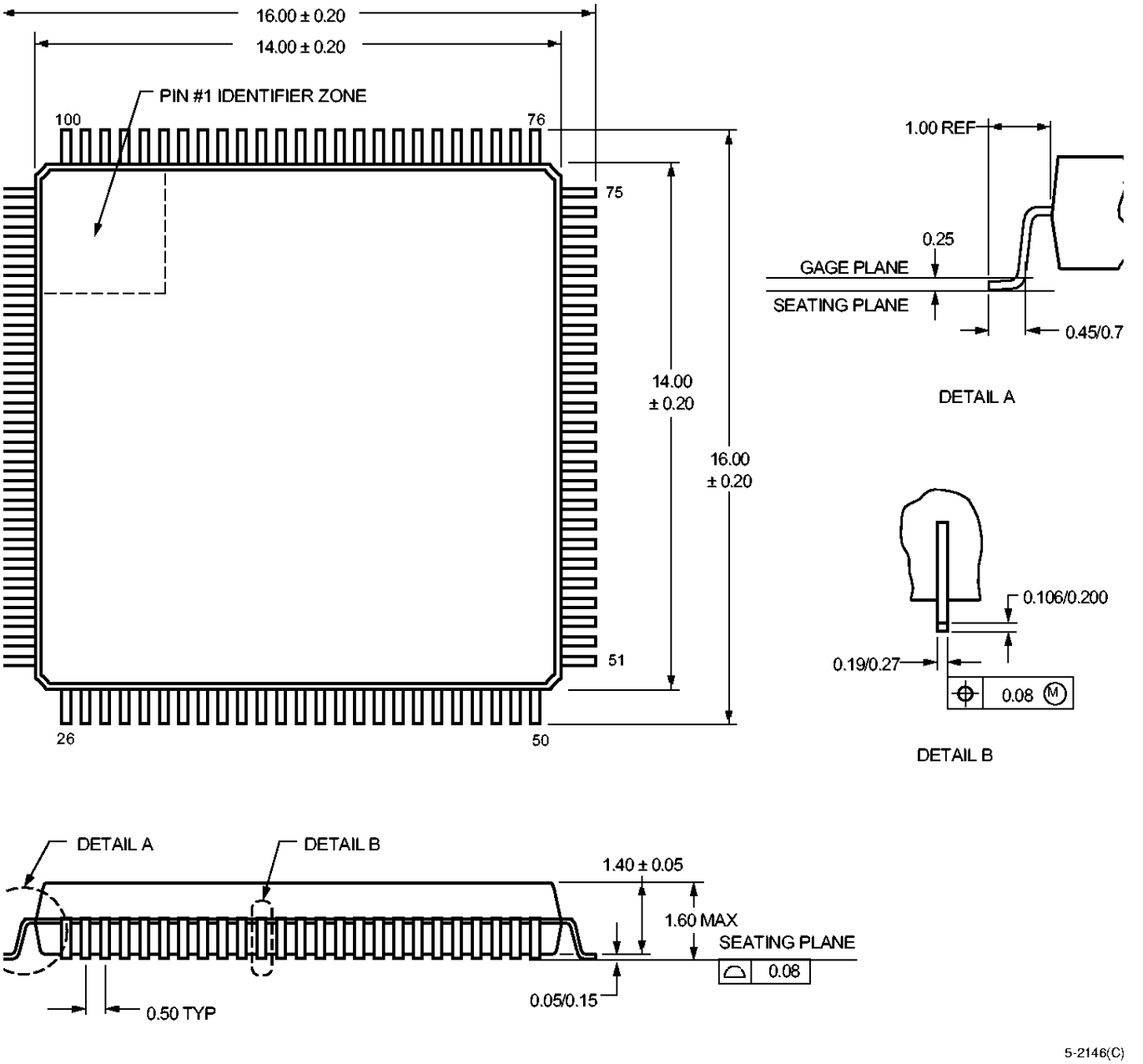
DETAIL B

5-2175(C)

10 Outline Diagrams (continued)

10.3 100-Pin TQFP Thin Quad Flat Pack

Dimensions are in millimeters.



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11 Ordering Information

This section describes DSP165X device coding and mask-programmable options.

11.1 Device Coding

Table 151 defines each DSP165X part number character.

Table 151. DSP165X Device Coding

Part Number Character Positions (Left to Right)							
1—4	5	6—7	8	9—10	11—12	13	14
165X Family	Package (J = MQFP T = TQFP)	ROM Size (Number of 16-bit Kwords)	Designator (H = HD, – or A = No Designation, F = Flash ROM)	ROM Code ID (AA—ZZ) or Flash Pinout Option (P0 = 1604/06, P1 = 1605)	Instruction Cycle Time (ns)	Temperature Class (– or Blank = Commercial, I = Industrial)	Supply Voltage [Blank (V_{DD} = 4.5 V to 5.5 V) or T (V_{DD} = 3.0 V to 3.6 V)]
1650	J or T	24	F	P0 or P1	25	– or Blank	Blank
					30	– or Blank	T
1651	J or T	4 (maximum)	H, –, or A	AA—ZZ	25	– or Blank	Blank
					30	I, –, or Blank	T
1652/ 1653	T	24 (maximum)	H or –	AA—ZZ	25	– or Blank	Blank
					30	I, –, or Blank	T

11.2 Mask-Programmable Options

The *FlashDSP*1650 contains a ROM which is mask-programmable (see Table 42 on page 59). Encoding a custom ROM selects the following programming options:

- The JTAG fields SLEWR, SECURE, BOPT, and ROMCODE.
- Power-Loss Control. Three power-loss control bits in **chipo**, PLC[0:2] are mask options for the DSP1651 and DSP1652/53 but are writable in the *FlashDSP*1650.
- ROM security. This option protects the internal ROM contents by not allowing access to the instruction/ coefficient memory map 3. Restricting access to memory map 3 makes it impossible to access IROM space when running from IRAM space.

For additional information, contact your Microelectronics Group Account Manager or the following:

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