DAC-UP10B
10-Bit Monolithic DAC
With Input Registers

FEATURES

- **Input registers**
- **10-Bit resolution**
- **Voltage output**
- **Internal reference**
- **Guaranteed monotonicity**

GENERAL DESCRIPTION

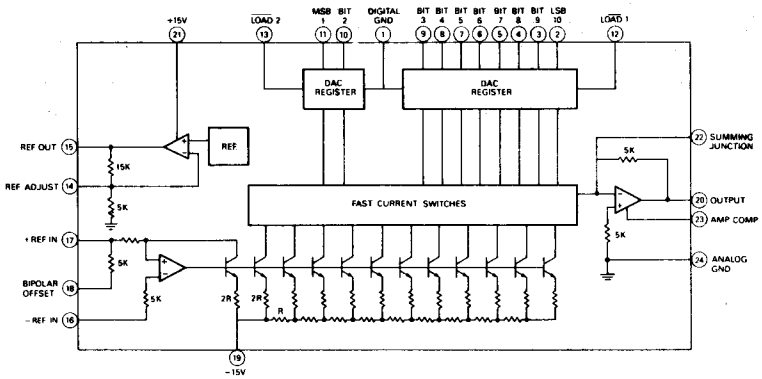
The DAC-UP10B is a low cost, monolithic 10-bit D/A converter with internal registers. The device also includes a high speed output amplifier, stable internal reference, and an input reference amplifier. Low loading latches, adjustable logic thresholds and addressing capability allow the DAC-UP10B to directly interface with many microprocessor and logic controlled systems.

The input registers are controlled by two enable lines ($\overline{\text{LOAD}}$ 1, $\overline{\text{LOAD}}$ 2). When the enable inputs are low, the registers are active, and any change on the digital inputs will be reflected on the analog output. When the enable inputs are high, the digital inputs become very high impedances and the data present is retained until the enable lines go low. The two enable inputs allow the converter to be directly interfaced with an 8-bit data bus.

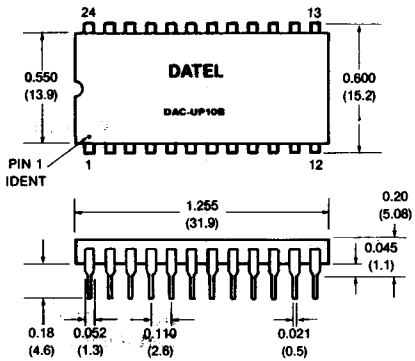
The output voltage range is 0 to +10V dc for unipolar mode, ±5V dc for bipolar. A full-scale output change settles to within 0.05% in 5 microseconds. The internal band gap reference is buffered and amplified to provide the 5V reference output. Either the internal reference or, for increased accuracy, an external reference can be used to bias the current switching networks.

Other characteristics of the DAC-UP10B include guaranteed monotonic performance, a Gain Temperature Coefficient of only 20 ppm/°C, and Zero Tempco of 5 ppm/°C. The power supply voltage range is ±11.4V dc to ±16.5V dc.

The DAC-UP10B is packaged in a 24-pin plastic DIP, and operation is specified over the 0 to +70°C operating temperature range.



MECHANICAL DIMENSIONS
INCHES (MM)



INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	DIG. GRND	13	$\overline{\text{LOAD}}$ 2
2	BIT 10 IN (LSB)	14	REF. ADJ
3	BIT 9 IN	15	REF. OUT
4	BIT 8 IN	16	- REF IN
5	BIT 7 IN	17	+ REF IN
6	BIT 6 IN	18	BIPOLAR OFF.
7	BIT 5 IN	19	- 15 VDC
8	BIT 4 IN	20	OUTPUT
9	BIT 3 IN	21	+ 15 VDC
10	BIT 2 IN	22	SUM. JUNC.
11	BIT 1 IN	23	AMP. COMP.
12	$\overline{\text{LOAD}}$ 1	24	ANALOG GRND.

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ABSOLUTE MAXIMUM RATINGS	
Positive Supply, Pin 21	+18V dc
Negative Supply, Pin 19	−18V dc
Digital Input Voltage, Pins 2-11	+18V dc
Reference Input, Pin 17	+12V dc
Summing Junction, Pin 22	+12V dc

FUNCTIONAL SPECIFICATIONS

Typical at +25°C, ±15V dc supplies, ref. in = +5V unless otherwise noted.

INPUTS	
Resolution	10 Bits
Coding, Unipolar	Straight Binary
Bipolar	Offset Binary
Input Logic Level,	
Bit ON ("1") min.[1]	+2V at 10 μA
Bit OFF ("0") max.[1]	+0.8V at 10 μA
Load Inputs	High ("1") = Hold Data
	Low ("0") = Transfer Data
Load Pulse Width, min.	150 nsec.
Reference Input Voltage	5V dc, ±10%
Reference Input Resistance	5 kΩ

OUTPUT	
Output Voltage Range, Unipolar	+10V dc
Bipolar	±5V dc
Output Current	5 mA
Reference Output Voltage[2]	5V ±10%
Reference Output Current, max.	3 mA

PERFORMANCE	
Linearity Error, max.	±1 LSB
Differential Linearity Error	±1 LSB
Monotonicity	Over Operating Temp. Range
Gain Error	Adjustable to Zero
Zero Error	Adjustable to Zero
Gain Tempco[3]	20 ppm/°C
Zero Tempco, Unipolar[3]	5 ppm/°C
Reference Tempco[2]	60 ppm/°C
Settling Time, 10V to 0.05%	5 μsec.
Power Supply Sensitivity, max.	±0.01% FS/%V_S

POWER REQUIREMENTS	
Rated Power Supply Voltage	±15V dc
Power Supply Voltage Range	±11.4V dc to ±16.5V dc
Supply Current, Quiescent max.[4]	+14 mA, −15 mA
Power Dissipation, max.[4]	435 mW

PHYSICAL/ENVIRONMENTAL	
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Package	24 Pin Plastic Dip

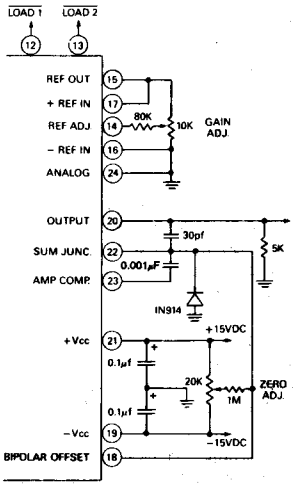
FOOTNOTES:

1. Bias circuits shown will provide the proper threshold voltage levels for various logic families. See technical note 3.
2. Ref. output current = 1 mA
3. Ref. in = +5V
4. V_S = ±15V dc, Iref = 1 mA

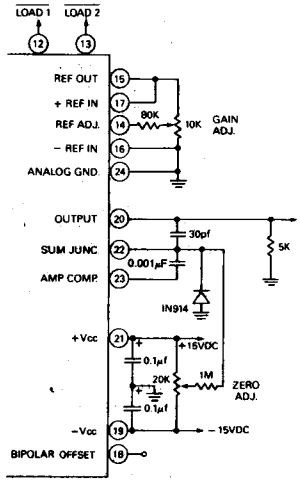
TECHNICAL NOTES

1. The Load control inputs (pins 12, 13) are level triggered inputs. The Load 2 input (pin 13) controls the two most significant bits while the Load 1 input (pin 12) controls the eight least significant bits. When the Load inputs are "Logic 1", the input registers will hold the data present, a "Logic 0", activates the registers, transferring data to the converter output.
2. A set-up time of 100 nanoseconds minimum must be allowed before the Load inputs go from low to high. In addition, a 50 nanosecond minimum Hold Time must be allowed for the input data after the Load inputs go from low to high. The minimum pulse width for the Load inputs is 150 nanoseconds. The maximum update rate is determined by the output settling time. See Timing Diagram.
3. The digital inputs of the DAC-UP10B utilize a differential logic system with a threshold level of +1.4 volts with respect to the voltage level on the digital ground pin (pin 1). Bias circuits are shown that will provide the proper threshold voltage levels for various logic families.
4. The −Ref input (pin 16) is uncommitted to allow utilization of negative polarity reference voltages. In this mode, the +Ref input (pin 17) is grounded and the negative reference is tied directly to the −Ref pin.
5. It is recommended that the ±15V power input pins both be bypassed to ground with 0.1 μF ceramic capacitors. Also, to minimize capacitance, external resistors should be mounted as close to the ref. adj. pin (pin 14) as possible. These precautions along with good layout practices will insure noise free operation.
6. The gain tempco of the DAC-UP10B without the internal reference is 20 ppm/°C. By using the internal reference, which has a tempco of 60 ppm/°C, a total tempco of 80 ppm/°C typical results for the converter. If greater temperature stability is required, a more stable external reference may be used.
7. The output amplifier incorporates output short circuit protection for both positive and negative excursions. Short circuit current is typically limited at ±15 mA.

CONNECTION AND CALIBRATION



BIPOLAR OPERATION

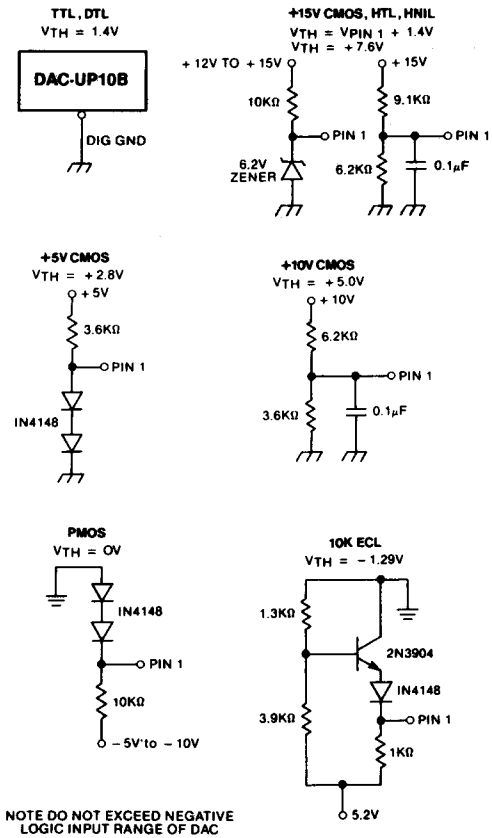


UNIPOLAR OPERATION

CALIBRATION PROCEDURE

1. Select the desired output range and connect as shown in OUTPUT RANGE SELECTION TABLE.
2. Apply Logic "0" to $\overline{\text{LOAD}}$ pins (pins 12, 13).
3. Zero and Offset Adjustments
   For unipolar operation, set all digital inputs to "0" and adjust ZERO ADJ potentiometer for zero output voltage. For bipolar operation, set all digital inputs to "0" and adjust ZERO ADJ potentiometer for negative full scale voltage of –5.000V.
4. GAIN ADJUSTMENT
   For either unipolar or bipolar operation, set all digital inputs to "1" and adjust GAIN ADJ potentiometer for the positive full scale voltage of +9.9902V (Unipolar) or +4.9902V (Bipolar).

LOGIC BIAS CIRCUITS



NOTE DO NOT EXCEED NEGATIVE LOGIC INPUT RANGE OF DAC

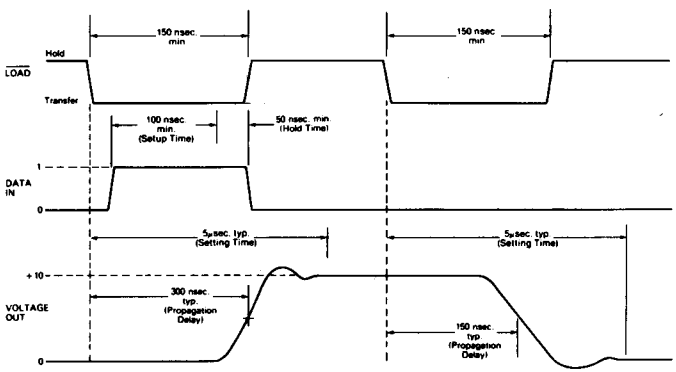
CODING TABLES

INPUT CODE			OUTPUT RANGES	
MSB		LSB	0 to +10V	±5V
1111	11	1111	+9.9902	+4.9902
1110	00	0000	+8.7500	+3.7500
1100	00	0000	+7.5000	+2.5000
1000	00	0000	+5.0000	0.0000
0100	00	0000	+2.5000	–2.5000
0010	00	0000	+1.2500	–3.7500
0000	00	0001	+0.0098	–4.9902
0000	00	0000	0.0000	–5.0000

OUTPUT RANGE SELECTION

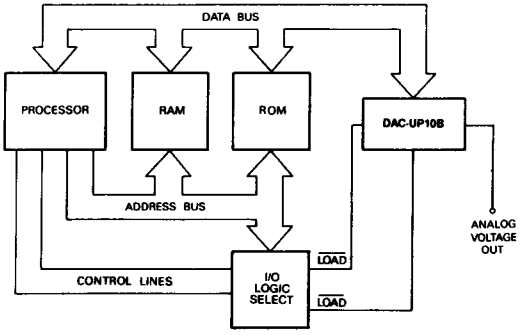
MODE	RANGE	CONNECTION
Unipolar	0 to ±10V	Pin 18 open
Bipolar	±5V	Pin 18 to Pin 20

TIMING DIAGRAM



APPLICATIONS

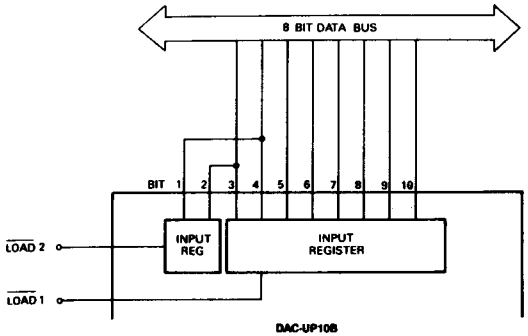
INTERFACING TO A μPROCESSOR



APPLICATIONS
Programmable Power Supplies
Test Equipment
Process and Control
Measurement Instruments
Computer I/O Equipment

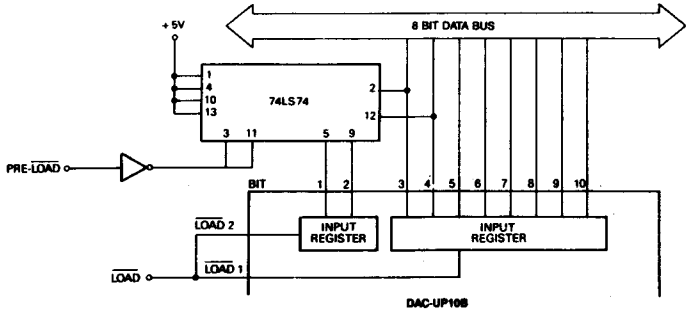
2

INTERFACING TO 8 BIT DATA BUS



NOTE:
The independent $\overline{\text{LOAD}}$ lines allow the DAC-UP10B to be directly interfaced with an 8-bit data bus. Data for the two MSB's is supplied and stored when $\overline{\text{LOAD}}$ 2 is activated low and returned high according to the DAC-UP10B timing requirements. Then $\overline{\text{LOAD}}$ 1 is activated low and the remaining eight LSB's of data are transferred into the DAC-UP10B. When $\overline{\text{LOAD}}$ 1 returns high, the loading of a ten bit data word from an eight bit data bus is complete.

PRELOADING 2 MSB'S TO PROVIDE SINGLE STEP OUTPUT



NOTE:

Occasionally the analog output must change to its data value within one data address operation. This is no problem when using the DAC-UP10B with a data bus with 10 or more data bits. It can be accomplished from an 8-bit data bus by utilizing an external latch circuit to preload the two MSB data values. After preloading the external latch with the two MSB values, the DAC-UP10B $\overline{\text{LOAD}}$ inputs are activated low and the eight LSB's and two MSB's are concurrently loaded into the DAC-UP10B in one operation.

ORDERING INFORMATION

MODEL NO.	OPERATING TEMP. RANGE
DAC-UP10BC	0 to +70°C

ACCESSORIES

Part Number	Description
TP10K, TP20K	Trimming Potentiometers