

2013

RENICE X5 mSATA SSD DATA SHEET



Renice Technology Co., Limited

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Revision History

| Revision | Description | Date |
|----------|--|------------|
| 1.0 | Formal Release | 04/10/2013 |
| 1.1 | Adding Power Failure Protection Function | 07/16/2013 |
| 1.2 | Adding Security Function and Write Protection Function | 08/02/2013 |
| 1.3 | Security Function modification | 12/22/2013 |
| 1.4 | Add RoHS and REACH compliant | 03/03/2014 |

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1. Introduction

1.1 Product Overview

Renice X5 50mm mSATA SSD is a compact SSD with Mini PCIe form factor and SATA 3.0Gb/s interface. By using MLC or SLC NAND flashes as storage media, it delivers high performance and reliability working in harsh environments like wide temperature, shock, vibration, dust, etc. Being fully compliant with JEDEC MO-300 industrial standard, X5 mSATA can be widely adopted in various embedded applications.

1.2 Features

- Performance:

 - Host Transfer Rate: 300MB/s

 - Max Sequential Data Read/Write: 240MB/145MB/s (MLC)
240MB/180MB/s (SLC)

- Form factor: 50.95mm X 30mm X 3.65mm (LxWxH)
- Weight: <10g
- Interface standard: mSATA SATAII 3.0Gb/s
- Density: 8GB~256GB (MLC) 2GB~64GB(SLC)
- Input voltage: 3.3V (±5%)
- Standard operating temperature range from 0 to +70°C
Industrial operating temperature range from -40 to +85°C
- Storage temperature range from -55 to +95°C
- Flash management algorithm: static and dynamic wear-leveling, bad block management algorithm
- Support dynamic power management and SMART (Self-Monitoring, Analysis and Reporting Technology)
- Support hardware BCH ECC engine: 72-bit per 1 KB
- Support TRIM (requires OS support)
- Data retention: 10 years @25C
- MTBF: >3,000,000 Hours @25C (Telcordia SR-332 standard)
- RoHS and REACH compliant

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2. Functional Block Diagram

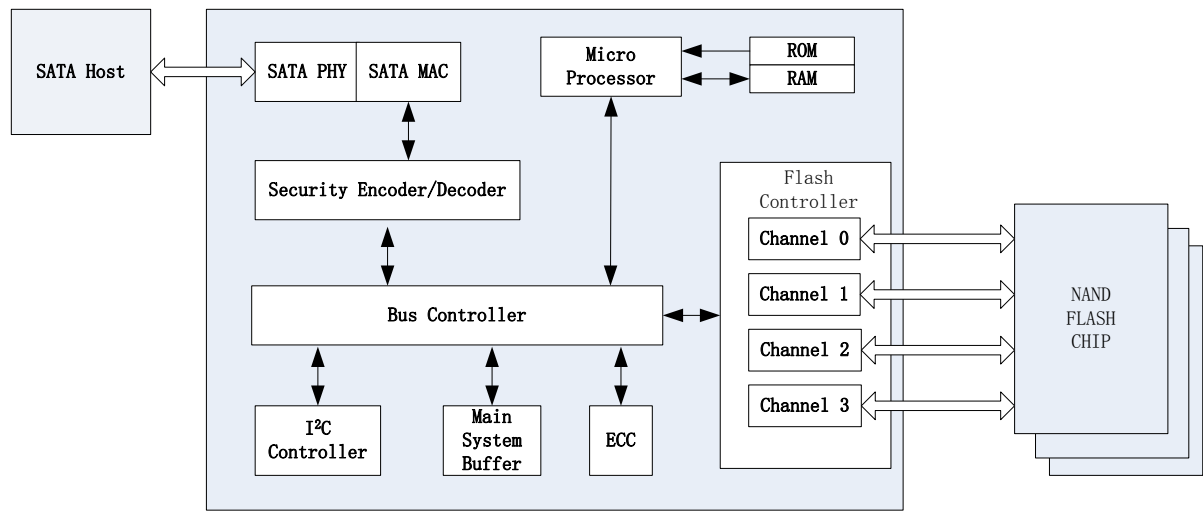


Figure 1: Functional Block Diagram

3. Physical Specification

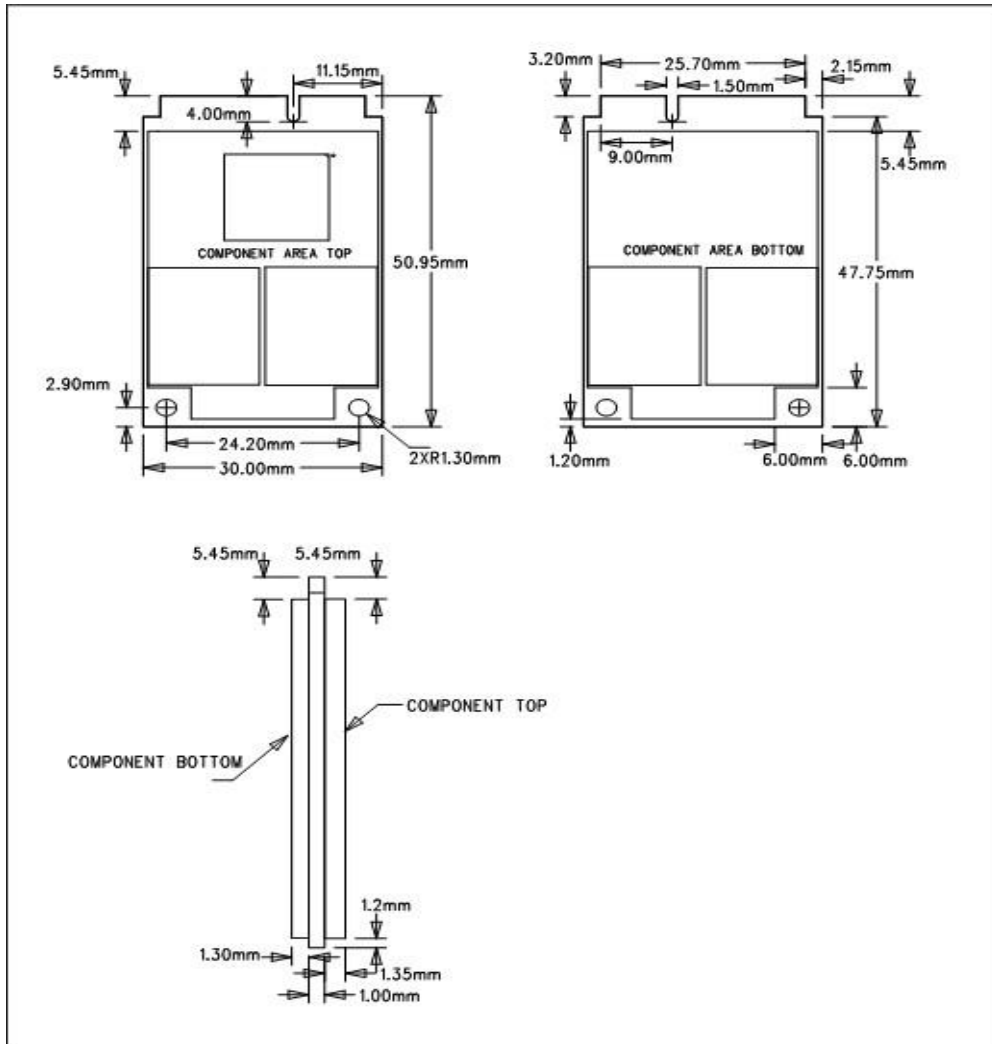


Figure 2: Mechanical Drawing

4. Host Interface

- Seamless SATA interoperability
- Plug-and-play field-proven SATA-v2.6-compliant interface
- 3 Gbps / 1.5 Gbps signaling (auto-negotiated)
- S.M.A.R.T. command transport (SCT) technology

5. Pin out Information

5.1 Pin Assignment

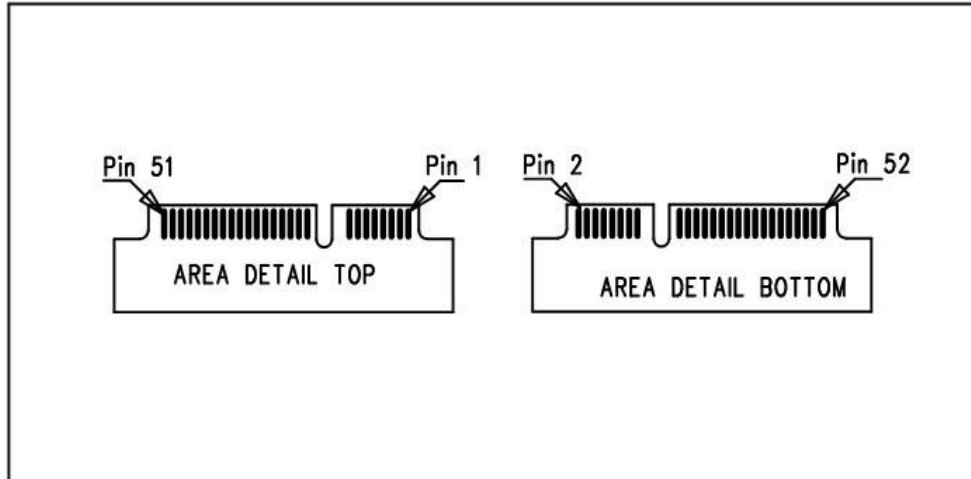


Figure 3: Pin Assignment

5.2 Connector Pin Signal Definitions

Table 1: Connector Pin Signal Definitions

| Pin | Definitions | Pin | Definitions |
|-----|------------------------------------|-----|-------------|
| P1 | NC | P2 | +3.3V |
| P3 | NC | P4 | GND |
| P5 | NC | P6 | NC |
| P7 | NC | P8 | NC |
| P9 | GND | P10 | NC |
| P11 | NC | P12 | NC |
| P13 | NC | P14 | NC |
| P15 | GND | P16 | NC |
| P17 | NC | P18 | GND |
| P19 | NC | P20 | NC |
| P21 | GND | P22 | NC |
| P23 | SATA Differential TX+ based on SSD | P24 | +3.3V |
| P25 | SATA Differential TX- based on SSD | P26 | GND |
| P27 | GND | P28 | NC |
| P29 | GND | P30 | NC |
| P31 | SATA Differential RX- based on SSD | P32 | NC |
| P33 | SATA Differential RX+ based on SSD | P34 | GND |
| P35 | GND | P36 | NC |
| P37 | GND | P38 | NC |
| P39 | +3.3V | P40 | GND |
| P41 | +3.3V | P42 | NC |
| P43 | GND | P44 | NC |
| P45 | Vendor | P46 | NC |
| P47 | Vendor | P48 | NC |
| P49 | DAS/DSS | P50 | GND |
| P51 | Presence Detection | P52 | +3.3V |

6. Power Specifications

6.1 Operating voltage

3.3V ($\pm 5\%$)

6.2 Power Supply voltage

1.2v for Core, 3.3V /1.8V for NAND and Core

6.3 Power Consumption (typical)

Operation (Read/Write) – (1.02W/1.1W)

Idle – 0.5W

7. Reliability Specification

Table 2: Reliability Specification

| Item | Features | |
|-------------|--|-----------------------|
| Temperature | Operation | Standard: 0~70°C |
| | | Industrial: -40~+85°C |
| | Storage | -55~+95°C |
| Humidity | 5-95% | |
| Vibration | 10Hz-2000Hz, 16.4 G (X, Y, Z axis, 1 hour /axis) | |
| Shock | Peak Acceleration: 1,500 G, 0.5ms(Half-sine wave, $\pm X, \pm Y, \pm Z$ axis, 1 time/axis) | |
| | Peak Acceleration: 50 G, 11ms(Half-sine wave, $\pm X, \pm Y, \pm Z$ axis, 3 times/axis) | |

7.1 Wear-leveling

Renice X5 mSATA SSD supports both static and dynamic wear-leveling, these two algorithms guarantee all type of flash memory at same level of erase cycles to improve lifetime limitation of NAND based storage.

7.2 H/W ECC and EDC for NAND Flash

Supports hardware BCH ECC engine: 72-bit per 1 KB

7.3 Power Failure Protection

Renice X5 mSATA SSD adopts Voltage Detector Circuit to detect current voltage status, when current voltage is detected abnormal, the power failure protection function of X5 SSD will work to prevent data crash or drive corruption in case of sudden power failure.

7.4 Over voltage and inrush current protection

The over voltage and inrush current protection mechanism of Renice X5 mSATA SSD is designed to be a protect circuitry on Device Power In.

Once the current or voltage is exceeded, it will be pull down to the normal value in very short time to protect the drive.

8. Command Set

Renice X5 mSATA SSD supports the commands as shown in the following table

Table 3: Command Set List

| Command | Code | Protocol |
|-------------------------------------|------------|-------------------|
| General Feature Set | | |
| Execute Drive Diagnostic | 90h | Device diagnostic |
| Flush Cache | E7h | Non-data |
| Identify Device | ECh | PIO data-in |
| Read DMA | C8h | DMA |
| Read Multiple | C4h | PIO data-in |
| Read Sector(s) | 20h | PIO data-in |
| Read Verify Sector(s) | 40h or 41h | Non-data |
| Set Feature | Efh | Non-data |
| Set Multiple Mode | C6h | Non-data |
| Write DMA | Cah | DMA |
| Write Multiple | C5h | PIO data-out |
| Write Sector(s) | 30h | PIO data-out |
| NOP | 00h | Non-data |
| Read Buffer | E4h | PIO data-in |
| Write Buffer | E8h | PIO data-out |
| Power Management Feature Set | | |
| Check Power Mode | E5h or 98h | Non-data |
| Idle | E3h or 97h | Non-data |
| Idle Immediate | E1h or 95h | Non-data |
| Sleep | E6h or 99h | Non-data |

| Command | Code | Protocol |
|--|-------------|-----------------|
| Standby | E2h or 96h | Non-data |
| Standby Immediate | E0h or 94h | Non-data |
| Security Mode Feature Set | | |
| Security Set Password | F1h | PIO data-out |
| Security Unlock | F2h | PIO data-out |
| Security Erase Prepare | F3h | Non-data |
| Security Erase Unit | F4h | PIO data-out |
| Security Freeze Lock | F5h | Non-data |
| Security Disable Password | F6h | PIO data-out |
| SMART Feature Set | | |
| SMART Disable Operations | B0h | Non-data |
| SMART Enable/Disable Auto save | B0h | Non-data |
| SMART Enable Operations | B0h | Non-data |
| SMART Return Status | B0h | Non-data |
| SMART Execute Off-Line Immediate | B0h | Non-data |
| SMART Read Data | B0h | PIO data-in |
| Host Protected Area Feature Set | | |
| Read Native Max Address | F8h | Non-data |
| Set Max Address | F9h | Non-data |
| Set Max Set Password | F9h | PIO data-out |
| Set Max Lock | F9h | Non-data |
| Set Max Freeze Lock | F9h | Non-data |
| Set Max Unlock | F9h | PIO data-out |
| 48-bit Address Feature Set | | |
| Flush Cache Ext | Eah | Non-data |
| Read Sector(s) Ext | 24h | PIO data-in |
| Read DMA Ext | 25h | DMA |
| Read Multiple Ext | 29h | PIO data-in |
| Read Native Max Address Ext | 27h | Non-data |
| Read Verify Sector(s) Ext | 42h | Non-data |
| Set Max Address Ext | 37h | Non-data |
| Write DMA Ext | 35h | DMA |
| Write DMA FUA Ext | 3Dh | DMA |
| Write Multiple Ext | 39h | PIO data-out |
| Write Multiple FUA Ext | Ceh | PIO data-out |
| Write Sector(s) Ext | 34h | PIO data-out |

8.1 IDENTIFY DEVICE

The IDENTIFY DEVICE command enables the host to receive parameter information from the device. The following table gives the definition and value of each field in the Identify Device Information.

Table 4: Identify Device Parameters

| Word | F / V | Default Value | Data Field Type Information |
|---------|-------|---------------|---|
| 0 | F | 044Ah | General configuration |
| 1 | X | XXXXh | Default number of cylinders |
| 2 | V | 0000h | Reserved |
| 3 | X | 00XXh | Default number of heads |
| 4 | X | 0000h | Obsolete |
| 5 | X | 0240h | Obsolete |
| 6 | F | XXXXh | Default number of sectors per track |
| 7 – 8 | V | XXXXh | Number of sectors per card (Word 7= MSW, Word 8 = LSW) |
| 9 | X | 0000h | Obsolete |
| 10 – 19 | F | XXXXh | Serial number in ASCII (Right justified) |
| 20 | X | 0002h | Obsolete |
| 21 | X | 0002h | Obsolete |
| 22 | X | 0000h | Obsolete |
| 23 – 26 | F | XXXXh | Firmware revision in ASCII. Big Endian Byte Order in Word. |
| 27 – 46 | F | XXXXh | Model number in ASCII (Left justified).Big Endian Byte Order in Word. |
| 47 | F | 8001h | Maximum number of sectors on Read/Write Multiple command |
| 48 | F | 0000h | Reserved |
| 49 | F | 0F00h | Capabilities |
| 50 | F | 4000h | Capabilities |
| 51 | F | 0200h | PIO data transfer cycle timing mode |
| 52 | X | 0000h | Obsolete |
| 53 | F | 0007h | Field validity |
| 54 | X | XXXXh | Current numbers of cylinders |
| 55 | X | XXXXh | Current numbers of heads |

| Word | F / V | Default Value | Data Field Type Information |
|---------|-------|---------------|---|
| 56 | X | XXXXh | Current sectors per track |
| 57 – 58 | X | XXXXh | Current capacity in sectors (LBAs)(Word 57 = LSW , Word 58 = MSW) |
| 59 | F | 0100h | Multiple sector setting |
| 60 – 61 | F | XXXXh | Total number of sectors addressable in LBA Mode |
| 62 | X | 0000h | Reserved |
| 63 | F | 0007h | Multiword DMA transfer Supports MDMA Mode 0, 1 and 2 |
| 64 | F | 0003h | Advanced PIO modes supported |
| 65 | F | 0078h | Minimum Multiword DMA transfer cycle time per word |
| 66 | F | 0078h | Recommended Multiword DMA transfer cycle time |
| 67 | F | 0078h | Minimum PIO transfer cycle time without flow control |
| 68 | F | 0078h | Minimum PIO transfer cycle time with IORDY flow control |
| 69 – 74 | F | 0000h | Reserved |
| 75 | F | 001Fh | Queue depth |
| 76 | F | 0006h | Serial ATA capabilities Supports Serial ATA Gen1 Supports Serial ATA Gen2 |
| | F | 0206h | • Supports receipt of host-initiated interface power management requests |
| 77 | V | 0000h | Reserved |
| 78 | F | 0008h | Device supports initiating interface power management |
| 79 | V | 0000h | Reserved |
| 80 | F | 0080h | Major version number (ATAPI-7) |
| 81 | F | 0000h | Minor version number |
| 82 | F | 742Bh | Command sets supported 0 |
| 83 | F | 5500h | Command sets supported 1 |
| 84 | F | 4002h | Command sets supported 2 |
| 85 – 87 | V | XXXXh | Command set/feature enabled |
| 88 | V | 007Fh | Ultra DMA mode supported and selected |

| Word | F / V | Default Value | Data Field Type Information |
|-----------|-------|---------------|---|
| 89 | F | 0003h | Time required for Security erase unit completion |
| 90 | F | 0000h | Time required for Enhanced security erase unit completion |
| 91 | V | 0000h | Current Advanced power management value |
| 92 | V | FFFEh | Master Password Revision Code |
| 93 – 99 | V | 0000h | Reserved |
| 100 – 103 | V | XXXXh | Maximum user LBA for 48-bit Address feature set |
| 104 – 127 | V | 0000h | Reserved |
| 128 | V | 0001h | Security status |
| 129 – 159 | X | 0000h | Vendor unique bytes |
| 160 | F | 0000h | Power requirement description |
| 161 | X | 0000h | Reserved |
| 162 | F | 0000h | Key management schemes supported |
| 163 | F | 0000h | CF Advanced True IDE Timing Mode Capability and Setting |
| 164 – 216 | V | 0000h | Reserved |
| 217 | F | 0100h | Non-rotating media (SSD) |
| 218 – 255 | X | 0000h | Reserved |

Notes:

- 1.F = content (byte) is fixed and does not change.
- 2.V = content (byte) is variable and may change depending on the state of the device or the commands executed by the device.
- 3.X = content (byte) is vendor specific and may be fixed or variable

9. SMART

Table 5: SMART Command Set

| Value | Command | Value | Command |
|-------|----------------------------|-------|--------------------------|
| D0 | Read Data | D5h | Reserved |
| D1 | Read Attribute Threshold | D6h | Reserved |
| D2 | Enable/Disable Autosave | D8h | Enable SMART Operations |
| D3 | Save Attribute Values | D9h | Disable SMART Operations |
| D4 | Execute OFF-LINE Immediate | Dah | Return Status |

Table 6: SMART Attribute Data Structure

The following 512 bytes make up the device SMART data structure. Users can obtain the data using the “Read Data” command (D0h)

| By | F / V | Description |
|-------------|-------|---|
| 0 | X | Revision code |
| 2 – 361 | X | Vendor specific |
| 3 | V | Off-line data collection status |
| 3 | X | Self-test execution status byte |
| 364 – 365 | V | Total time in seconds to complete off-line data collection activity |
| 3 | X | Vendor specific |
| 3 | F | Off-line data collection capability |
| 368 – 369 | F | SMART capability |
| 3 7 0 | F | Error logging capability • 7-1 Reserved • 0 1 = Device error logging supported |
| 3 | X | Vendor specific |
| 3 | F | Short self-test routine recommended polling time (in minutes) |
| 3 | F | Extended self-test routine recommended polling time (in minutes) |
| 3 | F | Conveyance self-test routine recommended polling time (in minutes) |
| 375 – 385 | R | Reserved |
| 386 – 395 | F | Firmware Version/Date Code |
| 396 – 397 | F | Number of initial invalid block(396= MSB, 397 = LSB) |
| 398 – 399 | F | Reserved |
| 400 – 406 | F | ‘SMI2250’ |
| 407 – 415 | X | Vendor specific |
| 4 | F | Reserved |
| 4 | F | Program/write the strong page only |
| 418 – 419 | V | Number of spare block |
| 420 – 445 | F | Reserved |
| 446 – 510 | X | Vendor specific |
| 5 | V | Data structure checksum |

Notes:

- 1.F = content (byte) is fixed and does not change.
- 2.V = content (byte) is variable and may change depending on the state of the device or the commands executed by the device.
- 3.X = content (byte) is vendor specific and may be fixed or variable.
- 4.R = content (byte) is reserved and shall be zero.

10. Security Function (Optional)

Renice X5 mSATA SSD can support Secure Erase function with a Hardware Key* for emergency data erasure based on customers' request. Secure Erase can be triggered by pressing the Secure Erase Key. The process of erasure will not be stopped until finished, even if power failure happens, it will be continued when power is back on.

No matter Renice X5 mSATA SSD is acting as master Drive or slave drive, once the Secure Erase function is triggered, SE will be carried out immediately whether the SSD is in idle mode(no read/write) , or work (read/write) mode. After SE is finished, the SSD gets to be uninitialized drive and can be used again after formatting.

Hardware key*: The X5 mSATA SSD is designed with SE jumper connector, the client is requested to connect an external hardware touch switch/button to trigger the SE function.

10.1 Technical Concept

SE is implemented by GPIO P10 of Controller Chip. SE could be triggered by pulling P10 down for 3 seconds, whether through H/W (Usually an external button) or S/W. Then Controller will send Delete Command to NAND Flash to start SE.

a. Trigger Time: 0~3 seconds

Controller will take it as mis-operation and no SE command will be sent.

b. Trigger Time: 3~10 seconds

All data on board will be deleted and data of FF pattern will be written in.

c. Trigger Time:10 seconds or above

Besides data, SSD firmware will be deleted.

If Power-Down or other operations breaking the SE occur during SE, Delete Command will be interrupted. Under such circumstance, Firmware records current Delete position and pause deletion. Once power supply gets normal, SE command will continue execution with highest priority.

10.2 SE Type

The specific SE type of X5 mSATA SSD is similar to NTISSP-9 which is one SE standard commonly seen from SSD solutions on market, however X5 only executes the SE command for

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one time. **(Note: The SE function of Renice X5 solution could be customized based on clients' standard.)**

X5 SE is done by 2 steps, Erase and Write.

1. Erase: Every memory block on the board is erased;
2. Write: Every Memory Chips location is recorded with a pattern FF.

So if clients need other types of SE, please forward us specific standards. And our R&D will figure out the availability.

10.3 Time taken for SE

Scenario 1: only Mapping Table deleted. Data on disk could be recovered maliciously.

Around 5 seconds

Scenario 2: Both Mapping Table and memory storage blocks are deleted. And disk will be written in fully with data of meaningless pattern.

Theoretical formula for Scenario 2:

e.g. Micron MT29F64G08CBABA NAND flash.

8GB=4096 BLOCK;

Each Block Erase needs 3ms based on Flash Data Sheet

Controller Used 2 plan and Interleave mode to scan the data;

Time= $4096 * 3ms / 2 / 1.5 = 4$ Seconds

Plan: the same meaning with Channel for the Data transmission;

Interleave: used for enhance the Data transmission speed In One Channel; Interleave value depends on NAND deployed, which is usually between 1.0 and 2.0. In our example we use 1.5 as a convenient median.

11. Write Protection Function(Optional)

Renice X5 mSATA SSD can support write protection function based on customers' request with a Hardware Button*. Write protection can be enabled by operating the Write Protection button. Once write protect function triggered, the whole disk could be for read only, in that case, no more data could be written into the disk to avoid the virus infection.

Hardware Button*: Renice X5 mSATA SSD is designed with Write Protection jumper connector, the client is requested to connect an external hardware touch switch/button to operate the Write Protection function.

12. Ordering Information

| Capacities/Flash type | Standard Temp | Industrial Temp |
|-----------------------|---------------|-----------------|
| 2GB/ SLC | RCS002-SX5M | RIS002-SX5M |
| 4GB/ SLC | RCS004-SX5M | RIS004-SX5M |
| 8GB/ SLC | RCS008-SX5M | RIS008-SX5M |
| 16GB/ SLC | RCS016-SX5M | RIS016-SX5M |
| 32GB/ SLC | RCS032-SX5M | RIS032-SX5M |
| 64GB/ SLC | RCS064-SX5M | RIS064-SX5M |
| 8GB/ MLC | RCM008-SX5M | RIM008-SX5M |
| 16GB/ MLC | RCM016-SX5M | RIM016-SX5M |
| 32GB/ MLC | RCM032-SX5M | RIM032-SX5M |
| 64GB/ MLC | RCM064-SX5M | RIM064-SX5M |
| 128GB/ MLC | RCM128-SX5M | RIM128-SX5M |
| 256GB/ MLC | RCM256-SX5M | RIM256-SX5M |

13. Product Part Number Naming Rule

