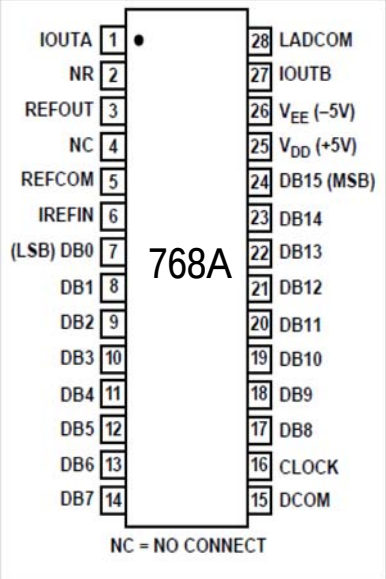
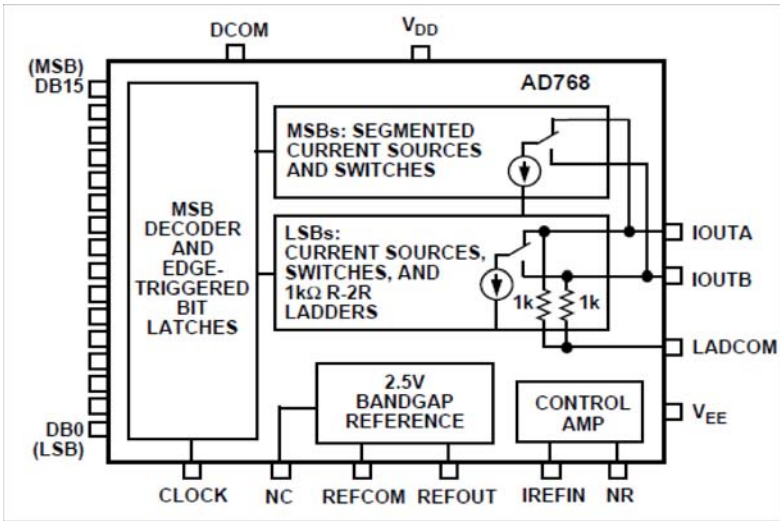
768A
16-BIT, 30 MSPS DIGITAL-TO-ANALOG CONVERTER





Functional Block Diagram

FEATURES:

- Total dose hardness:
  > 100 krad (Si), depending upon space mission

Excellent Single Event Effects
  - Immune to SEL LET > 83MeV-cm^2/mg at 125C
- 30 MSPS Update Rate
- 16-Bit Resolution
- Linearity: 1/2 LSB DNL at 14 Bits
  1/2 LSB INL at 14 Bits
- Fast Settling: 25ns Full-scale Settling to 0.025%
- SFDR at 1 MHz Output: 86 dBc
- THD at 1 MHZ Output: 71 dBc
- Low Glitch Impulse: 35 pV-s
- Power Dissipation: 465 mW
- On-chip Reference: 2.5 V

DESCRIPTION:

Maxwell Technologies' 768A 16-Bit DAC microcircuit features a greater than 100 krad (Si) total dose tolerance, depending upon space mission.

The 768A is manufactured on an Advance Bipolar process, combining the speed of bipolar transistors, the accuracy of laser-trimmable thin film resistors, and the efficencyof CMOS logic.

This product is available with screening up to Maxwell Technologies' Self-Defined Class S.

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TABLE 1. PINOUT DESCRIPTION

PIN	SYMBOL	DESCRIPTION
1	IOUTA	DAC Current Output. Full-scale current when all data bits are 1.
2	NR	Noise Reduction Node. add capacitor for noise reduction.
3	REFOUT	Reference Output Voltage. Nominal value is 2.5V.
4	NC	No Connection. Reserved for internal use.
5	REFCOM	Reference Ground.
6	$\overline{\text{IREFIN}}$	Reference Input Current. Nominal is 5 mA. DAC full-scale is 4X this current.
7	DB0	Data Bit 0
8	DB1	Data Bit 1
9	DB2	Data Bit 2
10	DB3	Data Bit 3
11	DB4	Data Bit 4
12	DB5	Data Bit 5
13	DB6	Data Bit 6
14	DB7	Data Bit 7
15	DCOM	Digital Ground.
16	CLOCK	Clock Input. Data latched on positive edge of clock.
17	DB8	Data Bit 8
18	DB9	Data Bit 9
19	DB10	Data Bit 10
20	DB11	Data Bit 11
21	DB12	Data Bit 12
22	DB13	Data Bit 13
23	DB14	Data Bit 14
24	DB15	Data Bit 15
25	V_{DD}	Positive Supply Voltage. Nominasl is +5V.
26	V_{EE}	Negative Supply Voltage. Nominasl is -5V
27	IOUTB	Complementary DAC Current Output. Full-scale current when all data bits are 0s.
28	LADCOM	DAC Ladder Common.

TABLE 2. 768A ABSOLUTE MAXIMUM RATINGS [1]

PARAMETER	MIN	MAX	UNIT
Positive Supply Voltage (V_{DD})	-0.5	+6.0	V
Negative Supply Voltage(V_{EE})	-6.0	+0.5	V
Analog Ground to Other Grounds (REFCOM)	-0.5	+0.5	V
Digital Ground to Other Grounds (DCOM)	-0.5	+0.5	V
Reference Output (REFOUT)	--	V_{DD} + 0.5	V
Reference Input Current (IREFIN)	--	+7.5	mA
Digital Inputs (DB0 - DB15, CLOCK)	-0.5	V_{DD} + 0.5	V
Analog Outputs (IOUTA, IOUTB)	-2.0	+5.0	V
Weight	--	2	grams
Thermal Resistance (Tjc)	--	12.5	°C/W
MAX Junction Temperature	--	+150	°C
Operating Temperature	-55	+85	°C
Storage Tempurature	-65	+150	°C

1. Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

TABLE 3. DELTA LIMITS[1]

PARAMETER	VARIATION
I_{DD}	±10% of specified value in Table 4
I_{EE}	±10% of specified value in Table 4
Vref	±10 mV

1) Parameters are measured and recorded as Deltas per MIL-STD-883 for Class S Devices

TABLE 4. 768A ELECTRICAL SPECIFICATIONS

(T_{MIN} TO T_{MAX}, V_{DD} = +5.0V +/- 5%, V_{EE} = -5.0V +/- 5%, LADCOM, REFCOM, DCOM = 0V, IREFIN = 5MA, CLOCK = 10MHZ, UNLESS OTHERWISE NOTED)

PARAMETER	SUBGROUPS	MIN	TYP	MAX	UNITS
RESOLUTION[1]	1, 2, 3	16	--	--	Bits
DC ACCURACY[1]					
Linearity Error TA = 25°C TMIN to TMAX	 1 2, 3	 -8 -8	 ±4 --	 +8 +8	LSB

TABLE 4. 768A ELECTRICAL SPECIFICATIONS

(T_{MIN} TO T_{MAX}, V_{DD} = +5.0V +/- 5%, V_{EE} = -5.0V +/- 5%, LADCOM, REFCOM, DCOM = 0V, IREFIN = 5MA, CLOCK = 10MHZ, UNLESS OTHERWISE NOTED)

PARAMETER	SUBGROUPS	MIN	TYP	MAX	UNITS
Differential Non-Linearity TA = 25°C TMIN to TMAX	 1 2, 3	 -6 -8	 ±2 --	 +6 +8	LSB
Monotonicity	Guarenteed over Specified Temp Range				
ANALOG OUTPUT					
Offset Error	1, 2, 3	-0.2	--	+0.2	% of FSR
Gain Error	1, 2, 3	-1.0	--	+1.0	% of FSR
Full-scale Output Current[2]	1, 2, 3	--	20	--	mA
Output Compliance Range	1, 2, 3	-1.2	--	+5.0	V
Output Resistance	1, 2, 3	0.8	1.0	1.2	kΩ
Output Capacitance	1, 2, 3	--	3	--	pF
REFERNCE OUTPUT					
Reference Voltage (Vref)	1, 2, 3	2.475	2.5	2.525	V
Reference Output Current[3, 7]	1, 2, 3	--	+5.0	+15	mA
REFERNCE INPUT					
Reference Input Current	1, 2, 3	1	5	7	mA
Reference Bandwidth[4] Small Signal, IREF = 5mA ± 0.1mA Large Signal, IREF= 4 mA ± 2mA	1, 2, 3 	 -- --	 28 9	 -- --	MHz
TEMPERATURE COEFFICIENTS[6]					
Unipolar Offset Drift	1, 2, 3	-5	--	+5	ppm of FSR/°C
Gain Drift (Excludes Internal Reference Drift)	1, 2, 3	-20	--	+20	ppm of FSR/°C
Gain Drift (Includes Internal Reference Drift)	1, 2, 3	-40	--	+40	ppm of FSR/°C
Reference Voltage Drift	1, 2, 3	-30	--	+30	ppm/°C
DYNAMIC PERFOMANCE[5]					
Maximum Output Update Rate[6]	9,10,11	30	40		MSPS
Output Settling Time (t_{ST}) (to 0.025%)[6]	1, 2, 3	--	25	35	ns
Output Propagation Delay(t_{PD})	1, 2, 3	--	10	--	ns
Glitch Impulse	1, 2, 3	--	35	--	pV-s
Output Rise Time (10% to 90%)	1, 2, 3	--	5	--	ns
Output Fall Time (10% to 90%)	1, 2, 3	--	5	--	ns
Output Noise (DB0 to DB15 High into 50Ω)	1, 2, 3	--	3	--	nV/Hz^{-2}
Diffrerential Gain Error	1, 2, 3	--	0.01	--	%
Differential Phase Error	1, 2, 3	--	0.01	--	Degree
DIGITAL INPUTS					
Logic “1” Voltage[7]	7, 8	3.5	--	--	V

TABLE 4. 768A ELECTRICAL SPECIFICATIONS

(T_{MIN} TO T_{MAX}, V_{DD} = +5.0V +/- 5%, V_{EE} = -5.0V +/- 5%, LADCOM, REFCOM, DCOM = 0V, IREFIN = 5MA, CLOCK = 10MHZ, UNLESS OTHERWISE NOTED)

PARAMETER	SUBGROUPS	MIN	TYP	MAX	UNITS
Logic "0" Voltage[7]	7, 8	--	--	1.5	V
Logic "1" Current	1, 2, 3	-10	--	+10	uA
Logic "0" Current	1, 2, 3	-10	--	+10	uA
Input Capacitance		--	20	--	pF
Input Set-up Time (t_S)[7]	7, 8	10	--	--	ns
Input Hold Time (t_H)[7]	7, 8	5	--	--	ns
Latch Pulse Width[7] (tLPW)	7, 8	10	--	--	ns
AC LINEARITY[8]					
Spurious-Free Dynamic Range (SDFR Within a Window) FOUT = 1.002 MHz, Clock = 10MHz, 2MHz Span) FOUT = 1.002 MHz, Clock = 20MHz, 2MHz Span) FOUT = 5.002 MHz, Clock = 30MHz, 10MHz Span)	4, 5, 6	 -- -- --	 86 85 78	 79 -- 	dB
Spurious-Free Dynamic Range (SDFR to Nyquist) FOUT = 1.002 MHz, Clock = 10MHz FOUT = 1.002 MHz, Clock = 20MHz FOUT = 5.002 MHz, Clock = 30MHz	4, 5, 6	 -- -- --	 74 73 67	 70 -- --	dB
Total Harmonic Distortion (THD) FOUT = 1.002 MHz, Clock = 10MHz FOUT = 1.002 MHz, Clock = 20MHz FOUT = 5.002 MHz, Clock = 30MHz	4, 5, 6	 -- -- --	 -71 -66 -61	 -68 - --	dB
POWER SUPPLY					
Positive Voltage Range	1, 2, 3	4.75	5	5.25	V
Negative Voltage Supply	1, 2, 3	-5.25	-5	-4.75	V
Positive Supply Current (I_{DD})	1, 2, 3	--	30	40	mA
Negative Supply Current (I_{EE})	1, 2, 3	--	63	73	mA
Nominal Power Dissipation	1, 2, 3	--	465	600	mW
Power SupplyRejection Ratio (PSRR)	1, 2, 3	-0.2	--	+0.2	% of FSR/V

1. Measured at IOUTA, driving a virtual ground.
2. Nominal FS current is 4X the current at IREFIN. Therefore, nominal FS current is 20mA when IREFIN = 5mA.
3. Output current is defined as total output current avalable for IREFIN and any external load.
4. Reference bandwidth is a function of external cap at NR pin.
5. Measured as unbuffered voltage output (1V Range) with FS current into 50Ω load at IOUTB.
6. Guaranteed by Design
7. Application of Signal
8. Not Tested

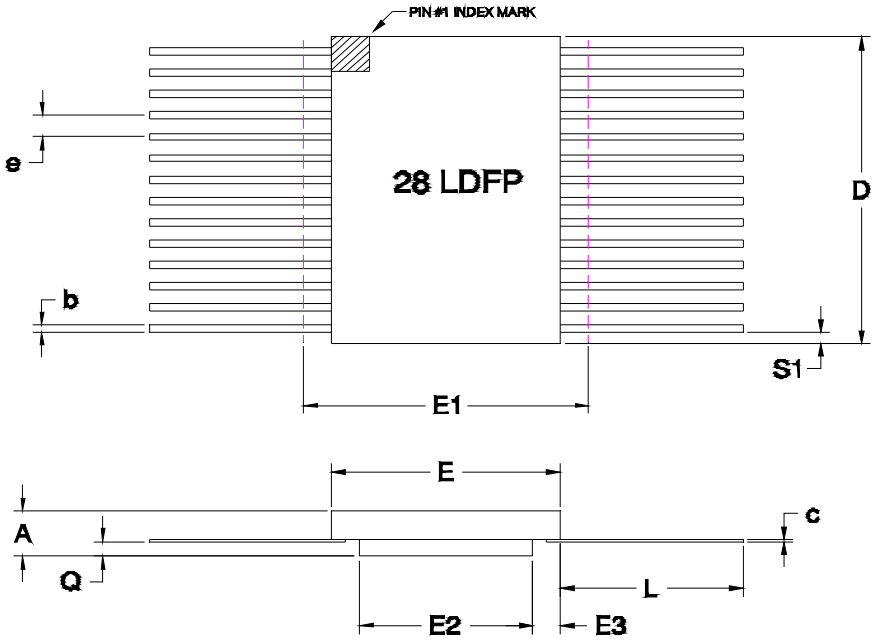

TABLE 5. 28 PIN FLAT PACKAGE

SYMBOL	DIMENSIONS		
	Min	Nom	MAX
A	0.090	0.109	0.143
b	0.015	0.017	0.022
c	0.004	0.005	0.009
D	--	0.720	0.740
E	0.380	0.410	0.420
E1	--	--	0.440
E2	0.180	0.280	--
E3	0.030	0.065	--
e	0.050 BSC		
L	0.390	0.400	0.410
Q	0.021	0.035	0.045
S1	0.000	0.027	--
N	28		

Note: All dimensions in inches
Top and Bottom of the package are internally tied to ground.

Important Notice:

These data sheets are created using the chip manufacturer's published specifications. Maxwell Technologies verifies functionality by testing key parameters either by 100% testing, sample testing or characterization.

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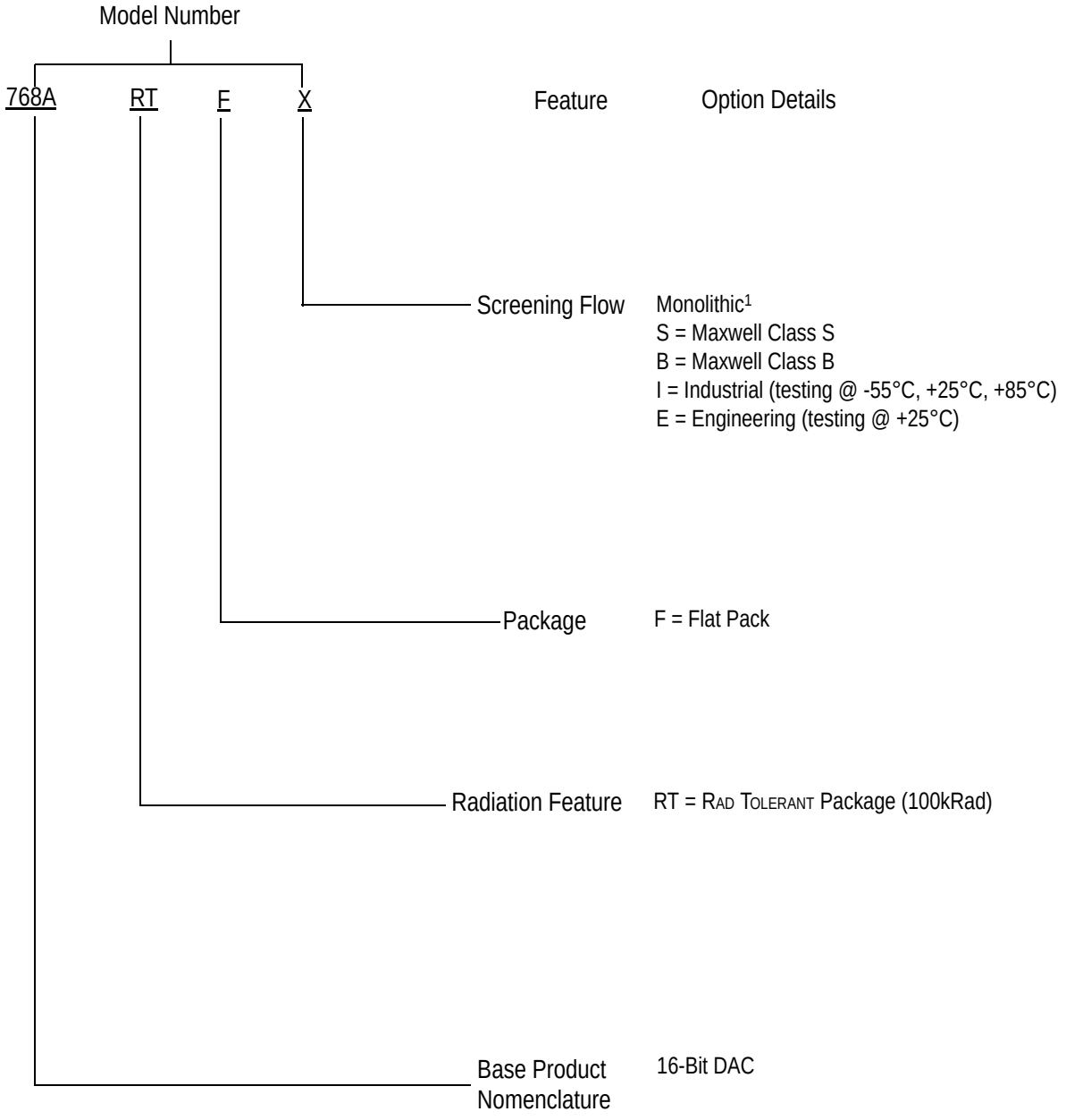
Product Ordering Options



1) Products are screened to Maxwell Technolgies Self-Defined Class B and Class S flows.