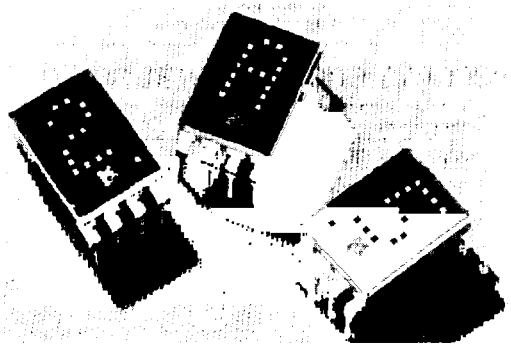
HEWLETT PACKARD

JAN QUALIFIED, HERMETIC, NUMERIC AND HEXADECIMAL DISPLAYS FOR MILITARY APPLICATIONS

4N51 / 4N51TXV / JM87157 / 00101AAX
4N52 / 4N52TXV / JM87157 / 00102AAX
4N53 / 4N53TXV / JM87157 / 00103AAX
4N54 / 4N54TXV / JM87157 / 00104AAX

Features

- **MILITARY QUALIFIED LISTED ON MIL-D-87157 QPL**
- **TRUE HERMETIC PACKAGE**
- **TXV VERSION AVAILABLE**
- **THREE CHARACTER OPTIONS Numeric, Hexadecimal, Over Range**
- **4 x 7 DOT MATRIX CHARACTER**
- **PERFORMANCE GUARANTEED OVER TEMPERATURE**
- **HIGH TEMPERATURE STABILIZED**
- **SOLDER DIPPED LEADS**
- **MEMORY LATCH/DECODER/DRIVER TTL Compatible**
- **CATEGORIZED FOR LUMINOUS INTENSITY**



Description

These standard red solid state displays have a 7.4 mm (0.29 inch) dot matrix character and an on-board IC with data memory latch/decoder and LED drivers in a glass/ceramic package. These devices utilize a solder glass frit seal and conform to the hermeticity requirements of MIL-D-87157, the general specification for LED displays. These 4N5X series displays are designed for use in military and aerospace applications.

These military qualified displays are designated as M87157/00101 AAX through -/00104AAX in the MIL-D-87157 Qualified Parts List (QPL). The letter designations at the end of the part numbers are defined as follows: "A" signifies MIL-D-87157 Quality Level A. "A" signifies solder dipped leads, "X" signifies the luminous intensity category.

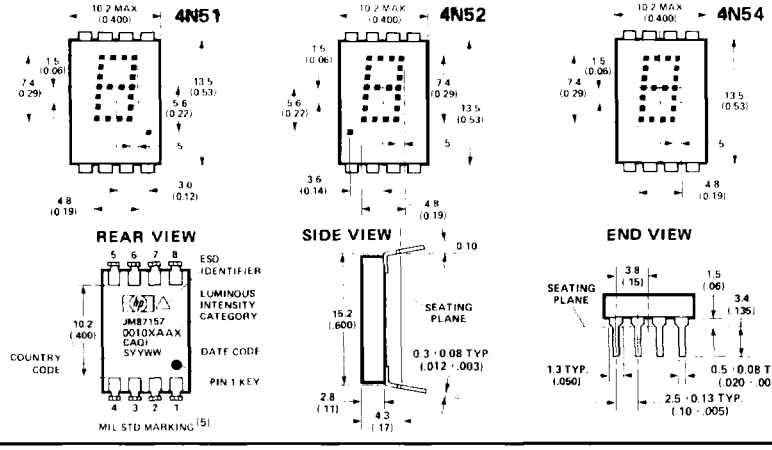
The 4N51 numeric display decodes positive 8421 BCD logic inputs into characters 0-9, a "—" sign, a test pattern, and four blanks in the invalid BCD states. The unit employs a right-hand decimal point.

The 4N52 is the same as the 4N51 except that the decimal point is located on the left-hand side of the digit.

The 4N54 hexadecimal display decodes positive 8421 logic inputs into 16 states, 0-9 and A-F. In place of the decimal point an input is provided for blanking the display (all LED's off), without losing the contents of the memory.

The 4N53 is a "±1." overrange display, including a right-hand decimal point.

Package Dimensions*



PIN	FUNCTION 4N51 4N52 NUMERIC	FUNCTION 4N54 HEXA-DECIMAL
1	Input 2	Input 2
2	Input 4	Input 4
3	Input 8	Input 8
4	Decimal point	Blanking control
5	Latch enable	Latch enable
6	Ground	Ground
7	V_{CC}	V_{CC}
8	Input 1	Input 1

NOTES:
1. Dimensions in millimetres and (inches).
2. Unless otherwise specified, the tolerance on all dimensions is ± .38mm (± .015").
3. Digit center line is ± .25mm (± .01") from package center line.
4. Solder dipped leads.
5. See over range package drawing for HP standard marking.

*JEDEC Registered Data.

Absolute Maximum Ratings*

Description	Symbol	Min.	Max.	Unit
Storage temperature, ambient	T_S	−65	+125	°C
Operating temperature, ambient [1,2]	T_A	−55	+100	°C
Supply voltage [3]	V_{CC}	−0.5	+7.0	V
Voltage applied to input logic, dp and enable pins	V_I, V_{DP}, V_E	−0.5	V_{CC}	V
Voltage applied to blanking input [7]	V_B	−0.5	V_{CC}	V
Maximum solder temperature at 1.59mm (.062 inch) below seating plane; t ⩽ 5 seconds			260	°C

Recommended Operating Conditions*

Description	Symbol	Min.	Nom.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Operating temperature, ambient [1,2]	T_A	−55		+100	°C
Enable Pulse Width	t_W	100			nsec
Time data must be held before positive transition of enable line	t_{SETUP}	50			nsec
Time data must be held after positive transition of enable line	t_{HOLD}	50			nsec
Enable pulse rise time	t_{TLH}			200	nsec

Electrical/Optical Characteristics* (T_A = −55°C to +100°C, unless otherwise specified)

Description	Symbol	Test Conditions	Min.	Typ. [4]	Max.	Unit
Supply Current	I_{CC}	V_{CC} = 5.5 V (Characters "5." or "B")		112	170	mA
Power dissipation	P_I			560	935	mW
Luminous intensity per LED (Digit average) [5,6]	I_V	V_{CC}=5.0V, T_A=25°C	40	85		µcd
Logic low-level input voltage	V_{IL}	V_{CC}=4.5V			0.8	V
Logic high-level input voltage	V_{IH}		2.0			V
Enable low-voltage; data being entered	V_{EL}				0.8	V
Enable high-voltage; data not being entered	V_{EH}		2.0			V
Blanking low-voltage; display not blanked [7]	V_{BL}				0.8	V
Blanking high-voltage; display blanked [7]	V_{BH}		3.5			V
Blanking low-level input current [7]	I_{BL}	V_{CC}=5.5V, V_{BL}=0.8V			50	µA
Blanking high-level input current [7]	I_{BH}	V_{CC}=5.5V, V_{BH}=4.5V			1.0	mA
Logic low-level input current	I_{IL}	V_{CC}=5.5V, V_{IL}=0.4V			−1.6	mA
Logic high-level input current	I_{IH}	V_{CC}=5.5V, V_{IH}=2.4V			+100	µA
Enable low-level input current	I_{EL}	V_{CC}=5.5V, V_{EL}=0.4V			−1.6	mA
Enable high-level input current	I_{EH}	V_{CC}=5.5V, V_{EH}=2.4V			+130	µA
Peak wavelength	λ_{PEAK}	T_A=25°C		655		nm
Dominant Wavelength [8]	λ_d	T_A=25°C		640		nm
Weight**				1.0		gm
Leak Rate					$5x10^{-8}$	cc/sec

Notes: 1. Nominal thermal resistance of a display mounted in a socket which is soldered into a printed circuit board: Θ_{JA}=50°C/W; Θ_{JC}=15°C/W. 2. Θ_{CA} of a mounted display should not exceed 35°C/W for operation up to T_A=+100°C. 3. Voltage values are with respect to device ground, pin 6. 4. All typical values at V_{CC}=5.0 Volts, T_A=25°C. 5. These displays are categorized for luminous intensity with the intensity category designated by a letter located on the back of the display contiguous with the Hewlett-Packard logo marking. 6. The luminous intensity at a specific ambient temperature, $I_V(T_A)$, may be calculated from this relationship: $I_V(T_A)=I_{V(25°C)}(.985)^{[T_A-25°C]}$ 7. Applies only to 4N54. 8. The dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and represents the single wavelength which defines the color of the device.

*JEDEC Registered Data. **Non Registered Data.

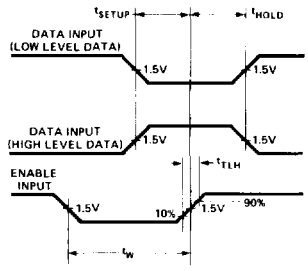


Figure 1. Timing Diagram of 4N51-4N54 Series Logic.

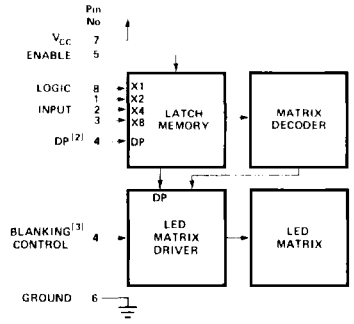


Figure 2. Block Diagram of 4N51-4N54 Series Logic.

TRUTH TABLE

BCD DATA[1]				4N51 AND 4N52	4N54
X_8	X_4	X_2	X_1		
L	L	L	L		
L	L	L	H		
L	L	H	L		
L	L	H	H		
L	H	L	L		
L	H	L	H		
L	H	H	L		
L	H	H	H		
H	L	L	L		
H	L	L	H		
H	L	H	L		
H	L	H	H	(BLANK)	
H	H	L	L	(BLANK)	
H	H	L	H		
H	H	H	L	(BLANK)	
H	H	H	H	(BLANK)	
DECIMAL PT.[2]				ON	V_{DP} L
				OFF	V_{DP} H
ENABLE[1]				LOAD DATA	V_E L
				LATCH DATA	V_E H
BLANKING[3]				DISPLAY ON	V_B L
				DISPLAY OFF	V_B H

Notes:

1. H = Logic High; L = Logic Low. With the enable input at logic high changes in BCD input logic levels or D.P. input have no effect upon display memory, displayed character, or D.P.
2. The decimal point input, DP, pertains only to the 4N51 and 4N52 displays.
3. The blanking control input, B, pertains only to the 4N54 hexadecimal display. Blanking input has no effect upon display memory.

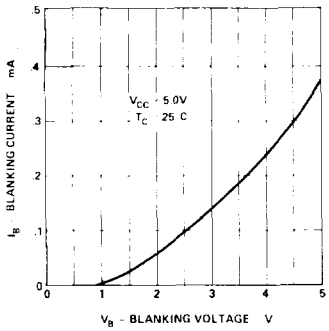


Figure 3. Typical Blanking Control Current vs. Voltage for 4N54.

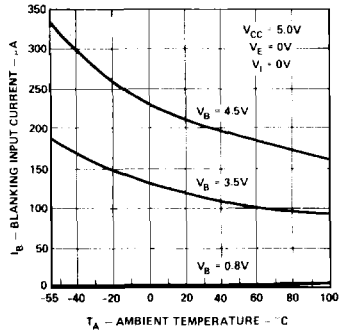


Figure 4. Typical Blanking Control Input Current vs. Ambient Temperature for 4N54.

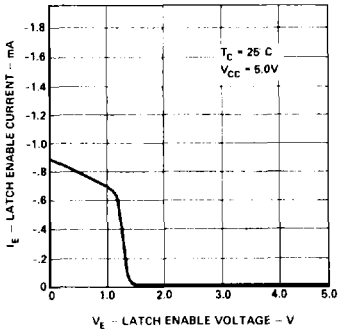


Figure 5. Typical Latch Enable Input Current vs. Voltage.

*JEDEC Registered Data.

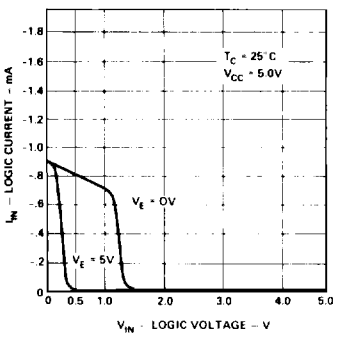


Figure 6. Typical Logic and Decimal Point Input Current vs. Voltage.

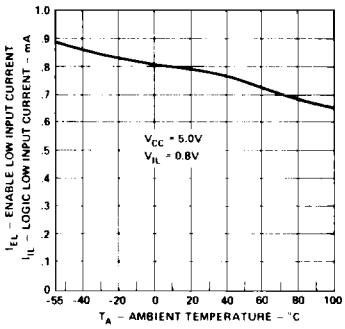


Figure 7. Typical Logic and Enable Low Input Current vs. Ambient Temperature.

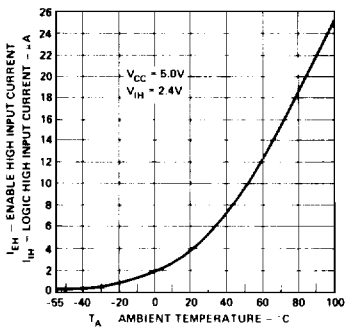


Figure 8. Typical Logic and Enable High Input Current vs. Ambient Temperature.

Operational Considerations

ELECTRICAL

The 4N51-4N54 series devices use a modified 4 x 7 dot matrix of light emitting diodes (LED's) to display decimal/hexadecimal numeric information. The LED's are driven by constant current drivers. BCD information is accepted by the display memory when the enable line is at logic low and the data is latched when the enable is at logic high. To avoid the latching of erroneous information, the enable pulse rise time should not exceed 200 nanoseconds. Using the enable pulse width and data setup and hold times listed in the Recommended Operating Conditions allows data to be clocked into an array of displays at a 6.7MHz rate.

The blanking control input on the 4N54 display blanks (turns off) the displayed hexadecimal information without disturbing the contents of display memory. The display is blanked at a minimum threshold level of 3.5 volts. This may be easily achieved by using an open collector TTL gate and a pull-up resistor. For example, (1/6) 7416 hexinverter buffer/driver and a 120 ohm pull-up resistor will provide sufficient drive to blank eight displays. The size of the blanking pull-up resistor may be calculated from the following formula, where N is the number of digits:

$$R_{blank} = (V_{CC} - 3.5V)/[N\ (1.0mA)]$$

The decimal point input is active low true and this data is latched into the display memory in the same fashion as the BCD data. The decimal point LED is driven by the on-board IC.

The ESD susceptibility of the IC devices is Class A of MIL-STD-883 or Class 2 of DOD-STD-1686 and DOD-HDBK-263.

MECHANICAL

4N51-4N54 series displays are hermetically tested for use in environments which require a high reliability device. These displays are designed and tested to meet a helium leak rate of 5 x 10^{-8} CC/SEC and a fluorocarbon gross leak bubble test.

These displays may be mounted by soldering directly to a printed circuit board or inserted into a socket. The lead-to-lead pin spacing is 2.54mm (0.100 inch) and the lead row spacing is 15.24mm (0.600 inch). These displays may be end stacked with 2.54mm (0.100 inch) spacing between outside pins of adjacent displays. Sockets such as Augat 324-AG2D (3 digits) or Augat 508-AG8D (one digit, right angle mounting) may be used.

The primary thermal path for power dissipation is through the device leads. Therefore, to insure reliable operation up to an ambient temperature of +100° C, it is important to maintain a case-to-ambient thermal resistance of less than 35° C/watt as measured on top of display pin 3.

Post solder cleaning may be accomplished using water, Freon/alcohol mixtures formulated for vapor cleaning processing (up to 2 minutes in vapors at boiling) or Freon/alcohol mixtures formulated for room temperature cleaning. Suggested solvents: Freon TF, Freon TE, Genesolv DI-15, Genesolv DE-15.

PRECONDITIONING

4N51-4N54 series displays are 100% preconditioned by 24 hour storage at 125° C.

CONTRAST ENHANCEMENT

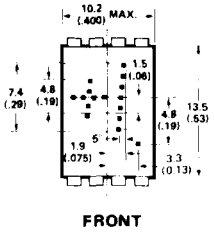
The 4N51-4N54 displays have been designed to provide the maximum posible ON/OFF contrast when placed behind an appropriate contrast enhancement filter. Some suggested filters are Panelgraphic Ruby Red 60 and Dark Red 63, SGL Homalite H100-1605, 3M Light Control Film and Polaroid HRCP Red Circular Polarizing Filter. For further information see Hewlett-Packard Application Note 1015.

*JEDEC Registered Data.

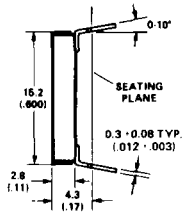
Solid State Over Range Display

For display applications requiring a ±, 1, or decimal point designation, the 4N53 over range display is available. This display module comes in the same package as the 4N51-4N54 series numeric display and is completely compatible with it.

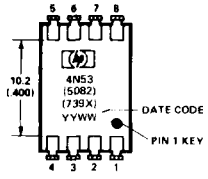
Package Dimensions*



FRONT

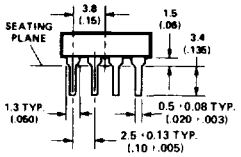


SIDE



REAR

HP STANDARD MARKING



END

NOTES:
1. DIMENSIONS IN MILLIMETRES AND (INCHES).
2. UNLESS OTHERWISE SPECIFIED, THE TOLERANCE ON ALL DIMENSIONS IS ±.38 MM (± .015 INCHES).

PIN	FUNCTION
1	Plus
2	Numeral One
3	Numeral One
4	DP
5	Open
6	Open
7	V_{cc}
8	Minus/Plus

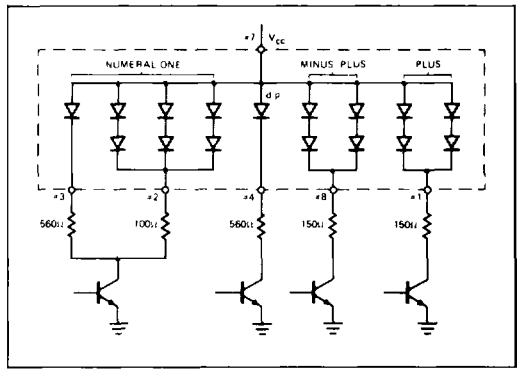


Figure 9. Typical Driving Circuit.

TRUTH TABLE

CHARACTER	PIN			
	1	2,3	4	8
+	H	X	X	H
–	L	X	X	H
1	X	H	X	X
Decimal Point	X	X	H	X
Blank	L	L	L	L

NOTES: L: Line switching transistor in Figure 9 cutoff.
H: Line switching transistor in Figure 9 saturated.
X: 'Don't care'

Electrical/Optical Characteristics*

4N53 (T_A = -55°C to +100°C, Unless Otherwise Specified)

DESCRIPTION	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Forward Voltage per LED	V_F	I_F = 10 mA		1.6	2.0	V
Power dissipation	P_T	I_F = 10 mA all diodes lit		280	320	mW
Luminous Intensity per LED (digit average)	I_v	I_F = 6 mA T_C = 25°C	40	85		µcd
Peak wavelength	λ_{peak}	T_C = 25°C		655		nm
Dominant Wavelength	λ_d	T_C = 25°C		640		nm
Weight * *				1.0		gm

Recommended Operating Conditions*

	SYMBOL	MIN	NOM	MAX	UNIT
LED supply voltage	V_{CC}	4.5	5.0	5.5	V
Forward current, each LED	I_F		5.0	10	mA

NOTE:
LED current must be externally limited. Refer to Figure 9 for recommended resistor values.

*JEDEC Registered Data. **Non Registered Data.

Absolute Maximum Ratings*

DESCRIPTION	SYMBOL	MIN.	MAX.	UNIT
Storage temperature, ambient	T_S	-65	+125	°C
Operating temperature, ambient	T_A	-55	+100	°C
Forward current, each LED	I_F		10	mA
Reverse voltage, each LED	V_R		4	V

High Reliability Testing

Two standard reliability testing programs are available. The military program provides QPL parts that comply to MIL-D-87157 Quality Level A, per Tables I, II, IIIa, and IVa. A second program is an HP modification to the full conformance program and offers the 100% screening portion of Level A, Table I, and Group A, Table II. In addition, a MIL-D-87157 Level B equivalent testing program is available upon request.

PART MARKING SYSTEM

Standard Product	With Table I and II	With Tables I, II, IIIa and IVa
PREFERRED PART NUMBER SYSTEM		
4N51	4N51TXV	JM87157/00101AAX
4N52	4N52TXV	JM87157/00102AAX
4N54	4N54TXV	JM87157/00103AAX
4N53	4N53TXV	JM87157/00104AAX

100% Screening

TABLE I.
QUALITY LEVEL A OF MIL-D-87157

Test Screen	MIL-STD-750 Method	Conditions
1. Precap Visual	2072	Interpreted by HP Procedure 5956-7572-52
2. High Temperature Storage	1032	T_A = 125°C, Time = 24 hours
3. Temperature Cycling	1051	Condition B, 10 Cycles, 15 Min. Dwell
4. Constant Acceleration	2006	10,000 G's at Y_1 orientation
5. Fine Leak	1071	Condition H
6. Gross Leak	1071	Condition C or K
7. Interim Electrical/Optical Tests[2]	—	I_V, I_{CC}, I_{BL}, I_{BH}, I_{EL}, I_{EH}, I_{IL}, and I_{IH} T_A = 25°C
8. Burn-In[1, 3]	1015	Condition B at V_{CC} = 5V and cycle through logic at 1 character per second. T_A = 100°C, t = 160 hours
9. Final Electrical Test[2]	—	Same as Step 7
10. Delta Determinations	—	ΔI_V = -20%, ΔI_{CC} = +10 mA, ΔI_{IH} = +10μA and ΔI_{EH} = ±13 μA
11. External Visual[1]	2009	

Notes:
1. MIL-STD-883 Test Method applies.
2. Limits and conditions are per the electrical/optical characteristics.
3. Burn-in for the over range display shall use Condition B at a nominal I_F = 8 mA per LED, with all LEDs illuminated for t = 160 hours minimum.

TABLE II
GROUP A ELECTRICAL TESTS — MIL-D-87157

Test	Parameters	LTPD
Subgroup 1 DC Electrical Tests at 25°C [1]	I_V, I_{CC}, I_{BL}, I_{BH}, I_{EL}, I_{EH}, I_{IL}, and I_{IH} and visual function, T_A = 25°C	5
Subgroup 2 DC Electrical Tests at High Temperature[1]	Same as Subgroup 1, except delete I_V and visual function. T_A = +100°C	7
Subgroup 3 DC Electrical Tests at Low Temperature[1]	Same as Subgroup 1, except delete I_V and visual function. T_A = -55°C	7
Subgroup 4, 5, and 6 not applicable		
Subgroup 7 Optical and Functional Tests at 25°C	Satisfied by Subgroup 1	5
Subgroup 8 External Visual	MIL-STD-883, Method 2009	7

1. Limits and conditions are per the electrical/optical characteristics.

TABLE IIIa
GROUP B, CLASS A AND B OF MIL-D-87157

Test	MIL-STD-750 Method	Conditions	Sample Size
Subgroup 1			
Resistance to Solvents	1022		4 Devices/ 0 Failures
Internal Visual and Design Verification[1]	2075[7]		1 Device/ 0 Failures
Subgroup 2[2,3]			
Solderability	2026	T_A = 245°C for 5 seconds	LTPD = 15
Subgroup 3			
Thermal Shock (Temp. Cycle)	1051	Condition B1, 15 Min. Dwell	LTPD = 15
Moisture Resistance[4]	1021		
Fine Leak	1071	Condition H	
Gross Leak	1071	Condition C or K	
Electrical/Optical Endpoints[5]	—	I_V, I_{CC}, I_{BL}, I_{BH}, I_{EL}, I_{EH}, I_{IL}, I_{IH} and visual function. T_A = 25°C	
Subgroup 4			
Operating Life Test (340 hrs.)[6]	1027	T_A = +100°C at V_{CC} = 5.0V and cycling through logic at 1 character per second.	LTPD = 10
Electrical/Optical Endpoints[5]	—	Same as Subgroup 3.	
Subgroup 5			
Non-operating (Storage) Life Test (340 hrs.)	1032	T_A = +125°C	LTPD = 10
Electrical/Optical Endpoints[5]	—	Same as Subgroup 3	

Notes:
1. Visual inspection performed through the display window.
2. Whenever electrical/optical tests are not required as endpoints, electrical rejects may be used.
3. The LTPD applies to the number of leads inspected except in no case shall less than 3 displays be used to provide the number of leads required.
4. Initial conditioning is a 15° inward bend, one cycle.
5. Limits and conditions are per the electrical/optical characteristics.
6. Burn-in for the over range display shall use Condition B at a nominal I_F = 8 mA per LED, with all LEDs illuminated for t = 160 hours minimum.
7. Equivalent to MIL-STD-883, Method 2014.

TABLE IVa
GROUP C, CLASS A AND B OF MIL-D-87157

Test	MIL-STD-750 Method	Conditions	Sample Size
Subgroup 1			
Physical Dimensions	2066		2 Devices/ 0 Failures
Subgroup 2[2,7,9]			LTPD = 15
Lead Integrity	2004	Condition B2	
Fine Leak	1071	Condition H	
Gross Leak	1071	Condition C or K	
Subgroup 3			
Shock	2016	1500G, Time = 0.5 ms, 5 blows in each orientation X_1, Y_1, Z_1	LTPD = 15
Vibration, Variable Frequency	2056		
Constant Acceleration	2006	10,000G at Y_1 orientation	
External Visual[4]	1010 or 1011		
Electrical/Optical Endpoints[8]	—	I_V, I_{CC}, I_{BL}, I_{BH}, I_{EL}, I_{EH}, I_{IL}, I_{IH} and visual Function, T_A = 25°C	
Subgroup 4[1,3]			
Salt Atmosphere	1041		LTPD = 15
External Visual[4]	1010 or 1011		
Subgroup 5			
Bond Strength[5]	2037	Condition A	LTPD = 20 (C = 0)
Subgroup 6			λ = 10
Operating Life Test[6]	1026	T_A = +100°C	
Electrical/Optical Endpoints[8]	—	Same as Subgroup 3	

1. Whenever electrical/optical tests are not required as endpoints, electrical rejects may be used.
2. The LTPD applies to the number of leads inspected except in no case shall less than three displays be used to provide the number of leads required.
3. Solderability samples shall not be used.
4. Visual requirements shall be as specified in MIL-STD-883, Methods 1010 or 1011.
5. Displays may be selected prior to seal.
6. If a given inspection lot undergoing Group B inspection has been selected to satisfy Group C inspection requirements, the 340 hour life tests may be continued on test to 1000 hours in order to satisfy the Group C Life Test requirements. In such cases, either the 340 hour endpoint measurements shall be made a basis for Group B lot acceptance or the 1000 hour endpoint measurement shall be used as the basis for both Group B and Group C acceptance.
7. MIL-STD-883 test method applies.
8. Limits and conditions are per the electrical/optical characteristics.
9. Initial conditioning is a 15° inward bend, three cycles.