MITEL SEMICONDUCTOR

SA808

3 Phase PWM Engine Serial Microprocessor Bus

Advance Information

DS5112 - 1.2 April 1999

The SA808 Motor Control IC has been designed specifically for Pulse-Width Modulation (PWM) control of 3 phase induction motors used in appliances such as washing machines, HVAC equipment and in light industrial machinery such as machine tools.

The IC allows complete control of Mitel Semiconductor's advanced, digital PWM waveform generation kernel by an external microprocessor or microcontroller using a 3-wire MICROWIRE™ - style serial interface.

Flexible options are available for the control of both power frequency (speed) and load voltage to ensure that motor flux is accurately controlled irrespective of the running speed.

Power frequency is resolved to 16 bits within a user-defined range (up to 4kHz). Acceleration and deceleration may be controlled actively by the external processor, but an option allows the definition of independent acceleration and deceleration rates using a single resistor and capacitor for each. A patented algorithm allows these rates to be modified according to the state of two analog inputs to prevent damage to the power electronics and load due to overvoltage or overcurrent conditions.

Load voltage (amplitude) may be controlled by the SA808 at all power frequencies using user-programmable linear or quadratic (Fan-law) characteristics. Alternatively, amplitude may be controlled directly by the external processor - serial interface synchronising frequency and amplitude values.

All other operational parameters are programmed into the device using the serial interface. These include carrier frequency, waveform type, minimum pulse length and pulse underlap time.

All PWM outputs have sufficient current capability to allow direct driving of opto-coupler isolation stages.

Since the PWM engine is capable of generating outputs much higher than normal line frequency, this device is also suitable for high speed drives.

Features

- Full Control via 3-Wire MICROWIRE™ Style Serial Interface.
- Three Selectable Power Waveforms including Deadbanded Triplen for Reduced Losses.
- On-chip Linear and Fan Law V/f Characteristics.
- Acceleration and Deceleration Times Controlled by Optional External RC.
- Variable Amplitude / Fixed Frequency Mode For Static Inverter Applications.

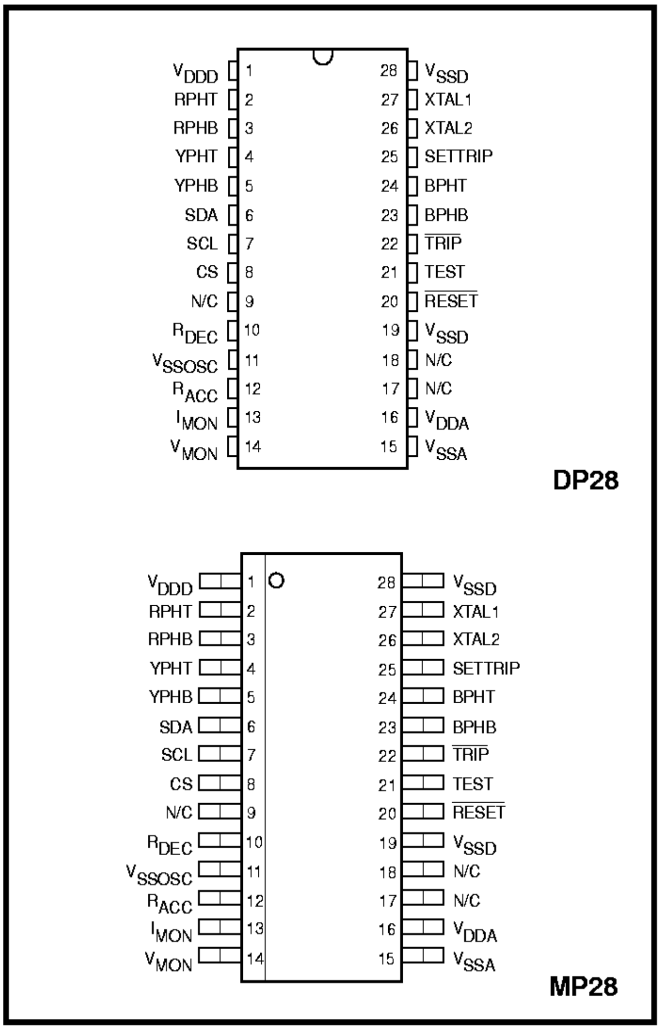


Fig.1 Pin connections - top view

- Built-in High Current Output Drivers.
- Carrier Frequency Selectable up to 24kHz for Silent Operation.
- Wide Power Frequency Range 0 to 4kHz.
- Selectable Minimum Pulse Width and Underlap Times.
- Double Edged Regular Sampling.
- Bootstrap Driver Precharge.

Ordering Information

SA808/IG/DP1S	28-Lead PDIP
SA808/IG/MP1S	28-Lead SOIC Wide body

MICROWIRE™ is a registered tradename of National Semiconductor Inc.

Absolute Maximum Ratings

Supply voltage, V_{DD}	7V
Voltage on any pin	V_{SS} –0·5V to V_{DD} +0·5V
Storage temperature	–55°C to +150°C
Operating temperature range	–40°C to +85°C

The temperature ranges quoted apply to all package types. Alternative package types maybe available. Further information is available on request.

Stresses above those listed in the Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions, or at any other condition above those indicated in the operations section of this specification, is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Electrical Characteristics

Test conditions (unless otherwise stated) V_{DD} = 5V ±10%, T_{amb} = 25°C

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Input High Voltage	V_{IH}	2	-	-	V	
Input Low Voltage	V_{IL}	-	-	0.8	V	
Input Low Current	I_{IL}					V_{IN} = 0V, V_{DD} = 5.5V
SET TRIP Input		–1.0	-	1.0	µA	
All other Inputs		-	-	10	µA	
Input High Current	I_{IH}					V_{IN} = V_{DD} = 5.5V
SET TRIP Input		20	-	135	µA	
All other Inputs		-	-	10	µA	
Output High Voltage	V_{OH}	4·0	4.5	-	V	I_{OH} = – 12mA
Output Low Voltage	V_{OL}	-	0.2	0.4	V	I_{OL} = +12mA
Static Supply Current	I_{DDS}	-	-	8	mA	O/Ps open cct.
Dynamic Supply Current	I_{DDD}	-	(TBD)	(TBD)	mA	XTAL = 25MHz
Supply Voltage	V_{DD}	4·5	5.0	5.5	V	
V_{MON} / I_{MON} Thresholds						V_{DD} = 5·0V
$(V_{thr} + V_{thf})/2$		2.44	$V_{DDA}/2$	2.56	V	
$V_{thr} – V_{thf}$		140	200	320	mV	
Clock Frequency	f_{CLK}	15	-	25	MHz	
External Clock Duty Cycle	D_{CLK}	40	-	60	%	
SET TRIP = 1 to outputs	f_{TRIP}	$3/f_{CLK}$	-	$4/f_{CLK}$	s	
tripped and $\overline{\text{TRIP}}$ = 0						
Minimum Reset Period	t_{RST}	-	$2CR_{ACC}$	-	s	
at power on						
R_{ACC}/R_{DEC} Freq. range	t_{AD}	0.5	-	100	KHz	
ACC/DEC Defeat Threshold	V_{DTF}	-	$0.125V_{DDA}$	-	V	

Pin Descriptions

Pin Number	Name	Type	Function
1	V_{DDD}	P	Positive supply – Digital
2	RPHT	O	Red Phase Top
3	RPHB	O	Red Phase Bottom
4	YPHT	O	Yellow Phase Top
5	YPHB	O	Yellow Phase Bottom
6	SDA	I/O	EEPROM / Serial Data
7	SCL	I/O	EEPROM / Serial Clock
8	CS	I/O	EEPROM / Serial Chip Select
9	NC	-	Not connected
10	R_{DEC}	I	External RC – Sets deceleration Osc. Rate
11	V_{SSOSC}	P	Ground (for oscillators)
12	R_{ACC}	I	External RC – Sets acceleration Osc. Rate
13	I_{MON}	I	Overcurrent - Forces deceleration. Active High
14	V_{MON}	I	Overvoltage - Inhibits Acceleration and Deceleration Active High
15	V_{SSA}	P	Ground - Analog
16	V_{DDA}	P	Positive Supply – Analog
17	NC	-	Not connected
18	NC	-	Not connected
19	V_{SSD}	P	Ground - Digital
20	$\overline{\text{RESET}}$	I	External Reset – Active Low
21	TEST	I	Used in factory test mode only
22	$\overline{\text{TRIP}}$	O	Trip Latch Status – Active Low
23	BPHB	O	Blue Phase Bottom
24	BPHT	O	Blue Phase Top
25	SET TRIP	I	Set Output Trip. Active High. Internal pulldown
26	XTAL2	I/O	Clock Crystal connection
27	XTAL1	I	Clock Crystal connection
28	V_{SSD}	P	Ground - Digital

Notes: (i) V_{DDA} and V_{DDD} pins must be connected together externally, and also all V_{SS} pins must be connected together externally.

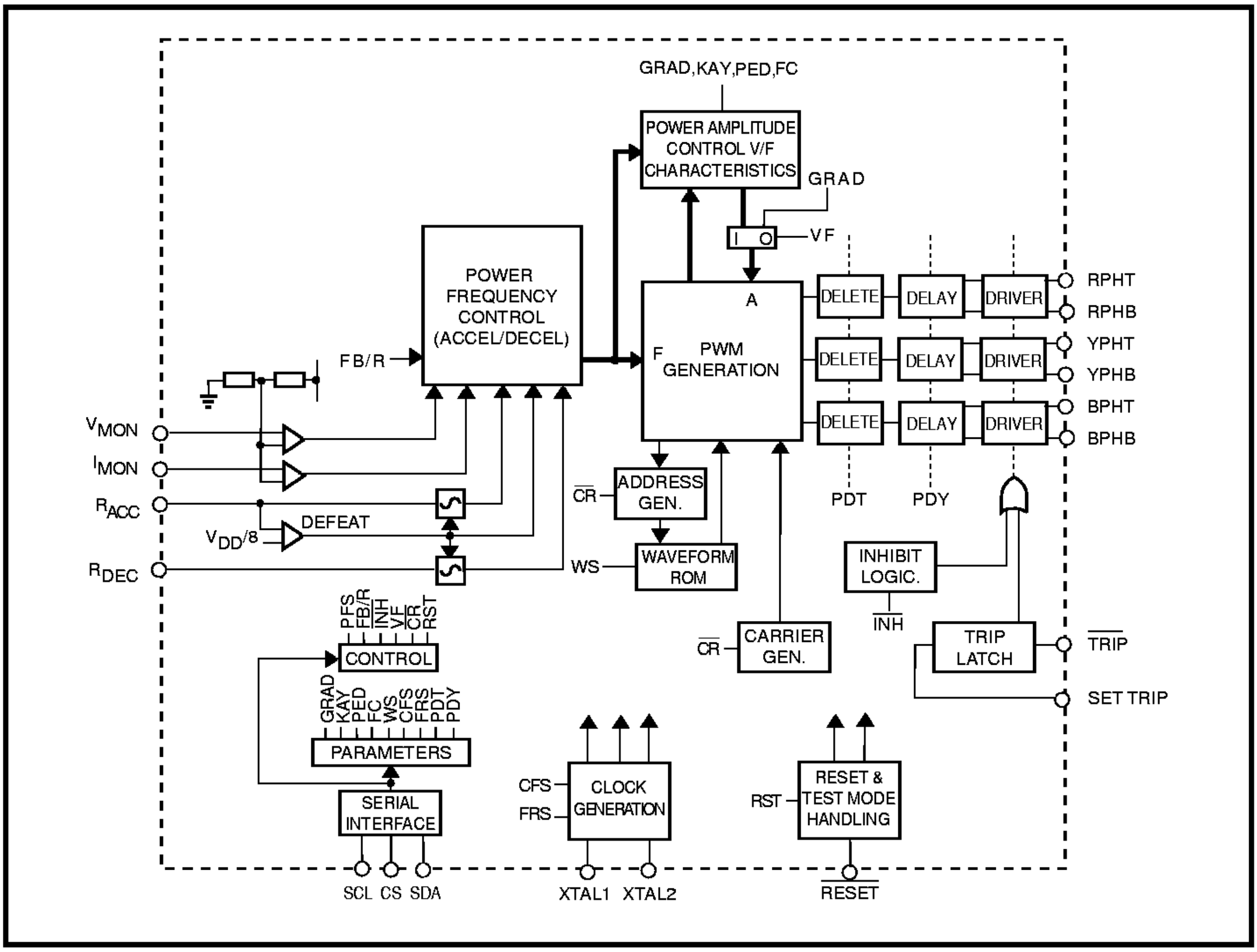


Fig.2 SA808 block diagram

Functional Description

The SA808 is a digital 3 phase pulse width modulation (PWM) generation core with peripheral blocks to allow control of parameters which affect the PWM data stream and to enable the pulse train to be optimised for driving power switch inverter circuits.

The device is controlled entirely by a simple 3 wire, write only serial interface which may be driven by most microprocessors and microcontrollers.

A PWM data stream arises from the comparison of a reference waveform and a carrier waveform, the PWM output changing state whenever the two are equal. For power control applications, the reference is known as the power waveform. Three power waveform shapes are available to the user, stored in digital form in on-chip waveform ROM. The chosen waveform is then scaled in the frequency and amplitude domains before comparison with the carrier. Sinusoid, Triplen and Deadbanded Triplen waveforms are included, the last two offering the potential for increased drive efficiency and reduced losses in the power switches compared to the use of a sinusoid power waveform.

Power frequency is controlled to 16 bit resolution via the serial interface. Acceleration and deceleration may be controlled by the external processor writing new power frequency values to the chip when required. However, the power frequency values can also be passed to the ACCEL/DECEL block of the the SA808 as target or setpoint values. The ACCEL/DECEL block then allows smooth changes between power frequencies controlled by on-chip oscillators. The frequency of these oscillators is controlled by external resistors and capacitors attached to the R_{ACC} and R_{DEC} pins, allowing independent rates of acceleration and deceleration respectively.

Two further inputs, V_{MON} and I_{MON} may be used to control acceleration and deceleration in the ACCEL/DECEL block. These override the normal frequency changing function by limiting deceleration or forcing deceleration to zero respectively. This mechanism may be used to provide over-voltage and over-current protection for the power switches.

The amplitude of the power waveform may be controlled by the device using either a linear or quadratic (Fan-law) dependence on the power frequency. Three parameters are available to the user to define the shape of the characteristic: gradient and pedestal for the linear characteristic, and a third factor for defining the shape of the Fan-law curve. Alternatively, amplitude calculation may be left to the external processor and values transferred via the serial interface. The serial interface control algorithm allows the synchronisation of power and amplitude values.

The raw output from the PWM generation block is processed by pulse deletion and pulse delay blocks before being output as complementary pairs of signals for driving top and bottom switches for each of the red, yellow and blue phases. The pulse deletion block allows the definition of the minimum length pulse to appear on the PWM outputs using a user-specified parameter. The pulse delay block introduces a user specifiable period during which top and bottom phase outputs are both switched off, thus avoiding shoot-through problems.

To facilitate the use of bootstrap driver circuits for the power switches, whenever the phase outputs are restarted after they have all been shut down, the bottom phase outputs are all pulsed high for a whole carrier cycle before normal operation is resumed. This gives a time during which the bootstrap capacitors may be charged before any top switch is driven.

An input, SET TRIP, is provided to enable rapid shutdown of all phase outputs in the event of an emergency.

The phase outputs are buffered by fast, high-current output drivers so that they may drive opto-isolators and gate driver ICs directly.

An on-chip clock oscillator allows the use of an external crystal or ceramic resonator to provide a stable, accurate clock. Alternatively the crystal clock inputs may be driven by an external clock.

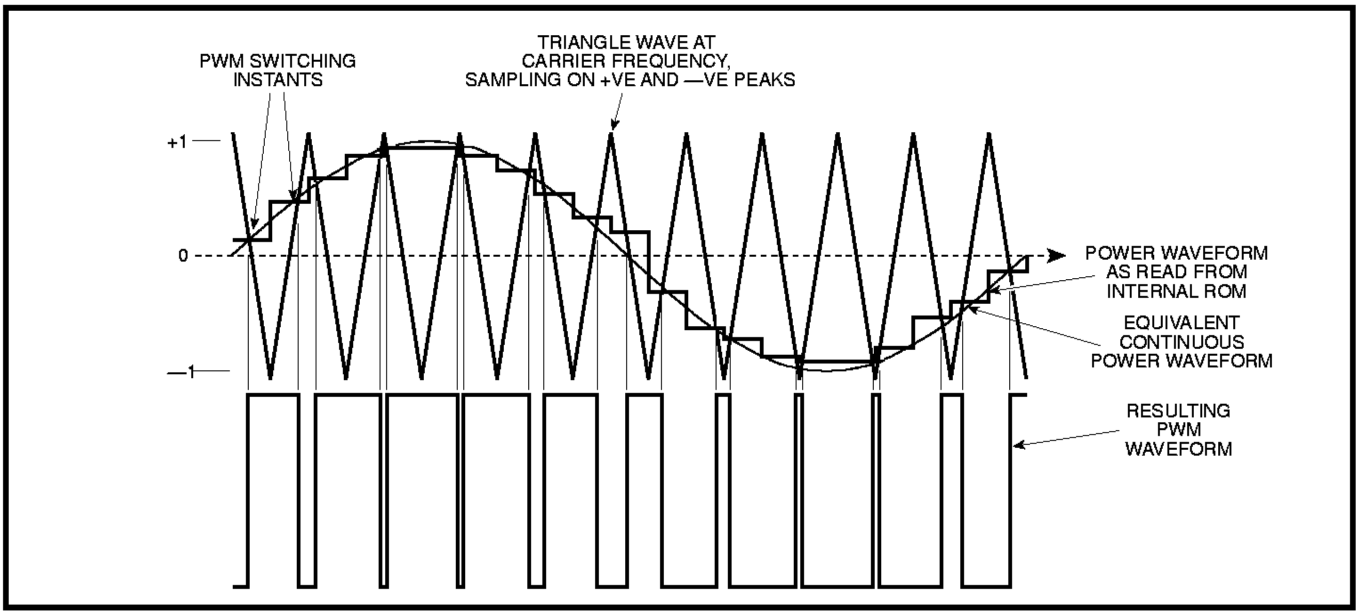


Fig.3 Asynchronous PWM generation with double-edged regular sampling as used by the SA808

PWM Generation Logic

An asynchronous method of PWM generation is used in uniform or ‘double-edged’ regular sampling of the waveform(s) stored in the internal ROM as illustrated in Fig.3.

In general, a pulse width modulation signal is derived by comparing a signal waveform, (in this case the power waveform), with a saw-tooth or triangular carrier waveform of significantly higher frequency. The intersections between the two waveforms, in the time domain, define the locations of transitions in the digital output train, and hence the width of the output pulses. The width of the pulses are directly proportional to the magnitude of the power waveform, thus the larger the magnitude, the longer the ‘ON’ pulse.

The SA808 uses a digital implementation of this technique which avoids drift problems associated with the use of analog circuitry. A triangular waveform is synthesised using an up/down counter and a digital comparator is used to compare this with the power waveform. The power waveform is sampled regularly at every peak and trough of the carrier waveform allowing both edges of the PWM output pulse to move in time, hence the term ‘double-edged’ regular sampling. (A saw-tooth carrier waveform would result in one fixed edge and one moving edge for each PWM pulse.)

The power waveform(s) are stored digitally in on-chip ROM (1536 samples per 360°). The power frequency is controlled by the rate at which the ROM is addressed – a rate which is not related to the carrier frequency on the SA808, hence the term ‘asynchronous method of PWM generation’. The waveform values obtained from the ROM may also be scaled to produce a variable voltage amplitude.

Fig.3 shows the triangular carrier waveform together with the stepped waveform which results from sampling the outputs of the ROM at the peaks and troughs of the carrier. (A continuous power waveform is also shown for reference.) It can be seen that the PWM edges of the waveform below are obtained at the points where the carrier and the sampled power waveform intersect. The carrier frequency is selectable to over 24kHz (assuming the maximum clock frequency of 25MHz is used), enabling ultrasonic operation for noise critical applications. With a 25MHz clock, power frequency ranges to over 4kHz are possible. The output phase sequence of the PWM outputs can also be changed to allow both forward and reverse motor operation. (Phase order convention for “forward” is Red-Yellow-Blue, and “reverse” is Red-Blue-Yellow.)

PWM output pulses can be ‘tailored’ to the inverter characteristics by defining the minimum allowable pulse width, (the SA808 will delete all shorter pulse from the ‘pure’ PWM pulse train), and the pulse delay (underlap) time, without the need for external circuitry. This gives cost advantages in both component savings and in allowing the same PWM circuitry to be used for the control of different motor drive circuits simply by changing the values downloaded via the serial interface.

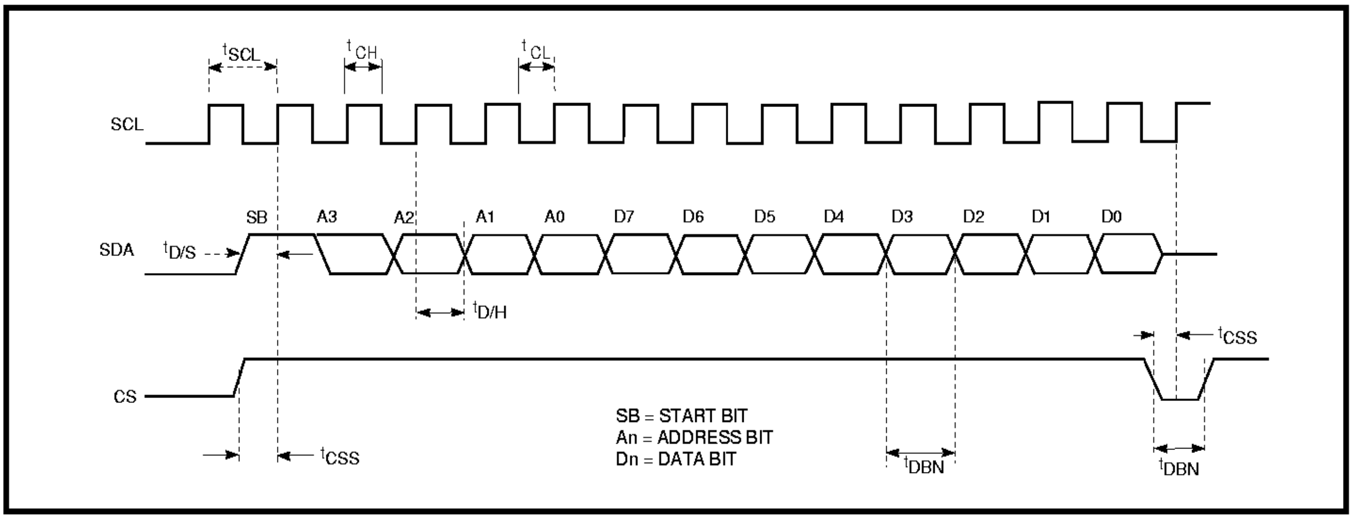


Fig.4 Serial interface timing diagram

Serial Interface Protocol

All control and operational parameters of the SA808 are accessed via a 3-wire, write-only MICROWIRE style serial interface. The serial clock may run at any speed up to 750kHz allowing data to be transferred at a maximum rate of 50kbytes/s (14 cycles are required per byte - see Fig.4).

Pins CS, SCL and SDA are chip select, clock and serial inputs for the serial interface respectively. All of these inputs are debounced, requiring data to remain in a stable state for 15f_{CLK} cycles before a change is registered inside the device.

The SDA input idles at a low level. With the chip selected (CS = 1), the SA808 reads data from SDA on successive rising edges at the SCL input (assuming that both inputs have been stable for 15 master clock cycles). The chip must be de-selected (CS = 0) for the next rising edge on SCL after a data word has been transmitted in order for the data to be latched inside the SA808. Providing that the data input remains low after the data word has been sent, the de-selection pulse need not follow the data word immediately. However, any new high value detected on the data input will be regarded as a new start bit and the first word will be overwritten. If the chip is de-selected at any time during a transmission, any data transmitted from the start bit to that point will be ignored.

A data word consists of a single high start bit, followed by a 4-Bit register address, MSB first (the instruction), followed by 8-Bits of data (also MSB first). See Table 3 for valid register addresses. Attempts to write to an invalid register address result in no action.

Note that no provision is made for a time-out or for checking or acknowledging incoming data.

Serial Interface Control Alogorithm

The action taken upon receiving a data word depends upon the register written. It is initiated by the rising edge of the crystal clock following the chip-select input (CS) going low and is detailed in Table 2. The complexity of this table arises from the use of 8-Bit serial data words to program 16 or 24-Bit values simultaneously.

Parameter	Symbol	Min.	Typ.	Max.	Units
Chip select setup time	t_{CSS}	2/f_{CLK}	-	-	s
Chip select hold time	t_{CSH}	8/f_{CLK}	-	-	s
Clock high time	t_{CH}	20/f_{CLK}	-	-	s
Clock low time	t_{CL}	20/f_{CLK}	-	-	s
Data in setup time	$t_{D/S}$	2/f_{CLK}	-	-	s
Data in hold time	$t_{D/H}$	2/f_{CLK}	-	-	s
Data valid (debounce) time	t_{DBN}	16/f_{CLK}	-	-	s
Clock period	t_{SCL}	50/f_{CLK}	-	-	s

Note: All timings in terms of crystal clock f_{CLK}

Table 1 - Serial interface timing characteristics

Register	Action
Control Setup1 Setup2 Setup3 Kay	Load incoming data to the appropriate internal register.
SpeedTop	Hold incoming data in a temporary register until data is written into the SpeedBot register.
SpeedBot	If VF = 0: (amplitude data is taken from Gradient register and not calculated) • If the Gradient temporary register contains unused data, make it the new amplitude value. • If the SpeedTop temporary register contains unused data, write it to the top 8 bits of the frequency demand register. • Load the incoming data into the bottom 8 bits of the frequency demand register. If VF = 1: (amplitude data is calculated using linear or fan-law characteristic) • If the SpeedTop temporary register contains unused data, write it to the top 8 bits of the frequency demand register. • Load the incoming data into the bottom 8 bits of the frequency demand register.
Gradient	If VF = 0: (amplitude data is taken from Gradient register and not calculated) • Hold incoming data in a temporary register until data is written into the SpeedBot register. If VF = 1: (using linear or fan-law characteristic) • Load incoming data to the appropriate internal register
Pedestal	• Load incoming data to the appropriate register
Register addresses 9 to 15	No action

Table 2 - Serial interface register operation

Frequency values programmed from the serial interface use the 16-Bit PFS words. The lower byte of the speed value may be updated without requiring other values to be set up. If the data for the upper frequency byte is sent, it is stored temporarily and only takes effect when data for a new lower byte is written.

If direct control of the amplitude of the waveform is required, new values must be transferred at the same time as the corresponding power frequency information. The amplitude value is written to the Gradient register address and held until the lower PFS byte is written or until both upper and lower PFS bytes have been written. In this mode, new frequency (low byte or both high and low bytes) may be written without updating the amplitude value, but a new frequency must be written in order to update the amplitude (the frequency value need not change, but the process of writing a new value must be executed).

Address	7	6	5	4	3	2	1	0	Register
0000	RST	$\overline{\text{CR}}$	TM3	VF	TM2	TM1	$\overline{\text{INH}}$	FB/R	Control
0001	CFS2	CFS1	CFS0	WS1	WS0	FRS2	FRS1	FRS0	Setup1
0010	PDT6	PDT5	PDT4	PDT3	PDT2	PDT1	PDT0	FC	Setup2
0011	PDY5	PDY4	PDY3	PDY2	PDY1	PDY0	ZTH1	ZTH0	Setup3
0100	PFS15	PFS14	PFS13	PFS12	PFS11	PFS10	PFS9	PFS8	SpeedTop
0101	PFS7	PFS6	PFS5	PFS4	PFS3	PFS2	PFS1	PFS0	SpeedBot
0110	GRAD7	GRAD6	GRAD5	GRAD4	GRAD3	GRAD2	GRAD1	GRAD0	Gradient
0111	PED7	PED6	PED5	PED4	PED3	PED2	PED1	PED0	Pedestal
1000	KAY7	KAY6	KAY5	KAY4	KAY3	KAY2	KAY1	KAY0	Kay

Table 3 Serial interface register map

Serial Interface Register Map

Table 3 shows the serial interface register address map. Subsequent sections define the purpose of all of the bits.

Serial interface Reset Conditions

When the external $\overline{\text{RESET}}$ is taken low the control register bits take the following values:

RST = 0, $\overline{\text{CR}}$ = 0, TM3 = 0, VF = 1, TM2 = 0, TM1 = 0, $\overline{\text{INH}}$ = 0, FB/R = 0

Writing a logic 1 to the software reset bit (RST) has a similar effect except that RST itself remains unaffected.

All other register values are not affected by either kind of reset condition.

Speed Control (PFS, R_{ACC}, R_{DEC} components)

Speed, or power frequency control is achieved for the SA808, by writing values to the PFS word in the Speed Top and Speed Bot registers. As indicated in a previous section, the PFS value may be updated by writing to only the Speed Bot register or by writing both Speed Top and Speed Bot registers in that order.

Within the chosen frequency range (see later), the value of PFS corresponds to a power frequency given by the equation:

$$f_{POWER} = \frac{f_{range}}{65535} \times PFS$$

A new PFS value may be treated in one of two ways according to the operation mode selected using the R_{ACC} and R_{DEC} inputs (see Table 4).

If the R_{ACC} and R_{DEC} inputs are both tied to ground then a new value of PFS written via the serial interface immediately becomes the new output power frequency value. All power frequency changes (acceleration and deceleration) are therefore under the control of the external processor.

R_{ACC}	R_{DEC}	Mode
Ext.RC	Ext.RC	Acceleration, deceleration enabled
$<0.125V_{DD}$	$<0.5V_{DD}$	Acceleration, deceleration defeated
$0.125V_{DD}$	$>0.5V_{DD}$	Must not be used

Table 4 Speed control modes

If, however, the R_{ACC} and R_{DEC} pins are not constrained to be below $0.125V_{DD}$ and $0.5V_{DD}$ respectively, then the SA808's patented acceleration and deceleration alogorithm may be used. The values of PFS written via the serial interface are now used as target or setpoint speeds and the SA808 will arrange for smooth changes between the new setpoint and the previous value of power frequency.

Additional over-voltage and over-current protection features are available as part of this algorithm, which is described in the next section.

The use of R_{ACC} and R_{DEC} pins to select modes imposes a requirement that when acceleration / deceleration oscillators are used, the $\overline{\text{RESET}}$ input must be held low long enough to guarantee that the 0.125 V_{DD} defeat threshold is crossed. Failure to do this may result in an incorrect mode being selected.

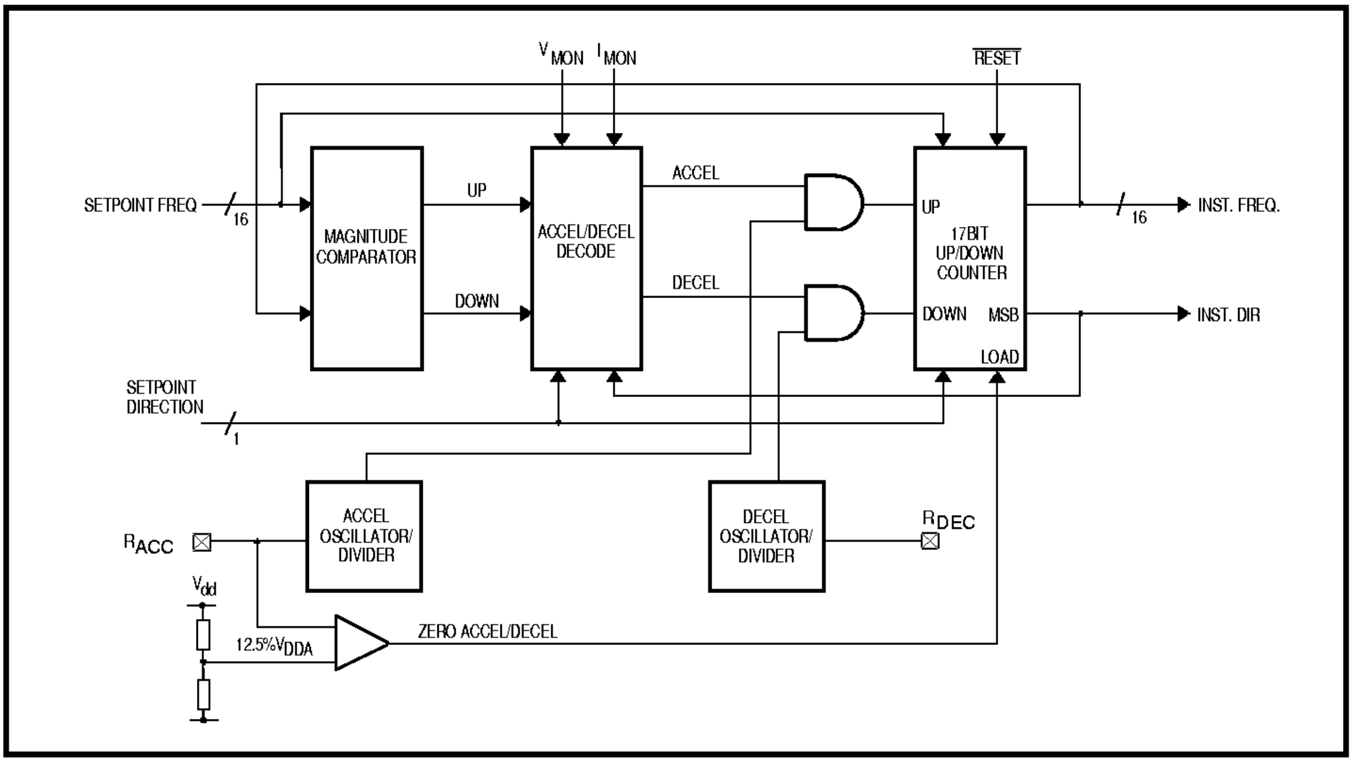


Fig.5 Acceleration/deceleration logic

Acceleration/Deceleration Logic

The acceleration/deceleration logic consists of a 16-bit magnitude comparator and an 17-bit up/down counter clocked by the output from the Accel or Decel oscillators (see Fig.5). The acceleration and deceleration rates are seperately selectable using external timing components. A resistor (R) is connected from the R_{ACC} pin to V_{DD} and a capacitor (C) from the R_{ACC} pin to V_{SS}. Similarly a separate RC network is connected to the R_{DEC} pin. The values of the resistors and capacitors may be the same or different to produce equal or unequal acceleration and deceleration times.

The time taken to accelerate from zero to the maximum speed value determined by the selected Power Frequency range (f_{RANGE}), or to decelerate from this value to zero is given by the expression:

$$t_{ACC/DEC} = 65536 \times R.C \times \ln 3$$

$$\cong \mathbf{72.10^3 \times R.C}$$

where $\mathbf{5K\Omega \leq R \leq 100K\Omega}$
$\mathbf{1nF \leq C \leq 25nF}$

If the R_{ACC} pin is connected to a level $<0.125V_{DD}$, and R_{DEC} $<0.5V_{DD}$, then the Accel/Decel function is defeated and any changes in Power Frequency demand are instantaneous. This makes the device suitable for waveform generation applications such as Static Inverters.

It is possible to drive the R_{ACC} and R_{DEC} inputs directly with an external clock signal(s), instead of using the RC oscillators. Typical input levels are $V_{IL} = 0.3V_{DD}$ and $V_{IH} = 0.6V_{DD}$ but care must be taken to ensure that the low level does not go below $0.125V_{DD}$ and the high level above $0.75V_{DD}$. The former may cause the device operating mode to be changed inadvertently; the latter may cause contention on the pin as the internal oscillator pull-down transistor switches on.

The magnitude comparator compares the scalar frequency demand from the serial interface with the instantaneous scalar frequency output from the up/down counter. The result is a 2-bit output as follows:-

UP	DOWN	Result
0	0	Same, No ACCEL or DECEL
0	1	LOWER
1	0	HIGHER
1	1	ILLEGAL STATE

Table 5 Acceleration/deceleration decoder

These 2 bits are used in conjunction with the V_{MON} and I_{MON} pins and the sign bits to obtain an absolute indication of the required acceleration/deceleration, according to the following rules:-

1) If the V_{MON} condition is invoked ($V_{MON} \geq 0.5V_{DD}$),any acceleration/deceleration will be prevented until V_{MON} falls below $0.5V_{DD}$. This condition has highest priority.

CONDITION	UP	DOWN	DIRECTION. BIT (FB/R)	INSTANT-ANEOUS DIRECTION	ACCEL	DECEL
					Active High	
1.	X	X	0	1	0	1
2.	X	X	1	0	0	1
3.	0	0	0	0	0	0
4.	0	0	1	1	0	0
5.	0	1	0	0	0	1
6.	0	1	1	1	0	1
7.	1	0	0	0	1	0
8.	1	0	1	1	1	0
9.	1	1	X	X	ILLEGAL STATE	

Table 6: Acceleration/deceleration logic conditions

Normal acceleration/deceleration will continue when V_{MON} falls below $0.5V_{DD}$, as dictated by the rest of the algorithm.

This input is used to prevent excessive deceleration rates from regenerating too much power into the external power switching circuitry and causing an overvoltage condition.

2) If I_{MON} is invoked (i.e. $\geq 0.5V_{DD}$) the scalar value of the instantaneous frequency is reduced at the predetermined deceleration rate irrespective of the states of UP and DOWN. If the instantaneous frequency attains the value zero whilst I_{MON} is $\geq 0.5V_{DD}$ the PWM outputs are turned off (logic 0) for the duration of this condition (this prevents undue motor heating whilst at rest). No acceleration or deceleration is allowed once the frequency has attained the value zero. When I_{MON} is released normal acceleration/deceleration resumes as required by the prevailing conditions. In addition, the PWM outputs are re-enabled.

This condition has lower priority than V_{MON} since the act of decelerating due to I_{MON} being taken high may itself invoke the V_{MON} condition.

This input is intended to prevent too high an acceleration rate from causing an overcurrent/overheat situation at the switching devices.

3) If I_{MON} and V_{MON} are inactive, the algorithm takes the UP and DOWN outputs from the magnitude comparator, together with the required direction (phase order) from the logic state of the FB/R bit in the Control Register and the instantaneous sign from the up/down counter to compute whether acceleration or deceleration is required:-

(a)If the required and instantaneous signs are different, the first requirement is to decelerate to rest since no change of direction is possible until this has occurred. Therefore, so long as this condition holds, decelerate (see 1 and 2 in Table 6).

(b)If the signs are the same and UP and DOWN are both zero then the required and instantaneous frequencies are matched both in terms of direction and magnitude, therefore neither acceleration or deceleration is required (see 3 and 4 in Table 6).

(c) If the signs are the same but either UP or DOWN is high then the phase order (direction of rotation), does not need to change, but the magnitude does. Therefore, if UP is high, accelerate or if DOWN is high, decelerate (see 5,6,7 and 8 in Table 6).

(d) UP and DOWN both high is an illegal state since both conditions cannot exist concurrently.

The ACCEL and DECEL signals are gated with the Accel or Decel oscillator output to increment or decrement the frequency.

This algorithm is shown below as a flow diagram, Fig.6.

The counter is a synchronous up/down counter, the most significant bit being the instantaneous sign or direction bit. The reset condition of this block is to force the instantaneous sign and frequency to be forward and zero respectively. Whenever the setpoint frequency is equal to zero and the instantaneous frequency reaches zero the phase outputs are inhibited (forced to zero). When starting from this state, (which is also the state immediately following power-up), the top phase outputs are temporarily disabled and the bottom phase outputs pulsed high for a whole carrier cycle before normal PWM operation is resumed. This is to allow a time for charging the top side capacitors in a bootstrapped driver circuit. This sequence is achieved without generating pulses shorter than the pulse deletion time.

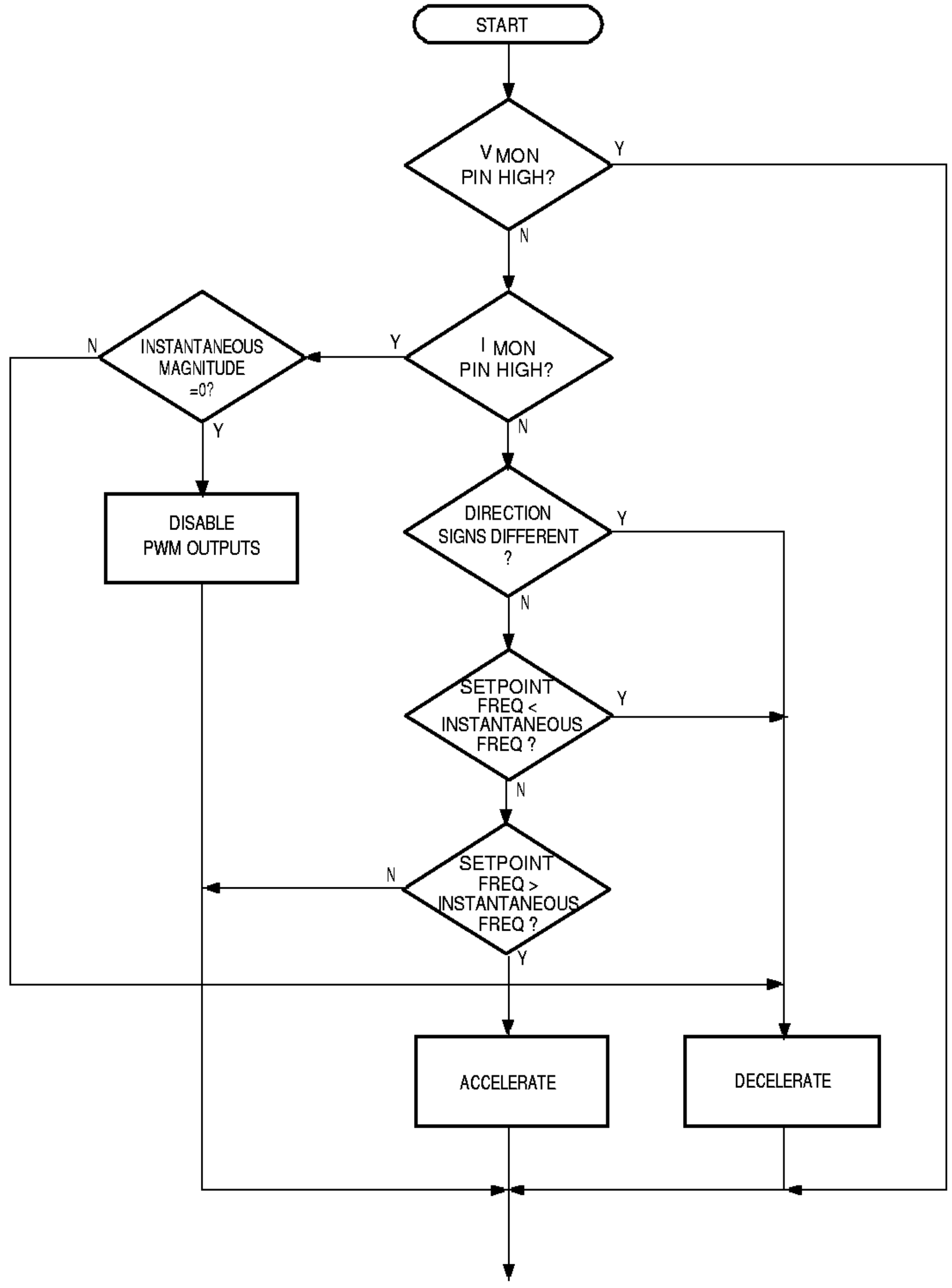


Fig.6 Acceleration/deceleration logic flow diagram

Voltage/Frequency Control (VF, FC, GRAD, KAY, PED)

In order to ensure adequate control of motor flux, the voltage across the motor coils must be controlled at all frequencies. This is achieved by scaling the power waveform before it is compared with the carrier waveform.

The SA808 offers 3 ways of controlling this scaling factor:

- The external processor may calculate power frequency and amplitude values and download them via the serial interface to be applied to the PWM core simultaneously.
- The SA808 can calculate the power instantaneous amplitude as a linear function of the power frequency using user specified parametrics (see Fig.7).
- The SA808 can calculate the power amplitude as a quadratic function of the instantaneous power frequency using user specified parameters (see Fig.8). This is most appropriate for fan/pump applications and is usually referred to as fan-law.

These options are selected using the VF and FC bits as shown in Table 7 and illustrated in Fig.9

VF	FC	Power Amplitude Control
0	X	External v/f control
1	0	Linear v/f characteristic selected
1	1	Fan-law v/f characteristic selected

Table 7

External V/F Control

If the VF bit is low then the external processor must calculate amplitude scaling factors. These are written to the Gradient register (GRAD) and are transferred only when a new power frequency value is written. The amplitude scaling factor A is given by the equation:

$$A(\%) = \frac{GRAD}{255} \times 100$$

Linear V/F Control

Fig.7 shows the linear characteristic implemented in the SA808.

A variable 'pedestal' voltage may be applied at zero frequency in order to overcome copper losses (which tend to dominate the overall losses at low speeds). The value should be chosen carefully so that the power dissipation in the motor at low frequencies is not excessive.

The voltage then increases in direct proportion to the frequency, up to the required 'Base (or baseplate) frequency'. This is often 50Hz or 60Hz, but may be

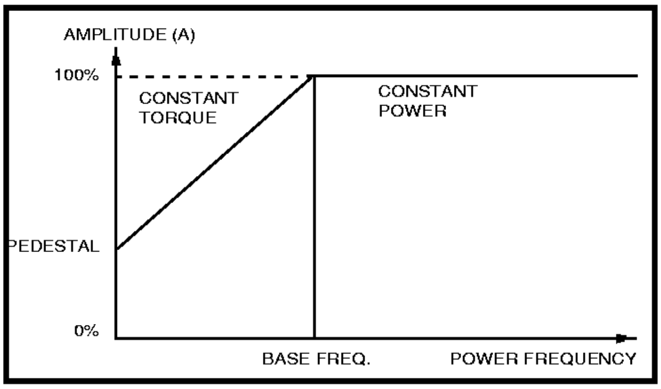


Fig.7 Linear characteristic

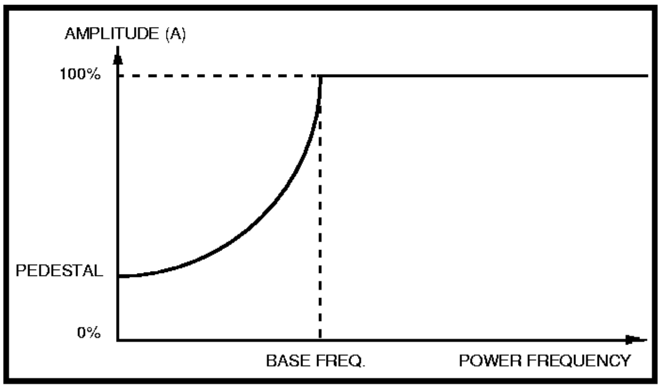


Fig.8 Fan-law characteristic

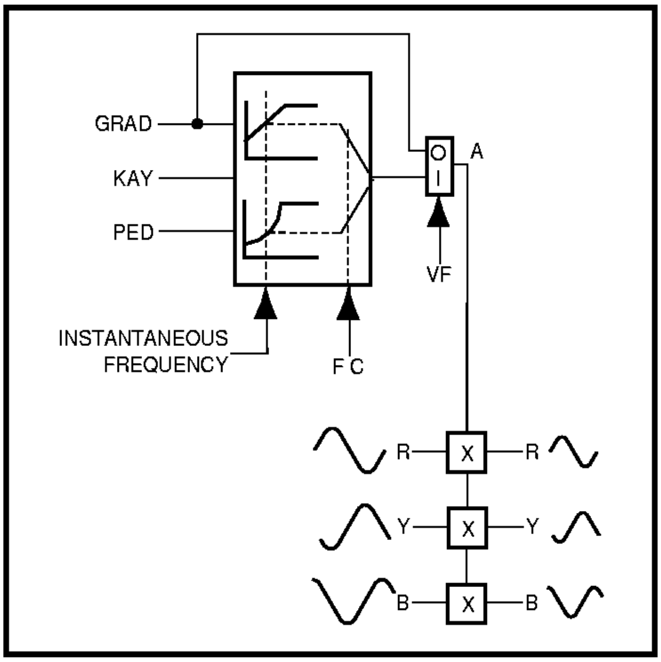


Fig.9 Voltage/frequency control diagram

selected to be anywhere in the frequency range. Frequencies up to the Base frequency are said to be in the Constant Torque region with Linear V/f operation.

Beyond the Base frequency, the amplitude is held at its maximum value. This inevitably leads to a fall in the generated torque with increasing frequency, hence this is termed the Constant Power region.

In the SA808, at any instantaneous frequency,

$$A(\%) = \left[\frac{(GRAD\ .\ F)}{16} + PED \right] x\ \frac{100}{255}$$

where F is the top 8 bits of the instantaneous frequency

i.e. $f(Hz) = \frac{F}{255}\ x\ f_{RANGE}\ (Hz)$

and if A > 100% then A = 100%

The parameter PED is calculated according to the equation:

$$Pedestal(\%) = \frac{PED \text{ x } 100}{255}$$

GRAD is also an 8 bit parameter which defines the slope of the V/f characteristic in the constant torque region of motor operation. This is usually calculated in terms of the motor baseplate frequency and the pedestal value as follows:

$$GRAD = \frac{(255 - PED) \text{ x } f_{RANGE}}{16 \text{ x } f_{base}} \quad \text{where GRAD} \le 255.$$

Note: i) It is possible to defeat the V/f profile by setting PED=255.

ii) The parameter KAY is not used when the linear characteristic is selected.

Fan-law V/F Control

Fig.8 shows the Fan-law characteristic implemented in the SA808.

The PED parameter has exactly the same function as defined in the linear V/f section. In the constant torque region for fan-law, the amplitude is related to the instantaneous frequency by the equation:

$$A\% = \left\{ \frac{1}{8192} \cdot GRAD \cdot F^2 + \frac{1}{512} \cdot KAY \cdot F + PED \right\} x \frac{100}{255}$$

where F is the top 8 bits of the instantaneous frequency

i.e. $f(Hz) = \frac{F}{255}\ x\ f_{RANGE}\ (Hz)$

and if A > 100% then A = 100%

and if $GRAD \cdot F + 16 \cdot KAY < 0$ then $A = PED \text{ x } \frac{100}{255}$

GRAD is an 8 bit value. KAY is of 7 bits magnitude, with the MSB providing a sign bit, (0 - positive, 1 - negative).

OTHER CONTROL FUNCTIONS (RST, $\overline{\text{CR}}$, $\overline{\text{INH}}$, FB/R, TM1-3)

This section describes the operation of the remaining bits in the Control register.

Software Reset (RST)

The software reset bit (RST) provides a facility to reset the device from the microprocessor interface instead of using the $\overline{\text{RESET}}$ pin. When active (high), the chip is put into the same state as that when $\overline{\text{RESET}}$ is asserted except the RST bit is not forced low. The reset condition may be cleared by writing '0' to the RST bit using the microprocessor interface, or by toggling the $\overline{\text{RESET}}$ pin.

Counter Reset ($\overline{\text{CR}}$)

This facility allows the internal power frequency phase counter to be set to 0° (red phase) whilst Counter Reset ($\overline{\text{CR}}$) is low. Normal frequency control is suspended, the red phase outputs have a 50% duty cycle and yellow and blue phases outputs have duty cycles corresponding to phases of +120° and –120° respectively.

Output Inhibit ($\overline{\text{INH}}$)

All PWM outputs become low when $\overline{\text{INH}}$ is asserted low. When $\overline{\text{INH}}$ is deasserted (high) the top phase outputs are temporarily disabled and the bottom phase outputs pulsed high for a whole carrier period, before normal PWM operation is resumed. Both assertion and deassertion of the inhibit condition are achieved without generating pulses shorter than the pulse deletion time.

Forward/Reverse (FB/R)

The phase sequence of the three phase PWM output waveforms is controlled by the Forward/Reverse bit FB/R.

The actual effect of changing this bit from 0 (forward) to 1 (reverse) is to reverse the power frequency phase counter from incrementing the phase angle to decrementing it. The required output waveforms are all continuous with time during a forward/reverse change.

In the forward mode the output phase sequence is red-yellow-blue and in the reverse mode the sequence is blue-yellow-red.

Test Mode Selection (TM1,TM2,TM3)

These register bits are used to select a factory test mode. They only have an effect if the correct procedure is followed to invoke test mode. (Factory use only).

Initialisation Parameters

This section describes the parameters which are normally downloaded over the serial interface immediately following power-up, and are not changed during operation.

Carrier Frequency (CFS)

The carrier frequency is a function of the externally applied clock frequency and a division ratio *n*, determined by the 3-bit CFS word set during initialisation. The values of *n* are selected as shown in Table 8.

CFS word	111	110	101	100	011	010	001	000
Value of *n*	7	6	5	4	3	2	1	0

Table 8 Values of clock division ratio n

The carrier frequency, f_{CARR}, is then given by:

$$f_{CARR} = \frac{f_{CLK}}{512 \times 2^{n+1}}$$

where f_{CLK} = clock input frequency.

Power Frequency Range (FRS)

In order to optimise the resolution of the SA808 the required range of power frequencies may be selected using this parameter. Within the selected range the frequency may be set with 16-bit resolution. It is recommended to use the next higher power frequency range than the maximum required motor frequency. The power frequency range defines the maximum limit of the power frequency. The operating power frequency is controlled by the 16-bit Frequency word from the Accel/Decel logic. The power frequency range is a function of the carrier waveform frequency (f_{CARR}) and a multiplication factor *m*, determined by the 3-bit FRS word. The value of *m* is determined as shown in Table 9.

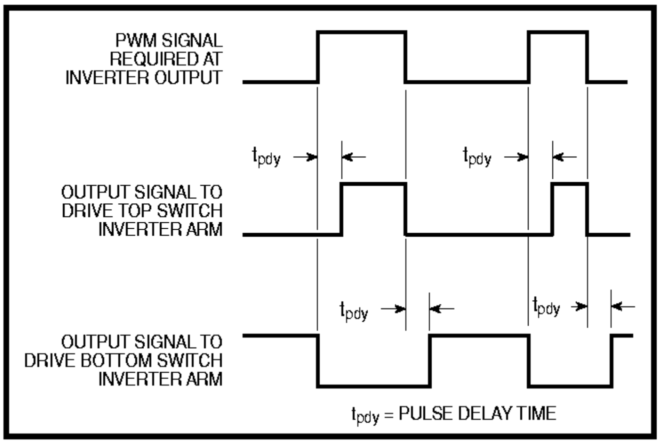


Fig.12 Effect of pulse delay

FRS word	110	101	100	011	010	001	000
Value of *m*	6	5	4	3	2	1	0

Table 9 Values of clock division ratio m

The power frequency range, f_{RANGE}, is then given by:

$$f_{RANGE} = \frac{f_{CARR} \times 2^m}{384}$$

where f_{CARR} = carrier frequency.

Pulse Delay Time (Underlap) (PDY)

For each phase output there are two PWM control signals controlling the upper and lower switches in the inverter. In theory these two control signals are always complementary. However, due to the finite and non-equal turn-on and turn-off times of power semiconductors, it is necessary to provide a short delay time during which both outputs are off in order to avoid a transient short circuit through the two devices. This period is known as ‘underlap’. The pulse delay affects all six PWM outputs by delaying the rising edge of each output by an equal amount. The pulse delay time is a function of the carrier waveform frequency and the PDY value, defined by the 6-bit pulse delay time word. The value of PDY is selected as shown in Table 10.

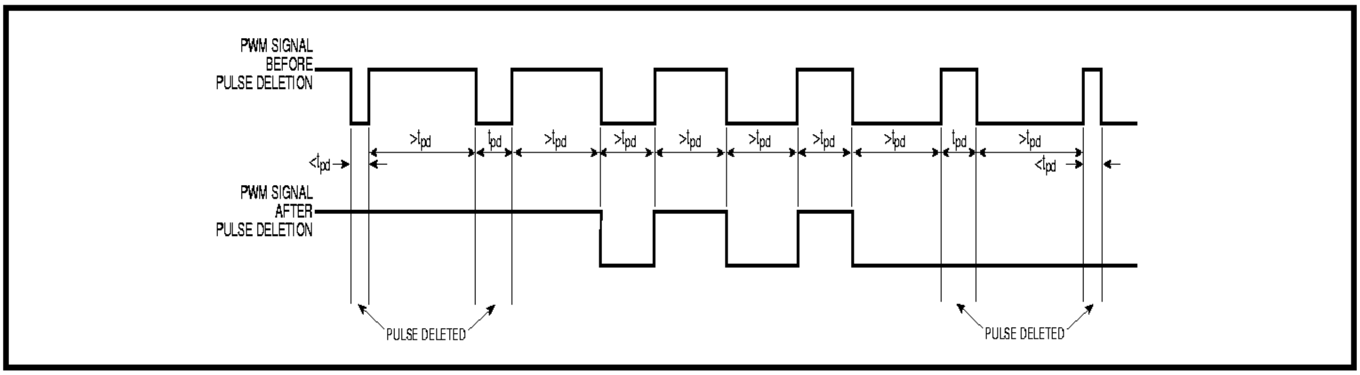


Fig.13 Effect of pulse deletion

PDY word	111111	111110	...etc...	000000
Value of *PDY*	63	62	...etc...	0

Table 10 Values of PDY

The pulse delay time, t_{pdy}, is then given by:

$$t_{pdy} = \frac{63 - \text{PDY}}{f_{CARR} \times 512}$$

where f_{CARR} = carrier frequency.

Fig.12 shows the effect of pulse delay on a pure PWM waveform.

It should be noted that as the pulse delay circuit follows the pulse deletion circuit (see Fig.2), the minimum pulse width seen at the PWM outputs will be shorter than the pulse deletion time set set using the PDT parameter. The actual shortest pulse generated is given by: $t_{pd} - t_{pdy}$.

Pulse Deletion Time (PDT)

Pure PWM pulse trains contain pulses which vary in duty cycle from 0% to 100%. Therefore pulse widths may become very small indeed. In practice short pulses have no useful purpose since the power semiconductors cannot fully turn on/off within the active period of the pulse. Such pulses only increase the power dissipation in the power devices. Therefore a minimum pulse width may be defined. All pulses shorter in duration than this are eliminated from the PWM train, whether they are low-going or high-going.

To eliminate short pulses the true PWM pulse train is passed through a pulse deletion circuit. The pulse deletion circuit compares pulse widths with the pulse deletion time set in the register. If a pulse (either positive or negative) is greater than the pulse deletion time, it is passed through unaltered, otherwise the pulse is deleted. The pulse deletion time, t_{pd} , is a function of the carrier wave frequency and PDT, defined by the 7-bit pulse deletion time word. The value of PDT is selected as shown in Table 11.

PDT word	1111111	1111110	...etc...	0000000
Value of *PDT*	127	126	...etc...	0

Table 11 Values of PDT

The pulse deletion time, t_{pd}, is then given by:

$$t_{pd} = \frac{127 - \text{PDT}}{f_{CARR} \times 512}$$

where f_{CARR} = carrier frequency.

Fig.13 shows the effect of pulse deletion on a pure PWM waveform.

Waveform Selection

Three waveforms are included as standard with the SA808. A pure sinewave is available for applications where waveform purity is important such as static inverter power supplies. For three phase induction motor control a Triplen waveform is included which provides maximum utilisation of the inverter DC link voltage using an harmonic injection technique. Also for motor control, a Deadbanded Triplen waveform may be selected which, in addition to providing DC link voltage boost, also acts to reduce the number of switching events in the power semiconductors to reduce the switching loss. A symmetrical technique is used to ensure that each power semiconductor benefits to the same degree.

Two bits, WS0 and WS1, are used to define the power waveform, according to Table 12:

WS1	WS0	Waveform
0	0	Sinusoid (default)
0	1	Triplen (harmonic injection)
1	0	Deadbanded Triplen (switching loss reduction)
1	1	Reserved

Table 12 Waveform selection

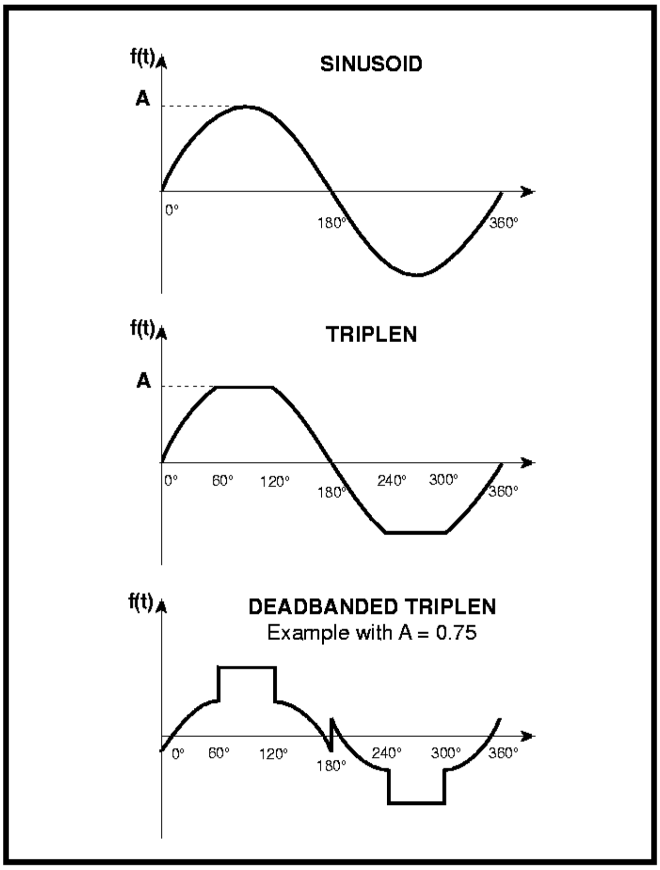


Fig.14 Power waveforms

The waveforms may be described by the following mathematical relationships and are shown graphically in Fig.14

Sinusoid:

$f(t) = A \sin(\omega t)$ where A = amplitude
ω = angular displacement

Triplen:

f(t)	Valid
$f(t) = A(2.\sin(\omega t + 30°) - 1)$	$0° \le \omega t < 60°$
$f(t) = A$	$60° \le \omega t \le 120°$
$f(t) = A(2.\sin(\omega t - 30°) - 1)$	$120° \le \omega t < 180°$
$f(t) = A(2.\sin(\omega t + 30°) + 1)$	$180° \le \omega t < 240°$
$f(t) = -A$	$240° \le \omega t \le 300°$
$f(t) = A(2.\sin(\omega t - 30°) + 1)$	$300° \le \omega t < 360°$

Deadbanding:

Below are the modulating functions for the Deadbanded Triplen waveform. These have been normalised and scaled to give a peak line voltage (phase to phase) of 2A. All the 3 phases are shown for clarity, f(t), g(t) and h(t).

Function	Valid
$f(t) = 2A.\sin(\omega t + 30°) - 1$ $g(t) = -1$ $h(t) = 2A.\sin(\omega t + 90°) - 1$	$0° < \omega t \le 60°$
$f(t) = 1$ $g(t) = 1 + 2A.\sin(\omega t - 150°)$ $h(t) = 1 + 2A.\sin(\omega t + 150°)$	$60° < \omega t \le 120°$
$f(t) = 2A.\sin(\omega t - 30°) - 1$ $g(t) = 2A.\sin(\omega t - 90°) - 1$ $h(t) = -1$	$120° < \omega t \le 180°$
$f(t) = 1 + 2A.\sin(\omega t + 30°)$ $g(t) = 1$ $h(t) = 1 + 2A.\sin(\omega t + 90°)$	$180° < \omega t \le 240°$
$f(t) = -1$ $g(t) = 2A.\sin(\omega t - 150°) - 1$ $h(t) = 2A.\sin(\omega t + 150°) - 1$	$240° < \omega t \le 300°$
$f(t) = 1 + 2A.\sin(\omega t - 30°)$ $g(t) = 1 + 2A.\sin(\omega t - 90°)$ $h(t) = 1$	$300° < \omega t \le 360°$

Line output voltages appearing across the load are:

$Vfg = f(t) - g(t)$
$Vgh = g(t) - h(t)$
$Vhf = h(t) - f(t)$

The line voltage waveforms are sinusoidal.

Hardware Input/Output Functions

SET TRIP Input

The SET TRIP allows an external, active high event to provide a rapid shutdown of the PWM signals. When the SET TRIP input is taken to a logic 1, a delay of 2-3 crystal clock cycles is triggered internally. If, during this time, the SET TRIP input has remained high, then the PWM outputs will be inhibited and the $\overline{\text{TRIP}}$ acknowledge output will become active.

This condition can only be cleared by applying a $\overline{\text{RESET}}$ pulse. The SET TRIP input has an internal pulldown. However it is recommended that this input is tied low if it is not used.

Output Trip Status

The $\overline{\text{TRIP}}$ output indicates the status of the trip latch and is active low. It does not become active until the end of the SET TRIP delay time (assuming that the SET TRIP input stays high for this period).

This output is capable of directly driving a LED through a current limiting resistor for display purposes.

$\overline{\text{RESET}}$ Input

When $\overline{\text{RESET}}$ input is taken low it performs the following functions:

i) All PWM outputs are forced low.

ii) All internal counters are reset to zero.

iii) The instantaneous frequency word is set to zero and the direction bit to 0 (forward).

When $\overline{\text{RESET}}$ is taken high:

iv) Test mode can be entered by application of a special code sequence. (Factory test use only).

v) The inhibit is removed from the PWM outputs and the trip latch set to inactive, provided that the SET TRIP input is inactive. The removal of the inhibit forces the phase bottom outputs to be driven high for a whole carrier cycle before the phase top outputs are enabled.

As a consequence of (iii) to (v) the device will be re-enabled and will re-accelerate from zero to the set frequency when reset after a TRIP event.

$\overline{\text{RESET}}$ input should be held low at power up for a short period, to allow the internal counters etc. to be reset. (minimum one f_{CLK} cycle). However when using the Accel/Decel oscillators, the $\overline{\text{RESET}}$ input must be kept low long enough, to ensure that the $0.125V_{DD}$ defeat threshold is crossed on the R_{ACC} input. This is determined by the charge rate of the external RC time constant, **(NOTE - Failure to do this can result in an incorrect mode being selected.)**

XTAL1/XTAL2

These pins are for a crystal or ceramic resonator, if used. Alternatively, XTAL1 may be used as an input for an externally generated clock signal. Any external input is constrained to having a mark/space ratio of 1:1 ± 20% to ensure correct device operation.

A small capacitor should be connected from each of these pins to the V_{SS} supply rail when using a crystal or ceramic resonator. The capacitor value is dependant on the crystal characteristics. A suitable value for common crystal types is 22pF to 56pF.

V_{MON} Input

Analog input which prevents any acceleration/deceleration events when $\geq V_{DD}/2$. This input has higher priority than the I_{MON} pin, and the V_{MON} condition therefore prevails if both V_{MON} and I_{MON} are active simultaneously.

Test Input

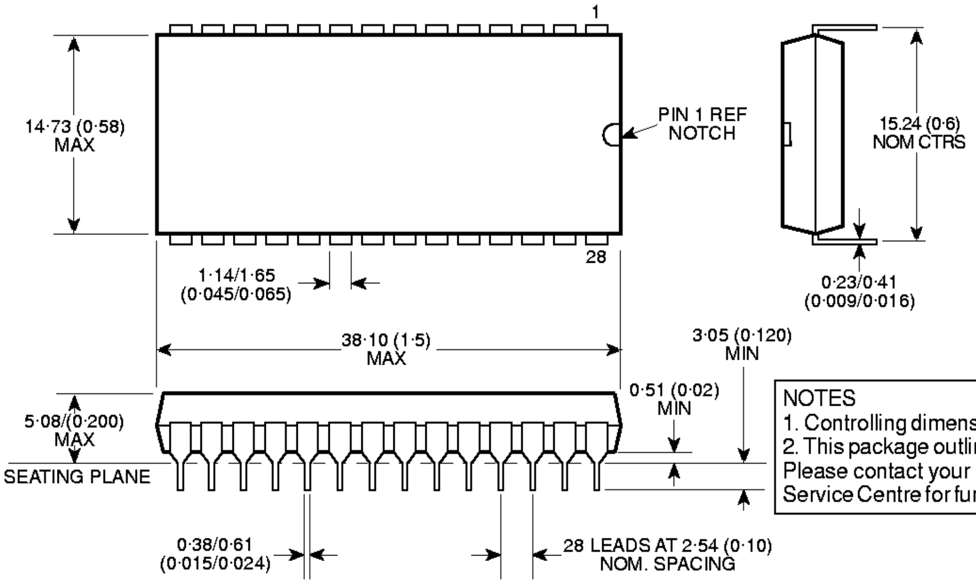
This input is used in factory test mode only, but must be tied either high or low to avoid excessive current consumption.

I_{MON} Input

Analog input which causes the instantaneous output frequency to reduce at the predetermined deceleration rate when $\geq V_{DD}/2$. If the frequency is reduced to zero whilst this input is $\geq V_{DD}/2$, the PWM outputs are temporarily turned off and the deceleration inhibited. Normal acceleration may resume when I_{MON} is below $\geq V_{DD}/2$. In addition, the PWM outputs are re-enabled in the event that the frequency had fallen to zero.

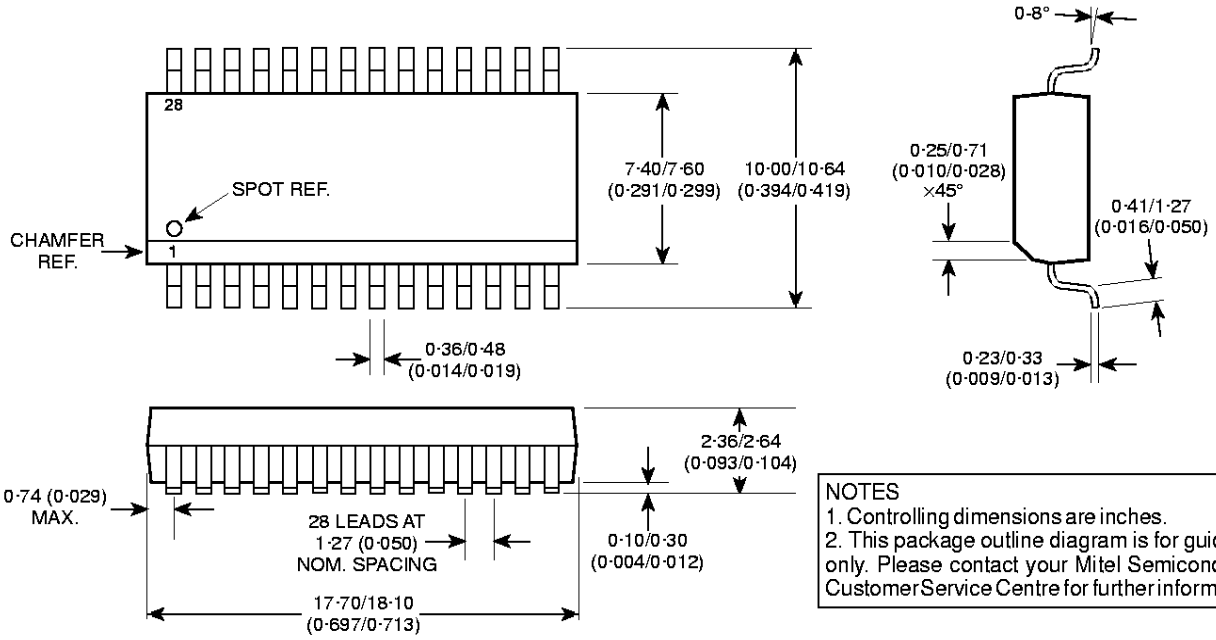
Package Details

Dimensions are shown thus: mm (in). For further package information, please contact your local Customer Service Centre.



NOTES
1. Controlling dimensions are inches.
2. This package outline diagram is for guidance only. Please contact your Mitel Semiconductor Customer Service Centre for further information.

28-LEAD PLASTIC DIL – DP28



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28-LEAD MINIATURE PLASTIC DIL - MP28

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