HD66702 LCD-II/E20
(Dot Matrix Liquid Crystal Display Controller and Driver)

—Preliminary—

Description

The LCD-II/E20 (HD66702) dot matrix liquid crystal display controller and driver LSI displays alphanumerics, kana characters, and symbols. It drives a dot matrix liquid crystal display under 4-bit or 8-bit microprocessor control. Since all the functions required for dot matrix liquid crystal display drive are internally provided on one chip, a small system can be configured with this LSI.

A single LCD-II/E20 can display up to two lines, each of 20 characters. The addition of driver LSI HD44100s enables a maximum display of two lines, each of 40 characters.

The LCD-II/E20 of 3-V power supply (whose development is under consideration) is suitable for any portable battery-driven apparatus requiring low power dissipation.

Ordering Information

Type No.	Package	Operating Voltage
HCD66702	144-pin bare chip	4.5 to 5.5 V
HCD66702L	144-pin bare chip	2.7 to 3.3 V

Features

- 5 × 7 and 5 × 10 dot matrix liquid crystal display controller and driver
- Internal display RAM of 80 × 8 bits (80 characters max.)
- Internal character generator ROM of 7200 bits:
  160 character fonts of 5 × 7 dots
  32 character fonts of 5 × 10 dots
- Internal character generator RAM of 64 × 8 bits:
  8 character fonts of 5 × 7 dots
  4 character fonts of 5 × 10 dots
- Internal liquid crystal display driver with 16 common signal drivers and 100 segment signal drivers
- Programmable duty cycles
  — 1/8 for 1 line of 5 × 7 dots + cursor
  — 1/11 for 1 line of 5 × 10 dots + cursor
  — 1/16 for 2 lines of 5 × 7 dots + cursor
- **Maximum display characters**
- Wide range of instruction functions:
  — Display clear, Cursor home, Display On/Off, Cursor On/Off, Display character blink, Cursor shift, Display shift
- Wide range of power supply (V_{cc}): 4.5 to 5.5 V (standard version), 2.7 to 3.3 V (low V_{cc} version)
- Internal automatic reset circuit after power on (provided by standard version only)
- Independent LCD drive voltage on the logic power supply (V_{cc}): 3.0 to 6.0 V

Display Type	Duty Cycle	When not Extended	When Extended with an HD44100H	Maximum Extension
1-line display	1/8	20 characters × 1 line	28 characters × 1 line	80 characters × 1 line
	1/11	20 characters × 1 line	28 characters × 1 line	80 characters × 1 line
2-line display	1/16	20 characters × 2 lines	28 characters × 2 lines	40 characters × 2 lines

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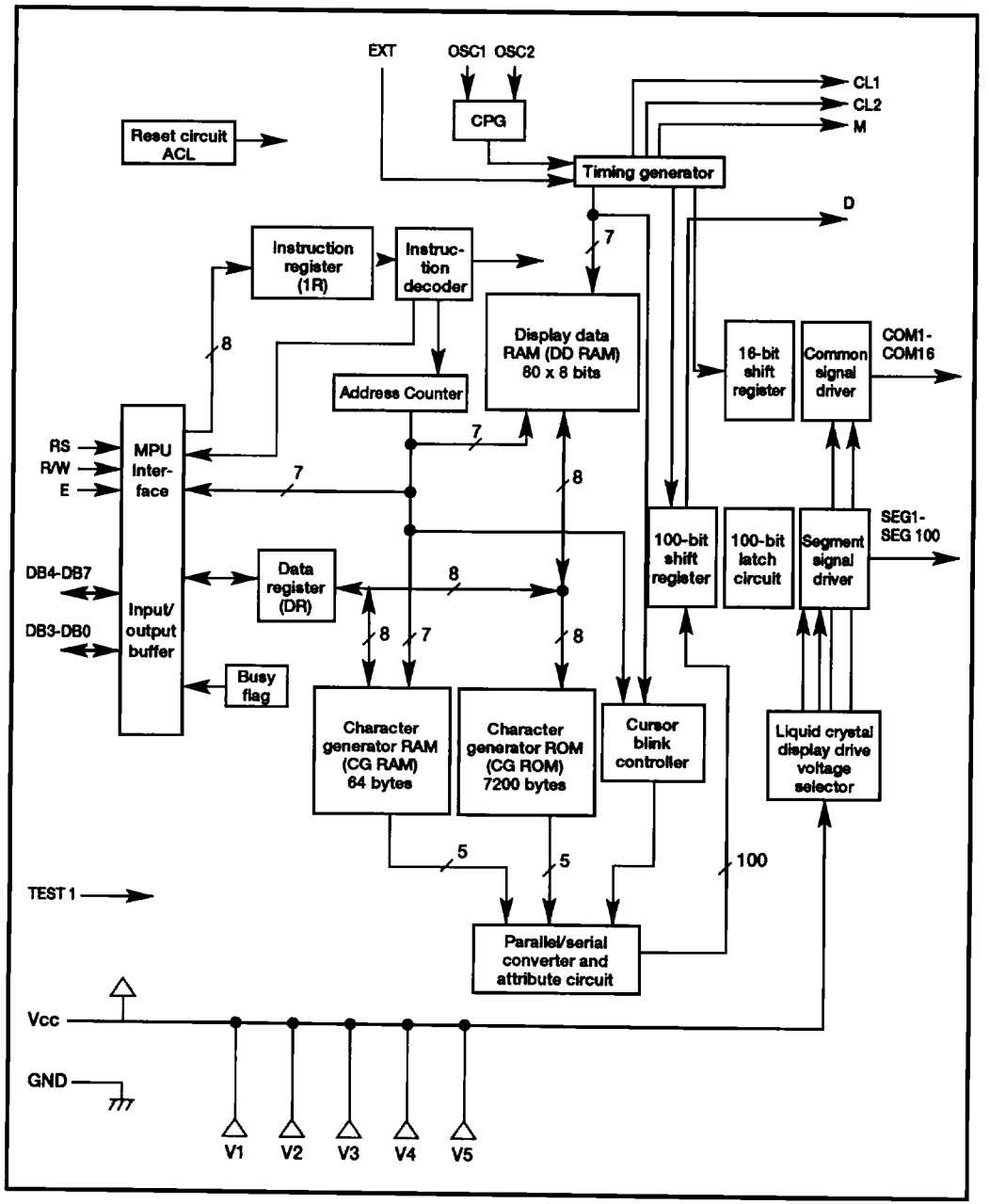
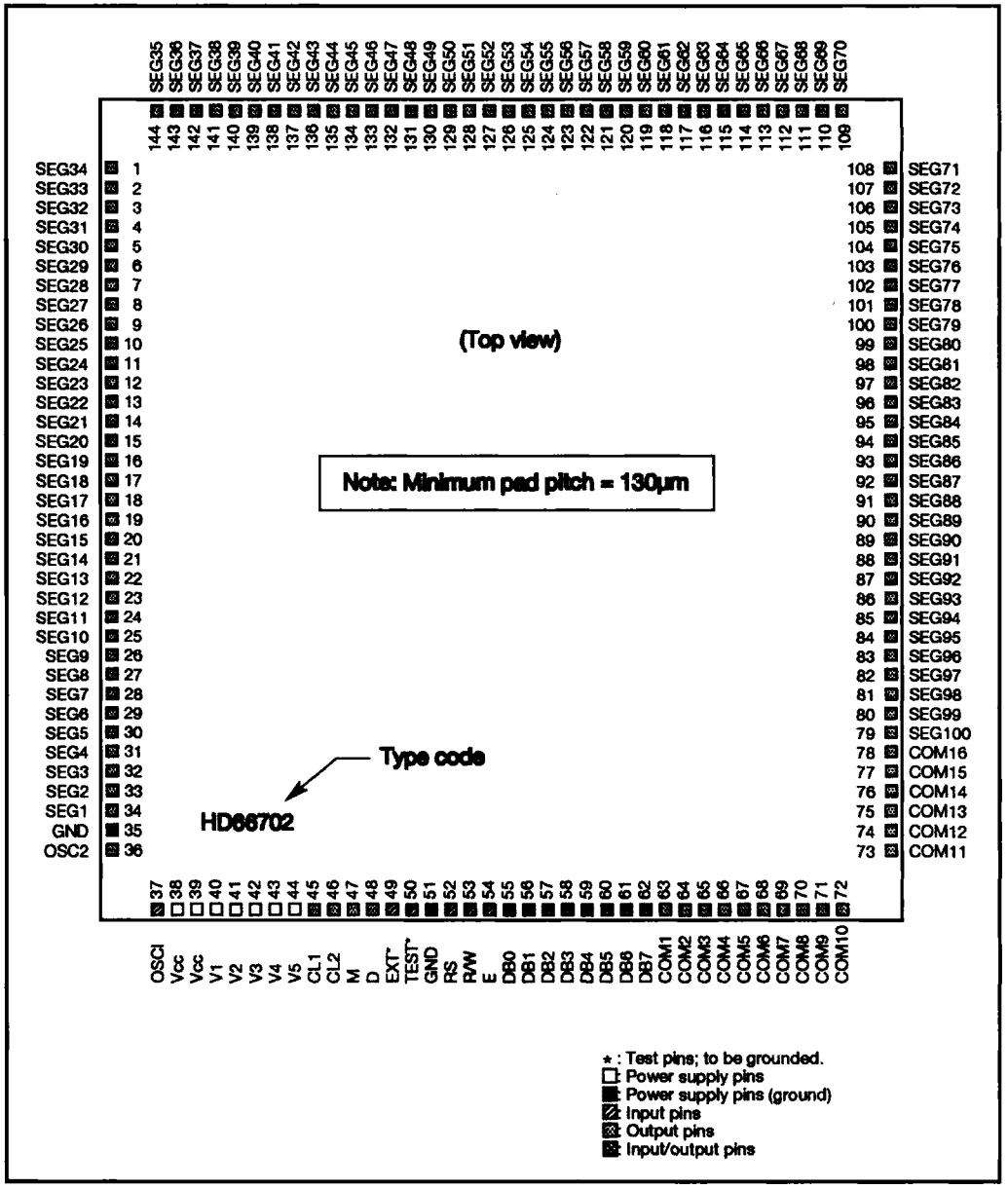
Block Diagram (LCD-II/E20 Interior)



LCD-II/E20 Pad Arrangement



LCD-II Family Comparison

Item		LCD-II (HD44780)	LCD-II/A (HD66780)	LCD-II/E20 (HD66702)
Power supply voltage		5 V ± 10%	5 V ± 10%	5 V ± 10% for standard version; 3 V ± 10% for low V_{CC} version
Liquid crystal drive voltage V_{LCD}	1/4 bias	3.0 to 11 V	3.0 V to V_{CC}	3.0 to 6.0 V
	1/5 bias	4.6 to 11 V	3.0 V to V_{CC}	3.0 to 6.0 V
Max display digits per chip		16 digits (8 digits × 2 lines)	16 digits (8 digits × 2 lines)	40 digits (20 digits × 2 lines)
Display duty cycle		1/8, 1/11 and 1/16	1/8, 1/11 and 1/16	1/8, 1/11 and 1/16
CG ROM		7,200 bits (160 character fonts of 5 × 7 dots and 32 character fonts of 5 × 10 dots)	12,000 bits (240 character fonts of 5 × 10 dots)	7,200 bits (160 character fonts of 5 × 7 dots and 32 character fonts of 5 × 10 dots)
CG RAM		64 bytes	64 bytes	64 bytes
DD RAM		80 bytes	80 bytes	80 bytes
Segment signals		40	40	100
Common signals		16	16	16
Liquid crystal drive waveform		A	B	B
Ladder resistor for liquid crystal drive power supply		External	External	External
Clock source		External resistor, external ceramic filter, or external clock	External resistor, external ceramic filter, or external clock	External resistor, or external clock
Rf oscillation frequency (frame frequency)		270 kHz ± 30% (59 to 110 Hz for 1/8 and 1/16 duty cycles; 43 to 80 Hz for 1/11 duty cycle)	270 kHz ± 30% (59 to 110 Hz for 1/8 and 1/16 duty cycles; 43 to 80 Hz for 1/11 duty cycle)	320 kHz ± 30% (69 to 128 Hz for 1/8 and 1/16 duty cycles; 50 to 93 Hz for 1/11 duty cycle)
Rf resistance		91 kΩ ± 2%	83 kΩ ± 2%	68 kΩ (T.B.D.) for standard version; 56 kΩ (T.B.D.) for low V_{CC} version
Instructions		Fully compatible within the LCD-II family		
CPU bus timing		1 MHz	2 MHz	1 MHz
Package		QFP1420-80, QFP1414-80, and 80-pin bare chip	QFP1420-80 and QFP1414-80	144-pin bare chip (no package)

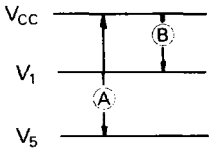
Note: Development of QFP2020-144 (144-pin quad flat package) is under consideration.

Electrical Characteristics

Absolute Maximum Ratings for Low V_{cc} Version

Item	Symbol	Unit	Rating	Note
Power supply voltage (1)	V_{cc}	V	–0.3 to +7.0	
Power supply voltage (2)	V_1 to V_5	V	–0.3 to +7.0	3
Input voltage	V_t	V	–0.3 to V_{cc} + 0.3	
Operating temperature	T_{opr}	°C	–20 to + 75	4
Storage temperature	T_{stg}	°C	–55 to + 125	

Notes: 1. If LSIs are used above absolute maximum ratings, they may be permanently destroyed. Using them within electrical characteristic limits is strongly recommended for normal operation. Use beyond these conditions will cause malfunction and poor reliability.
2. All voltage values are referenced to GND = 0 V.
3. Applies to V_1 to V_5; must maintain $V_{cc} \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_5$; see below.



Ⓐ = $V_{cc} - V_5$
Ⓑ = $V_{cc} - V_1$
Ⓐ ≧ 1.5 V
Ⓑ ≦ 0.25 × Ⓐ

The conditions of V_1 and V_5 voltages are for proper operation of the LSI and not for the LCD output level. The LCD drive voltage condition for the LCD output level is specified in "LCD voltage VLCD."

4. This temperature is for packaged devices; +75°C is the guaranteed operating temperature for bare chip devices.

DC Characteristics for Low V_{cc} Version (V_{cc} = 3 V ± 10%, T_a = –20°C to +75°C*1)

Item	Symbol	Unit	Test Conditions	min.	typ.	max.	Note
Input high voltage (1)	V_{IH1}	V		T.B.D.	—	V_{cc}	2
Input low voltage (1)	V_{IL1}	V		–0.3	—	T.B.D.	2
Input high voltage (2) (OSC1)	V_{IH2}	V		T.B.D.	—	V_{cc}	11
Input low voltage (2) (OSC1)	V_{IL2}	V		—	—	T.B.D.	11
Output high voltage (1) (DB_0–DB_7)	V_{OH1}	V	$-I_{OH}$ = 0.1 mA	T.B.D.	—	—	3
Output low voltage (1) (DB_0–DB_7)	V_{OL1}	V	I_{OL} = 0.1 mA	—	—	T.B.D.	3
Output high voltage (2) (except DB_0–DB_7)	V_{OH2}	V	$-I_{OH}$ = 0.04 mA	T.B.D.	—	—	4
Output low voltage (2) (except DB_0–DB_7)	V_{OL2}	V	I_{OL} = 0.04 mA	—	—	T.B.D.	4
Driver ON resistance (COM pin)	R_{COM}	kΩ	± I_d = 0.05 mA (all COM pins)	—	—	20	9
Driver ON resistance (SEG pin)	R_{SEG}	kΩ	± I_d = 0.05 mA (all SEG pins)	—	—	30	9
Input/Output leakage current	I_{LI}	µA	V_{in} = 0 to V_{cc}	–1	—	1	5
Pull-up MOS current (RS, R/W)	$-I_p$	µA	V_{cc} = 3 V	T.B.D.	T.B.D.	T.B.D.	
Power supply current	I_{cc}	mA	Rf oscillation, external clock operation, V_{cc} = 3 V fOSC = 320 kHz		T.B.D.		6, 10
LCD voltage	V_{LCD1}	V	$V_{cc} - V_5$ 1/5 bias	3.0	—	6.0	12
	V_{LCD2}	V	$V_{cc} - V_5$ 1/4 bias	3.0	—	6.0	12

Notes for DC Characteristics on pages 983 and 984.

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AC Characteristics for Low V_{cc} Version (V_{cc} = 3 V ± 10%, T_a = –20°C to +75°C*1)

Clock Characteristics

Item	Symbol	Unit	Test Conditions	min.	typ.	max.	Note
External clock operating frequency	f_{cp}	kHz		125	—	410	7
External clock duty cycle	Duty	%		45	50	55	7
External clock rise time	t_{rcp}	µs		—	—	0.2	7
External clock fall time	t_{rcp}	µs		—	—	0.2	7
Rf oscillation internal clock operating frequency	f_{OSC}	kHz	Rf = T.B.D.	230	320	410	8

Notes on pages 983 and 984

Bus Timing Characteristics

Write Operation

Item	Symbol	Unit	Test Conditions	min.	typ.	max.
Enable cycle time	t_{CYCE}	ns	Figure 1	1000	—	—
Enable pulse high level width	PW_{EH}	ns	Figure 1	450	—	—
Enable rise/fall time	t_{Er}, t_{Ef}	ns	Figure 1	—	—	25
Setup time for RS, R/W, E	t_{AS}	ns	Figure 1	40	—	—
Address hold time	t_{AH}	ns	Figure 1	10	—	—
Data setup time	t_{DSW}	ns	Figure 1	195	—	—
Data hold time	t_H	ns	Figure 1	10	—	—

Read Operation

Item	Symbol	Unit	Test Conditions	min.	typ.	max.
Enable cycle time	t_{CYCE}	ns	Figure 2	1000	—	—
Enable pulse high level width	PW_{EH}	ns	Figure 2	450	—	—
Enable rise/fall time	t_{Er}, t_{Ef}	ns	Figure 2	—	—	25
Setup time for RS, R/W, E	t_{AS}	ns	Figure 2	40	—	—
Address hold time	t_{AH}	ns	Figure 2	10	—	—
Data delay time	t_{DDR}	ns	Figure 2	—	—	320
Data hold time	t_{DHR}	ns	Figure 2	20	—	—

Segment extension signal timing

Item	Symbol	Unit	Test Conditions	min.	typ.	max.
Clock pulse high level width	t_{CWH}	ns	Figure 3	800	—	—
Clock pulse low level width	t_{CWL}	ns	Figure 3	800	—	—
Clock setup time	t_{CSU}	ns	Figure 3	500	—	—
Data setup time	t_{SU}	ns	Figure 3	300	—	—
Data hold time	t_{DH}	ns	Figure 3	300	—	—
M delay time	t_{DM}	ns	Figure 3	–1000	—	1000
Clock rise/fall time	t_{ct}	ns	Figure 3		—	100

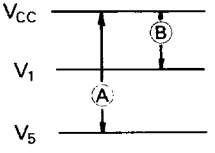
Power supply conditions for using internal reset circuit
Since the internal reset circuit will not operate normally in the 3-V V_{cc} LCD-II/E20, initialize the LSI by instruction.

Bus Timing Characteristics

Absolute Maximum Ratings for Standard V_{cc} Version

Item	Symbol	Unit	Rating	Note
Power supply voltage (1)	V_{cc}	V	–0.3 to +7.0	
Power supply voltage (2)	V_1 to V_5	V	–0.3 to +7.0	3
Input voltage	V_t	V	–0.3 to V_{cc} + 0.3	
Operating temperature	T_{opr}	°C	–20 to + 75	4
Storage temperature	T_{stg}	°C	–55 to + 125	

Notes: 1. If LSIs are used above absolute maximum ratings, they may be permanently destroyed. Using them within electrical characteristic limits is strongly recommended for normal operation. Use beyond these conditions will cause malfunction and poor reliability.
2. All voltage values are referenced to GND = 0 V.
3. Applies to V_1 to V_5; must maintain $V_{cc} \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_5$; see below.



Ⓐ = $V_{cc} - V_5$
Ⓑ = $V_{cc} - V_1$
Ⓐ ≥ 1.5 V
Ⓑ ≤ 0.25 × Ⓐ

The conditions of V_1 and V_5 voltages are for proper operation of the LSI and not for the LCD output level. The LCD drive voltage condition for the LCD output level is specified in "LCD voltage VLCD."

4. This temperature is for packaged devices; +75°C is the guaranteed operating temperature for bare chip devices.

DC Characteristics for Standard Version (V_{cc} = 5 V ± 10%, T_a = –20°C to +75°C*1)

Item	Symbol	Unit	Test Conditions	min.	typ.	max.	Note
Input high voltage (1)	V_{IH1}	V		2.2	—	V_{cc}	2
Input low voltage (1)	V_{IL1}	V		–0.3	—	0.6	2
Input high voltage (2) (OSC1)	V_{IH2}	V		V_{cc} – 1	—	V_{cc}	11
Input low voltage (2) (OSC1)	V_{IL2}	V		—	—	1.0	11
Output high voltage (1) (DB_0–DB_7)	V_{OH1}	V	$-I_{OH}$ = 0.205 mA	2.4	—	—	3
Output low voltage (1) (DB_0–DB_7)	V_{OL1}	V	I_{OL} = 1.6 mA	—	—	0.4	3
Output high voltage (2) (except DB_0–DB_7)	V_{OH2}	V	$-I_{OH}$ = 0.04 mA	0.9 V_{cc}	—	—	4
Output low voltage (2) (except DB_0–DB_7)	V_{OL2}	V	I_{OL} = 0.04 mA	—	—	0.1 V_{cc}	4
Driver ON resistance (COM pin)	R_{COM}	kΩ	± I_d = 0.05 mA (all COM pins)	—	—	20	9
Driver ON resistance (SEG pin)	R_{SEG}	kΩ	± I_d = 0.05 mA (all SEG pins)	—	—	30	9
Input/Output leakage current	I_{LI}	µA	V_{in} = 0 to V_{cc}	–1	—	1	5
Pull-up MOS current (RS, R/W)	$-I_p$	µA	V_{cc} = 5 V	T.B.D.	125	T.B.D.	
Power supply current for RS, R/W	I_{cc}	mA	Rf oscillation, external clock operation, V_{cc} = 5 V f_{OSC} = 320 kHz		T.B.D.		6, 10
LCD voltage	V_{LCD1}	V	$V_{cc} - V_5$ 1/5 bias	3.0	—	6.0	12
	V_{LCD2}	V	$V_{cc} - V_5$ 1/4 bias	3.0	—	6.0	12

Notes for DC Characteristics on pages 983 and 984.

AC Characteristics for Standard Version (V_{CC} = 5 V ± 10%, T_a = –20°C to +75°C*1)

Clock Characteristics

Item	Symbol	Unit	Test Conditions	min.	typ.	max.	Note
External clock operating frequency	f_{cp}	kHz		125	—	410	7
External clock duty cycle	Duty	%		45	50	55	7
External clock rise time	t_{rcp}	µs		—	—	0.2	7
External clock fall time	t_{rcp}	µs		—	—	0.2	7
Rf oscillation internal clock operating frequency	fOSC	kHz	Rf = T.B.D.	230	320	410	8

Notes on pages 983 and 984

Bus Timing Characteristics (see note on page 14 for load circuits)

Write Operation

Item	Symbol	Unit	Test Conditions	min.	typ.	max.
Enable cycle time	t_{CYCE}	ns	Figure 1	1000	—	—
Enable pulse high level width	PW_{EH}	ns	Figure 1	450	—	—
Enable rise/fall time	t_{Er}, t_{Ef}	ns	Figure 1	—	—	25
Setup time for RS, R/W, E	t_{AS}	ns	Figure 1	40	—	—
Address hold time	t_{AH}	ns	Figure 1	10	—	—
Data setup time	t_{DSW}	ns	Figure 1	195	—	—
Data hold time	t_H	ns	Figure 1	10	—	—

Read Operation

Item	Symbol	Unit	Test Conditions	min.	typ.	max.
Enable cycle time	t_{CYCE}	ns	Figure 2	1000	—	—
Enable pulse high level width	PW_{EH}	ns	Figure 2	450	—	—
Enable rise/fall time	t_{Er}, t_{Ef}	ns	Figure 2	—	—	25
Setup time for RS, R/W, E	t_{AS}	ns	Figure 2	40	—	—
Address hold time	t_{AH}	ns	Figure 2	10	—	—
Data delay time	t_{DDR}	ns	Figure 2	—	—	320
Data hold time	t_{DHR}	ns	Figure 2	20	—	—

Segment extension signal timing

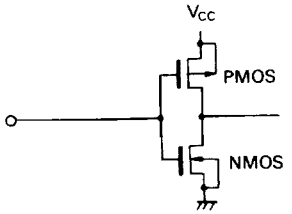
Item	Symbol	Unit	Test Conditions	min.	typ.	max.
Clock pulse high level width	t_{CWH}	ns	Figure 3	800	—	—
Clock pulse low level width	t_{CWL}	ns	Figure 3	800	—	—
Clock setup time	t_{CSU}	ns	Figure 3	500	—	—
Data setup time	t_{SU}	ns	Figure 3	300	—	—
Data hold time	t_{DH}	ns	Figure 3	300	—	—
M delay time	t_{DM}	ns	Figure 3	–1000	—	1000
Clock rise/fall time	t_{ct}	ns	Figure 3	—	—	100

Power supply conditions for using internal reset circuit

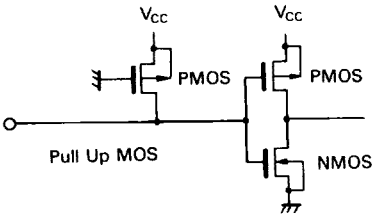
Item	Symbol	Unit	Test Conditions	min.	typ.	max.
Power supply rise time	t_{rCC}	ms	Figure 4	0.1	—	10
Power supply off time	t_{OFF}	ms	Figure 4	1	—	—

Note: 1. The following are I/O terminal configurations except for liquid crystal display output.

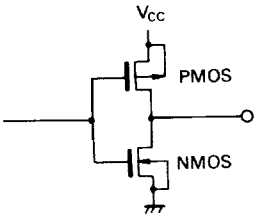
- Input Terminal Applicable Terminals: E
  (MOS without pull up)



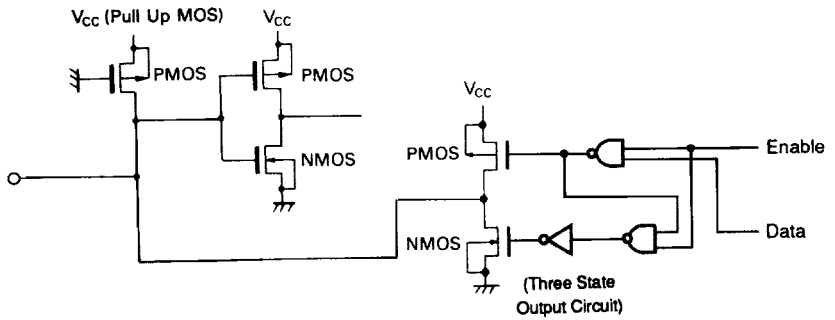
- Applicable Terminals: RS, R/W
  (MOS with pull up)



- Output Terminal
  Applicable Terminals: CL_1, CL_2, M, D

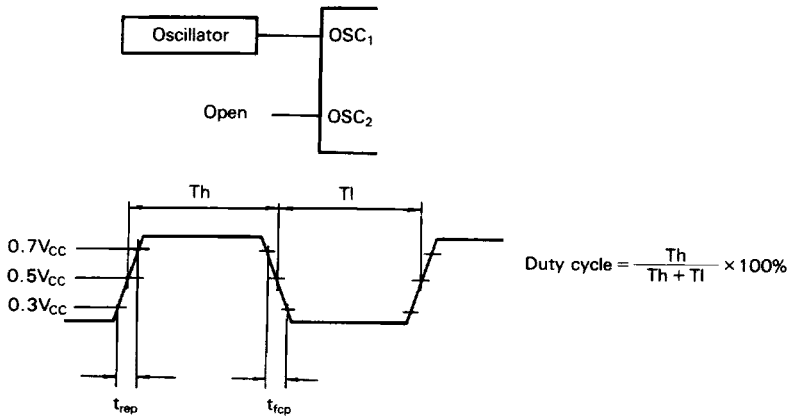


- I/O Terminal
  Applicable Terminals: DB_0 to DB_7

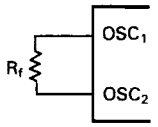


Note: 2. Input terminals and I/O terminals. Excludes OSC_1 terminals.
Note: 3. I/O terminals.
Note: 4. Output terminals.
Note: 5. Current flowing through pull-up MOSs and output drive MOSs is excluded.
Note: 6. Input/output current is excluded. When CMOS input is at an intermediate level, excessive current flows through the input circuit to the power supply. To avoid this, input level must be fixed at high or low.

Note: 7. External clock operation.



Note: 8. Internal oscillator operation using oscillation resistor Rf.



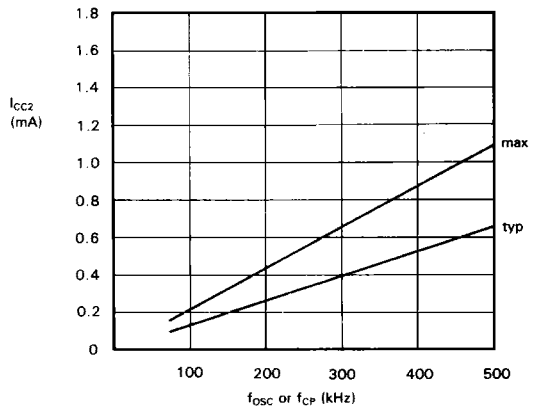
Rf: 56 kΩ ± 2% (V_{cc} = 3 V)
Rf: 68 kΩ ± 2% (V_{cc} = 5 V)

Reference values (T.B.D.)

Since oscillation frequency varies depending on OSC_1 and OSC_2 terminal capacitance, wiring length for these terminals should be minimized.

Note: 9. Applies to both V_{COM} and V_{SEG} voltage drops.
V_{COM}: From power suply terminal V_{cc}, V_1, V_4, V_5 to each common signal terminal (COM_1 to COM_{16})
V_{SEG}: From power suply terminal V_{cc}, V_2, V_3, V_6 to each segment signal terminal (SEG_1 to SEG_{40})

Note: 10. Relation between operation frequency and current consumption is shown in this diagram (V_{cc} = 5 V).



Note: 11. Applied to OSC_1 terminal.
Note: 12. The condition for COM pin voltage drop (V_{COM}) and SEG pin voltage drop (V_{SEG}).

Timing Characteristics

Write operation

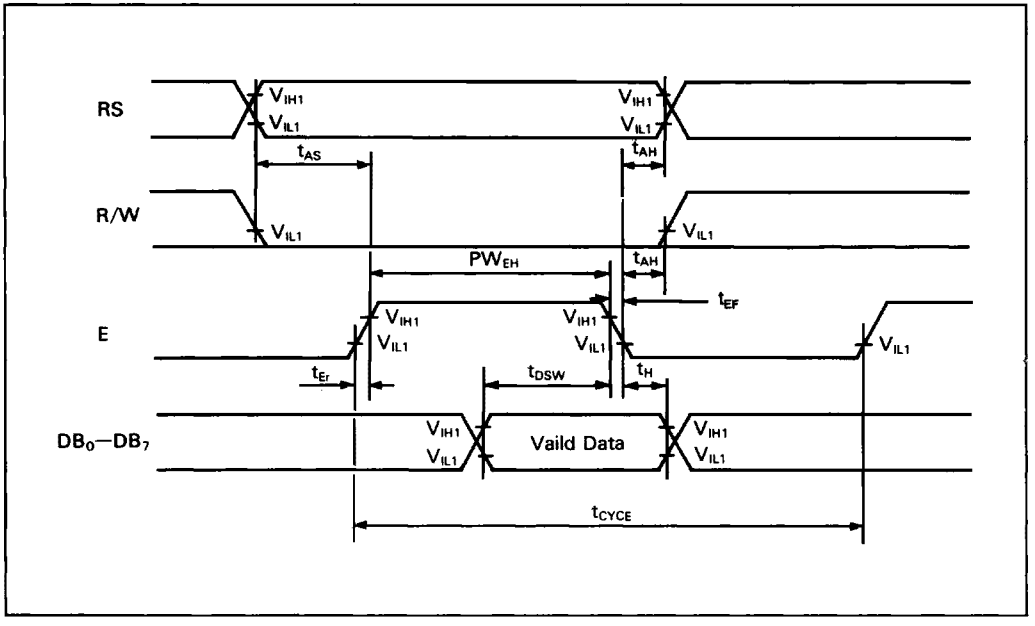


Figure 1 Write Operation

Read operation

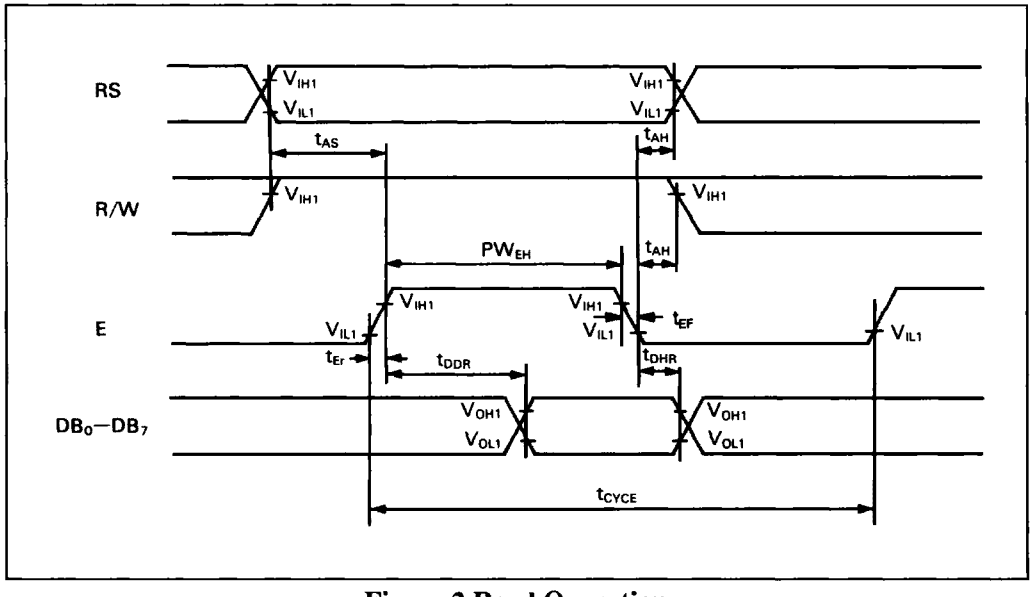


Figure 2 Read Operation

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Interface signals with driver LSI HD44100H

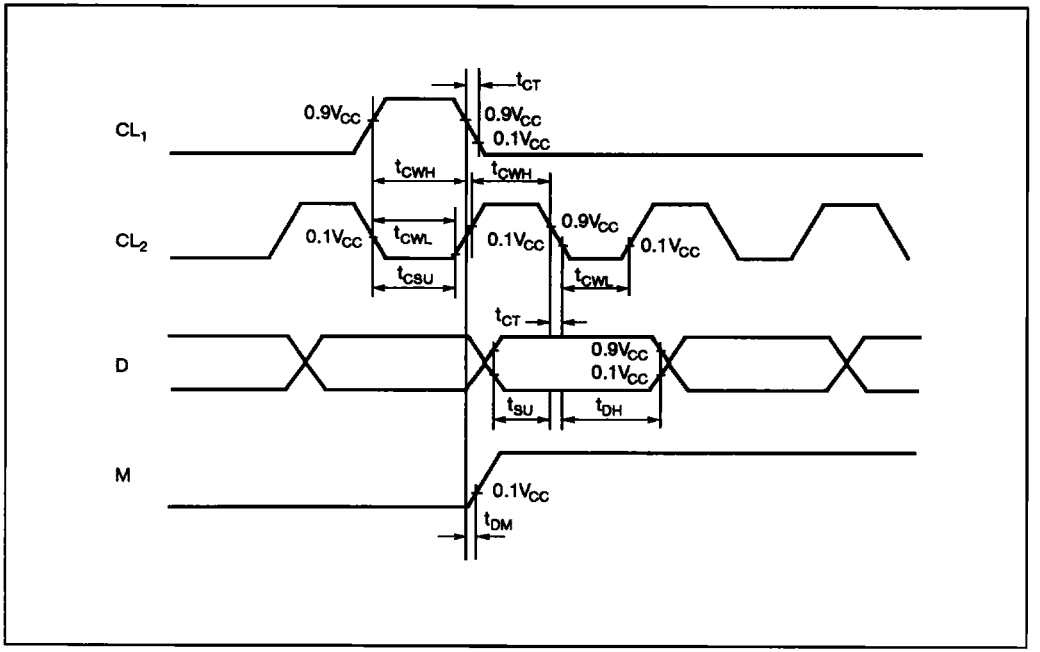


Figure 3 Extension Driver Interface Timing

Power on sequence

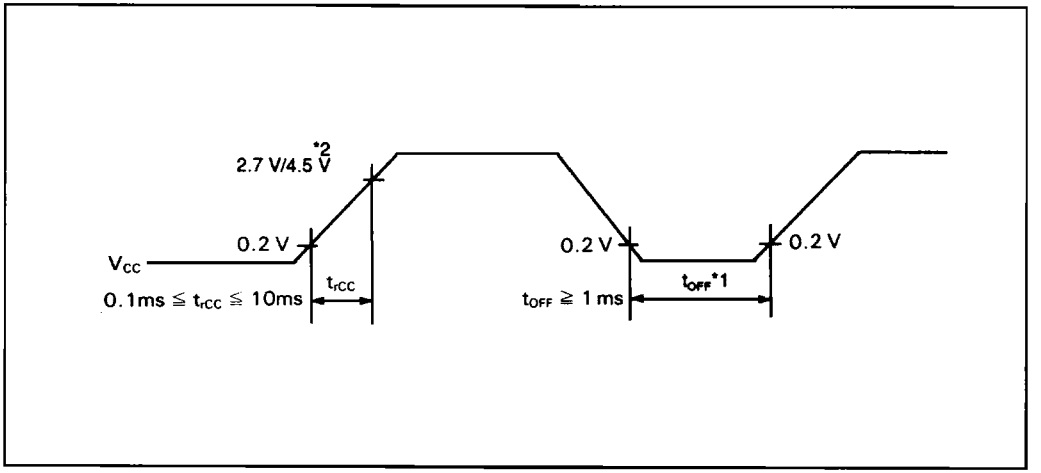
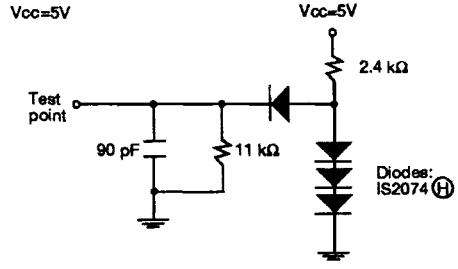


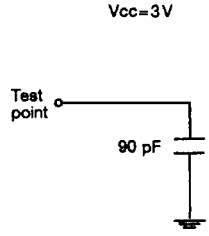
Figure 4 Power on Sequence

Notes: 1. t_{off} defines the time of power off for momentary power supply dip or when power supply is repeatedly turned on and off.
2. 2.7 when V_{CC} = 5 V, and 4.5 V when V_{CC} = 3 V.
3. Since the internal reset circuit will not operate normally if the above conditions are not satisfied, initialize the LSI by instruction. Refer to "Initializing by Instruction."

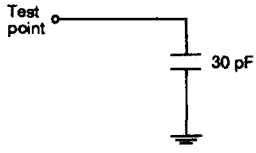
Note: Load Circuits

Data bus DB_0–DB_7





Segment extention signals



Terminal Function

Table 1 Functional Description of Terminals

Signal Name	No. of Lines	Input/ Output	Connected to	Function
RS	1	Input	MPU	Signal to select registers. 0: Instruction register (for write) Busy flag: address counter (for read) 1: Data register (for read and write)
R/W	1	Input	MPU	Signal to select read (R) and write (W). 0: Write 1: Read
E	1	Input	MPU	Operation start signal for data read/write.
DB_4–DB_7	4	Input/Output	MPU	Higher order 4 bidirectional three-state data bus lines. Used for data transfer between the MPU and the LCD-II/E20. DB_7 can be used as a BUSY flag.
DB_0–DB_3	4	Input/Output	MPU	Lower order 4 bidirectional three-state data bus lines. Used for data transfer between the MPU and the LCD-II/E20. These four are not used during 4-bit operation.
CL_1	1	Output	HD44100H	Clock to latch serial data D sent to the driver LSI HD44100H.
CL_2	1	Output	HD44100H	Clock to shift serial data D.
M	1	Output	HD44100H	Switch signal to convert liquid crystal drive waveform to AC.
D	1	Output	HD44100H	Sends character pattern data corresponding to each common signal serially.
COM_1–COM_{16}	16	Output	Liquid crystal display	Common signals that are not used are changed to non-selection waveforms. That is, COM_9–COM_{10} are non-selection waveforms at 1/8 duty factor, and COM_{12}–COM_{16} are non-selection waveforms at 1/11 duty factor.
SEG_1–SEG_{100}	100	Output	Liquid crystal display	Segment signal.
V_1–V_5	5		Power supply	Power supply for liquid crystal display drive.
V_{cc}, GND	2		Power supply	V_{cc}: +5 V, GND: 0 V.
TEST	1	Input	—	Test pin; to be grounded.
EXT	1	Input	—	Test pin; to be grounded.

Function Of Each Block

Register

The HD66702 had two 8-bit registers, an instruction register (IR), and a data register (DR).

The IR stores instruction codes such as display clear and cursor shift, and address information for display data RAM (DD RAM) and character generator RAM (CG RAM). The IR can be written from the MPU but not read by the MPU.

The DR temporarily stores data to be written into the DD RAM or the CG RAM and data to be read out from DD RAM or CG RAM. Data written into the DR from the MPU is automatically written into the DD RAM or the CG RAM by internal operation. The DR is also used for data storage when reading data is read from the DD RAM or the CG RAM. When address information is written into the IR, data is read into the DR from the DD RAM or the CG RAM by internal operation. Data transfer to the MPU is then completed by the MPU reading DR. After the MPU reads the DR, data in the DD RAM or CG RAM at the next address is sent to the DR for the next read from the MPU. Register selector (RS) signals make their selection from these two registers.

Busy flag (BF)

When the busy flag is 1, the HD66702 is in the internal operation mode, and the next instruction will not be accepted. As table 2 shows, the busy flag is output to DB_7 when RS = 0 and R/W = 1. The next instruction must be written after ensuring that the busy flag is 0.

Address counter (AC)

The address counter (AC) assigns addresses to DD and CG RAMs. When an instruction for address is written in IR, the address information is sent from IR to AC. Selection of either DD or CG RAM is also determined concurrently by the instruction.

After writing into (or reading from) DD or CG RAM display data, AC is automatically incremented by +1 (or decremented by −1). AC contents are output to DB_0–DB_6 when RS = 0 and R/W = 1, as shown in table 2.

Table 2 Register Selection

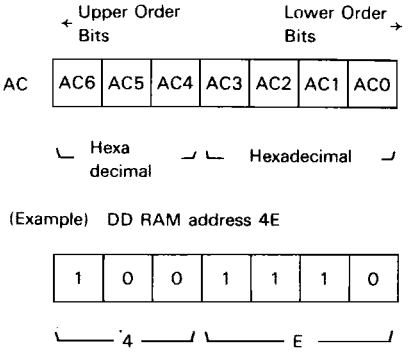
RS	R/W	Operation
0	0	IR write as internal operation (Display clear, etc.)
0	1	Read busy flag (DB_7) and address counter (DB_0–DB_6)
1	0	DR write as internal operation (DR to DD or CG RAM)
1	1	DR read as internal operation (DD or CG RAM to DR)

Display data RAM (DD RAM)

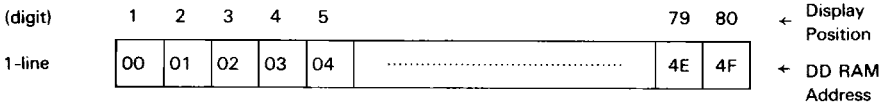
The display data RAM (DD RAM) stores display data represented in 8-bit character codes. Its capacity is 80 × 8 bits, or 80 characters. The display data RAM (DD RAM) that is not used for display can be used as a general data RAM.

Relations between DD RAM addresses and positions on the liquid crystal display are shown below.

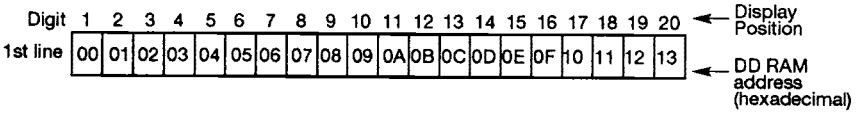
The DD RAM address (A_{DD}) is set in the address counter (AC) and is represented in hexadecimal.



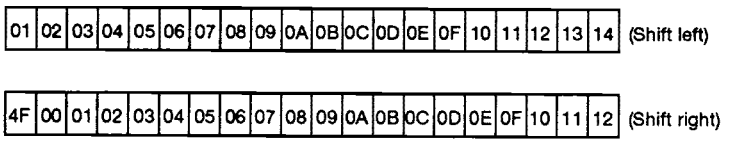
1-Line Display (N = 0)



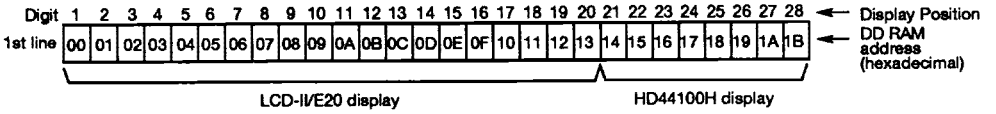
1. When there are fewer than 80 display characters, the display begins at the head position. For example, 20 characters using an HD66702 are displayed as:



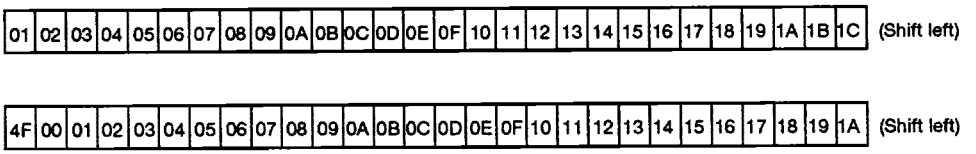
When the display shift operation is performed, the DD RAM address moves as:



2. 28-character display using an HD66702 and an HD44100H is as shown below:

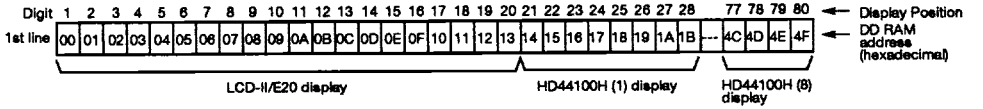


When the display shift operation is performed, the DD RAM address moves as:

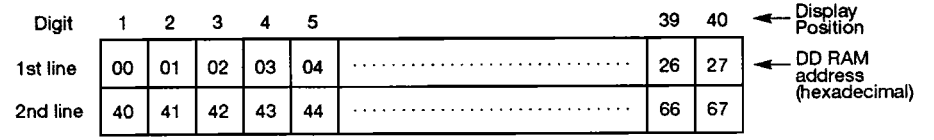


3. The relation between display position and DD RAM address when the number of display digits is increased through the use of one HD66702 and two or more HD44100H's can be considered an extension of 2.

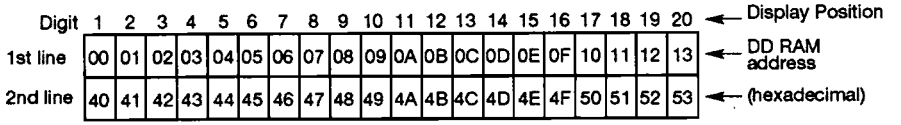
Since the increase can be 8 digits for each additional HD44100H, up to 80 digits can be displayed by externally connecting 8 HD44100H's.



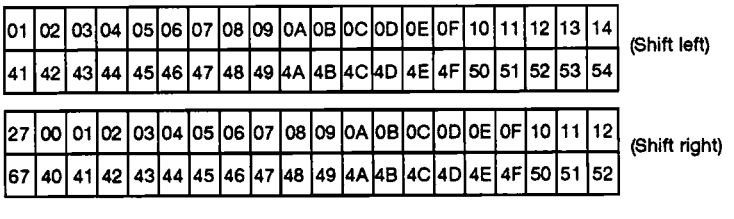
2-Line Display (N = 1)



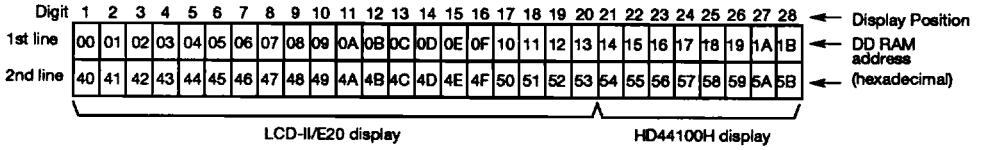
1. When the number of display characters is less than 40 × 2 lines, the 2 lines are displayed from the head. Note that the first line end address and the second line start address are not consecutive. For example, when an HD66702 is used, 20 characters × 2 lines are displayed as:



When display shift is performed, the DD RAM address moves as:



2. 28 characters × 2 lines are displayed when an HD66702 and an HD44100H are used.



When display shift is performed, the DD RAM address moves as follows:

01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C
41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	51	52	53	54	55	56	57	58	59	5A	5B	5C

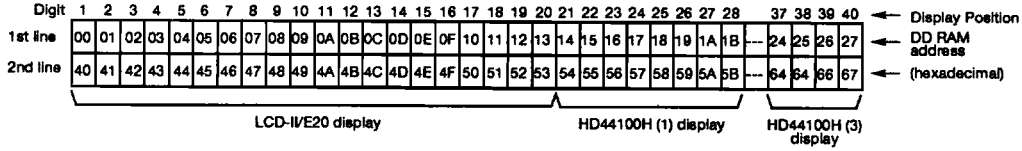
(Shift left)

27	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16	17	18	19	1A
67	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	51	52	53	54	55	56	57	58	59	5A

(Shift right)

3. The relation between display position and DD RAM address when the number of display digits is increased by using one HD66702 and two or more HD44100H's, can be considered an extension of 2.

Since the increase can be 8 digits × 2 lines for each additional HD44100H, up to 40 digits 2 lines can be displayed by connecting three HD44100H's externally.



Character Generator ROM (CG ROM)

The character generator ROM generates 5 × 7 dot or 5 × 10 dot character patterns from 8-bit character codes. It can generate 160 5 × 7 dot character patterns and 32 5 × 10 dot character patterns. Table 5 shows the relation between character codes and character patterns in the Hitachi standard HD66702. User defined character patterns are also available by mask-programmed ROM.

Character Generator RAM (CG RAM)

In the character generator RAM, the user can rewrite character patterns by program. With 5 × 7 dots, 8 character patterns can be written and with 5 × 10 dots, 4 characters can be written.

Write the character codes in the left column of table 5 to display character patterns stored in CG RAM.

Table 6 shows the relation between CG RAM addresses and data and display patterns.

As table 6 shows, an area that is not used for display can be used as a general data RAM.

Modifying Character Patterns

1. Character Pattern Development Procedure

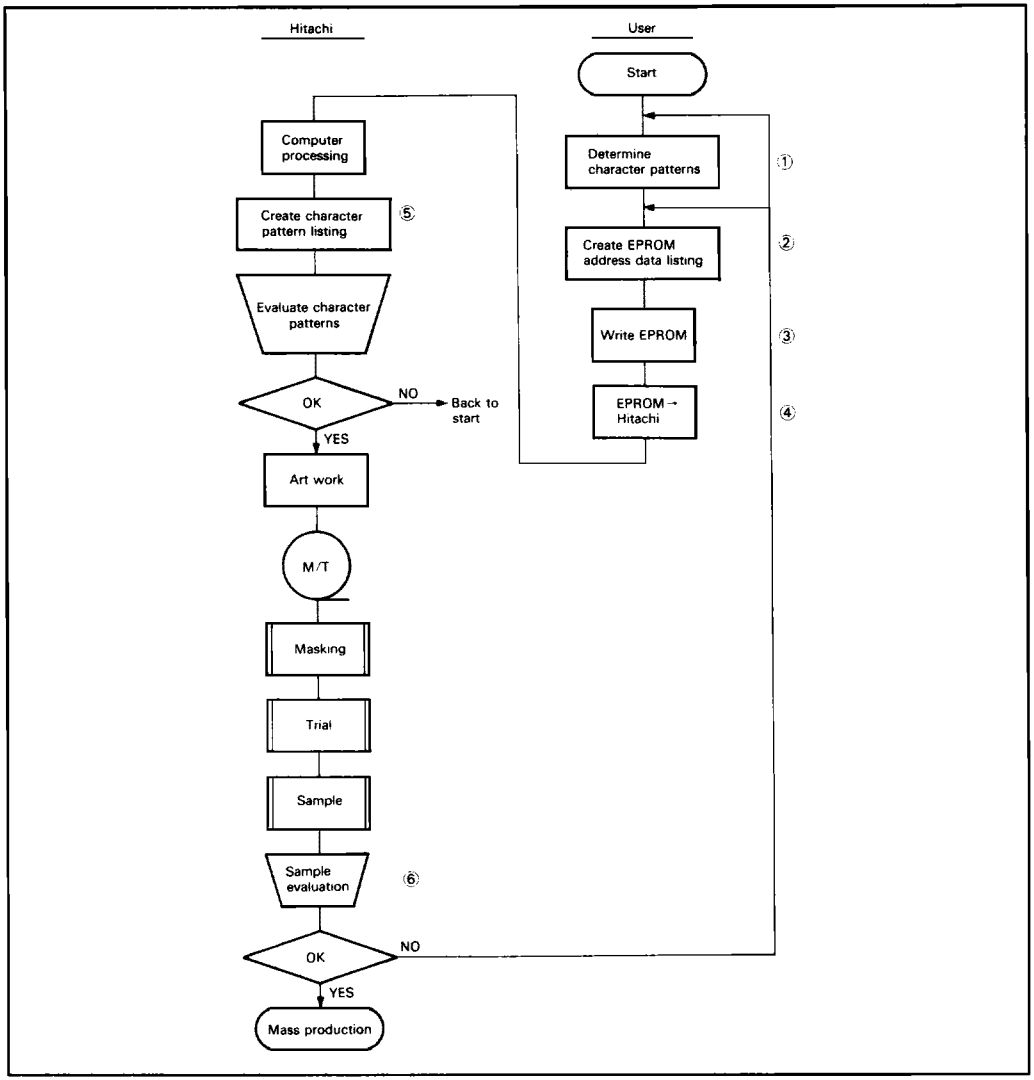


Figure 5 Character Pattern Development Procedure

The numbers in figure 5 correspond to the following operations:

① Determine the correspondence between character codes and character patterns.

② Create a listing indicating the correspondence between EPROM addresses and data.

③ Program character patterns in the EPROM.

④ Send the EPROM to Hitachi.

⑤ Hitachi performs computer processing with the EPROM to create a character pattern listing and sends it to the user.

⑥ If there is no problem in the character pattern listing, Hitachi creates a trial LSI and sends samples to the user. The user evaluates the samples. When it is confirmed that character patterns are correctly written, Hitachi starts mass production of the LSI.

2. Programming Character Patterns

This section explains the correspondence between addresses and data used to program character patterns in EPROM. The LCD-II/E20 character generator ROM can generate 160 5 × 70-dot character patterns and 32 5 × 10-dot character patterns for a total of 192 different character patterns.

a. 5 × 7-dot Character Pattern

For a 5 × 7-dot character pattern, EPROM address data and character pattern correspond with each other as shown below. Table 3 is an example of the correspondence between EPROM address data and character pattern (5 × 7 dots).

Table 3 Example of Correspondence between EPROM Address Data and Character Pattern (5 × 7 dots)

EPROM address											Data				
															(LSB)
A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	O_4	O_3	O_2	O_1	O_0
0	1	0	1	0	0	1	0	0	0	0	1	1	1	1	0
								0	0	1	1	0	0	0	1
								0	1	0	1	0	0	0	1
								0	1	1	1	1	1	1	0
								1	0	0	1	0	1	0	0
								1	0	1	1	0	0	1	0
								1	1	0	1	0	0	0	1
								1	1	1	0	0	0	0	0

Fill line 8 (cursor position) with 0

Character code — Line position

(1) EPROM address A_{10} to A_3 correspond to a character code.

(2) EPROM addresses A_2 to A_0 specify a line position of character pattern.

(3) EPROM data O_4 to O_0 correspond to character pattern data.

(4) A lit display position (black) corresponds to 1.

(5) Fill line 8 (cursor position) of character pattern with 0.

(6) EPROM data O_5 to O_7 are not used.

b. 5 × 10-dot Character Pattern

For a 5 × 10-dot character pattern, EPROM address data and character pattern correspond with each other as shown in table 4.

(1) EPROM addresses A_{10} to A_3 correspond to a character code. Set A_8 and A_9 of character pattern line 9 and later lines to 0.
(2) EPROM addresses A_2 to A_0 specify a line position of character pattern.
(3) EPROM data O_4 to O_0 correspond to character pattern data.
(4) A lit display position (black) corresponds to 1.
(5) Fill line 11 (cursor position) of character pattern with 0.
(6) EPROM data O_5 to O_7 are not used.

c. Handling Unused Character Patterns

(1) EPROM data outside the character pattern area
Ignored by the character generator ROM for display operation so it can be 0 or 1.

(2) EPROM data in CG RAM area
Ignored by the character generator ROM for display operation so it can be 0 or 1.

(3) EPROM data used when the user does not use any HD66702 character pattern
Handled in one of the two ways explained below. Select one of the two ways according to the user application.

(a) When unused character patterns are not programed
If an unused character code is written in the LCD-II/E20 DD RAM, all dots are lit. No programming for a character pattern is equivalent to all bits lit. (This is because EPROM is filled with 1s when the EPROM is erased.)

(b) Program 0 for unused character patterns
Nothing is displayed even if unused character codes are written in LCD-II/E20 DD RAM. (This is equivalent to space.)

Table 4 Example of Correspondence between EPROM Address Data and Character Pattern (5 × 10 dots)

EPROM address											Data				
															(LSB)
A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	O_4	O_3	O_2	O_1	O_0
								0	0	0	0	0	0	0	0
								0	0	1	0	0	0	0	0
								0	1	0	0	1	1	0	1
1	1	1	1	0	0	0	1	0	1	1	1	0	0	1	1
								1	0	0	1	0	0	0	1
								1	0	1	1	0	0	0	1
								1	1	0	0	1	1	1	1
								1	1	1	0	0	0	0	1
1	0	0	1	0	0	0	1	0	0	0	0	0	0	0	1
1	0	0	1	0	0	0	1	0	0	1	0	0	0	0	1
1	0	0	1	0	0	0	1	0	1	0	0	0	0	0	0

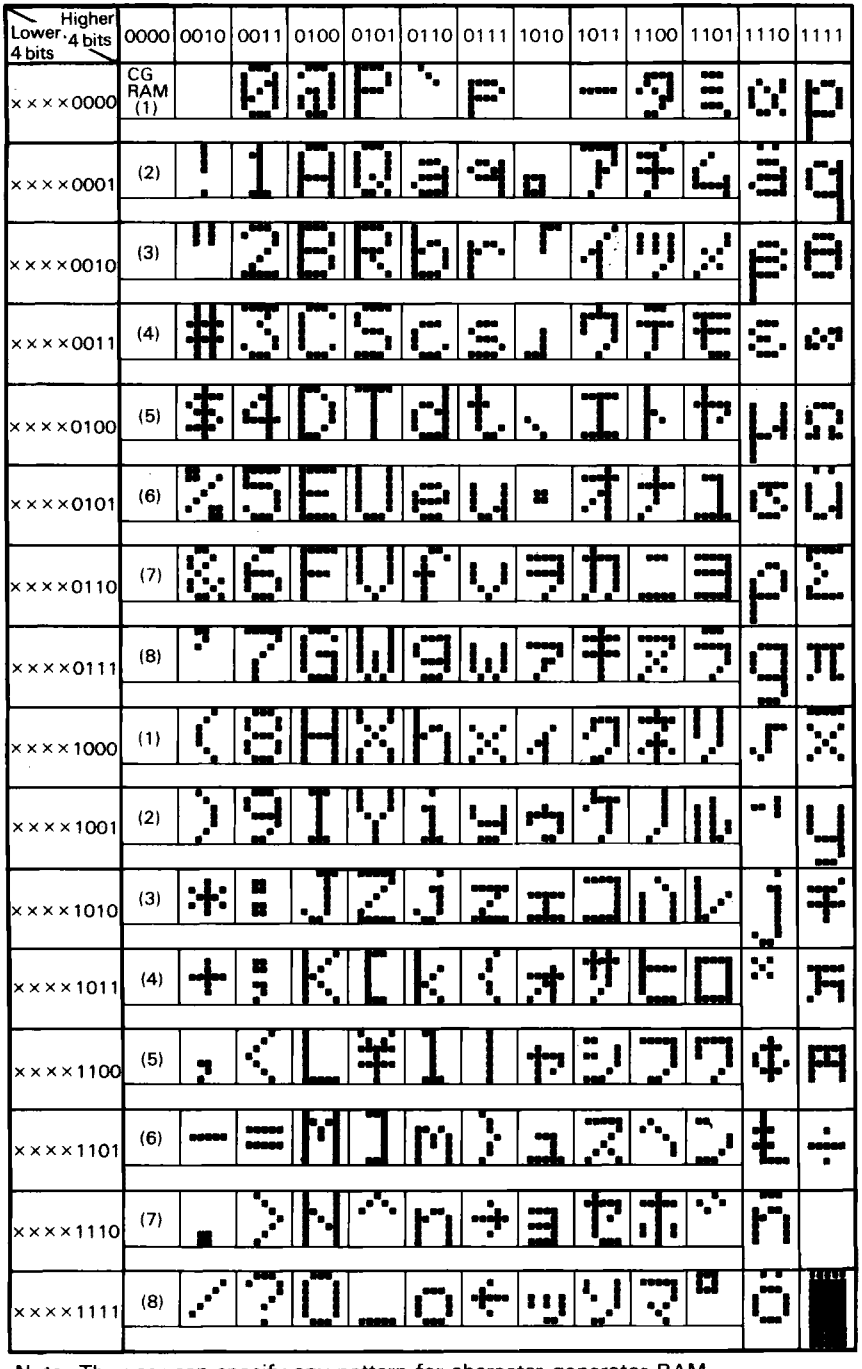
Character code

Line position

Fill line 11 (cursor position) with 0

8

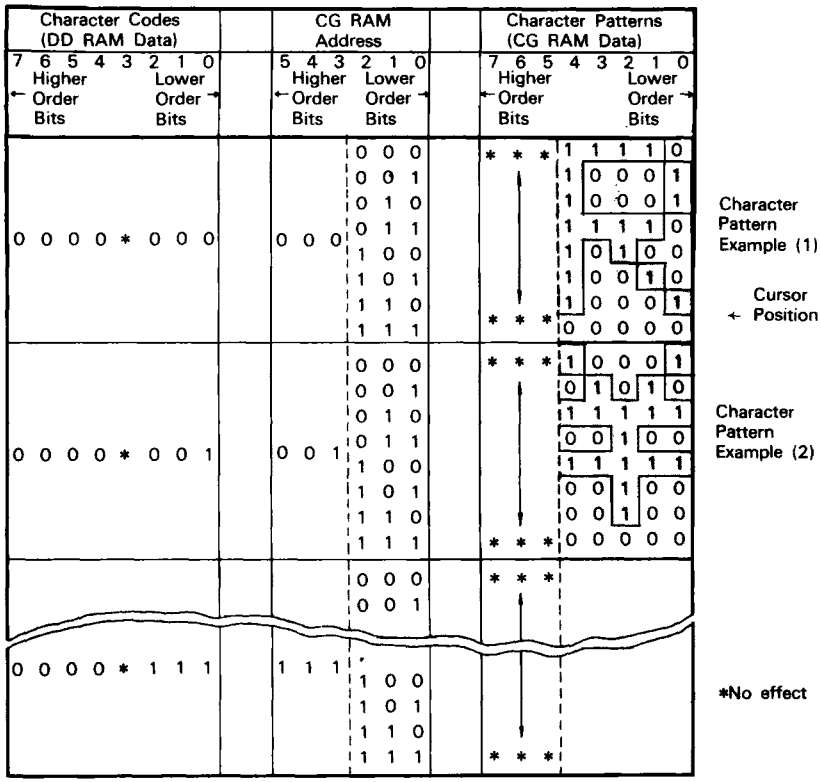
Table 5 Correspondence between Character Codes and Character Pattern (Hitachi Standard HD66702)



Note: The user can specify any pattern for character-generator RAM.

Table 6 Relation between CG RAM Addresses and Character Codes (DD RAM) and Character Patterns (CG RAM Data)

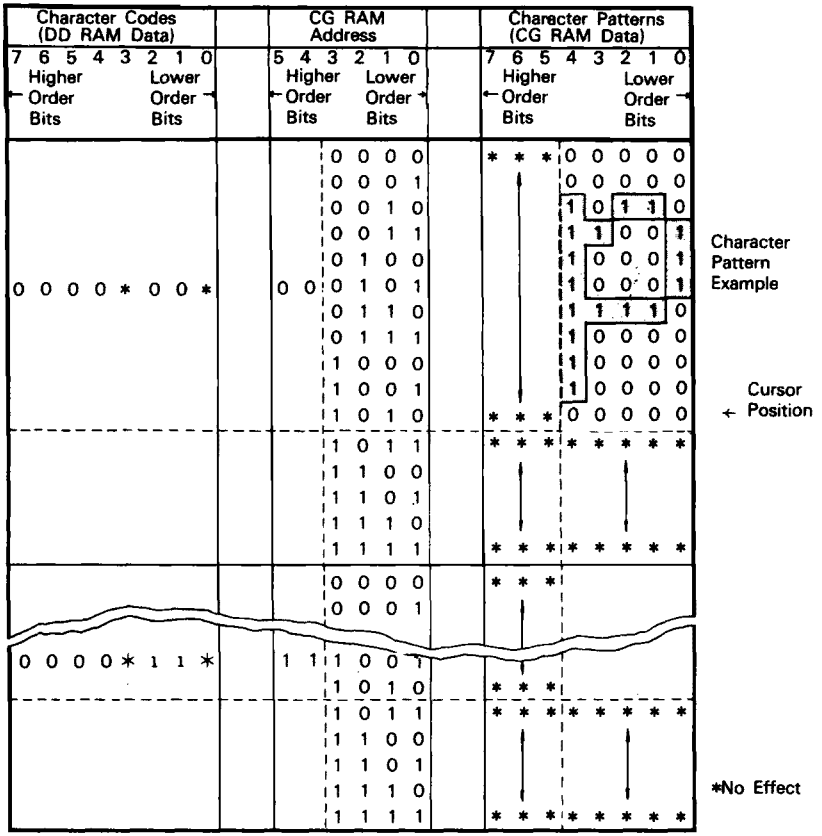
For 5 x 7 dot character patterns



Notes:
1. Character code bits 0–2 correspond to CG RAM address bits 3–5 (3 bits: 8 types).
2. CG RAM address bits 0–2 designate character pattern line position. The 8th line is the cursor position and display is formed by logical OR with the cursor.
   Maintain the 8th line data, corresponding to the cursor display position, in the 0 state for cursor display. When the 8th line data is 1, bit 1 lights up regardless of cursor presence.
3. Character pattern row positions correspond to CG RAM data bits 0–4, as shown in the figure (bit 4 being at the left end).
   Since CG RAM data bits 5–7 are not used for display, they can be used for the general data RAM.
4. As shown in tables 3 and 4, CG RAM character patterns are selected when character code bits 4–7 are all 0. However, since character code bit 3 has no effect, the "R" display in the character pattern example is selected by character code "00" (hexadecimal) or "08" (hexadecimal).
5. 1 for CG RAM data corresponds to display selection and 0 to non-selection.

Table 6 Relation between CG RAM Addresses and Character Codes (DD RAM) and Character Patterns (CG RAM Data) (Continued)

For 5 × 10 dot character patterns



Notes: 1. Character code bits 1, 2 correspond to CG RAM address bits 4, 5 (2 bits: 4 types).
2. CG RAM address bits 0-3 designate character pattern line position. The 11th line is the cursor position and display is formed by logical OR with the cursor.
Maintain the 11th line data corresponding to the cursor display position in the 0 state for cursor display. When the 11th line data is 1, bit 1 lights up regardless of cursor presence. Since the 12th-16th lines are not used for display, they can be used for general data RAM.
3. Character pattern row positions are the same as 5 × 7 dot character pattern positions.
4. CG RAM character patterns are selected when character code bits 4-7 are all 0. However, since character code bit 0 and 3 have no effect, "P" display in the character pattern example is selected by character codes "00", "01", "08" and "09" (hexadecimal).
5. 1 for CG RAM data corresponds to display selection and 0 to non-selection.

Timing Generation Circuit

The timing generation circuit generates timing signals to operate internal circuits such as DD RAM, CG ROM, and CG RAM. RAM read timing needed for display and internal operation timing by MPU access are separately generated so they do not interfere with each other. Therefore, when writing data to the DD RAM, for example, there will be no undesirable influence, such as flickering, in areas other than the display area. This circuit also generates timing signals to operate the externally connected driver LSI HD44100H.

Liquid Crystal Display Driver Circuit

The liquid crystal display driver circuit consists of 16 common signal drivers and 100 segment signal drivers. When character font and number of lines are selected by a program, the required common signal drivers automatically output drive waveforms, the other common signal drivers continue to output non-selection waveforms.

The segment signal driver has essentially the same configuration as the driver LSI HD44100H. Character pattern data is sent serially through a 100-bit shift register and latched when all needed data has arrived. The latched data controls the driver for generating drive waveform outputs. The serial data can be sent to HD44100H's, externally connected in cascade, used for display digit number extension.

Serial data send always starts at the display data character pattern corresponding to the last address of the display data RAM (DD RAM).

Since serial data is latched when the display data character pattern corresponding to the starting address enters the internal shift register, the HD66702 drives the head display. The rest displays, corresponding to latter addresses, are added with each additional HD44100H.

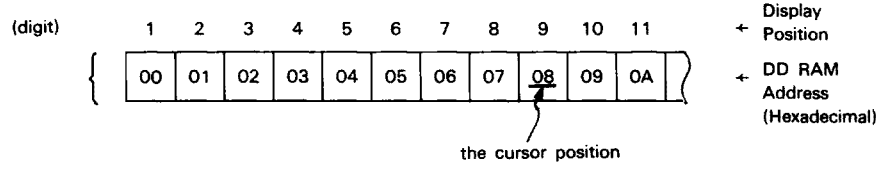
Cursor/Blink Control Circuit

The cursor/blink control circuit generates the cursor or blink. The cursor or the blink appear in the digit at the display data RAM (DD RAM) address set in the address counter (AC).

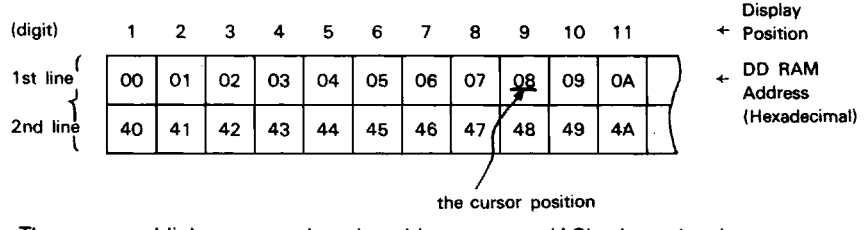
When the address counter is $(08)_{16}$, the cursor position is:

	AC6	AC5	AC4	AC3	AC2	AC1	AC0
AC	0	0	0	1	0	0	0

In a 1-line display



In a 2-line display



Note: The cursor or blink appears when the address counter (AC) selects the character generator RAM (CG RAM). But the cursor and blink are meaningless.
The cursor or blink is displayed in the meaningless position when AC is a CG RAM address.

8

Interfacing To MPU

In the HD66702, data can be sent in either two 4-bit operations or one 8-bit operations so it can interface to both 4- and 8-bit MPUs.

1. When interface data is 4-bits long, data is transferred using only 4 buslines: DB_4–DB_7. DB_0–DB_3 are not used. Data transfer between the HD66702 and the MPU completes when 4-bit data is transferred twice. Data of the higher order 4 bits (contents of DB_4–DB_7 when interface data is 8 bits long) is transferred first, then the lower order 4 bits (contents of DB_0–DB_3 when interface data is 8 bits long) is transferred.

   Check the busy flag after 4-bit data has been transferred twice (one instruction). Two 4-bit operations will then transfer the busy flag and address counter data.

2. When interface data is 8 bits long, data is transferred using the 8 data buslines DB_0–DB_7.

Reset Function

Initializing by Internal Reset Circuit

The HD66702 automatically initializes (resets) when power is turned on using the internal reset circuit. The following instructions are executed during initialization. The busy flag (BF) is kept in busy state until initialization ends (BF = 1). The busy state is 10 ms after V_{cc} rises to 4.5 V.

1. Display clear

2. Function set:
   DL = 1: 8-bit-long interface data
   N = 0: 1-line display
   F = 0: 5 × 7 dot character font

3. Display on/off control:
   D = 0: Display off
   C = 0: Cursor off
   B = 0: Blink off

4. Entry mode set:
   I/D = 1: +1 (increment)
   S = 0: No shift

Note: When conditions in "Power Supply Conditions Using Internal Reset Circuit" are not met, the internal reset circuit will not operate normally and initialization will not be performed. In this case initialize by MPU according to "Initializing by Instruction".

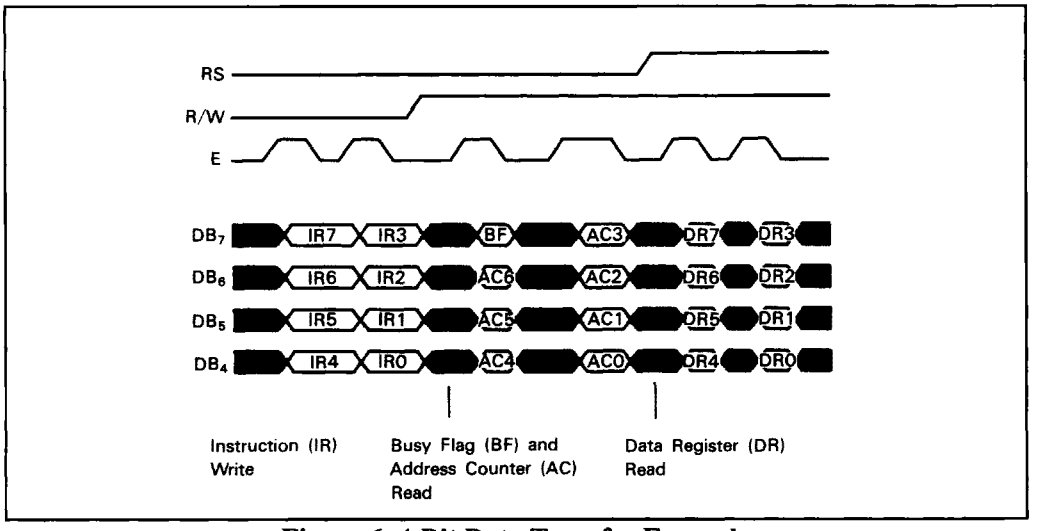


Figure 6 4-Bit Data Transfer Example

Instructions

Outline

Only two HD66702 registers, the instruction register (IR) and the data register (DR) can be directly controlled by the MPU. Prior to internal operation start, control information is temporarily stored in these registers, to allow interface from HD66702 internal operation to various types of MPUs that operate in different speeds or to allow interface to peripheral control ICs. HD66702 internal operation is determined by signals sent from the MPU. These signals include register selection signals (RS), read/write signals (R/W) and data bus signals (OB_0–DB_7), and are here called instructions. Table 7 shows the instructions and their execution time. Details are explained in subsequent sections.

Instructions are of 4 types, those that,

1. Designate HD66702 functions such as display format, data length, etc.
2. Give internal RAM addresses
3. Perform data transfer with internal RAM
4. Others

In normal use, category 3 instructions are used most frequently. However, automatic incrementing by +1 (or decrementing by–1) of HD66702 internal RAM addresses after each data write lessens the MPU program load. The display shift especially can perform concurrently with display data write, enabling the user to develop systems in minimum time with maximum programing efficiency. For an explanation of the shift function in its relation to display, see table 12.

When an instruction is executing during internal operation, no instruction other than the busy flag/address read instruction will be executed.

Because the busy flag is set to 1 while an instruction is being executed, check to make sure it is 1 before sending an instruction from the MPU.

Note: Make sure the HD66702 is not in the busy state (BF = 0) before sending the instruction from the MPU to the HD66702. If the instruction is sent without checking the busy flag, the time between first and next instructions is much longer than the instruction time. See table 7 for a list of each instruction execution time.

Table 7 Instructions

Instruction	Code RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0	Description	Execution Time (max) (when f_{cp} or f_{osc} is 320 kHz)
Clear Display	0	0	0	0	0	0	0	0	0	1	Clears entire display and sets DD RAM address 0 in address counter.	1.28 ms
Return Home	0	0	0	0	0	0	0	0	1	*	Sets DD RAM address 0 in address counter. Also returns display being shifted to original position. DD RAM contents remain unchanged.	1.28 ms
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	S	Sets cursor move direction and specifies shift of display. These operations are performed during data write and read.	31 µs
Display On/Off Control	0	0	0	0	0	0	1	D	C	B	Sets On/OFF of entire display (D), cursor ON/OFF (C), and blink of cursor position character (B).	31 µs
Cursor or Display Shift	0	0	0	0	0	1	S/C	R/L	*	*	Moves cursor and shifts display without changing DD RAM contents.	31 µs
Function Set	0	0	0	0	1	DL	N	F	*	*	Sets interface data length (DL), number of display lines (L) and character font (F).	31 µs
Set CG RAM Address	0	0	0	1	ACG						Sets CG RAM address. CG RAM data is sent and received after this setting.	31 µs
Set DD RAM Address	0	0	1	ADD							Sets DD RAM address. DD RAM data is sent and received after this setting.	31 µs
Read Busy Flag & Address	0	1	BF	AC							Reads Busy flag (BF) indicating internal operation is being performed and reads address counter contents.	0 µs
Write Data to CG or DD RAM	1	0	Write Data								Writes data into DD RAM or CG RAM.	31 µs t_{ADD}=4.7 µs (Note)
Read Data from CG or DD RAM	1	1	Read Data								Reads data from DD RAM or CG RAM.	31 µs t_{ADD}=4.7 µs (Note)
	I/D = 1: Increment I/D = 0: Decrement S = 1: Accompanies display shift S/C = 1: Display shift S/C = 0: Cursor move R/L = 1: Shift to the right R/L = 0: Shift to the left DL = 1: 8 bits, DL = 0: 4 bits N = 1: 2 lines, N = 0: 1 line F = 1: 5 x 10 dots, F = 0: 5 x 7 dots BF = 1: Internally operating BF = 0: Can accept instruction										DD RAM: Display data RAM CG RAM: Character generator RAM A_{CG}: CG RAM address A_{DD}: DD RAM address: Corresponds to cursor address AC: Address counter used for both DD and CG RAM address.	Execution time changes when frequency changes Example: When f_{CD} or F_{OSC} is 270 kHz: $31\ \mu s \times \frac{320}{270} = 37\ \mu s$

*No effect

Note: After execution of a CG RAM/DD RAM data write or read instruction, the RAM address counter is increased or decreased by 1. The RAM address counter is updated after the busy flag turns off. In figure 7, tADD is the time elapsed after the busy flag turns off until the address counter is updated.

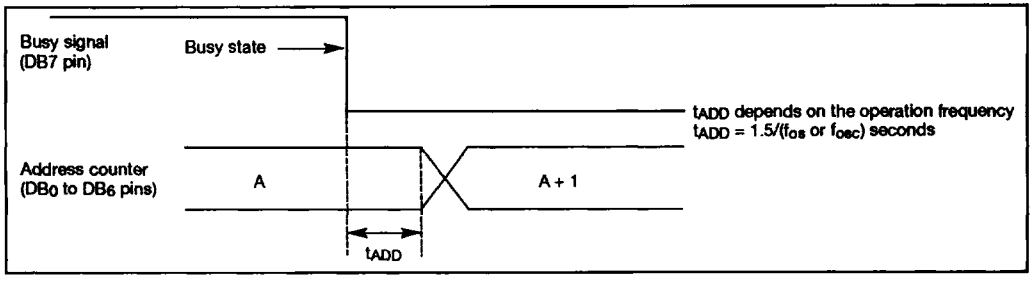


Figure 7 Address Counter Update

Description of Details

1. Clear Display

	RS	R/W	DB_7							DB_0
Code	0	0	0	0	0	0	0	0	0	1

Writes space code 20 (hexadecimal) (character pattern for character code 20 must be blank pattern) into all DD RAM addresses. Sets DD RAM address 0 in address counter. Returns display to its original status if it was shifted. In other words, the display disappears and the cursor or blink go to the left edge of the display (the first line if 2 lines are displayed). Set I/D = 1 (increment mode) in entry mode. S of entry mode doesn't change.

2. Return Home

	RS	R/W	DB_7							DB_0
Code	0	0	0	0	0	0	0	0	1	*

* Don't care

Sets the DD RAM address 0 in address counter. Returns display to its original status if it was shifted. DD RAM contents do not change.

The cursor or blink go to the left edge of the display (the first line if 2 lines are displayed).

3. Entry Mode Set

	RS	R/W	DB_7							DB_0
Code	0	0	0	0	0	0	0	1	I/D	S

I/D: Increments (I/D = 1) or decrements (I/D = 0) the DD RAM address by 1 when a character code is written into or read from the DD RAM.

The cursor or blink moves to the right when incremented by 1 and to the left when decremented by 1. The same applies to writing and reading of CG RAM.

S: Shifts the entire display either to the right or to the left when S is 1; to the left when I/D = 1 and to the right when I/D = 0.

Thus it looks as if the cursor stands still and the display moves. The display does not shift when reading from the DD RAM when writing into or reading out from the CG RAM causes a shift when S = 0.

4. Display On/Off Control

	RS	R/W	DB_7							DB_0
Code	0	0	0	0	0	0	1	D	C	B

D: The display is on when D = 1 and off when D = 0. When off due to D = 0, display data remains in the DD RAM. It can be displayed instantly by setting D = 1.

C: The cursor is displayed when C = 1 and is not displayed when C = 0. Even if the cursor disappears, the function of I/D, etc. does not change during display data write. The cursor is displayed using 5 dots in the 8th line when the 5 × 7 dot character font is selected and 5 dots in the 11th line when the 5 × 10 dot character font is selected (Figure 8).

B: The character indicated by the cursor blinks when B = 1 (Figure 8). The blink is displayed by switching between all blank dots and display characters at 320 ms intervals when f_{cp} or f_{osc} = 320 kHz. The cursor and the blink can be set to display simultaneously. (The blink frequency changes according to the reciprocal of f_{cp} or f_{osc}.

$$320 \times \frac{320}{270} = 379.2 \text{ ms when } f_{cp} = 270 \text{ kHz.})$$

5. Cursor or Display Shift

	RS	R/W	DB_7							DB_0
Code	0	0	0	0	0	1	S/C	R/L	*	*

*Don't care

Shifts cursor position or display to the right or left without writing or reading display data (Table 8). This function is used to correct or search for the display. In a 2-line display, the cursor moves to the 2nd line when it passes the 40th digit of the 1st line. Notice that the 1st and 2nd line displays will shift at the same time.

When the displayed data is shifted repeatedly each line only moves hirizontally. The 2nd line display does not shift into the 1st line position.

Address counter (AC) contents do not change if the only action performed is display shift.

6. Function Set

	RS	R/W	DB_7							DB_0
Code	0	0	0	0	1	DL	N	F	*	*

*Don't care

DL: Sets interface data length. Data is sent or received in 8 bit lengths (DB_7–DB_0) when DL = 1 and in 4 bit lengths (DB_7–DB_4) when DL = 0.

When the 4 bit length is selected, data must be sent or received twice.

N: Sets number of display lines.

F: Sets character font.

Note: Perform the function at the head of the program before executing any instructions (except "Busy flag/address read"). From this point, the function set instruction cannot be executed unless the interface data length is changed.

7. Set CG RAM Address

	RS	R/W	DB_7							DB_0
Code	0	0	0	1	A	A	A	A	A	A
			← Higher Order Bits						Lower Order Bits →	

Sets the CG RAM address binary AAAAAA into the address counter.

Data is then written or read from the MPU for the CG RAM.

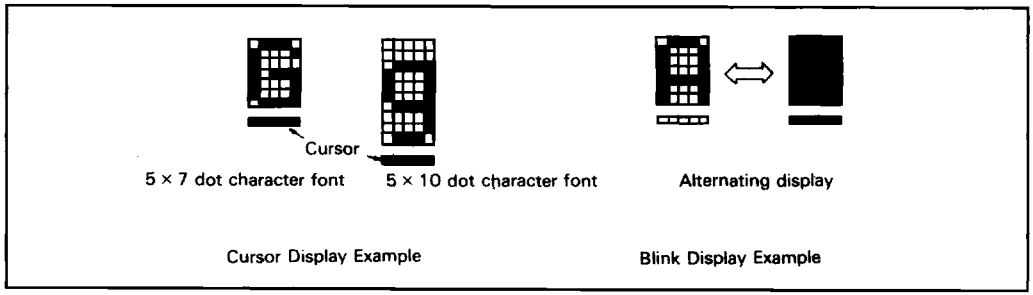


Figure 8 Cursor and Blink

8. Set DD RAM Address

	RS	R/W	DB_7							DB_0
Code	0	0	1	A	A	A	A	A	A	A
			← Higher Order Bits						Lower Order Bits →	

Sets the DD RAM address binary AAAAAAA into the address counter.

Data is then written or read from the MPU for the DD RAM.

However, when N = 0 (1-line display), AAAAAAA can be 00-4F (hexadecimal). When N = 1 (2-line display), AAAAAAA can be 00-27 (hexadecimal) for the first line, and 40-67 (hexadecimal) for the second line.

9. Read Busy Flag and Address

	RS	R/W	DB_7							DB_0
Code	0	1	BF	A	A	A	A	A	A	A
			← Higher Order Bits						Lower Order Bits →	

Reads the busy flag (BF) that indicates that the system is now internally operating on a previously received instruction. BF = 1 indicates that internal operation is in progress. The next instruction will not accepted until BF is set to 0. Check the BF status before the next wire operation. At the same, the value of the address counter expressed in binary as AAAAAAA is read out. The address counter is used by both CG and DD RAM addresses, and its value is determined by the previous instruction. Address contents are the same as in items 7 and 8.

Table 8 Shift Function

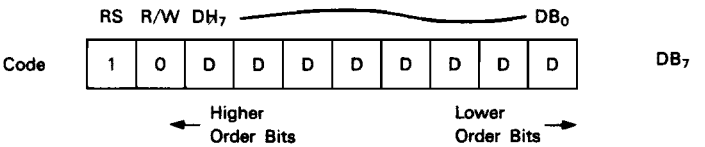
S/C	R/L	
0	0	Shifts the cursor position to the left. (AC is decremented by one.)
0	1	Shifts the cursor position to the right. (AC is incremented by one.)
1	0	Shifts the entire display to the left. The cursor follows the display shift.
1	1	Shifts the entire display to the right. The cursor follows the display shift.

Table 9 Function Set

N	F	No. of Display Lines	Character Font	Duty Factor	Remarks
0	0	1	5 x 7 dots	1/8	
0	1	1	5 x 10 dots	1/11	
1	*	2	5 x 7 dots	1/16	Cannot display 2 lines with 5 x 10 dot character font

*Don't care

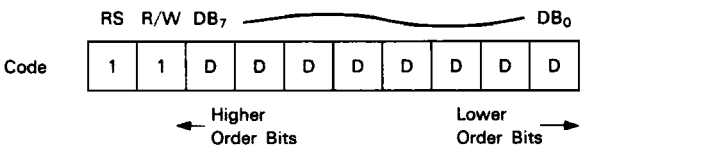
10. Write Data to CG or DD RAM



Writes binary 8-bit data DDDDDDDD to the CG or the DD RAM.

Whether the CG or DD RAM is to be written into is determined by the previous specification of CG RAM or DD RAM address setting. After write, the address is automatically incremented or decremented by 1 according to entry mode. The entry mode also determines display shift.

11. Read Data from CG or DD RAM



Reads binary 8-bit data DDDDDDDD from the CG or DD RAM.

The previous designation determines whether the CG or DD RAM is to be read. Before entering either the CG RAM or DD RAM address set instruction. If you don't, the first read data will be invalidated. When serially executing read instructions, the next address data is normally read from the second read. The address set instruction need not be executed just before the read instruction when shifting the cursor by cursor shift instruction (when reading out DD RAM). The cursor shift instruction operation is the same as that of the DD RAM's address set instruction.

After a read, the entry mode automatically increases or decreases the address by 1. However, display shift is not executed no matter what the entry mode is.

Note: The address counter (AC) is automatically incremented or decremented by 1 after write instructions to either CG RAM or DD RAM. RAM data selected by the AC cannot then be read out even if read instructions are executed. The conditions for correct data readout are: execute either the address set instruction or cursor shift instruction (only with DD RAM), then just before reading out execute the "read" instruction from the second time the "read" instruction is sent.

Connecting directly to the 8-bit MPU bus line

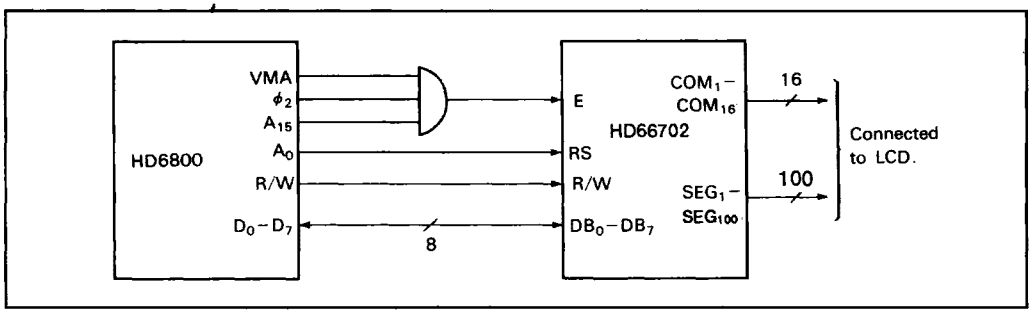


Figure 11 8-Bit MPU Interface

Example of interfacing to the HD6805

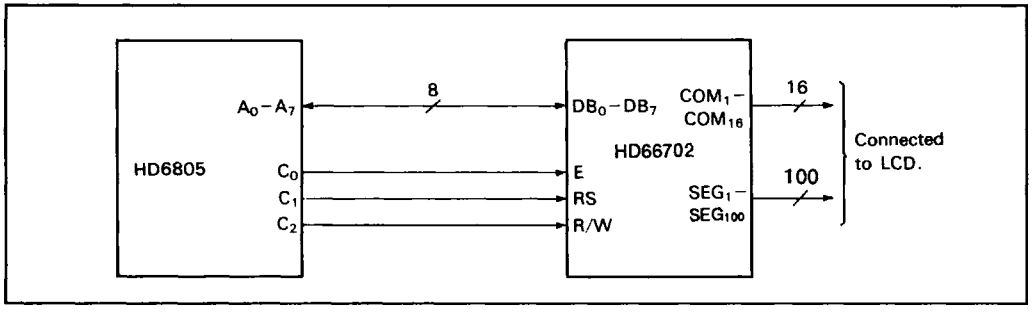


Figure 12 HD6805 Interface

8

Example of interfacing to the HD6301

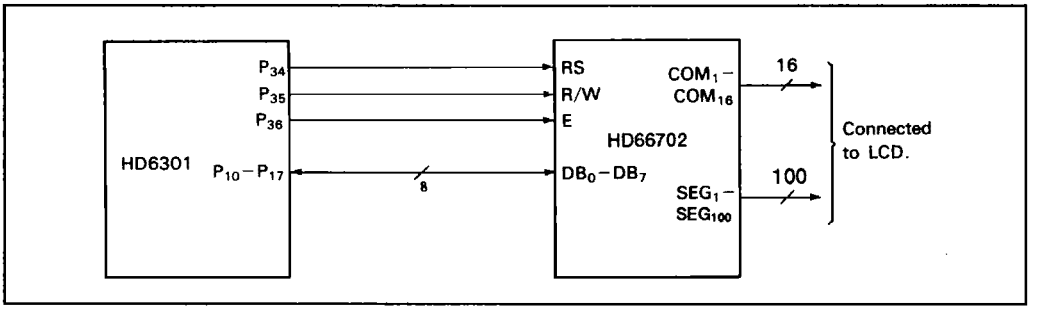


Figure 13 HD6301 Interface

How To Use The HD66702

Interface to MPU

1. Interface to 8-Bit MPU

When connecting to 8-bit MPU through PIA

Figure 15 is an example of using a PIA or I/O port (for single chip microcomputer) as an interface device. Input and output of the device is TTL compatible.

In the example, PB_0 to PB_7 are connected to the data buses DB_0 to DB_7 and PA_0 to PA_2 are connected to E, R/W and RS respectively.

Pay attention to the timing relation between E and other signals when reading or writing data and using PIA as an interface.

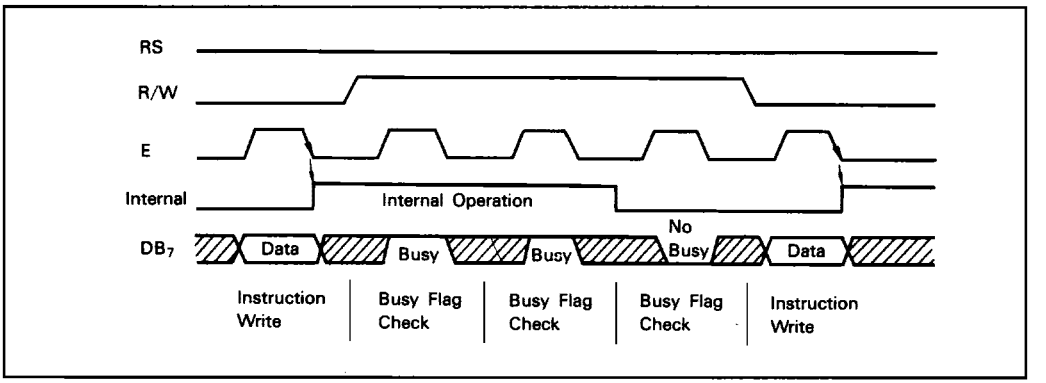


Figure 14 Example of Busy Flag Check Timing Sequence

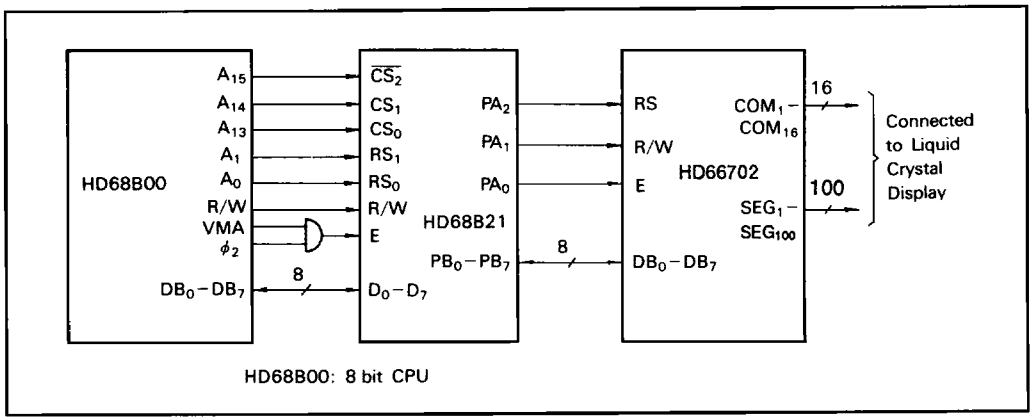


Figure 15 Example of Interface to HD68B00 Using PIA (HD68B21)

2. Interface to 4-bit MPU

The HD66702 can be connected to a 4-bit MPU through the 4-bit MPU I/O port. If the I/O port has enough bits, data can be transferred in 8-bit lengths, but if there are insufficient bits, the transfer is made in two operations of 4 bit each (with designation of interface data length for 4 bits). In the latter case, the timing sequence becomes somewhat complex (See figure 16).

Figure 17 shows an example of interface to the HMCS43C.

Note: that 2 cycles are needed for the busy flag check as well as the data trnsfer. 4-bit operation is selected by program.

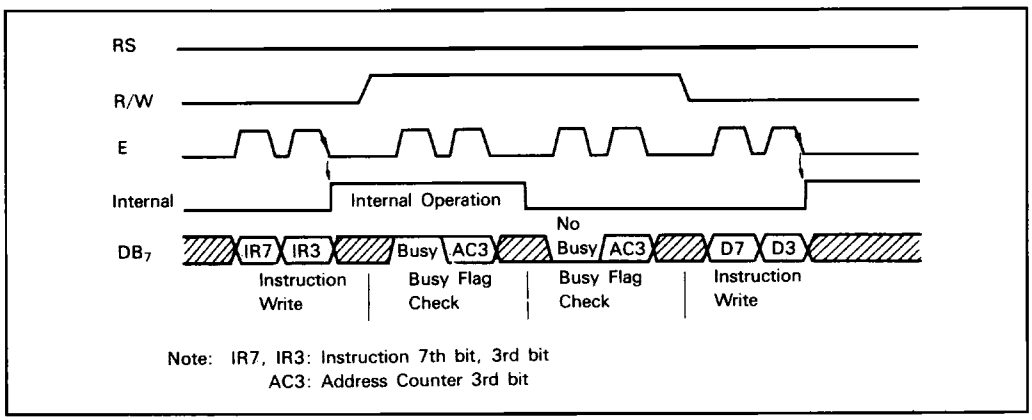


Figure 16 An Example of 4-Bit Data Transfer Timing Sequence

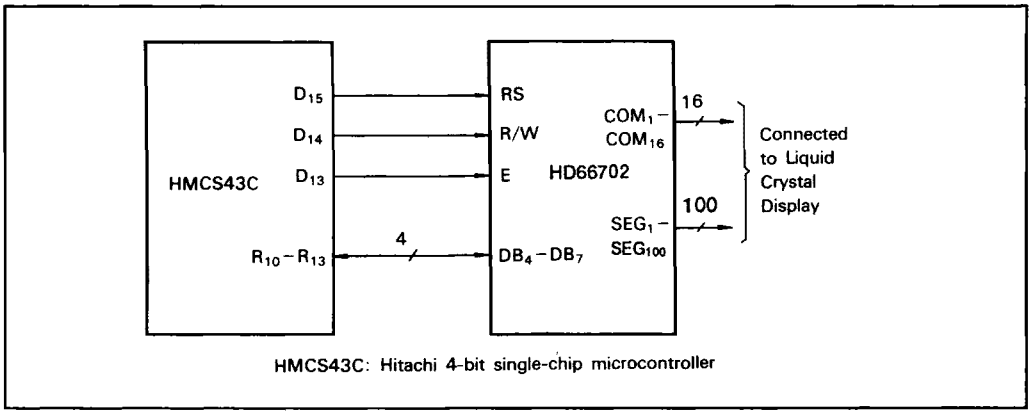


Figure 17 Example of Interface to the HMCS43C

Interface to Liquid Crystal Display

1. Character Font and Number of Lines

   The HD66702 can perform 2 types of display, 5 × 7 dots and 5 × 10 dots character font, with a cursor on each.

   Up to 2 lines are displayed with 5 × 7 dots and 1 line with 5 × 10 dots. Therefore, three types of common signals are available (Table 10).

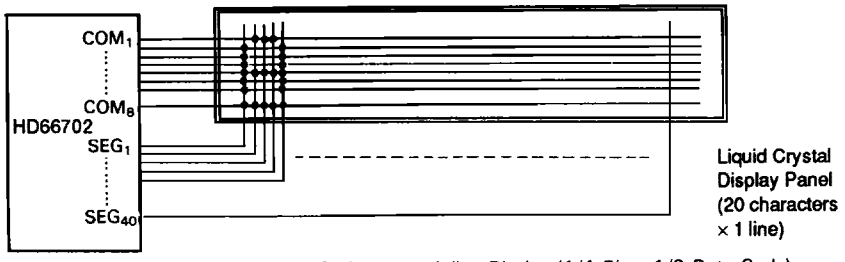
   Number of line and font types can be selected by program. (See Table 7, Instructions).

2. Connection to HD67702 and Liquid Crystal Display

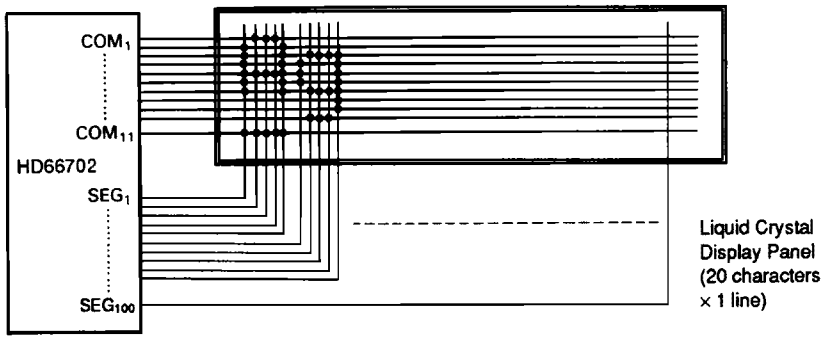
   Figure 18 shows connection examples.

Table 10 Common Signals

Number of Lines	Character Font	Number of Common Signals	Duty Factor
1	5 x 7 dots + Cursor	8	1/8
1	5 x 10 dots + Cursor	11	1/11
2	5 x 7 dots + Cursor	16	1/16



(a) Example of a 5×7 dot, 8 character×1 line Display (1/4 Bias, 1/8 Duty Cycle)

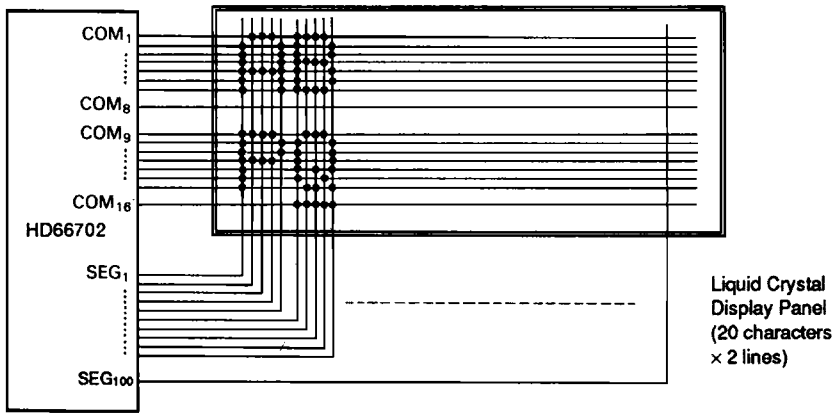


(b) Example of 5 × 10 dot, 20 character × 1 line Display (1/4 Bias, 1/8 Duty Cycle)

Figure 18 Liquid Crystal Display and Connections to HD66702

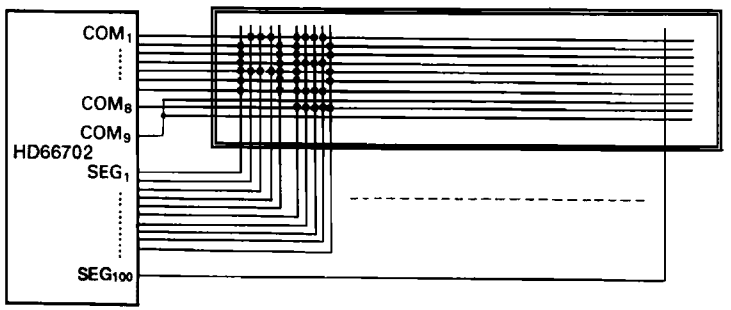
Since 5 SEG signal lines can display one digit, one HD66702 can display up to 20 digits for 1-line display and 40 digits for 2-line display.

In Figure 19 examples (a) and (b), there are unused common signal terminals, which always output non-selection waveforms. When the liquid crystal display panel has unused extra scanning lines, avoid undesirable influences due to crosstalk in the floating state by connecting the extra scanning lines to these common signal terminals (Figure 20).



(c) Example of 5 × 7 dot, 20 character × 2 lines Display (1/5 Bias, 1/16 Duty Cycle)

Figure 19 Liquid Crystal Display and Connections to HD66702 (Cont'd.)



5 × 7 dot, 20 character × 1 line Display (1/4 Bias, 1/8 Duty Cycle)

Figure 20 Using COM9 to Avoid Crosstalk on Unneeded Scanning Line

3. Connection of Changed Matrix Layout

In the preceding examples, the number of lines matched the number of scanning lines. The display types Figure 21 are made possible by changing the matrix layout in the liquid crystal display panel. In either case, the only change is the layout. Display characteristics and the number of liquid crystal display characters depend on the number of common signals (or duty factor). Note that the display data RAM (DD RAM) addresses for 10 characters × 2 lines and 40 characters × 1 line are the same as shown in Figure 19.

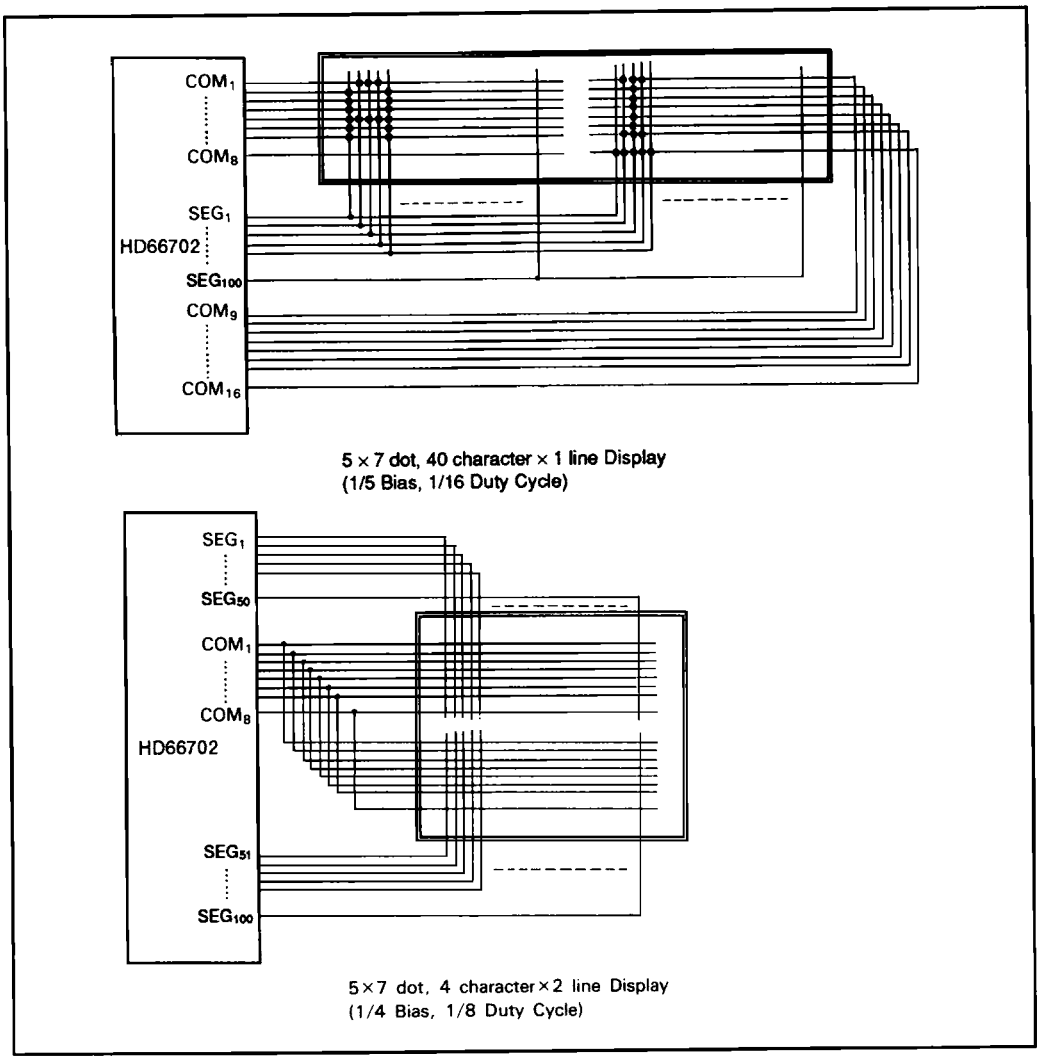


Figure 21 Changed Matrix Layout Displays

Power Supply for Liquid Crystal Display Drive

Various voltage levels must be applied to HD66702 terminals V_1 to V_5 to obtain liquid crystal display drive waveforms. The voltages must be changed according to duty factor. Table 11 shows the relation.

V_{LCD} gives the peak values for liquid crystal display drive waveforms. Resistance dividing provides each voltage as shown in Figure 22.

Table 11 Duty Factor and Power Supply for Liquid Crystal Display Drive

Duty Factor		1/8, 1/11	1/16
Power Supply	Bias	1/4	1/5
V_1		V_{cc} – 1/4 V_{LCD}	Vcc – 1/5 V_{LCD}
V_2		V_{cc} – 1/2 V_{LCD}	Vcc – 2/5 V_{LCD}
V_3		V_{cc} – 1/2 V_{LCD}	Vcc – 3/5 V_{LCD}
V_4		V_{cc} – 3/4 V_{LCD}	Vcc – 4/5 V_{LCD}
V_5		V_{cc} – V_{LCD}	Vcc – V_{LCD}

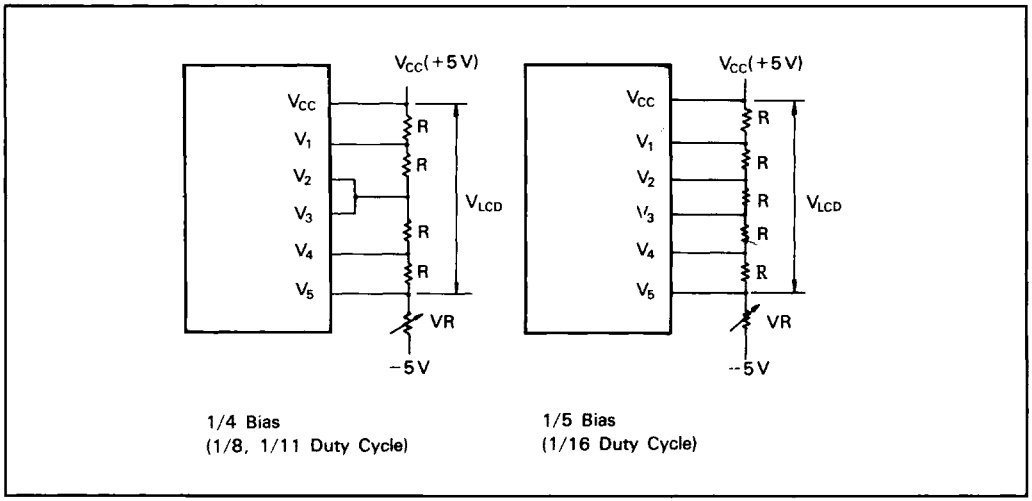
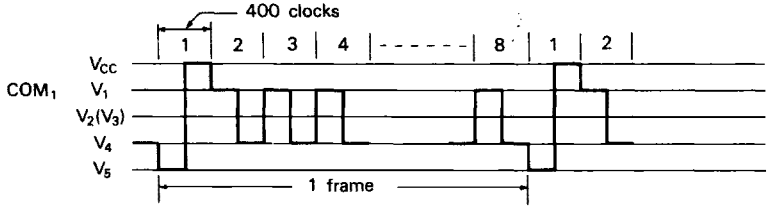


Figure 22 Drive Voltage Supply Example

Relation between Oscillation Frequency and Liquid Crystal Display Frame Frequency

The examples in Figure 23 of liquid crystal display frame frequency apply only when oscillation frequency is 320 kHz (1 clock pulse = 3.125 μs).

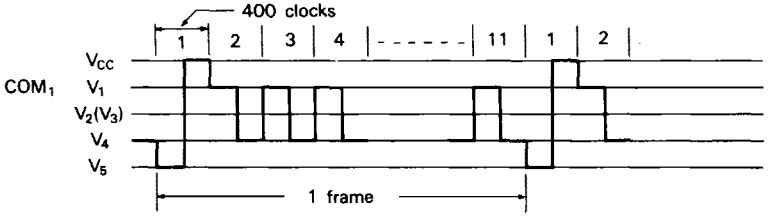
1. 1/8 Duty Cycle



1 frame = 3.125 (μs) × 400 × 8 = 10000 (μs) = 10 (ms)

Frame frequency = $\frac{1}{10\ (ms)}$ = 100 (Hz)

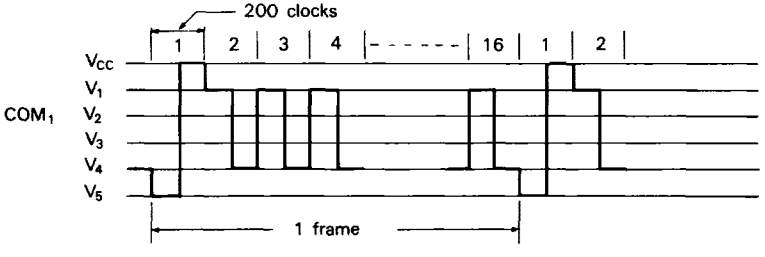
2. 1/11 Duty Cycle



1 frame = 3.125 (μs) × 400 × 11 = 13750 (μs) = 13.75 (ms)

Frame frequency = $\frac{1}{13.75\ (ms)}$ = 72.7 (Hz)

3. 1/16 Duty Cycle



1 frame = 3.125 (μs) × 200 × 16 = 10000 (μs) = 10 (ms)

Frame frequency = $\frac{1}{10\ (ms)}$ = 100 (Hz)

Figure 23 Frame Frequency

Connection with Driver LSI HD44100H

You can increase the number of display digits by externally connecting an HD44100H liquid crystal display driver LSI to the HD66702. When connected to the HD66702, the HD44100H is used as segment signal driver. The HD44100H can be connected to the HD66702 directly since it supplies CL_1, CL_2, M, and D signals and power for liquid crystal display drive. Figure 24 shows a connection example.

Caution: Connection of voltage supply terminals V_1 through V_6 for liquid crystal display drive is complicated. The EXT pin must be fixed low if the HD44100H is connected to the HD66702.

Up to 8 HD44100H units can be connected for 1-line display (duty factor 1/8 or 1/11) and up to 3 units for the 2-line display (duty factor 1/16). RAM size limits the HD66702 to a maximum of 80 character display digits. The connection method in figure 22 remains unchanged for both 1-line and 2-line display or 5 × 7 and 5 × 10 dot character fonts.

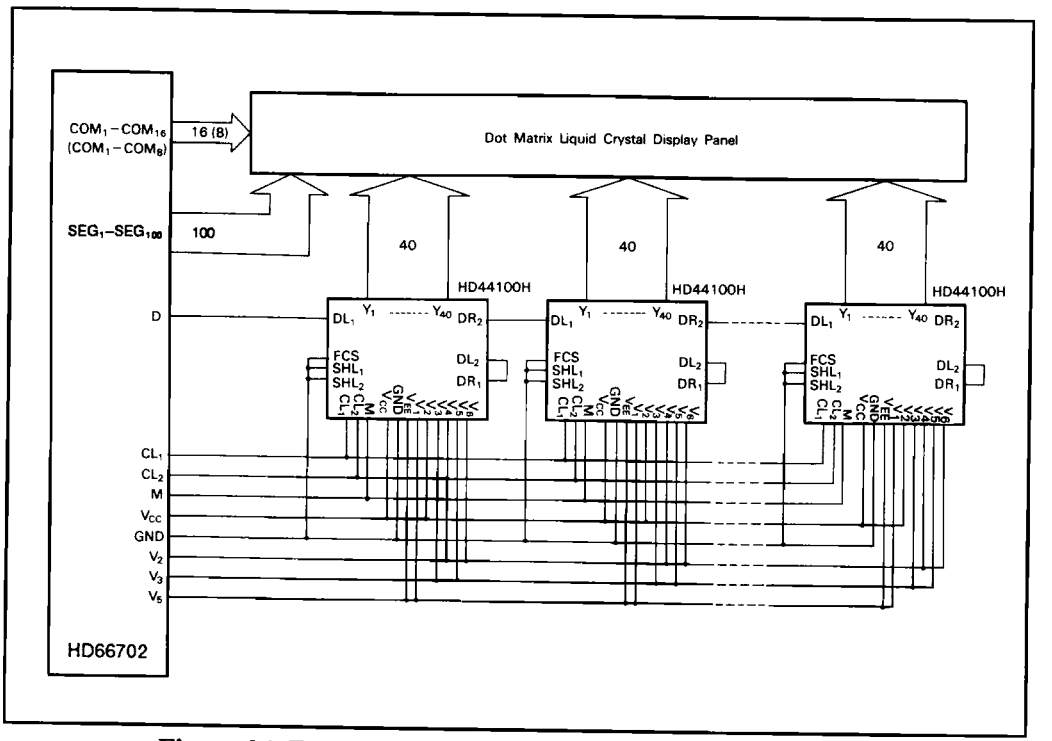


Figure 24 Example of Connecting HD44100H to HD66702

Instruction and Display Correspondence

1. 8-bit operation, 20-digit × 1-line display (using internal reset)

   Table 12 shows an example of 8-bit × 1-line display in 8-bit operation. The HD66702 functions must be set by function set instruction prior to display. Since the display data RAM can store data for 80 characters, as explained before, the RAM can be used for displays like a lighting board when combined with display shift operation.

   Since the display shift operation changes display position only and DD RAM contents remain unchanged, display data entered first can be output when the return home operation is performed.

2. 4-bit operation, 20-digit × 1-line display (using internal reset)

   The program must set functions prior to 4-bit operation. Table 13 shows an example. When power is turned on, 8-bit operation is automatically selected and the first write is performed as an 8-bit operation. Since nothing is connected to DB_0–DB_3, a rewrite is then required. However, since one operation is completed in two accesses of 4-bit operation, a rewrite is needed as function (see table 13). Thus, DB_4–DB_7 of the function set is written twice.

3. 8-bit operation, 20-digit × 2-line display

   For 2-line display, the cursor automatically moves from the first to the second line after the 40th digit of the 1st line has been written. Thus, if there are only 20 characters in the first line, the DD RAM address must again be set after the 20th character is completed. (See table 14). Note that the first and second lines of the display shift are performed. In the example, the display shift is performed when the cursor is on the second line. However, if the shift operation is performed when the cursor is on the first line, both the first and the second lines move together. When you repeat the shift, the display of the second line will not move to the first line, the same display will only move within each line many times.

Note: When using the internal reset, the conditions in "Power Supply Condition Using Internal Reset Circuit" must be satisfied. If not, the LCD-II/E20 must be initialized by instruction. (As the internal reset does not function correctly in the 3-V LCD-II/E20, it must always be initialized by instruction.) See "Initializing by Instruction."

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Table 12 8-Bit Operation, 20-Digit 1-Line Display Example (Using Internal Reset)

Step No.	Instruction	Display	Operation
1	Power Supply On (HD66780 is initialized by the internal reset circuit)		Initialized. No display appears.
2	Function Set RS R/W DB7 · · · DB0 0 0 0 0 1 1 0 0 * *		Sets to 8-bit operation and selects 1-line display and one of the three character fonts. (Number of display lines and character font cannot be changed after this.)
3	Display On/Off Control 0 0 0 0 0 0 1 1 1 0		Turns on display and cursor. Entire display is on space mode because of initialization.
4	Entry Mode Set 0 0 0 0 0 0 0 0 1 1 0		Sets mode to increment the address by one and to shift the cursor to the right at the time of write to the DD/CG RAM. Display is not shifted.
5	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 0 0 0	H	Writes "H". The DD RAM has already been selected by initialization when the power is turned on. The cursor is incremented by one and shifted to the right.
6	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 0 0 1	HI	Writes "I".
7	⋮	⋮	
8	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 0 0 1	HITACHI	Writes "I".
9	Entry Mode Set 0 0 0 0 0 0 0 1 1 1	HITACHI	Sets mode for display shift at the time of write.
10	Write Data to CG RAM/DD RAM 1 0 0 0 1 0 0 0 0 0	ITACHI	Writes space.
11	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 1 0 1	TACHI M	Writes "M".
12	⋮	⋮	
13	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 1 1 1	MICROKO	Writes "O".
14	Cursor or Display Shift 0 0 0 0 0 1 0 0 * *	MICROKO	Shifts only the cursor position to the left.
15	Cursor or Display Shift 0 0 0 0 0 1 0 0 * *	MICROKO	Shifts only the cursor position to the left.
16	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 0 0 1 1	ICROCO	Writes "C" (correction). The display moves to the left.
17	Cursor or Display Shift 0 0 0 0 0 1 1 1 * *	MICROCO	Shifts the display and cursor position to the right.
18	Cursor or Display Shift 0 0 0 0 0 1 0 1 * *	MICROCO	Shifts only the cursor position to the right.
19	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 1 0 1	ICROCOM	Writes "M".
20	⋮	⋮	
21	Return Home 0 0 0 0 0 0 0 0 1 0	HITACHI	Returns both display and cursor to the original position (address 0).

Table 13 4-Bit Operation, 20-Digit 1-Line Display Example (Using Internal Reset)

Step No.	Instruction	Display	Operation
1	Power Supply On (HD66780 is initialized by the internal reset circuit)		Initialized. No display appears.
2	Function Set RS R/W DB_7 · · · DB_4 0 0 0 0 1 0		Sets to 4-bit operation. In this case, operation is handled as 8 bits by initialization, and only this instruction completes with one write.
3	Function Set 0 0 0 0 1 0 0 0 0 0 * *		Sets to 4-bit operation and selects 1-line display and one of the three character fonts. 4-bit operation starts from this point on and resetting is needed. (Number of display lines and character font cannot be changed after this.)
4	Display On/Off Control 0 0 0 0 0 0 0 0 1 1 1 0		Turns on display and cursor. Entire display is in space mode because of initialization.
5	Entry Mode Set 0 0 0 0 0 0 0 0 0 1 1 0		Sets mode to increment the address by one and to shift the cursor to the right, at the time of write, to the DD/CG RAM. Display is not shifted.
6	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 0 1 0 0 0	H	Writes "H". The DD RAM has already been selected by initialization when the power is turned on. The cursor is incremented by one and shifted to the right.

After this, control is the same as 8-bit operation.

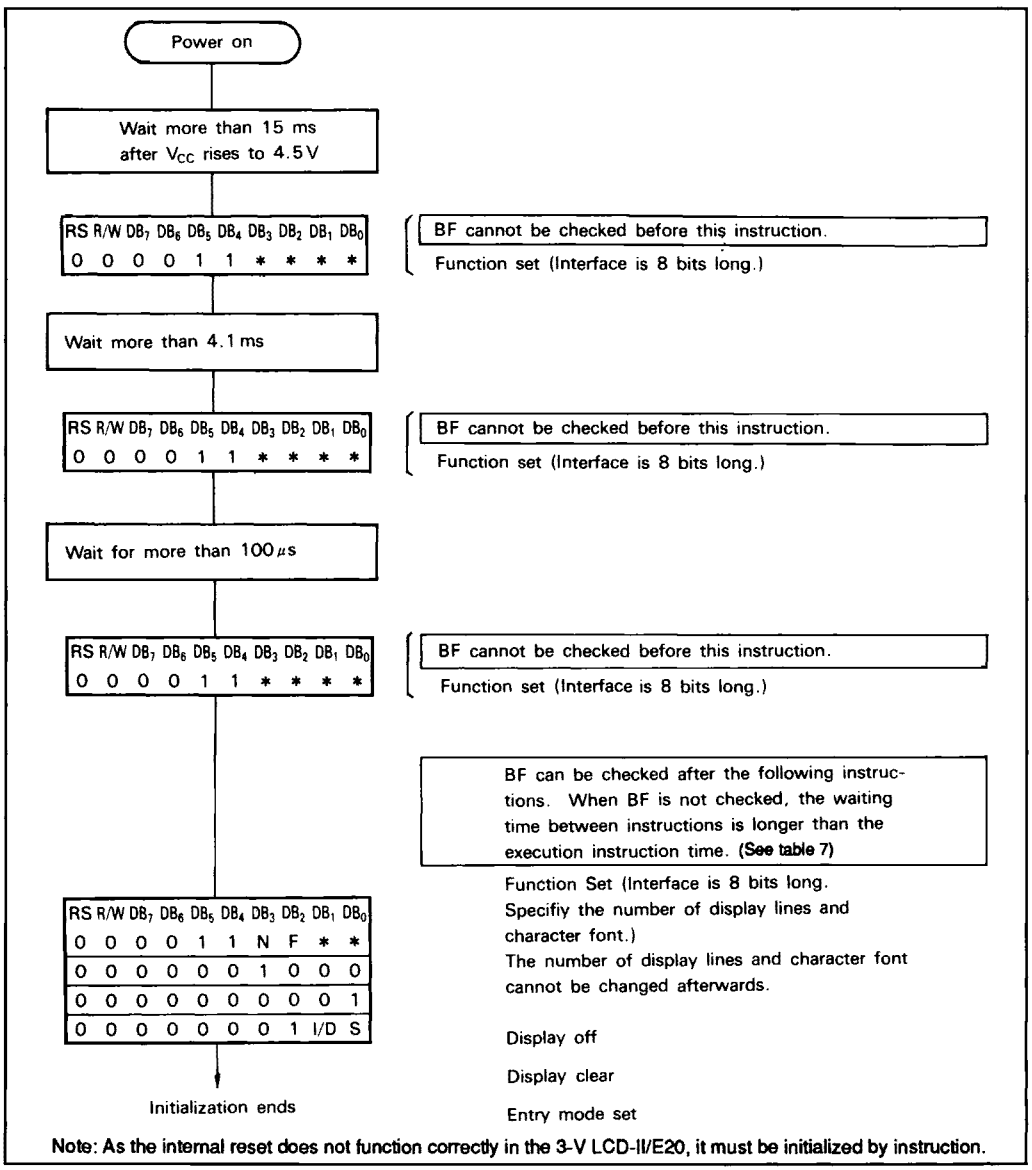
Table 14 8-Bit Operation, 20-Digit × 2-Line Display Example (Using Internal Reset)

No.	Instruction	Display	Operation
1	Power supply on (HD66702 is intialized by the internal reset circuit)		Initalized. No display appears.
2	Function Set RS R/W DB_7 ~ DB_0 0 0 0 0 1 1 1 0 * *		Sets to 8-bit operation and selects 2-line display and 5 × 7 dot character font.
3	Display On/Off Control 0 0 0 0 0 0 1 1 1 0		Turns on display and cursor. All display is in space mode because of initialization.
4	Entry Mode Set 0 0 0 0 0 0 0 1 1 0		Sets mode to increment the address by one and to shift the cursor to the right, at the time of write, to the DD/CG RAM. Display is not shifted.
5	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 0 0 0	H_	Writes "H". The DD RAM has already been selected by initialization when the power is turned on. The cursor is incremented by one and shifted to the right.
6	:	:	
7	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 0 0 1	HITACHI_	Writes "I".
8	Set DD RAM Address 0 0 1 1 0 0 0 0 0 0	HITACHI _	Sets RAM address so that the cursor is positioned at the head of the 2nd line.
9	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 1 0 1	HITACHI M_	Writes "M".
10	:	:	
11	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 1 1 1	HITACHI MICROCO_	Writes "O".
12	Entry Mode Set 0 0 0 0 0 0 0 1 1 1	HITACHI MICROCO_	Sets mode for display shift at the time of write.
13	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 1 0 1	ITACHI ICROCOM_	Writes "M". Display is shifted to the right. The first and second lines' shift operate at the same time.
14	:	:	
15	Return Home 0 0 0 0 0 0 0 0 1 0	HITACHI MICROCOM	Returns both display and cursor to the original position (Address 0).

Initializing by Instruction

If the power supply conditions for correctly operating the internal reset circuit are not met, initialization by instruction is required. Use the procedure in Figures 25 and 26 for initialization.

1:



Note: As the internal reset does not function correctly in the 3-V LCD-II/E20, it must be initialized by instruction.

Figure 25 8-Bit Interface

2:

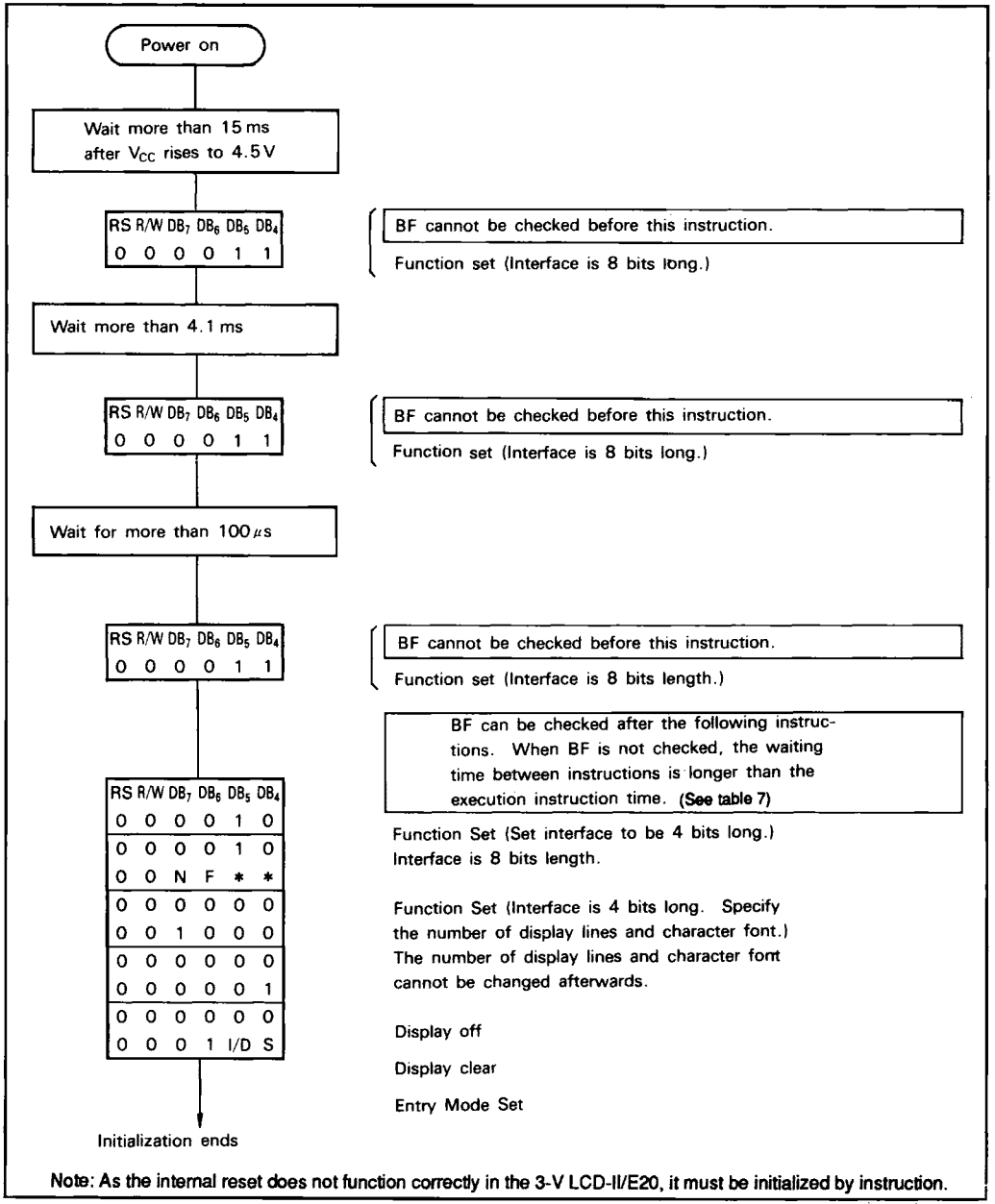


Figure 26 4-Bit Interface