

July 1988

DESCRIPTION

The SSI 78P8060 is a CMOS digital IC that receives and deserializes serial unipolar data in a T1, D2 or T1, D3 format. The IC is functionally identical and pin compatible with the Rockwell R8060 but offers reduced power consumption and provides greater output current drive (fully TTL).

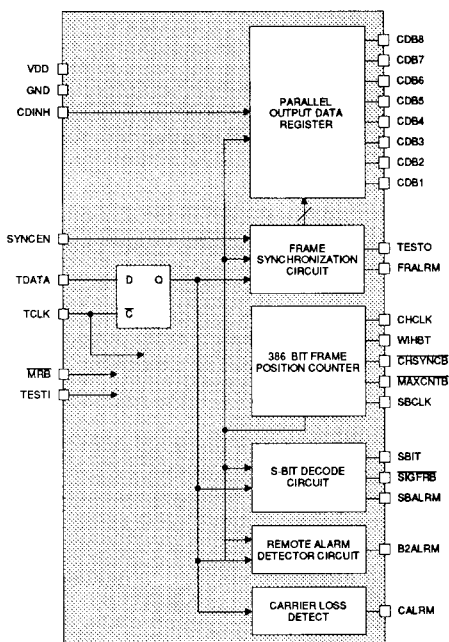
The IC receives 1.544 MBit/s unipolar data and an extracted clock. The data pattern is in 193 bit frames, each frame consisting of a frame bit (FT) or a signaling bit (FS) followed by 192 bits of data representing 24 channels of 8-bit words. F frames and S frames alternate. The receiver synchronizes by locking to (FT) which occurs every 386 bits and which continually alters between 1 and 0, and deserializes the data stream into 24 eight-bit wide channels which are clocked out of the 8 data bit pins at a 192,000 channel/s rate with each channel repeated at a 8000 frame/s rate. Signaling bits (FS), which are positioned 193 bits behind the frame bit, are output at the SBIT pin.

Remote alarm reporting is monitored and an alarm is indicated at the B2ALRM pin if 255 consecutive bit two zeros are received. The incoming data is monitored for loss of carrier and an alarm is indicated at the CALRM pin if 31 consecutive zero bits are received.

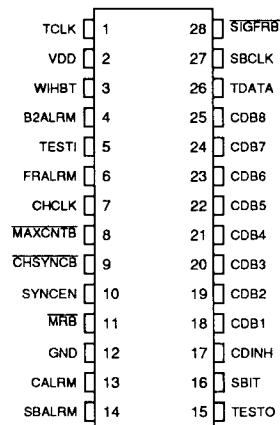
FEATURES

- Locks onto and deserializes incoming T1, D2 and T1, D3 data in 5 ms
- Generates timing signals to synchronize channel and frame information
- Monitors and detects
 - FS bit
 - Frame sync
 - Carrier
 - Remote alarm reporting
- TTL compatible
- CMOS low power dissipation, 5 mW typical
- Single 5V supply

BLOCK DIAGRAM



PIN DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

SSI 78P8060

CMOS Digital IC

T1 Transmitter

PIN DESCRIPTION

NAME	TYPE	DESCRIPTION
TCLK	I	Data Clock. Nominal clock frequency is 1.544 MHz. Data bits are clocked into the chip on the falling edge of the clock.
WIHBT	O	Write Inhibit Clock. Strobes high once every channel for two TCLK periods and is used to load the 8-bit parallel channel output data into external circuitry.
B2ALRM	O	Bit 2 Alarm Signal, active high. Goes high indicating a remote alarm when 255 consecutive 0's are received in the bit 2 position. Resets low after bit 2 becomes 1.
TESTI	I	Test Input, when low puts the circuit in its test mode. Must be high or left open during normal operation.
FRALRM	O	Frame Alarm, active high. Goes high when frame sync is lost.
CHCLK	O	Output Data Channel Clock. Going high signals new parallel data output.
MAXCNTB	O	Strobes low once every two frames for one TCLK period during the expected input of FT.
CHSYNCB	O	Channel Sync Clock. Strobes low once every frame for six TCLK periods during channel 1.
SYNCEN	I	Frame Synchronization Enable. When low, disables the automatic resync search initiated by a frame alarm condition.
MRB	I	Master Reset. Active low resets the circuit.
GND	-	Ground
CALRM	O	Carrier Alarm Signal, active high. Goes high if 31 consecutive zeros are received in the TDATA input. Resets low when TDATA becomes 1.
SBALRM	O	FS Alarm Signal, active high. Signals an FS alarm when the previous FS bits have been 0 followed by 1111. SBALRM is reset low when the FS bit pattern 10001 occurs. The SBALRM transition occurs during channel 1 of FS frame.
TESTO	O	Test Mode Output.
SBIT	O	Signalling Bit. Outputs the FS received 2 frames before the current FS.
CDINH	I	Channel Data Inhibit. When high forces CDB1 through CDB7 pins high. CDB8 is not affected.
CDB1-8	O	Bit 1, the sign bit, will be serially received first, followed by bits 2 (MBS) through bit 8 (LBS). The rising edge of CHCLK indicates output channel data has been clocked out and occurs as the final bit (bit 8) is received.
TDATA	I	Serial Data Input.
SBCLK	O	4 KHz signal that is low during even frames and high during odd frames.
SIGFRB	O	Signal Frame Clock. Strobes low during frames 6 and 12.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (Operation above absolute maximum ratings may permanently damage the device.)

PARAMETER	RATING	UNIT
Positive 5.0V Supply Voltage, VDD	7	V
Storage Temperature	- 65 to 150	°C
Lead Temperature (Soldering 10 sec.)	260	°C
Input Pins	-0.3V to VDD + 0.3V	V
Output Pins	-0.3V to VDD + 0.3V or 15 mA	V
Inputs and outputs are protected against static discharge with industry standard protection devices.		

RECOMMENDED OPERATING CONDITIONS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
VDD Supply Current IDD	Clock active, Outputs open, Inputs to rail			5	mA
CLOCK Frequency		10		1600	KHz
VDD	VDD	4.5		5.5	V
Temperature		0		70	°C

DC REQUIREMENTS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Input Hi Voltage VIH		2.0			V
Input Lo Voltage VIL				0.8	V
Output Hi Voltage VOH	I source = -1.0 mA	2.4			V
Output Lo Voltage VOL	I sink = 2.0 mA			0.4	V

TIMING CHARACTERISTICS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
TDATA Setup Time t1s	from CLOCK edge falling	100			ns
TDATA Hold Time t1h	from CLOCK edge falling	100			ns
Setup Time t2h	(1) from WIHBT edge rising	0			ns
CDB1-8 Hold Time t3h	from CHCLK edge rising	0	200		ns
Output Delay td1	(2) from CLOCK edge rising		300		ns
Output Delay	(3) from CLOCK edge rising		400		ns

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CMOS Digital IC

T1 Transmitter

TIMING CHARACTERISTICS (Continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
CALRM Delay	from CLOCK edge			300	ns
FRALRM Delay	from CLOCK edge			600	ns
Output Rise, Fall Time t_r, t_f	90% to 10%			100	ns
SYNCEN low (inhibit sync)	before FRALARM edge rising	200			ns
SYNCEN high (initiate sync)	before MRB edge rising	200			ns
CBD1-7 valid/high	after CDINH edge falling/rising			150	ns
FRALRM high	after MRB falling edge			250	ns
(1) SIGFRM, FRALRM (2) CHCLK, $\overline{\text{CHSYNCB}}$, WIHBT, $\overline{\text{MAXCNTB}}$, SBCLK (3) SIGFRM, SBALRM, B2ALRM, SBIT, CDB1-8					

FRAME ALARM

FRALRM goes high indicating an out-of-frame condition when:

- (1) The frame synchronization algorithm is in progress.
- (2) $\overline{\text{MRB}}$ is low.
- (3) The current FT is in error and a previous FT error occurred in the past four frames.
- (4) After falling edge of CALRM.

FRALRM returns low when:

- (1) Frame synchronization is complete.
- (2) CALRM is high.

OUTPUT CLOCK SIGNALS DURING FRAME SYNCHRONIZATION FUNCTION

During frame sync, output signals CHCLK, $\overline{\text{CHSYNCB}}$ and WIHBT will continue normally for two frame periods, then they will go high. For most data patterns frame sync requires less than 5 milliseconds to acquire frame lock.

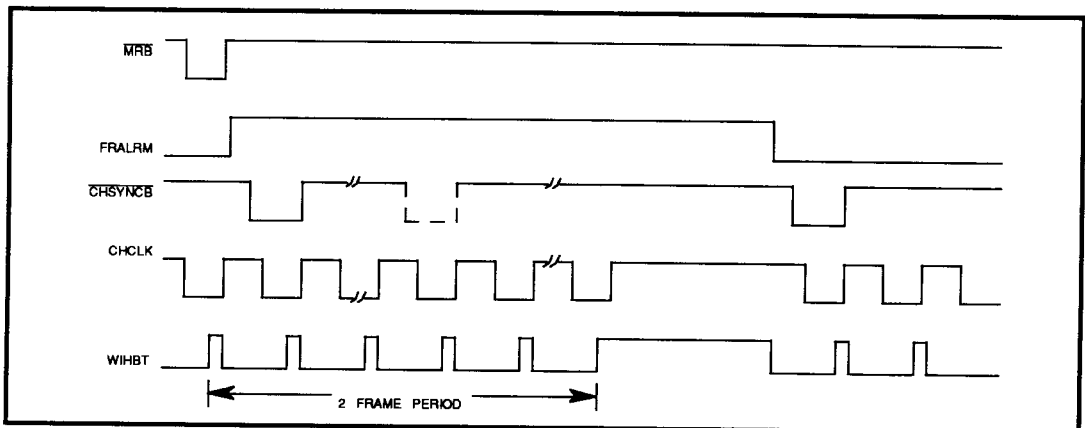


FIGURE 1: Signal Relationship during Frame Alarm and Search for Resynchronization

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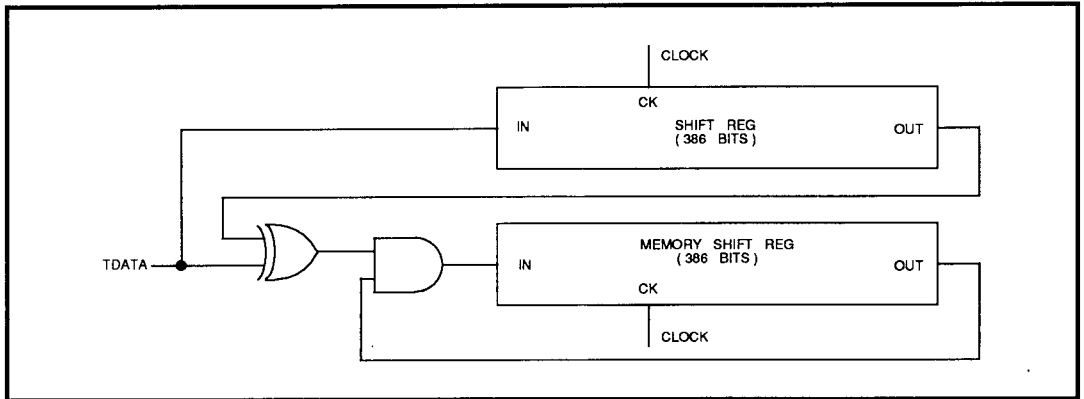


FIGURE 2: Frame Sync Algorithm

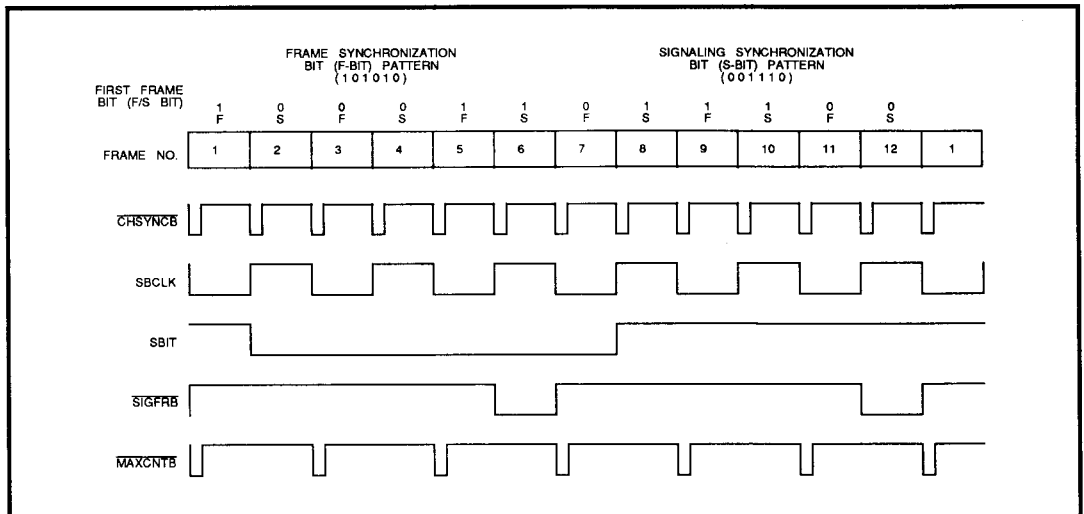


FIGURE 3: Multiframe Signal Relationships

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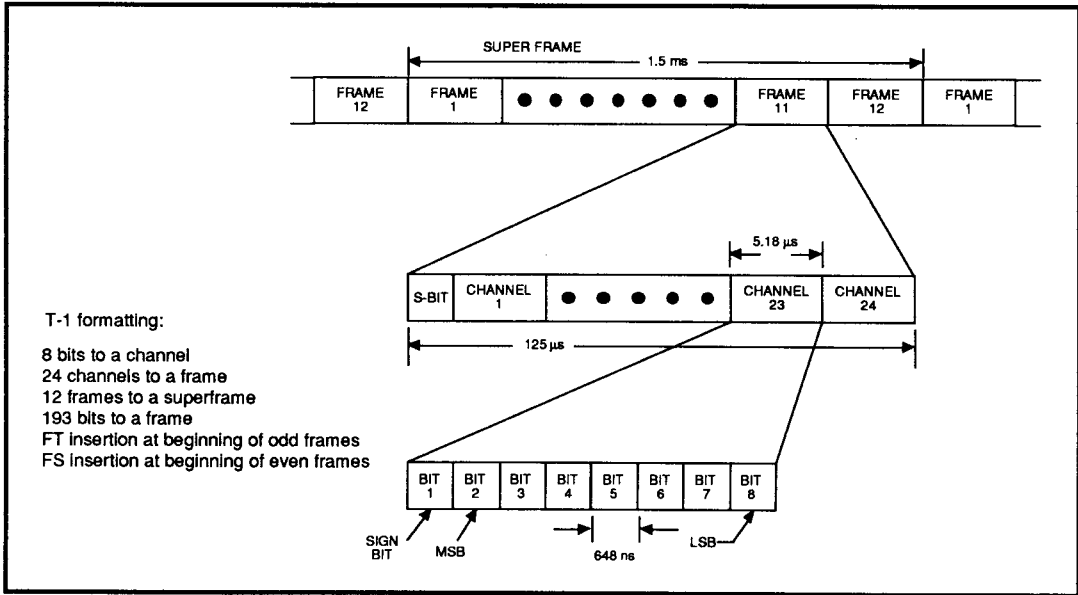


FIGURE 4: T1 Framing Format

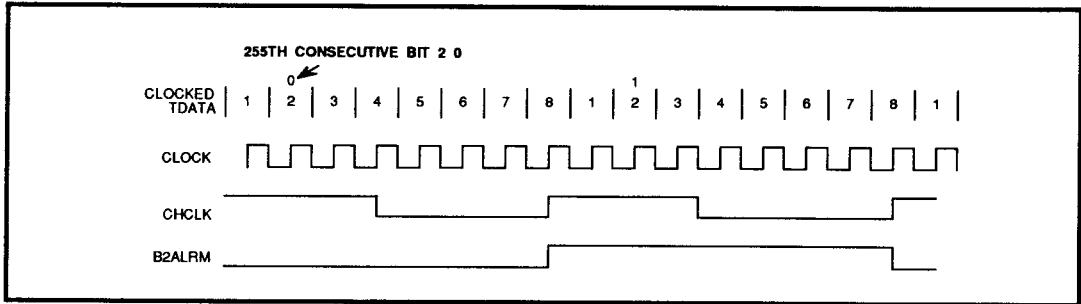


FIGURE 5: B2ALRM

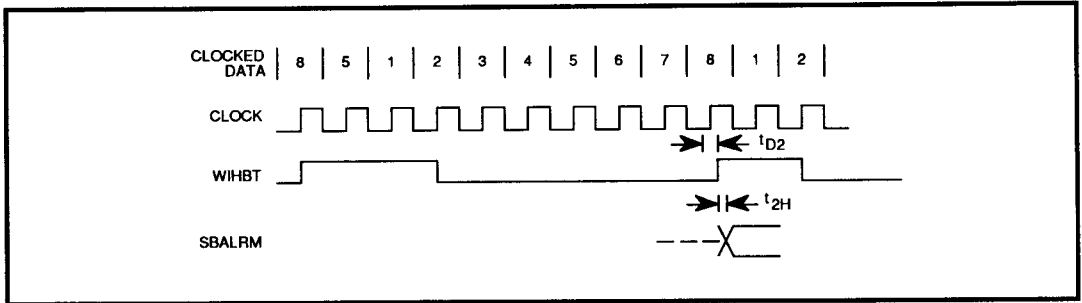


FIGURE 6: SBALRM

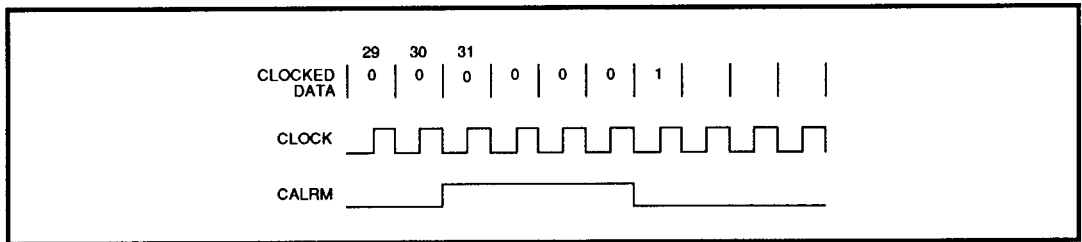


FIGURE 7: CALRM

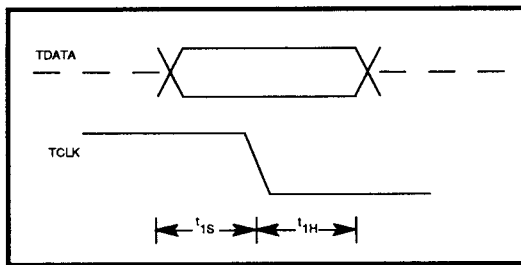


FIGURE 8: Input Timing

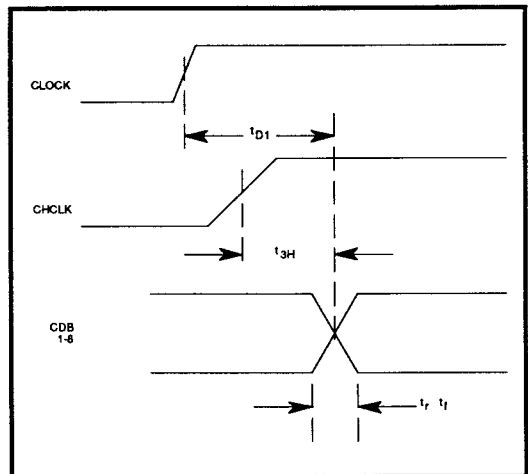


FIGURE 9: Output Timing

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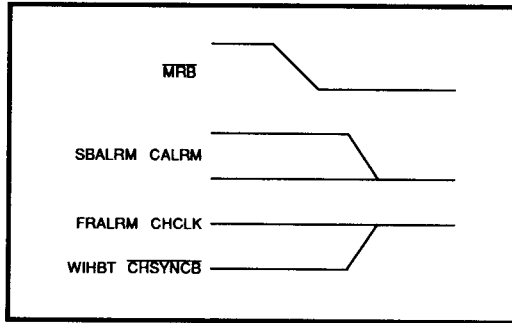


FIGURE 10: MRB Timing

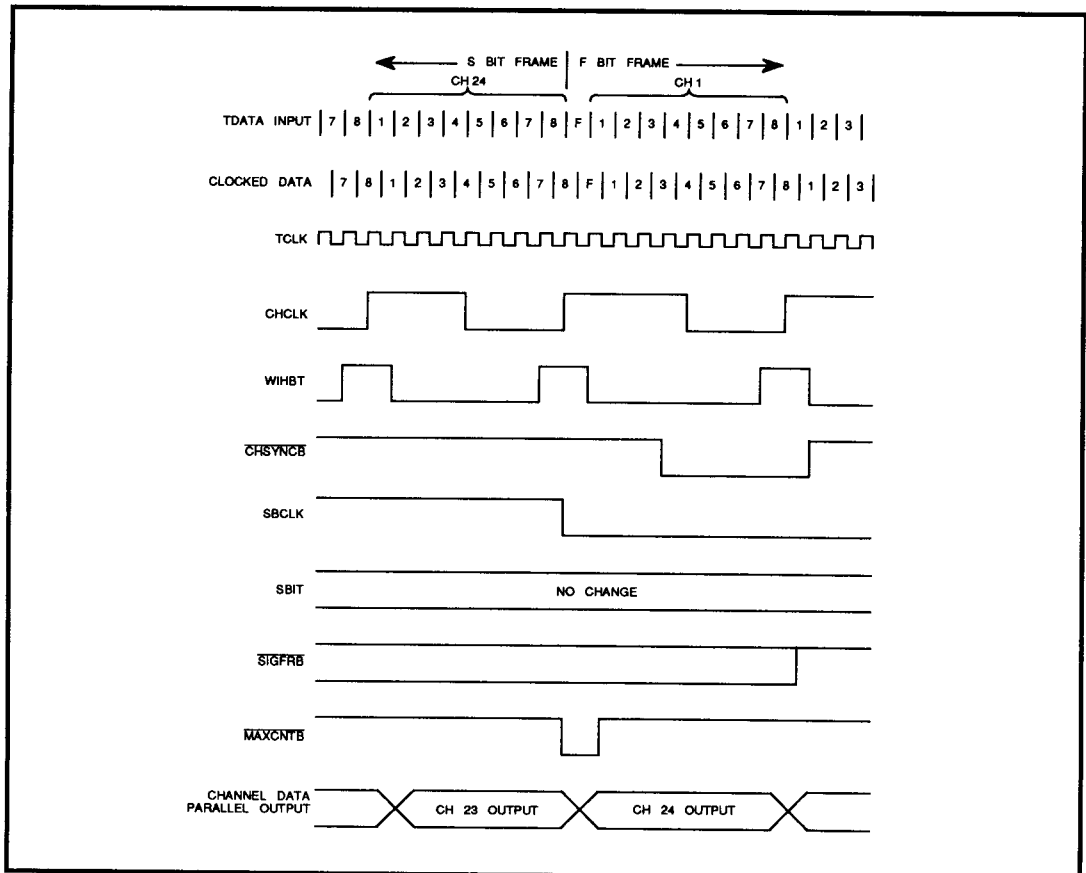


FIGURE 11: Signal Relationship at Beginning of FS Frame (S-BIT)

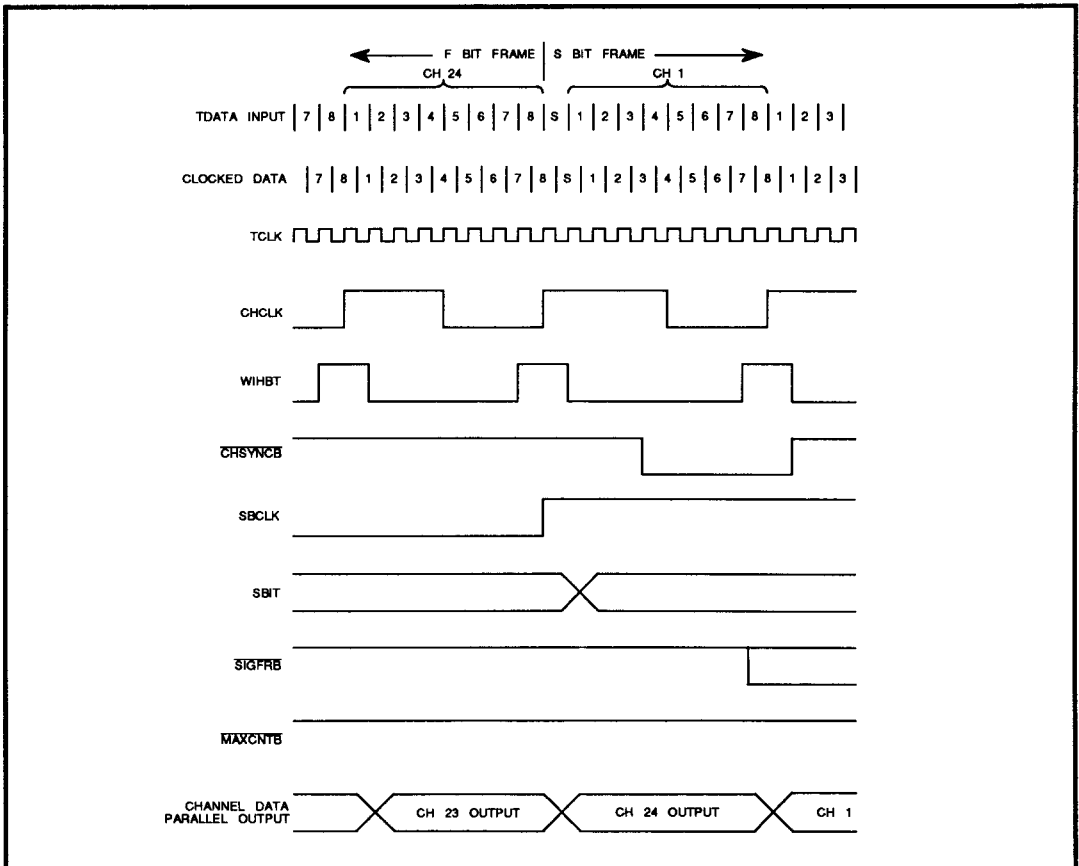
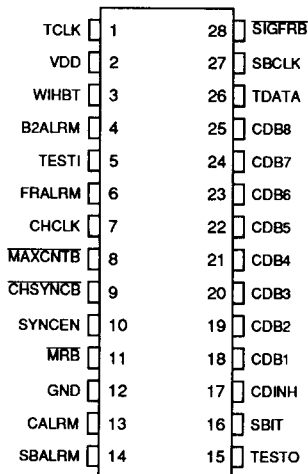


FIGURE 12: Signal Relationship at Beginning of FT Frame (F-BIT)

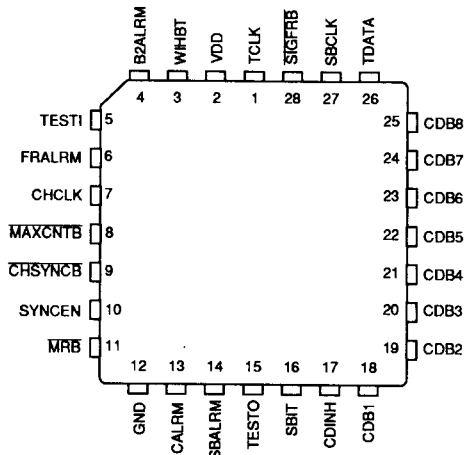
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PACKAGE PIN DESIGNATIONS

(TOP VIEW)



28-Pin DIP



28-Pin PLCC

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 78P8060		
28-Pin DIP	SSI 78P8060-CP	78P8060-CP
28-Pin PLCC	SSI 78P8060-CH	78P8060-CH

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