National Semiconductor

NM95MS14
Plug 'n Play Front-End Devices for ISA-Bus Systems

General Description

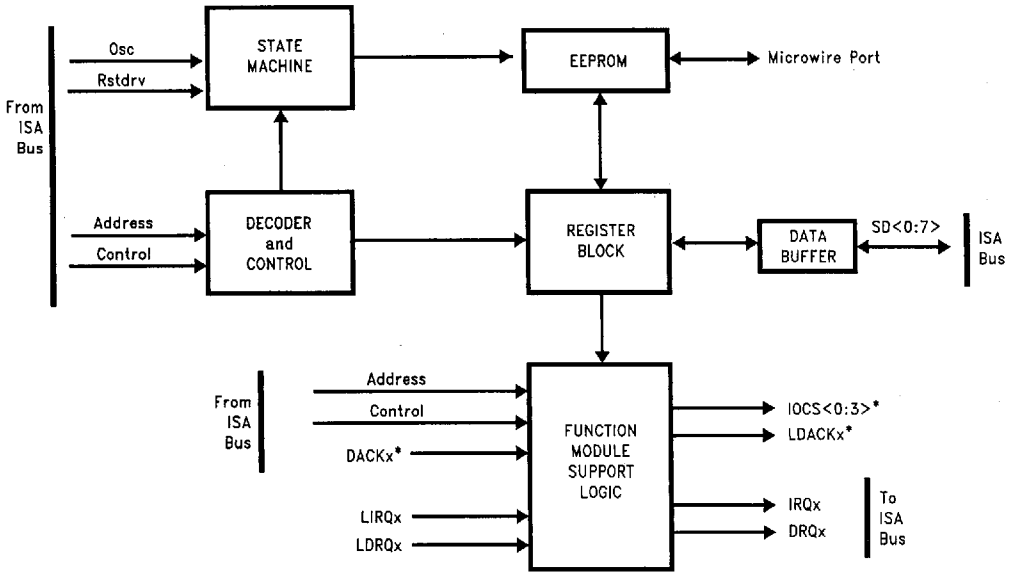
The NM95MS14 is the smaller of a family of devices designed to provide complete Plug 'n Play Capability for ISA bus systems. The NM95MS14 includes the necessary state machine logic to manage the Plug 'n Play protocol in addition to switches for steering Interrupt and DMA requests. It also features a built-in 2k bits of serial EEPROM for storing the resource data specified in the Plug 'n Play Standard. In addition, 4k bits of EEPROM is available for use by other on-board logic. This device provides a "truly complete" single-chip solution for implementing Plug 'n Play on ISA-Bus Adapter cards. The NM95MS14 supports one logical device with a flexible choice of DMA/IRQ selection and I/O Chip-select generation.

NM95MS14 is implemented using National's Advanced CMOS process and operates single power supply. The NM95MS14 is available in a 48-pin TQFP package.

Features

- Complete implementation of Plug 'n Play standard
  - — Direct interface to ISA bus
- Two modes of operation
  - — DMA mode
  - — Extended Interrupt mode
- 6 or 8 ISA bus interrupt lines and 2 DRQ/DACK lines supported
- On-chip EEPROM for resource request table
- Additional 4 Kbits of on-chip EEPROM available for external access
- 24 mA drivers for data outputs
- 48-pin TQFP, 52-pin PLCC packages

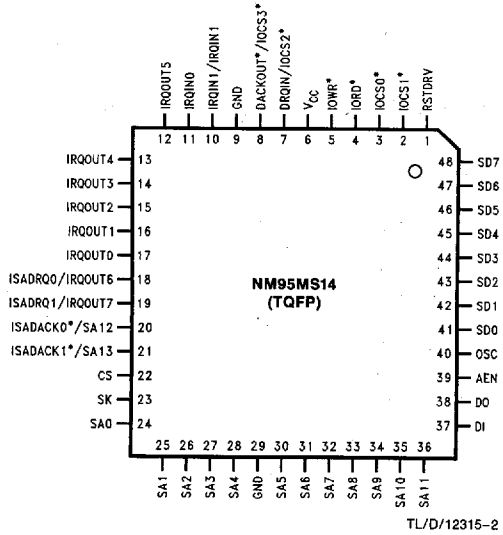
Block Diagram



TL/D/12315–1

Connection Diagram

Commercial Temperature Range (0°C to +70°C)



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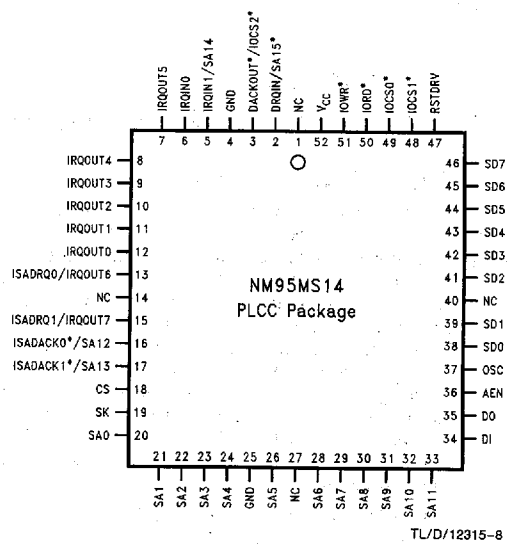
Order Number NM95MS14VBH



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Order Number NM95MS14V

Signals	Type	Description
SA<11:0>	I	Address inputs from the ISA bus.
IORD*	I	I/O read strobe from the ISA bus.
IOWR*	I	I/O write strobe from the ISA bus.
AEN	I	Address Enable from ISA Bus—used in conjunction with DMA.
SD<7:0>	I/O	Data bus—lower byte—from/to the ISA bus.
OSC (Note 1)	I	"OSC" Clock from the ISA bus—used for internal state machines.
RSTDRV	I	Reset input from the ISA bus.
CS	I	Chip select for Microwire port. There should be a pulldown resistor of 4.7k on CS pin if unused externally.
SK, DI	I	Clock and Data input lines for Microwire bus connection to access a portion (4k) on chip EEPROM.
DO	O	Data output line for the Microwire interface detailed above. There should be a pull-up resistor of 4.7k on this line, if used externally.
IRQOUT<5:0>	O	Connection to ISA bus interrupt request pins. On-chip interrupt request(s) may be connected to any 6 of the ISA IRQ lines.
IRQIN<1:0>	I	Interrupt request from on-board logic
DRQin/IOCS2*	I	DMA request from on-board logic, or Programmable chipselect (2) depending on mode selected.
DACKOUT*/IOCS3*	O	DMA Acknowledge for on-board logic or Programmable chipselect (3) depending on mode selected.
ISADRQ<1:0>/ IRQOUT<7:6>	O	Connection for two ISA bus DMA Request lines, or additional interrupt request lines depending on the mode selected.
ISADACK<1:0>*/ SA<13:12>	I	DMA Acknowledge from the ISA bus or additional address lines depending on the mode selected.
IOCS<1:0>*	O	Programmable chip selects to address on-board peripheral.

Signal name with a "" means its an active low signal.

Note 1: "OSC" clock from ISA Bus is fixed at a standard frequency of 14.318 MHz. NM95MS14 is designed and tested for 14.318 MHz. However the NM95MS14 can handle frequencies up to 24 MHz though it is not 100% tested.

Pinout Details for the NM95MS14

Mode 00 = DMA Mode; Mode 01 = Extended Interrupt Mode

Pin #	Pin Name		
TQFP	DMA	Ext. Intr.	PLCC
1	RSTDRV	RSTDRV	47
2	IOCS1*	IOCS1*	48
3	IOCS0*	IOCS0*	49
4	IORD*	IORD*	50
5	IOWR*	IOWR*	51
6	V_{CC}	V_{CC}	52
7	DRQIN	IOCS2*	2
8	DACKOUT*	IOCS3*	3
9	GND	GND	4
10	IRQIN1	IRQIN1	5
11	IRQIN0	IRQIN0	6
12	IRQOUT5	IRQOUT5	7
13	IRQOUT4	IRQOUT4	8
14	IRQOUT3	IRQOUT3	9
15	IRQOUT2	IRQOUT2	10
16	IRQOUT1	IRQOUT1	11

Pin #	Pin Name		
TQFP	DMA	Ext. Intr.	PLCC
17	IRQOUT0	IRQOUT0	12
18	ISADRQ0	IRQOUT6	13
19	ISADRQ1	IRQOUT7	15
20	ISADACK0*	SA12	16
21	ISADACK1*	SA13	17
22	CS	CS	18
23	SK	SK	19
24	SA0	SA0	20
25	SA1	SA1	21
26	SA2	SA2	22
27	SA3	SA3	23
28	SA4	SA4	24
29	GND	GND	25
30	SA5	SA5	26
31	SA6	SA6	28
32	SA7	SA7	29

Pin #	Pin Name		
TQFP	DMA	Ext. Intr.	PLCC
33	SA8	SA8	30
34	SA9	SA9	31
35	SA10	SA10	32
36	SA11	SA11	33
37	DI	DI	34
38	DO	DO	35
39	AEN	AEN	36
40	OSC	OSC	37
41	SD0	SD0	38
42	SD1	SD1	39
43	SD2	SD2	41
44	SD3	SD3	42
45	SD4	SD4	43
46	SD5	SD5	44
47	SD6	SD6	45
48	SD7	SD7	46

Note: Mode selection (00 or 01) is done by setting MS bits in the EEPROM configuration register. Detailed information about this is described in User's Guide.
PLCC = No connect on pin 1, 14, 27, and 40. Availability is limited. Ask NSC.

Absolute Maximum Ratings

Ambient Storage Temperature	−65°C to +150°C
All Input or Output Voltages with Respect to Ground	V_{CC} + 1V to −0.3V
Lead Temperature (Soldering, 10 seconds)	+300°C
ESD Rating	2000V Min

Operating Conditions

Ambient Operating Temperature	
NM95MS14	0°C to +70°C
Positive Power Supply (V_{CC})	4.5V to 5.5V

DC Electrical Characteristics

Symbol	Parameter	Test Conditions	Limits			Units
			Min	Typ (Note 1)	Max	
I_{CCA}	Active Power Supply Current	f_{SCL} = 100 kHz		TBD	10.0	mA
I_{LI}	Input Leakage Current	V_{IN} = GND or V_{CC}		0.2	1.0	μA
I_{LO}	Output Leakage Current	V_{OUT} = GND to V_{CC}			1.0	μA
V_{IL}	Input Low Voltage			−0.1	0.8	V
V_{IH}	Input High Voltage		2.0		V_{CC} + 1.0	V
V_{OL}	Output Low Voltage	I_{OL} = 24 mA (Note 3) I_{OL} = 2.1 mA (Note 4)			0.4	V
V_{OH}	Output High Voltage	I_{OH} = −3 mA (Note 3) I_{OH} = −400 μA (Note 4)	2.4 2.4			V V

Capacitance T_A = +25°C, f = 1.0 MHz, V_{CC} = 5V

Symbol	Test	Conditions	Max	Units
$C_{I/O}$ (Note 2)	Input/Output Capacitance	$V_{I/O}$ = 0V	8	pF
C_{IN} (Note 2)	Input Capacitance	V_{IN} = 0V	6	pF
C_{OUT} (Note 2)	Output Capacitance	V_{OUT} = 0V	6	pF

Note 1: Typical values are for T_A = 25°C and nominal supply voltage (5V).

Note 2: This parameter is periodically sampled and not 100% tested.

Note 3: These values are for ISA signals like SD[0:7], IRQx, DRQx.

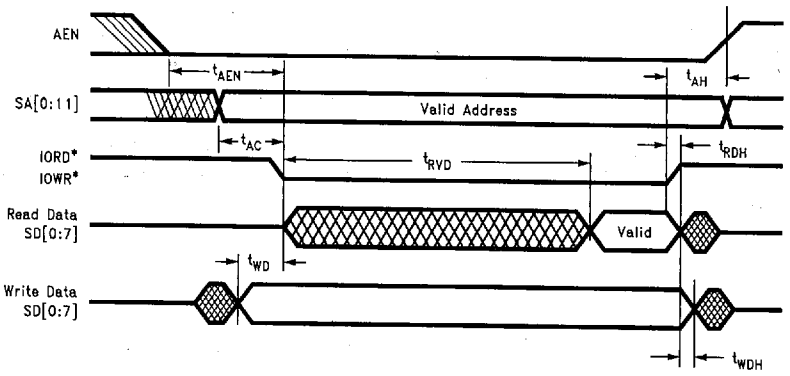
Note 4: These values are for card signal like IOCS[0:3]*, DO(EEPROM).

AC Electrical Characteristics

Symbol	Parameter	Min	Max	Unit
t_{AEN}	AEN Valid to Command Active	100		ns
t_{AC}	Address Valid to Command Active	88		ns
t_{RVD}	Active Read to Valid Data		200	ns
t_{AH}	Address, AEN Hold from Inactive Command	30		ns
t_{RDH}	Read Data Hold from Inactive Read		5	ns
t_{WD}	Write Data Valid before Write Active	22		ns
t_{WDH}	Write Data Hold after Write Inactive	25		ns
t_{CSA}	Chip Selects Valid from Address Valid	5	25	ns
t_{CSC}	Chip Selects Valid from Command Active	5	25	ns
t_{IDD}	Propagation Delay for IRQ/DRQ/DACK	5	25	ns

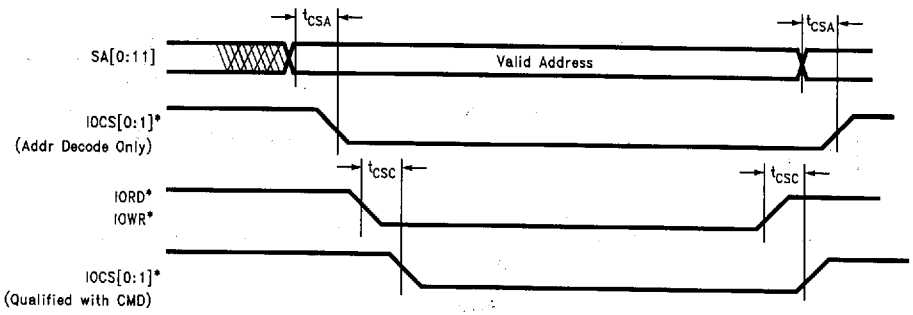
Timing Diagrams

(1) Timings for ISA Read/Write Cycle



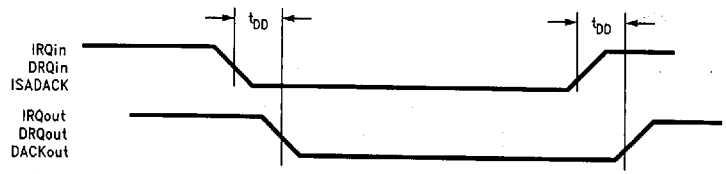
TL/D/12315–3

(2) Decode Delay for Chipselect Generation



TL/D/12315–4

(3) Propagation Delay for IRQ/DRQ/DACK



TL/D/12315–5

INTRODUCTION

The NM95MS14 is a single-chip solution for the ISA Plug 'n Play (PnP) specification. It implements the complete state machine and the necessary logic for supporting configurable Interrrupts and DMA channels on the ISA bus for one logical device. Apart from providing "Plug 'n Play" capability, it has built-in EEPROM that eliminates external EEPROM. This device is available in a space saving 48-pin Thin Quad Flat Pack (TQFP) package.

Functional Description

NM95MS14 has two modes of operation, viz, *"DMA mode"* and *"Extended Interrupt mode"*. These modes are programmed using the mode select (MS) bits in one of the configuration registers (Refer to the User's guide for detailed information). Each of these modes are discussed below.

DMA Mode

In the DMA mode, support is provided for

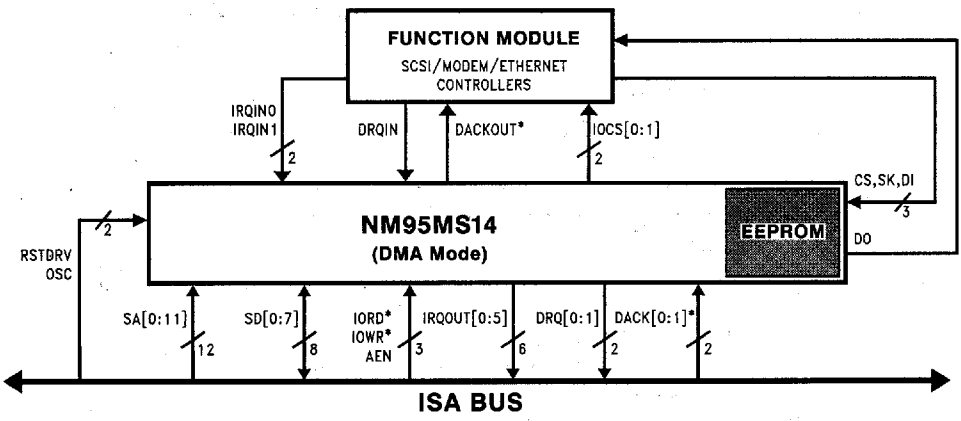
A) One on-board DMA request that is switchable to any two DMA channels on the ISA bus.

B) Two on-board interrupt request lines switchable to any six IRQ lines on the ISA bus.

C) Two programmable I/O chip selects for on-board logic.

Figure 1 shows a Block Diagram of NM95MS14 configured for DMA Mode.

Block Diagrams (Continued)



TL/D/12315–6

FIGURE 1

Extended Interrupt Mode

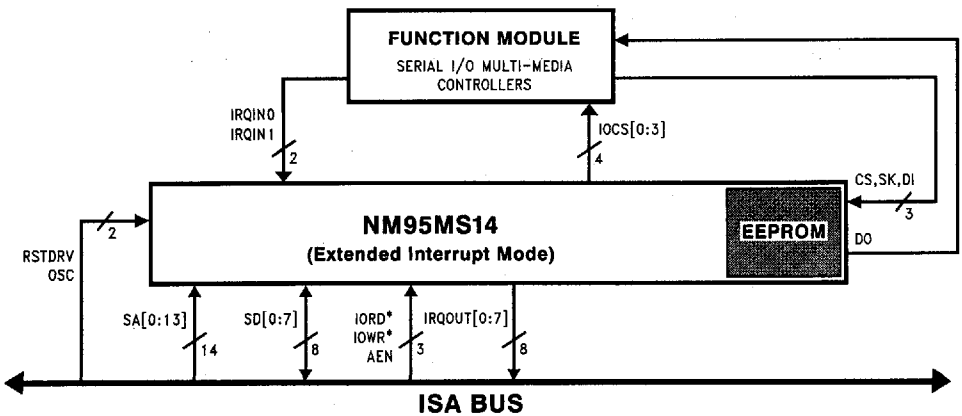
In the Ext. Int mode, support is provided for:

A) Two on-board interrupt request lines switchable to any eight IRQ lines on the ISA bus.

B) Four programmable I/O chip selects for on-board logic.

C) ISA address SA12 and SA13 are also included for extended decode.

Figure 2 shows a Block Diagram of NM95MS14 configured for Extended Interrupt Mode.



TL/D/12315–7

FIGURE 2

Chipselect Generation

Individual I/O chipselect can be generated in the following two ways:

A) Address Decode only
B) Address Decode qualified by Command (IORD*, IOWR*).

"Address Decode only" provision enables to generate the IOCS16* signal (directly from the chipselect) early enough to meet the ISA specifications during 16-bit transfers.

On-Chip EEPROM

NM95MS14 has 6k of EEPROM on chip. All the PnP resource data structure for the logical device is stored in this EEPROM. Of the 6k bits, 4k bits are available for the logical device's external usage. The logical device can access the EEPROM through a microwire port, which is essentially a 4-wire serial bus. The pins CS, SK, DI & DO follow the exact timing as the standard microwire bus and are compatible to the NM93Cxx family of EEPROMs.

EEPROM Programming

The entire 6k bits of EEPROM can be programmed through the ISA bus. The EEPROM can be programmed by putting the device (NM95MS14) in the Config. state (as defined in the PnP standard). Under this state 4 registers at address 0xF0–0xF3 are accessible to program the EEPROM. The data to be programmed is loaded in register at address 0xF3 and 0xF2 (LSB and MSB respectively). The address to be programmed is loaded in register at address 0xF1. The Ninth bit of address for 6k bits of memory is provided through the register at address 0xF0. Both read write are possible. The actual operation does not begin until Go Ahead (GA) bit is set. Programming a word takes approximately 10 ms. The status of the operation can be polled by the Status bit. This bit is set when the operation is in progress and will be reset when complete. The register at address 0xF0 is the STATUS and COMMAND register. This is the handshake register in programming the EEPROM and is explained below in a tabular format.

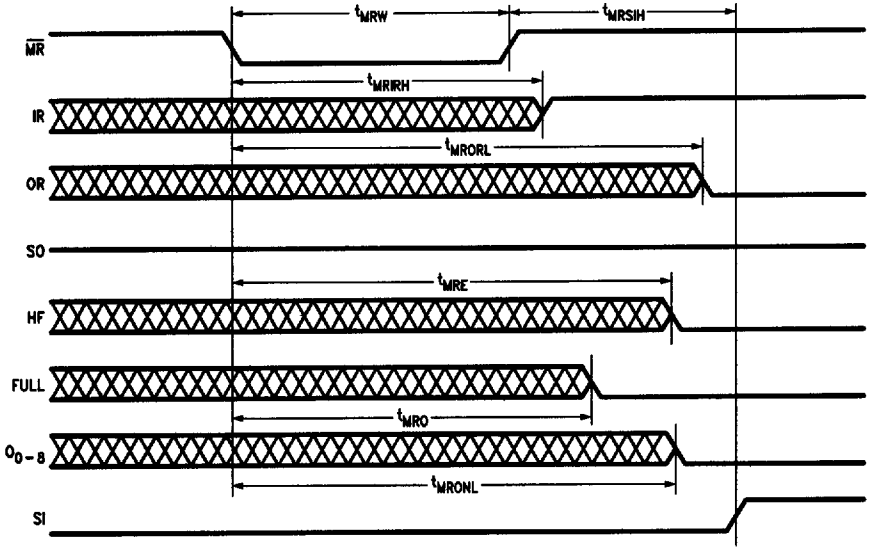
COMMAND register	0xF0	Bit[1:0]	- OP Code bits 10 - Read operation 01 - Write operation
		Bit[2]	GA(Go ahead bits) If set to 1 the programming will continue.
		Bit[6:4]	- Reserved, should be 0.
		Bit[7]	- It provides A8 of the address. A[0:7] is provided by 0xF1 reg.
Address Register	0xF1	AddressRegister [A0–A7]	
Data Register	0xF2	Data Byte [MSB]	
Data Register	0xF3	Data Byte [LSB]	
STATUS Register	0x05	Bit[0]	- Status/Busy bit "0" is busy, "1" is done.

Functional Description (Continued)

Mode 2: Master Reset

Sequence of Operation

1. Input and Output Ready, HF and FULL can be in any state before the reset sequence with Master Reset ($\overline{MR}$) HIGH.
2. Master Reset goes LOW and clears the FIFO, setting up all essential internal states. Master Reset must be LOW pulse width t_{MRW} before rising again.
3. Master Reset rises.
4. IR rises (if not HIGH already) to indicate ready to write state recovery time t_{MRIRH} after the falling edge of $\overline{MR}$. Both HF and FULL will go LOW indicating an empty FIFO, occurring recovery times t_{MRE} and t_{MRO} respectively after the falling edge of $\overline{MR}$. OR falls recovery time t_{MRORL} after $\overline{MR}$ falls. Data at outputs goes LOW recovery time t_{MRONL} after $\overline{MR}$ goes LOW.
5. Shift-In can be taken HIGH after a minimum recovery time t_{MRSIH} after $\overline{MR}$ goes HIGH.



TL/F/10144–6

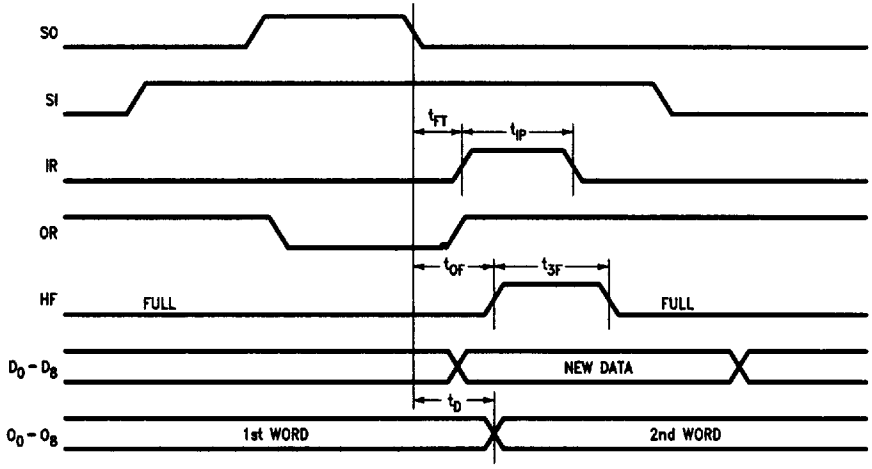
FIGURE 2. Mode of Operation Mode 2

Functional Description (Continued)

Mode 3: With FIFO Full, Shift-In is Held HIGH In Anticipation of an Empty Location

Sequence of Operation

1. The FIFO is initially full and Shift-In goes HIGH. OR is initially HIGH. Shift-Out is LOW. IR is LOW.
2. Shift-Out is pulsed HIGH, Shift-Out pulse propagates and the first data word is latched on the rising edge of SO. OR falls on this edge. On the falling edge of SO, the second data word appears after propagation delay t_D. New data is written into the FIFO after SO goes LOW.
3. Input Ready goes HIGH one fall-through time, t_{FT}, after the falling edge of SO. Also, HF goes HIGH one t_{OF} after SO falls, indicating that the FIFO is no longer full.
4. IR returns LOW pulse width t_{IP} after rising and shifting new data in. Also, HF returns LOW pulse width t_{3F} after rising, indicating the FIFO is once more full.
5. Shift-In is brought LOW to complete the shift-in process and maintain normal operation



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Note: $\overline{MR}$ and FULL are HIGH; $\overline{OE}$ is LOW.

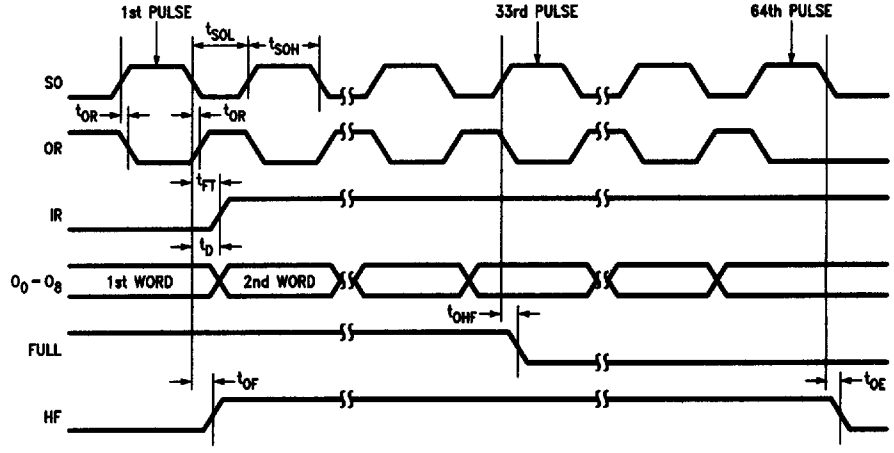
FIGURE 3. Modes of Operation Mode 3

Functional Description (Continued)

Mode 4: Shift-Out Sequence, FIFO Full to Empty

Sequence of Operation

1. FIFO is initially full and OR is HIGH, indicating valid data is at the output. IR is LOW.
2. SO goes HIGH, resulting in OR going LOW one propagation delay, t_{OR}, after SO rises. OR LOW indicates output stage is busy.
3. SO goes LOW, new data reaches output one propagation delay, t_D, after SO falls; OR goes HIGH one propagation delay, t_{OR}, after SO falls and HF rises one propagation delay, t_{OF}, after SO falls. IR rises one fall-through time, t_{FT}, after SO falls.
4. Repeat process through the 64th SO pulse. FULL flag goes LOW one propagation delay, t_{OHF}, after the rising edge of 33rd SO, indicating that the FIFO is less than half full. On the falling edge of the 64th SO, HF goes LOW one propagation delay, t_{OE}, after SO, indicating the FIFO is empty. The SO pulse may rise and fall again with an attempt to unload an empty FIFO. This results in no change in the data on the outputs as the 64th word stays latched.



TL/F/10144–8

Note: SI and $\overline{OE}$ are LOW; $\overline{MR}$ is HIGH; D_0–D_8 are immaterial.

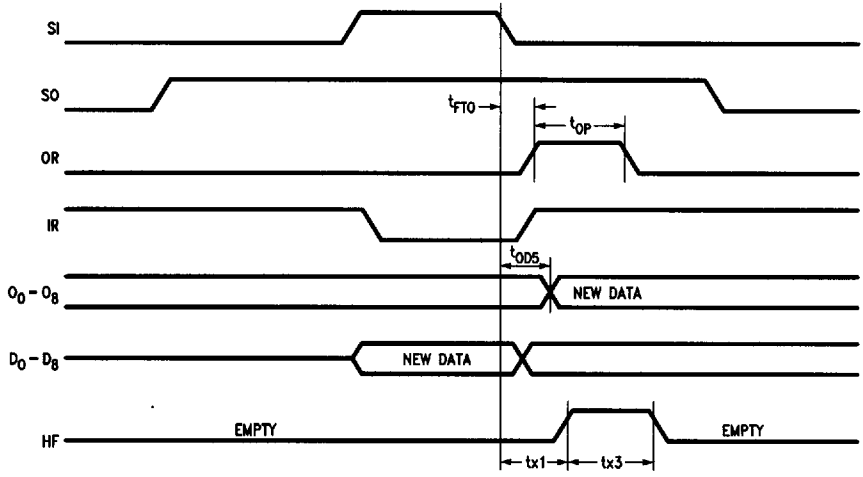
FIGURE 4. Modes of Operation Mode 4

Functional Description (Continued)

Mode 5: With FIFO Empty, Shift-Out is Held HIGH in Anticipation of Data

Sequence of Operation

1. FIFO is initially empty; Shift-Out goes HIGH.
2. Shift-In pulse loads data into the FIFO and IR falls. HF rises propagation delay t_{X1} after the falling edge of SI.
3. OR rises a fall-through time of t_{FTO} after the falling edge of Shift-In, indicating that new data is ready to be output.
4. Data arrives at output one propagation delay, t_{OD5}, after the falling edge of Shift-In.
5. OR goes LOW pulse width t_{OP} after rising and HF goes LOW pulse width t_{X3} after rising, indicating that the FIFO is empty once more.
6. Shift-Out goes LOW, necessary to complete the Shift-Out process.



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Note: FULL is LOW; $\overline{MR}$ is HIGH; $\overline{OE}$ is LOW; $t_{DOF} = t_{FTO} - t_{OD5}$. Data output transition—valid data arrives at output stage t_{DOF} after OR is HIGH.

FIGURE 5. Modes of Operation Mode 5