GM16C550

ASYNCHRONOUS COMMUNICATIONS ELEMENT WITH FIFOs

Version 0.95

Descriptions

The GM16C550 is an asynchronous communications element (ACE) that is functionally equivalent to the GM16C450, and addition-ally incorporates a 16byte FIFOs are available on both the transmitter and receiver, and can be activated by placing the device in the FIFO mode. After a reset, the registers of the GM16C550 are identical to those of the GM16C450.

The UART performs serial-to-parallel conversion on data characters received from a peripheral device or a MODEM, and parallel-to- serial conversion on data characters received from the CPU. The CPU can read the complete status of the UART at any time during the functional operation. Status information reported includes the type and condition of the transfer operations being performed by the UART, as well as any error conditions (parity, overrun, framing, or break interrupt).

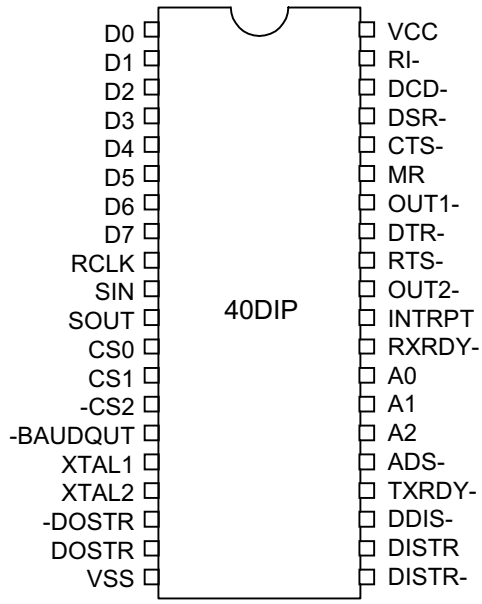
Features

- Compatible to the Industry Standard 16C550
- Modem control signals include CTS, RTS,DSR DTR, RI and DCD
- Programmable serial characteristics :
  - 5-, 6-, 7- or 8-bit characters
  - Even-, odd-, or no-parity bit generation and detection
  - 1-, 11/2- or 2-stop bit generation
  - Baud rate generation (DC to 256K baud)
- 16 byte FIFO reduces CPU interrupts.
- Independent control of transmit, receive, line status, data set interrupts, FIFOs.
- Full status reporting capabilities
- Three-state, TTL drive capabilities for bi-directional data bus and control bus.
- 40DIP/44PLCC/48LQFP

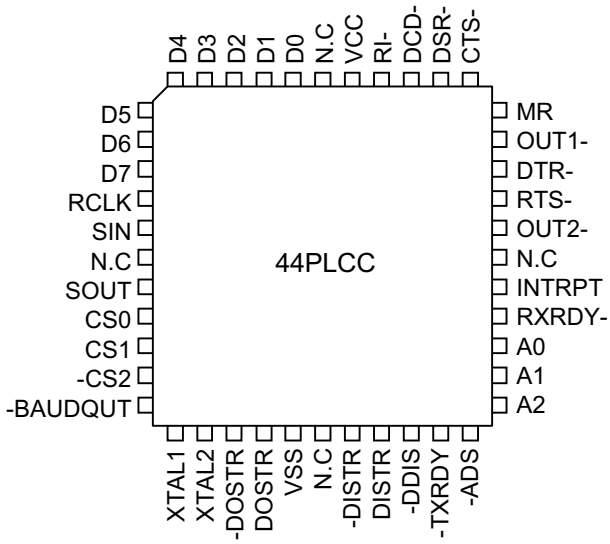
Device Code Name

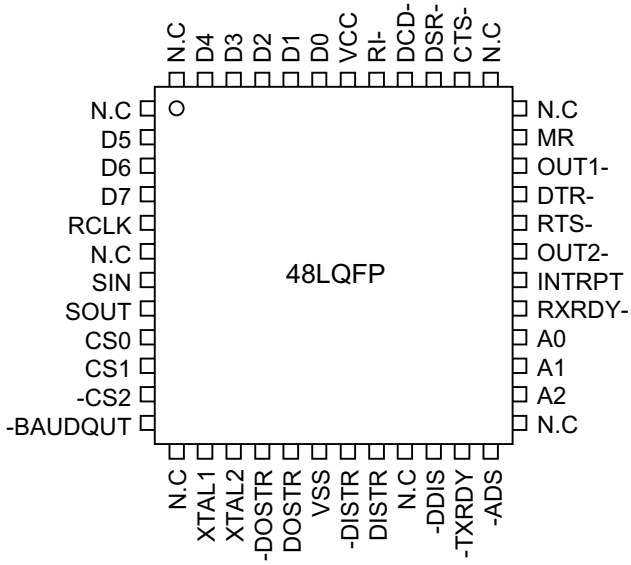
Part Number	Voltage	PKG
GM16C550	5V	40 DIP
GM16C550-44		44 PLCC
GM16C550-48		48 LQFP
GM16C550-48L	5V/3.3V	

Pin Configuration



Pin Configuration - continue





Absolute Maximum Ratings

Temperature under Bias	0℃ to 70℃
Storage Temperature	- 65℃ to 150℃
All Input or Output Voltages with respect to Vss	- 0.5V to 7.0V
Power Dissipation	500mW

Note :
Maximum ratings indicates limits beyond which permanent damage may occur. Continuous operation at these limits is not intended and should be limited to those conditions specified under DC electrical characteristics

DC Electrical Characteristics

T_A = 0℃ ~ 70℃, Vcc = 5V ± 5% & 3.3V ± 5%, Vss = 0V unless otherwise specified

Symbol	Parameter	3.3V		5V		Units	Conditions
		Min	Max	Min	Max		
V_{ILX}	Clock Input Low Voltage	−0.3	0.8	−0.5	0.8	V	
V_{IHX}	Clock Input High Voltage	1.6	Vcc	2.0	Vcc	V	
V_{IL}	Input Low Voltage	−0.3	0.8	−0.5	0.8	V	
V_{IH}	Input High Voltage	2.0	Vcc	2.2	Vcc	V	
V_{OL}	Output Low Voltage				0.4	V	I_{OL} = 1.6mA
			0.4				I_{OL} = __mA
V_{OH}	Output High Voltage			2.4		V	I_{OH} = −1.0mA
		2.0					I_{OH} = __mA
V_{CC} (AV)	Average Power Supply Current (Vcc)		4.5		10	mA	Vcc = 5.25V or 3.5V
I_{IL}	Input Leakage		±10		±10	uA	Vcc = 5.25V or 3.5V, Vss = 0V Vin = 0V, 3.5V/5.25V
I_{CL}	Clock Leakage		±10		±10	uA	
I_{OZ}	3-state Leakage		±20		±20	uA	Vout = 0V, 3.5V/5.25V
V_{ILMR}	MR Schmitt V_{IL}		0.8		0.8	V	
V_{IHMR}	MR Schmitt V_{IH}	2.0		2.2		V	

Capacitance T_A = 25℃ Vcc = Vss = 0V

Symbol	Parameter	Min	Typ	Max	Units	Conditions
CXIN	Clock Input Capacitance		15	20	pF	Fc = 1MHz
CXOUT	Clock Output Capacitance		20	30	pF	Unmeasured pins
CIN	Input Capacitance		6	10	pF	Returned to Vss
COUT	Output Capacitance		10	20	pF	

AC Characteristics $T_A = 0°C$ to $+70°C, V_{CC} = 5V/3.3V$

Symbol	Parameter	Min	Max	Units	Conditions
^tADS	Address Srobe Width	60		ns	
^tAH	Address Hold Time	0		ns	
^tAR	$\overline{RD}$, RD Delay from Address	30		ns	Note 1
^tAS	Address Setup Time	60		ns	
^tAW	$\overline{WR}$, WR Delay from Select	30		ns	Note 1
^tCH	Chip Select Hold Time	0		ns	
^tCS	Chip Select Setup time	60		ns	
^tCSR	$\overline{RD}$, RD Delay from Chip Select	30		ns	Note 1
^tCSW	$\overline{WR}$, WR Delay from Select	30		ns	Note 1
^tDH	Data Hold Time	30		ns	
^tDS	Date Setup Time	30		ns	
^tHZ	$\overline{RD}$, RD to Floating Data Delay	0	100	ns	100 pF loading, Note 3
^tMR	Master Reset Pulse Width	5		ns	
^rRA	Address Hold Time from $\overline{RD}$, RD	20		ns	Note 1
^tRC	Read Cycle Delay	125		ns	
^tRCS	Chip Select Hold Time from $\overline{RD}$, RD	20		ns	Note 1
^tRD	$\overline{RD}$, RD Strobe Width	125		ns	
^tRDD	$\overline{RD}$, RD to Driver Enable/Disable		60	ns	100 pF loading, Note 3
^tRVD	Delay from - $\overline{RD}$, RD to Data		125	ns	100 pF loading,
^tWA	Address Hold Time from $\overline{WR}$, WR	20		ns	Note 1
^tWC	Write Cycle Delay	150		ns	
^tWCA	Chip Select Hold Time from $\overline{WR}$, WR	20		ns	Note 1
^tWR	$\overline{WR}$, WR Strobe Width	100		ns	
^tXH	Duration of clock High Pulse	55		ns	External Clock (8.0 MHz Max.)
^tXL	Duration of clock Low Pulse	55		ns	Exrternal Clock (8.9 MHz Max.)
RC	Read Cycle= $^tAR+^tRD+^tRC$	280		ns	Note 4
WC	Write Cycle= $^tAW+^tWR+^tWC$	280		ns	

Baud Generator

N	Baud Divisor	1	2^{16} -1		
^tBHD	Baud Output Positive Edge Delay		175	ns	100 pF load
^tBLD	Baud Output Negative Edge Delay		175	ns	100 pF load
^tHW	Baud Output Up Time	75		ns	f_X = 8.0MHz , +2, 100 pF load
^tLW	Baud Output Down Time	100		ns	f_X = 8.0MHz , +2, 100 pF load

AC Characteristics $T_A = 0°C$ to $+70°C$, $V_{CC} = 5V/3.3V$

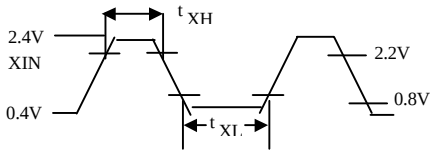
Symbol	Parameter	Min	Max	Units	Conditions
Receiver					
^tRINT	Delay from $\overline{RD}, RD$ (RD RBR/ or RD LSR) to Reset Interupt	1		µs	100 pF load
^tSCD	Delay from RCLK to Sample Time	2		µs	
^tSINT	Delay from Stop to Set Interrupt	1		RCLK Cycles	Note 2
Transmitter					
^tHR	Delay from $\overline{WR}, WR$ (WR THR) To Reset Interrupt		175	ns	100 pF load
^tIR	Delay from $\overline{RD}, RD$ (RD IIR) To Reset Interrupt (THRE)		250	ns	100 pF load
^tIRS	Delay from Initial INTR Reset To Transmit Start	8	24	Baudout Cycles	
^tSI	Delay from Initial Write to Interrupt	16	24	Baudout Cycles	Note 5
^tSTI	Delay from Stop to Interrupt (THRE)	8	8	Baudout Cycles	Note 5
^tSXV	Delay from Start to TXRDY Active		8	Baudout Cycles	100 pF load
^tWXI	Delay from Write to TXRDY inactive		195	ns	100 pF load
Modem Control					
^tMDO	Delay from $\overline{WR}, WR$ (WR MCR) to Output		200	ns	100 pF load
^tRIM	Delay to Reset Interrupt from $\overline{RD}, RD$ (RD MSR)		250	ns	100 pF load
^tSIM	Delay to Set Interrupt from MODEM Input		250	ns	100 pF load

Notes

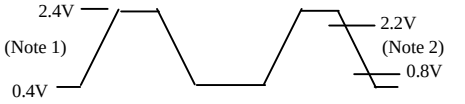
1. Applicable only when $\overline{ADS}$ is tied low.
2. In the FIFO mode (FCRO=1) the trigger level interrupts, the receiver data available indication, the active RXRDY indica-tion and the overrun error indication will be delayed 3 RCLKs. Status indicators (PE, FE, BI) will be delayed 3 RCLKs after the first byte has been received. For subsequently received bytes these indicators will be updated immediately after RDRBR goes inactive. Timeout interrupt is delayed 8 RCLKs.
3. Change and discharge time is determined by VOL, VOH and the external loading.
4. In FIFO mode RC=425 ns (minimum) between reads of the receiver FIFO and the status registers (interrupt identifica- tion register or line status register).
5. This delay will be lengthened by 1 character time, minus the last stop bit time if the transmitter interrupt delay circuit is active (See FIFO Interrupt Mode Operatione)

Timing Waveforms (All timings are referenced to valid 0 and valid)

External Clock Input (8.0 MHz Max.)

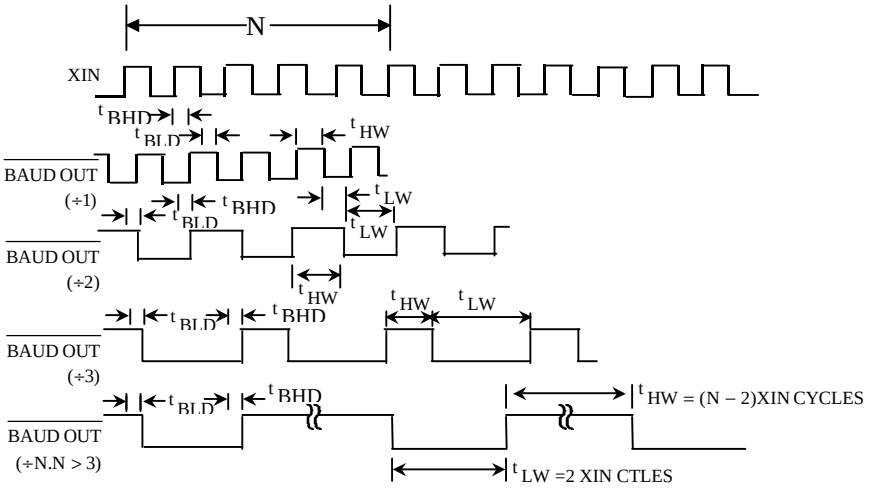


AT Test Points



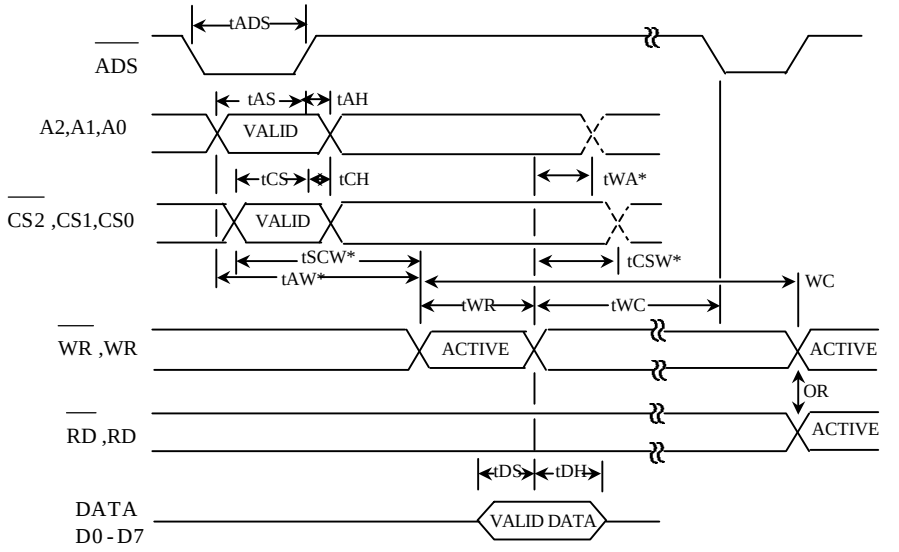
Note 1: The 2.4V and 0.4V levels are the voltages that the inputs are driven to during AC testing.
Note 2: The 2.2V and 0.8V levels are the voltages at which the timing tests are made.

$\overline{\text{BAUDOUT}}$ Timing



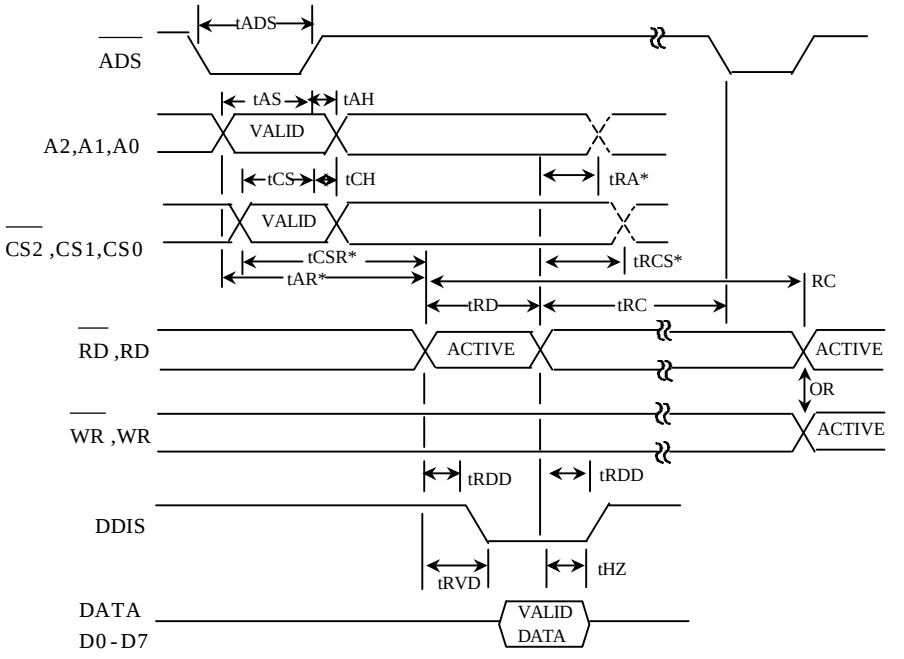
Timing Waveforms (Continued)

Write Cycle



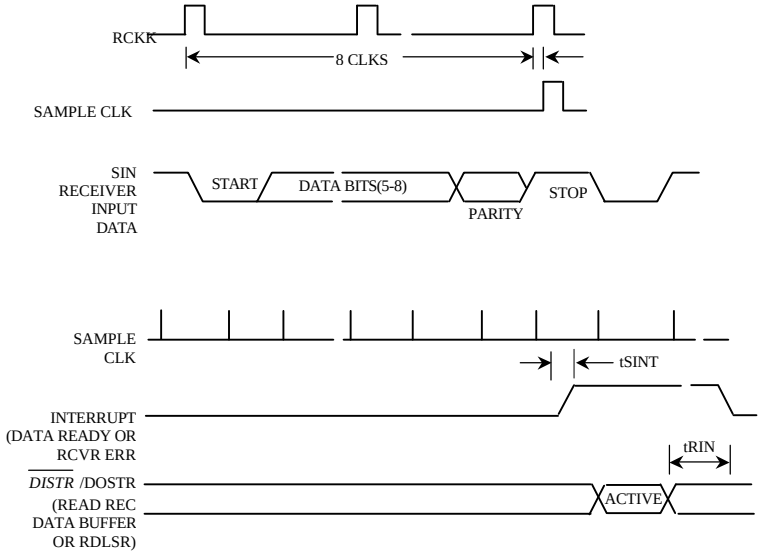
*Applicable Only When $\overline{ADS}$ is Tied Low.

Read Cycle

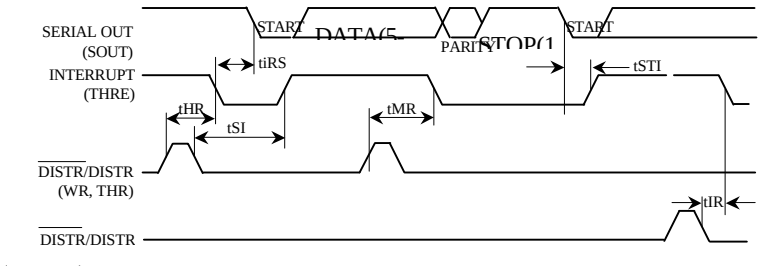


*Applicable Only When $\overline{ADS}$ is Tied Low.

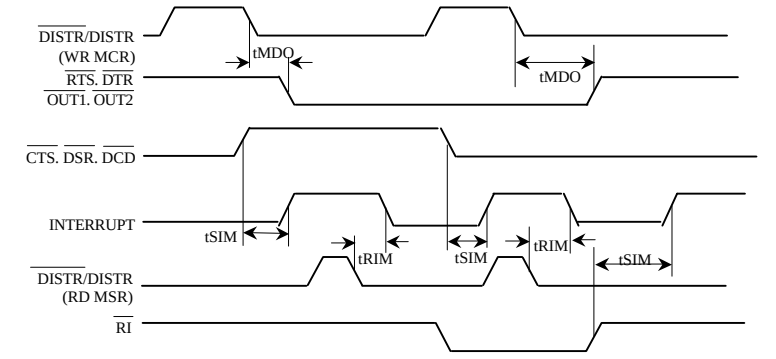
Receiver Timing



Transmitter Timing



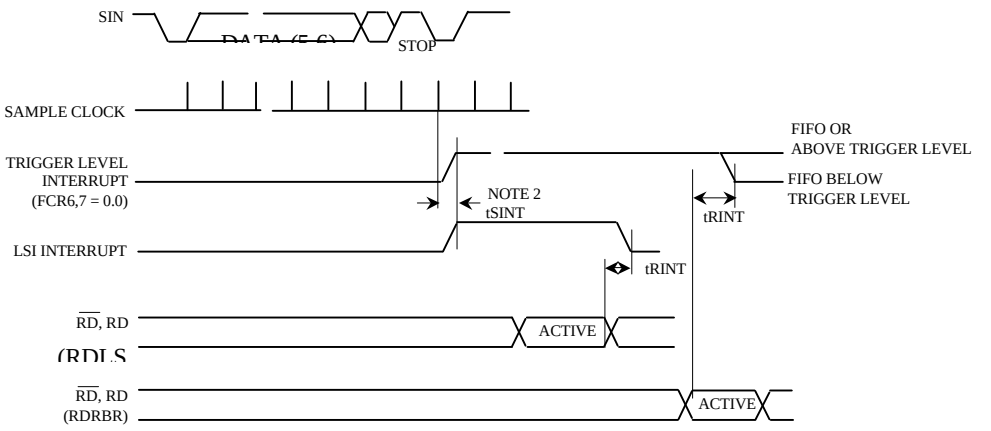
MODEM Comtrol Timing



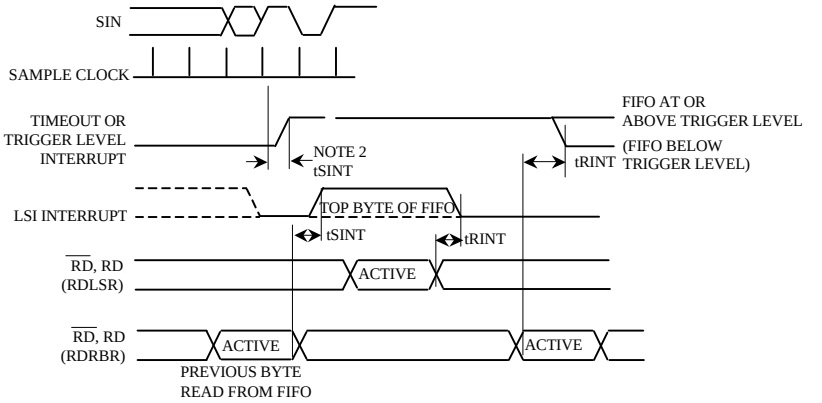
Note 1: See Write Cycle Timing
Note 2: See Read Cycle Timing

Timing Waveforms (continued)

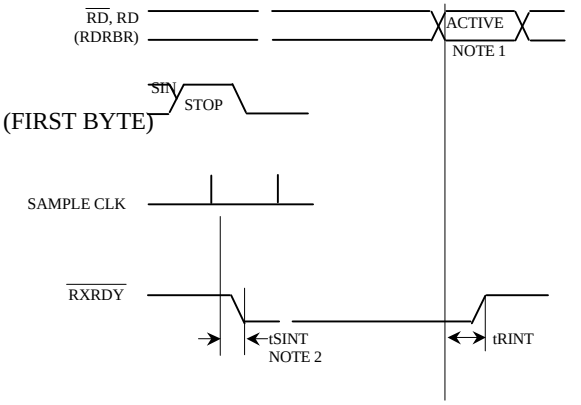
RAVR FIFO First byte (This Sets RDR)



RCVR FIFO Byte Other Than the First Byte (RDR is Already Set)



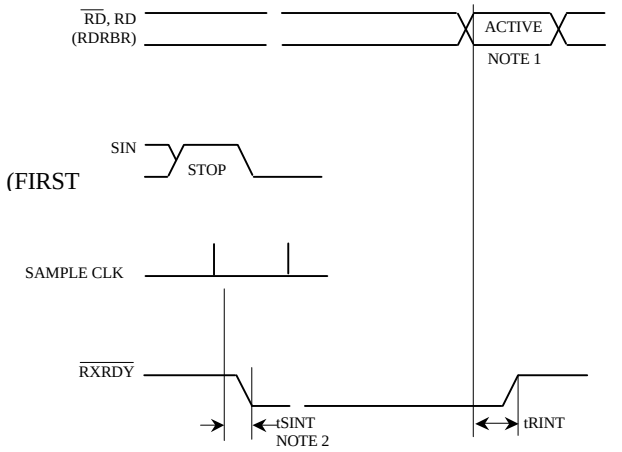
Receiver Ready (pin 29) FCRO = 0 or FCRO = 1 and FCRO = 3 (Mode 0)



Note 1: This is the reading of the last byte in the FIFO
Note 2: If FCRO =1, then Tsint = 3 RCLKs. For a timeout tSINT = 0 RCLKs.

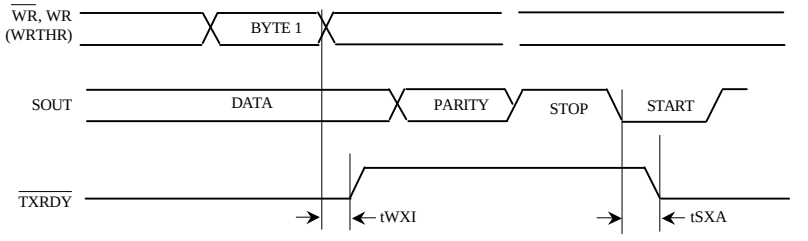
Timing waveforms (Continued)

Receiver Ready (pin 29) FCRO = 0 or FCRO = 1 and FCRO = 1 (Mode 1)

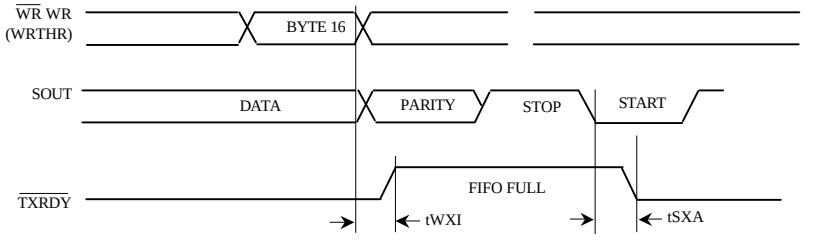


Note 1 : This si the reading of the last byte in the FIFO
Note 2 : If FCRO = 1, Tsint = 3 RCLKs.

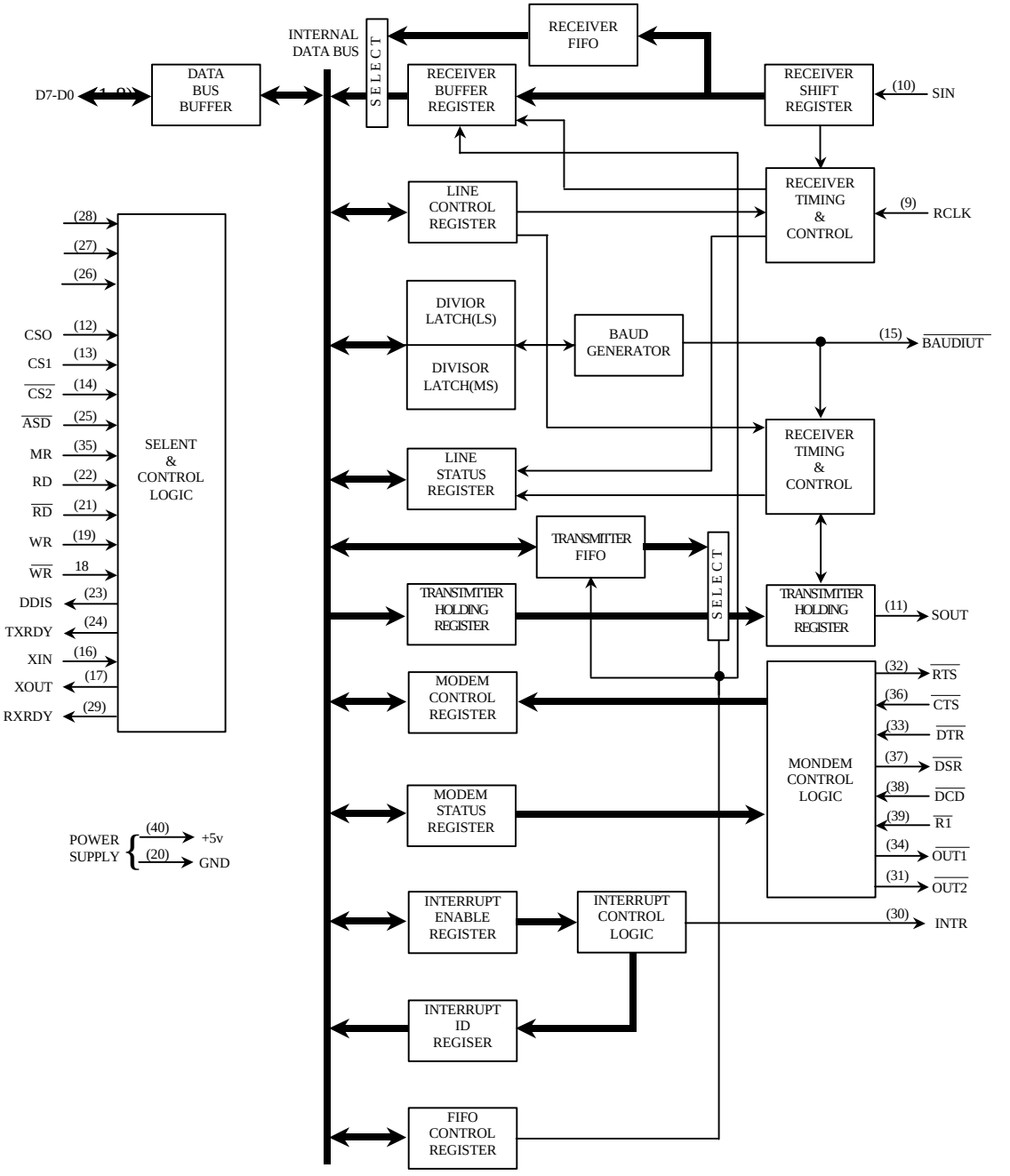
RCVR FIFO Byte Other Than First Byte (RDR is Already Set)



Transmitter Ready (pin 24) FCRO = 1 and FCR = 1 (Mode 1)



INTERNAL BLOCK DIAGRAM



Pin Descriptions

The following describes the function of all UART pins. Some of these descriptions reference internal circuits.
In the following descriptions, a low represents a logic 0 (0V nominal) and a high represents a logic 1 (+2.4V nominal).

INPUT SIGNALS

Chip Select (CS0, CS1, $\overline{CS2}$) Pins 12-14: When CS0 and CS1 are high and $\overline{CS2}$ is low, the chip is selected. This enable communication between the UART and the CPU. The positive edge of an active Address Strobe signal latches the decoded chip select signals, completing chip selection. If $\overline{ADS}$ is always low, valid chip selects should stabilize according to the CSW parameter.

Read (RD, $\overline{RD}$), Pins 22 and 21: When Rd is high or RD is low while the chip selected, the CPR can read status information or data from the selected UART register.

Note: Only an active RD or $\overline{RD}$ input is required to transfer data from the UART during a read operation. Therefore tie either the RD input permanently low or the RD input permanently high, when it is not used.

Write (WR, $\overline{WR}$), Pin 19 and 18: When WR is high or $\overline{WR}$ is low while the chip selected, the CPU can write control words or data into the selected UART register.

Note: Only an active WR or $\overline{WR}$ input is required to transfer data to the UART during a write operation. Therefore, tie either the WR input permanently low or the $\overline{WR}$ input permanently high, when it is not used.

Address Strobe ($\overline{ADS}$), Pin 25: The positive edge of an active Address Strobe ($\overline{ADS}$) signal latches the Register Select (A0, A1, A2) and Chip Select (CS0, CS1, CS2) signals.

Note: An active ADS input is required when the Register Select (A0, A1, A2) signals are not stable for the duration of a read or a write operation. If not required, tie the ADS input permanently low.

Register Select (A0, A1, A2), Pins 26-28: Address signals connected to these 3 inputs select a UART register for the CPU to read from or write to during data transfer. A table of registers and addresses is shown below. Note that the state of the Divisor Latch Access Bit (DLAB), which is the most significant bit of the Line Control Register, affects the selection of certain UART registers. The DLAB must be set high by the system software to access the Baud Generator Divisor Latches.

Master Reset (MR), Pin 35: When this input is high it clears all the registers (except the Receiver Buffer, Transmitter Holding, and Divisor Latches), and the control logic of the UART. The state of various output signals (SOUT, INTR, $\overline{OUT1}$, $\overline{OUT2}$, $\overline{RTS}$, DTR) are affected by an active MR input (Refer to Table 1). This input is buffered with a TTL-compatible Schmitt Trigger with 0.5V typical hysteresis.

Receiver Clock (RCLK), Pin 9: This input is the 16 X baud rate clock for the receiver section of the chip.

Ring Indicator ($\overline{RI}$), Pin 39: When low, this indicates that a telephone ringing signal is received by the MODEM or data set. The $\overline{RI}$ signal is a MODEM status input whose condition can be tested by the CPU reading bit 6 ($\overline{RI}$) of the MODEM Status Register. Bit 6is the complement of the RI signal. Bit 2 (TERI) of the MODEM

Register Address

DLAB	A_2	A_1	A_0	Register
0	0	0	0	Receiver Buffer (read) Transmitter Holding Register (Write)
0	0	0	1	Interrupt Enable
×	0	1	0	Interrupt Identification (read)
×	0	1	0	FIFO Control (Write)
×	0	1	1	Line Control
×	1	0	0	MODEM Control
×	1	0	1	Line Status
×	1	1	0	MODEM Status
×	1	1	1	Scratch
1	0	0	0	Divisor Latch (least significant byte)
0				
1	0	0	1	Divisor Latch (most significant byte)

Serial Input (SIN), Pin 10: Serial data input from the communications link (peripheral device, MODEM, or data set).

Clear to Send ($\overline{CTS}$), Pin 36: When low, this indicates that the MODEM or data set is ready to exchange data. The $\overline{CTS}$ signal is a MODEM status input whose conditions can be tested by the CPU reading bit 4 (CTS) of the MODEM Status Register. Bit 4 is the complement of the $\overline{CTS}$ signal. Bit 0 (DCTS) of the MODEM Status Register indicates whether the $\overline{CTS}$ input has changed state since the previous reading of the MODEM Status Register. $\overline{CTS}$ has no effect on the Transmitter.

Note: Whenever the CTS bit of the MODEM Status Register changes state, an interrupt is generated if the MODEM Status Interrupt is enabled.

Data Set Ready ($\overline{DSR}$), Pin 37: When low, this indicates that the MODEM or data set is ready to establish the communications link with the UART. The $\overline{DSR}$ signal is a MODEM status input whose condition can be tested by the CPU reading bit 5 (DSR) of the MODEM Status Register. Bit 5 is the complement of the $\overline{DSR}$ signal. Bit 1 (DDSR) of the MODEM Status Register indicates whether the $\overline{DSR}$ input has changed state since the previous reading of the MODEM Status Register.

Note: Whenever the DSR bit of the MODEM Status Register changes state, an interrupt is generated if the MODEM Status interrupt is enabled.

Data Carrier Detect ($\overline{DCD}$), Pin 38: When low, indicates that the data carrier has been detected by the MODEM or data set. The $\overline{DCD}$ signal is a MODEM status input whose condition can be tested by the Register. Bit 7 is the complement of the $\overline{DCD}$ signal. Bit 3 (DDCD) of the MODEM Status Register indicates whether the $\overline{DCD}$ input has changed state since the previous reading of the MODEM Status Register. $\overline{DCD}$ has no effect on the receiver.

Note: Whenever the DCD bit of the MODEM Status Register changes state, an interrupt is generated if the MODEM Status Interrupt is enabled.

Status Register indicates whether the $\overline{RI}$ input signal has changed from a low to a high state since the previous reading of the MODEM Status Register

Note : Whenever the RI bit of the MODEM Status Register changes from a high to a low state, an interrupt is generated if the MODEM Status Interrupt is enabled.

Vcc, Pin 40 : +5V supply.
Vss, Pin 20 : Ground(0V) reference.

OUTPUT SIGNALS

Data Terminal Ready ($\overline{DTR}$), Pin 33: When low, this informs the MODEM or data set that the UART is ready to establish communications link. The $\overline{DTR}$ output signal can be set to an active low by programming bit 0 (DTR) of the MODEM Control Register to high level. A Master Reset operation sets this signal to its inactive (high) state. Loop mode operation holds this signal in its inactive state.

Request to Send ($\overline{RTS}$), Pin 32: When low, this informs the MODEM and data set that the UART is ready to exchange data. The RTS output signal can be set to an active low by programming bit 1 (RTS) of the MODEM Control Register. A Master Reset operation sets this signal to its inactive state. Loop node operation holds this signal in its inactive state.

Output 1 ($\overline{OUT1}$), Pin 34: This user-designed out-put can be set to an active low by programming bit 2 (OUT1) of the MODEM Control Register to a high level. A Master Reset operation sets this signal to its inactive state. Loop Mode operation holds this signal to its inactive state.

Output 2 ($\overline{OUT2}$), Pin 31: This user-designated output can be set to an active low by programming bit 3 (OUT2) of the MODEM Control Register to a high level. A Master Reset operation sets this signal to its inactive (high) state. Loop mode operation holds this signal to its inactive state.

TXRDY, RXRDY, Pin 24, 29: Transmitter and Receiver DMA signaling is available through two pins (24 and 29). When operating in the FIFO mode, one of two types DMA signaling per pin can be selected via FCR3, When operating as in the GM16C16450 Mode., only DMA Mode 0 is allowed. Mode 0 supports single transfer DMA where a transfer is made between CPU bus cycles. Mode 1 supports multi-transfer DMA where multiple transfers ard made continuously until the RCVR FIFO has been emptied or the XMIT FIFO has been filled.

RXRDY Mode 0: When in the GM16C450 Mode (FCR0 = 0) or in the FIFO Mode (FCRO = 1, RCR3 = 0) and there is at least 1 character in the RCVR FIFO of RCVR holding register, the RXRDY pin (29) will be low active. Once it is activated the RXRCY pin will go inactive when there are no more characters in the FIFO of holding register.

RXRDY Mode 1: In the FIFO Mode (FCR0 = 1) when the FRC3 = 1 and the trigger level or the timeout has been reached, the RXRDY pin will go low active. Once it is activated it will go inactive when there are no more characters in the FIFO or holding register.

TXRDY Mode 0: in the GM16C450 Mode (FCR0 = 0) or in the FIFO Mode (FCR = 1, FCR3 = 0) and there are no characters in the XMIT FIFO or XMIT hold register, the TXRDY pin(24) will be low active. Once it is activated the TXRDY pin will go inactive after the first character is loaded into the XMIT FIFO or holding register.

TXRDY Mode 1: In the FIFO Mode (FCR0 = 1) when FCR3 = 1 and there is at least one unfilled position in the XMIT FIFO, it will go low active. This pin will become inactive when the XMIT FIFO is completely full.

Driver Disable (DDIS), Pin 23: this goes low whenever the CPU is reading data from the UART. It can disable or control the direction of a data bus transceiver between the CPU and the UART.

Baud Out ($\overline{BAUDOUT}$), Pin 23: This is the 16X clock signal from the transmitter section of the UART. The clock rate is equal to the main reference oscillator frequency divided by the specified divisor in the Baud Generator Divisor Latches. The BAUDOUT may also be used for the receiver section by tying this output to the RCLK input of the chip.

Interrupt (INTR), Pin 30: This pin goes high when-ever any one of the following interrupt types has an active high cognition and is enabled via the IER; Receiver Error Flag; Received Data Avail-able; timeout (FIFO Mode only); Transmitter Holding Register Empty; and MODEM Status, The INTR signal is reset low upon the appropriate interrupt service or a Master Reset operation.

Serial output (SOUT), Pin 11: Composite serial data output to the communications link (peripheral. MODEM or data set). The SOUT signal is set to the Marking (logic 1) state upon a Master Reset operation.

INPUT / OUTPUT SIGNALS

Data (D7-D0) Bus, Pin 1-8: This bus comprises eight TRI-state input/output lines. The bus provides bi-directional communications between the UART and the CPU, Data, control words. And status information are transferred via the D7-D0 Data Bus.

External Clock Input/Output (XIN, XOUT), Pins 16 and 17: These two pins connect the main timing reference (crystal or signal clock) to the UART.

TABLE I. UART Reset Configuration

Register / Signal △	Reset Control	Reset State
Interrupt Enable Register	Master Reset	0000 0000 (Note 1)
Interrupt Identification Register	Master Reset	0000 0001
FIFO Control	Master Reset	0000 0000
Line Control Register	Master Reset	0000 0000
MODEM Control Register	Master Reset	0000 0000
Line status Register	Master Reset	0110 0000
MODEM Status Register	Master Reset	xxxx 0000 (Note 2)
SOUT	Master Reset	High
INTR (RCVR Errs)	Read LSR/MR	Low
INTR (RCVR Data Ready)	Read RBR/MR	Low
INTR (THRE)	Read IIR/Write THR/MR	Low
INTR (Modem Status Changes)	Read MSR/MR	Low
$\overline{\text{OUT2}}$	Master Reset	High
$\overline{\text{RTS}}$	Master Reset	High
$\overline{\text{DTR}}$	Master Reset	High
$\overline{\text{OUT1}}$	Master Reset	High
RCVR FIFO	MR/RCR1-FCR0/ FCR0	All Bits Low
XMIT FIFO	MR/RCR1-FCR0/ FCR0	All Bits Low

Note 1 : Boldface bits are Permanently low.
Note 2 : Bits 7-4 are driven by the input signals.

TABLE II. Summary of Registe rs

Bit No.	Register Address											
	0 DLAB =	0 DLAB =	1 DLAB0=	1	2	3	4	5	6	7	0 DLAB =	1 DLAB =
	Receiver Buffer Register (Read Only)	Transmitter Holding Register (Write Only)	Interrupt Enable Register	Interrupt Enable Register	FIFO Control Register (Write Only)	Line Control Register	MODEM Control Register	Line Status Register	MODEM Status Register	Scratch Register	Divisor Latch (LS)	Divisor Latch (MS)
	RBR	THR	IER	IIR	FCR	LCR	MCR	LSR	MSR	SCR	DLL	DLM
0	Data bit 0	Data bit 0	Enable Received Data Available Interupt (ERBFI)	"0" if Interrupt Pending	FIFO Enable	Word Length Select Bit 0 (WLS0)	Data Terminal Ready (DTR)	Data Ready (DR)	Delta Clear To Send (DCTS)	Bit 0	Bit 0	Bit 8
1	Data bit 1	Data bit 1	Enable Transmitter Holding Register Empty Interrupt (ETBEI)	Interrupt ID Bit (0)	RCVR FIFO Reset	Word Length Select Bit 1 (WLS1)	Request to Send (RTS)	Overrun Error (OE)	Delta Data Set Ready (DDSR)	Bit 1	Bit 1	Bit 9
2	Data bit 2	Data bit 2	Enable Receiver Line Status	Interrupt ID Bit (1)	XMIT FIFO Reset	Number of Stop Bits (STB)	Out1	Parity Error (PE)	Trading Edge Ring Indicator (TERI)	Bit 2	Bit 2	Bit 10
3	Data bit 3	Data bit 3	Enable MODEM Status Interrupt	Interrupt ID Bit (2) (Note 2)	DMA Mode select	Parity Enable (PEN)	Out2	Framing Error (FE)	Delta Data Camer Delect	Bit 3	Bit 3	Bit 11
4	Data bit 4	Data bit 4	0	0	Reserved	Even Parity Select (EPS)	Loop	Break Interrupt (BI)	Clear to Send (CTS)	Bit 4	Bit 4	Bit 12
5	Data bit 5	Data bit 5	0	0	Reserved	Stick Parity	0	Transmitter Holding Register (THRE)	Data Set Ready (DSR)	Bit 5	Bit 5	Bit 13
6	Data bit 6	Data bit 6	0	$FIFO_3$ enabled (note 2)	RCVR Trigger (LSB)	Set Break	0	Transmitter Empty (TEMT)	Ring Indicator (RI)	Bit 6	Bit 6	Bit 14
7	Data bit 7	Data bit 7	0	$FIFO_3$ enabled (note 2)	RCVR Trigger (MSB)	Divisor Latch Access Bit (DLA3)	0	Error in RCBR FIFO (Note2)	Data Camer Detect (DCD)	Bit 7	Bit 7	Bit 15

Note 1: Bit 0 is the least significant bit seriously transmitted or received
Note 2:these bits are always 0 in the GM16C450 Mode

Registers

The system programmer may be Access any of the UART registers summarized in Table II via the CPU.
These registers control UART operations including transmission and reception of data. Each register bit in Table II has its name and reset state shown.

LINE CONTROL REGISTER

The system programmer specifies the format of the asynchronous data communications exchange and set the Divisor Latch Access bit via the Line Control Register (LCR). The programmer can also read the contents of the Line Control Register. The read capability simplifies system programming and eliminates the need for separate storage in system memory of the LCR. Details on each bit follow:

Bit 0 and 1: These two bits specify the number of bits in each transmitted or received serial character. The encoding of bits 0 and 1 is as follows.

Bit 1	Bit 0	Character Length
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits

Bit 2: This bit specifies the number of Stop bits transmitted and received in each serial character. If bit 2 is a logic 0, one Stop bit is generated in the transmitted data. If Bit 2 is a logic 1 when a 5-bit word length is selected via bits 0 and 1, one and a half Stop bits are generated. If bit 2 is a logic 1 When either a 6-, 7-, or 8-bit word length is selected, two Stop bit are generated. The Receiver checks the first Stop bit only, regardless of the number of Stop bit selected.

Bit 3: This bit is the Parity Enable bit. When bit 3 is a logic 1, a Parity bit is generated (transmit data) or checked (receive data) between the last data word bit and Stop bit of the serial data. (The Parity bit is used to produce an even or odd number of 1s when the data word bits and the Parity bit are summed).

Bit 4: This bit is the Even Parity Select bit. When bit 3 is a logic 1 and bit 4 is a logic 0, and odd number of logic 1s is transmitted or checked in the data word bits and Parity bit. When bit 3is a logic 1 and it 4 is a logic 1, an even number of logic 1s is transmitted or checked.

Bit 5: This bit is the Stick Parity bit. When bit3, 4 and 5 are logic 1 the Parity bit is transmitted and checked as a logic 0. If bit 3 and 5 are 1 and bit 4 is a logic 0 then the Parity bit is transmitted and checked as a logic 1. If bit 5 is a logic 0 Stick Parity is disabled.

Bit 6: This bit is the Break Control bit. It causes a break condition to be transmitted to the received UART. When it is set to logic 1, The serial output (SOUT) is forced to the Spacing (logic 0) state. The break is disabled by setting bit 6 to a logic 0. The Break Control bit acts only on SOUT and has no effect on the transmitted logic.

Note : This feature enables the CPU to alert a terminal in during the break. The Transmitter can be used as a character timer to accurately establish the break duration.

a computer communications system.

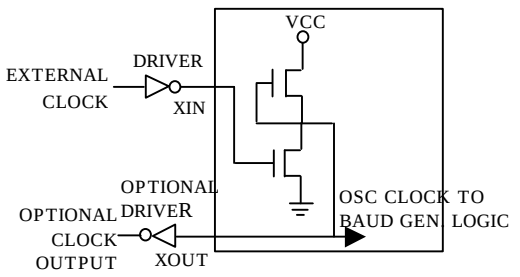
If the following sequence is followed. no erroneous or extraneous characters will be transmitted because of the break.

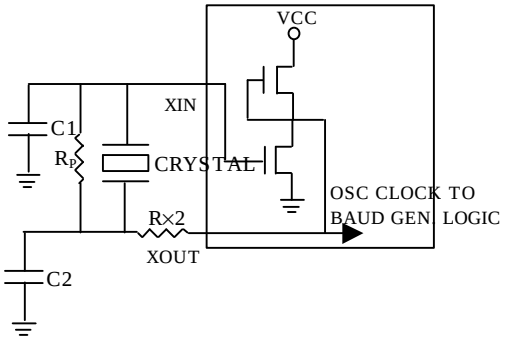
1. Load on all Os, pad character, in response to THRE.
2. Set break after the next THRE
3. Wait for the transmitter to be idle. (TEMT = 1), and clear break when normal transmission has to be tired.

During the bread, the Transmitter can be used as a character timer to accurately establish the break duration.

Bit 7: This bit is the Divisor Latch Access Bit (DLAB). It must be set high (logic) to access the Divisor Latches of the Baud Generator during a Read or Write operation. It must be set low (logic 0) to access the Receiver Buffer, the Transmitter Holding Register, or the Interrupt Enable Register.

Typical Clock Circuits





Typical Crystal Oscillator Network

Crystal	R_P	$R_{·2}$	C_1	C_2
3.1MHz	1MΩ	1.5k	10-30pF	40-60pF
1.8MHz	1MΩ	1.5k	10-30pF	40-60pF

TABLE III. Baud Rates Using 1.8432 MHz Crystal

Desired Baud Rate	Decimal Divisor Used to Generate 16 ´ Clock	Percent Error Difference Between Desired and Actual
50	2304	-
75	1536	-
110	1047	0.026
134.5	857	0.058
150	768	
300	384	–
600	192	–
1200	96	–
1800	64	–
2000	58	0.69
2400	48	-
3600	32	-
4800	24	-
7200	16	-
9600	12	-
19200	6	-
38400	3	-
56000	2	2.86

TABLE IV. Baud Rates Using 3.072 MHz crystal

Desired Baud Rate	Decimal Divisor Used to Generate 16´ Clock	Percent Error Difference Between Desired and Actual
50	3840	-
75	2560	-
110	1745	0.026
134.5	1428	0.034
150	1280	-
300	640	-
600	320	-
1200	160	-
1800	107	0.312
2000	96	-
2400	80	-
3600	53	0.628
4800	40	-
7200	27	1.23
9600	20	-
19200	10	-
38400	5	-

TABLE V. Baud Rate Using 8MHz Crystal

Desired Baud Rate	Decimal Divisor Used to Generate 16´ Clock	Percent Error Difference Between Desired and Actual
50	10000	-
75	6667	0.005
110	4545	0.010
134.5	3717	0.013
150	3333	0.010
300	1667	0.020
600	833	0.040
1200	417	0.080
1800	277	0.080
2000	250	-
2400	208	0.160
3600	139	0.080
4800	104	0.160
7200	69	0.644
9600	52	0.160
19200	26	0.160
38400	13	0.160
56000	9	0.790
128000	4	2.344
256000	2	2.344

TABLE VI.. Interrupt Control Functions

FIFO Mode Only	Interrupt Identification			Interrupt Set and Reset Function			
Bit 3	**Bit 2**	**Bit 1**	**Bit 0**	**Priority Level**	**Interrupt Type**	**Interrupt Source**	**Interrupt Reset Control**
0	0	0	1	-	None	None	-
0	1	1	0	Highest	Receiver Line Status	Overrun Error or Parity Error or Framing Error or Break Interrupt	Reading the Line Status Register
0	1	0	0	Second	Received Data Available	Receiver Data Available or Trigger Level Reached	Reading the Receiver Buffer Register or the FIFO Drops Below the Trigger Level
1	1	0	0	Second	Character Timeout Indication	No Characters Have Been Removed From or Input to the RCVR FIFO During the Last 4 char. Times and There is at Least 1 char. In it During This Time	Reading the Receiver Buffer Register
0	0	1	0	Third	Transmitter Holding Register Empty	Transmitter Holding Register Empty	Reading the IIR Register (if Source of interrupt) or Writing into the Transmitter Holding Register
0	0	0	0	Fourth	MODEM Status	Clear to Send or Data Set Ready or Ring Indicator or Data Carrier Detect	Reading the MODEM Status Register

PROGRAMMABLE BAUD GENERATOR

The UART contains a programmable Baud Generator that is capable of taking any clock input from 2 to 2^{16}–1. 4MHz is the highest input clock frequency recommended when the divisor = 1. The output frequency of the Baud Generator is 16 × the Baud [divisor # = (frequency input) ÷ (baud rate ×16)] Two 8-bit latches store the divisor in a 16-bit binary format. These Divisor Latches must be loaded during initialization to ensure proper operation of the Baud Generator. Upon loading either or the Divisor Latches, a 16-bit Baud counter is immediately loaded.

Tables III, IV and V provide decimal divisors to use with crystal frequencies of 1.8432 MHz 3.072MHz and 8 MHz, respectively. For baud rates of 38400 and below, the error obtain is minimal. The accuracy of the desired baud rate is dependent on the crystal frequency chosen. Using a divisor of zero is not recommended.

LINE STATUS REGISTER

This register provides status information to the CPU concerning the data transfer. Table II shows the contents of the Line Status Register. Details on each bit follow.

Bit 0: This bit is the receiver Data Ready (DR) indicator. Bit 0 is set to logic 1whenever a complete incoming character has been received and transferred into the Receiver Buffer Register or the FIFO. Bit 1 is reset to a logic 0 by reading all of the data in the Receiver Buffer Register or the FIFO.

Bit 1: This bit is the Overrun Error (OE) indicator. Bit 1 indicates that data in the Receiver Buffer Register was not read by the CPU before the next character was transferred into the Receiver Buffer Register, thereby destroying the previous character. The OE indicator is set to a logic 1 upon detection of an overrun condition and reset whenever the CPU reads the contents of the Line Status Register
If the FIFO mode data continues to fill the FIFO beyond the trigger level, An overrun error will occur only been completely received in the shift register. OE is indicated to the CPU as soon as it happens. The character on the shift register is overwritten, but is not transferred to the FIFO.

Bit 2: This bit is the Parity Error (PE) indicator. Bit 2 indicates that the received data character does not have the correct even or odd parity. As selected by the even –parity-select bit. The PE bit is set to a logic 1 upon detection of a parity error and is reset to a logic 0 whenever the CPU reads the contents of the Line Status Register. In the FIFO mode this error is associated with the particular character in the when its associated character is at the top of the FIFO.

Bit 3: This bit is the Framing Error (FE) indicator.
Bit3 indicates that the received character did not have a valid Stop bit. Bit 3is set to logic 1 whenever the Stop bit following the last data bit or parity bit is detected as a logic 0 bit (Spacing level). The FE indicator is reset whenever the CPU reads the contents of the Line Status Register. In the FIFO mode this error is associated with the particular character in the FIFO it applies to. This error is revealed to the CPU when its associated character is at the top of the FIFO. The UART will try to resynchronize after a framing error. To do this it assumes that the framing error was due to the next start bit so it samples this “start” bit twice and then takes in the “data”.

Bit 4: This bit is the Break Interrupt (BI) indicator.
Bit 4 is set to a logic 1 when ever the received data input is held in the spacing (logic) state for longer than a full word transmission time (that is, the total time of Start Bit + data bits + Parity + Stop bits). The BI indicator is reset whenever the CPU reads the contents of the line Status Register. In the FIFO mode this error is associated with the particular character in the FIFO it applies to. This error is revealed to the CPU when its associated character is at the top of the FIFO. When break occurs only one zero character is loaded into the FIFO. The next character transfer is enabled after SIN goes to the marking state and receives the next valid start bit.

Note: Bits 1 through 4 are the error conditions that produce a Receiver Line Status interrupt whenever any of the corresponding conditions are detected and the interrupt is enabled.

Bit 5: This bit is the Transmitter Holding Register Empty (THRE) indicator. Bit 5 indicates that the UART is ready to accept a new character for transmission. In addition, this bit causes the UART to issue an interrupt to the CPU when the Transmit Holding Register Empty Interrupt enable is set high. The THRE bit is set to logic 1 when a character is transferred from the Transmitter Holding Register into the Transmitter Shift Register. The bit is reset to logic 0 concurrently with the loading of the Transmitter Holding Register by the CPU, In the FIFO mode this bit is set when the XMIT FIFO is empty; it is cleared when at least 1 byte is written to the XMIT FIFO.

Bit 6: This bit is the Transmitter Empty (TEMT) indicator. Bit 6 is set to a logic 1 whenever the Transmitter Holding Register (THR) and the Trans-mitter shift register (TSR) are both empty. It is reset to a logic 0 whenever either the THR or TSR contains a data character. In the FIFO mode this bit is set to one whenever the transmitter FIFO and shift register are both empty.

Bit 7: in the GM16C450 Mode this is a 0. In the FIFO mode LSR7 is set when there is least one parity error, framing error or break indication in the FIFO. LSR7 is cleared when the CPU reads the LSR, if there are no subsequent errors in the FIFO.

Note: The Line Status Register is intended for read op-erations only. Writing to this register is not recom-mended as this operation is only used for factory testing.

FIFO CONTROL REGISTER

This is a write only register at the same location as the IIR (the IIR is a read only register). This register is used to enable the FIFOs, set the RCVR FIFO trigger level, and select the type of DMA signaling.

Bit 0: Writing a 1 to FCR0 enables both the XMIT and RCVR FIFOs. Resetting FCR0 will clear all bytes in both FIFOs. When changing from FIFO Mode to GM16C450 Mode and vice versa, data is automatically cleared from the FIFOs. This bit must be a 1 when other RCR bits are written to or they will not be programmed.

Bit 1: Writing a 1 to FCR1 clears all bytes in the RCVR FIFO and resets its counter logic to 0. The shift register is not cleared. The 1 that is written to this bit position is self-clearing.

Bit 2: Writing a 1 to FCR2 clears all bytes in the XMIT FIFO and resets its counter logic to 0. The shift register is not cleared. The 1 that is written to this bit position is self-clearing.

Bit 3: Setting FCR 3 to a 1 will cause the RXRDY and TXRDY pins to change from mode 0 to mode 1 if FCR0 = 1 (see description of RXRDY and TXRDY pins).

Bit4, 5: FCR4 to FCR5 are reserved for future use.

Bit6, 7: FCR6 to FCR7 are used to set the trigger level for the RCVR FIFO interrupt.

7	6	RCVR FIFO Trigger Level (Bytes)
0	0	01
0	1	04
1	0	08
1	1	14

INTERRUPT IDENTIFICATION REGISTER

In order to provide minimum software overhead during data character transfers, the UART prioritizes interrupts into four levels and records these in the interrupt Identification Register. The four levels of interrupt conditions in order of priority are Receiver Line Status; Received Data Ready; Transmitter Holding Register Empty; and MODEM Status. When the CPU accesses the IIR, the UART freezes all interrupts and indicates the highest priority pending interrupt to the CPU. While this CPU access is occurring, the UART records niw interrupts, but access is complete. Table II shows the contents of the IIR. Details on each bit follow:

Bit 0: This bit can be used in a prioritized interrupt environment to indicate whether an interrupt is pending. When bit 0 is a logic 0, an interrupt is pending and the IIR contents may be used as a pointer to the appropriate interrupt service routine. When bit 0 is a logic 1, no interrupt is pending.

Bit 1 and 2: These two of the IIR are used to identify highest priority interrupt pending as indicated in Table VI.

Bit 3: In the GB16C450 Mode this bit is 0. In the FIFO mode this bit is set along with bit 2 when a timeout interrupt is pending.

Bit 4 and 5: These two bits of the IIR are always logic 0.

Bit 6 and 7: These two bits are set when FCR0 =1.

INTERRUPT ENABLE REGISTER

This register enables the five types of UART interrupts. Each interrupt can individually activate the interrupt (INTR) output signal. It is possible to totally disable the interrupt system by resetting bits 0 through 3 of the Interrupt Enable Register (IER).
Similarly, setting bits of the IER register to a logic 1, enables the selected interrupt(s). Disabling an interrupt prevents it from being indicated as active in the IIR and from activating the INTR output signal. All other system functions operate in their normal manner, including the setting of the Line Status and MODEM Status Registers. Table II shows the contents of the IER. Details on each bit follow.

Bit 0: This bit enables the Received Data Available Interrupt (and timeout interrupts in the FIFO mode) when set to logic1.

Bit 2: This bit enables the Receiver Line Status interrupt when set to logic 1

Bit 3: This bit enables the MODEM Status interrupt when set to logic 1

Bit 4 through 7: These four bits are always logic 0.

MODEM CONTROL REGISTER

This register controls the interface with the MODEM or data set (or peripheral device emulating a MODEM). The contents of the MODEM Control Register are indicated in Table II and are described below.

Bit 0: This bit controls the Data Terminal Ready (DTR) output. When bit 0 is set to a logic 1, the DTR output is forced to a logic 0. When bit 0 is reset to a logic 0, the DTR output is forced to a logic 1.

Note: The DTR output of the UART may be applied to an EIA inverting line driver (such as the GD751-88) to obtain the proper polarity input at the succeeding MODEM or data set.

Bit 1: This bit controls the Request to Send (RTS) output. Bit 1 affects the RTS output in a manner identical to that described above for bit 0.

Bit 2: This bit controls the output 1 (OUT1) signal , which is an auxillary user-designated output. Bit 2 affects the OUT1 output in a manner identical to that described above for bit 0.

Bit 3: This bit controls the output 2(OUT2) signal, which is an auxillary user-designated output . Bit 3 affects the OUT2 output in a manner identical to that described above for bit 0.

Bit 4: This bit provides a local loopback feature for Diagnostic testing of the UART. When bit 4 is set to logic 1, the following occur ; the transmitter Serial output (SOUT) is set to the Marking (logic 1) State; the receiver Serial Input (SIN) is disconnected; the output of the Transmitter Shift

Register is "looped back" into the Receiver Shift Register input; the four MODEM Control inputs (CTS , RTS , RI , and DCD) are disconnected; and the four MODEM Control outputs (DTR , RTS , OUT1 and OUT2) are internally connected to the four MODEM Control inputs, and the MODEM Control output pins are forced to their inactive state (high). In the diagnostic mode, data that is transmitted is immediately received. This feature allows the processor to verify the transmitter and received-data paths of the UART.

In the diagnostic mode, the receiver and transmitter interrupts are fully operational. Their sources are external to the part. The MODEM Control Interrupts are also operational, but the interrupts sources are now the lower four bits or the MODEM Control inputs. The interrupts are still controlled by the Interrupt Enable Register.

Bits 5 through 7: These bits are permanently set to logic 0.

MODEM STATUS REGISTER

This register provides the current state of the control lines from the MODEM (or peripheral device) to the CPU. In addition to this current-state information, four bits of the MODEM Status Register provide change information. These bits are set to a logic 1 Whenever a control input from the MODEM changes state. They are reset to logic 0 whenever the CPU reads the MODEM Status Register.

The contents of the MODEM Status Register are indicated in Table II and described below.

Bit 0: This bit is the Delta Clear to Send (DCTS) indicator. Bit 0 indicates that the CTS input to the chip has changed state since the last time it was read by the CPU.

Bit 1: This bit is the Delta Data Set Ready (DDSR) indicator. Bit 1 indicates that the DSR input to the chip has changed state since the last tome it was read by the CPU.

Bit 2: This bit is the Trailing Edge of Ring Indicator (TERI) detector. Bit 2 indicates that the RI input to the chip has changed from a low to a high state.

Bit 3: This bit is the Delta Data Carrier Detect (DDCD) indicator. Bit 3 indicates that the DCD input to the chip has changed state.
Note: Whenever bit 0, 1, 2 or 3 is set to logic 1, a MODEM Status Interrupt is generated.

Bit 4: This bit is the complement of the Clear to Send ($\overline{CTS}$) input. If bit 4(loop) of the MCR is set to a 1, this bit is equivalent to RTS in the MCR.

Bit 5: This bit is the complement of the Data Set Ready (DSR) input. If Bit 4 of the MCR is set to a 1, this bit is equivalent to DTR in the MCR.

Bit 6: This bit is the complement of the Ring Indicator. ($\overline{RI}$) input. If bit 4 of the MCR is set to a 1, this bit is equivalent to OUT1 in the MCR.

Bit 7: This bit is the complement of the Data Carrier Detect(DCD) input. If but 4 of the MCR is set to a 1, this bit is equivalent to out2 in the MCR.

SCRATCHPAD REGISTER

This 8-bit Read/Write Register does not control the UART in anyway. It is intended as a scratchpad register to be used by the programmer to hold data temporarily.

FIFO INTERRUPT MODE OPERATION

When the RCVR FIFO and receiver interrupts are enabled (FCR0 = 1, IER0 =1) RCVR interrupts will occur as follows:

A. The receive data available interrupts will be issued to the CPU when the FIFO has reached its programmed trigger level; it will be cleared as soon as the FIFO drops below its programmed trigger level.

B. The IIR receive data available indicate also occurs when the FIFO trigger level is reached, and like the interrupt it is cleared when the FIFO drops below the trigger level.

C. The receiver line status interrupt (IIR-06), as before, has higher priority than received data available (IIR-04) interrupt.

D. The data ready bit (LSR0)is set as soon as a character is transferred from the shift register to the RCVR FIFO. It is reset when the FIFO is empty.

When RCVR FIFO and receiver interrupts are enabled, RCVR FIFO timeout interrupts will occur as follows:

A. A FIFO timeout interrupt will occur, if the following conditions exist:

- at least one character is in the FIFO
- the most recent serial character received was longer than 4 continuous character times ago (if 2 stop bits are programmed the second one is included in this time delay).
- The most recent CPU read if the FIFO was longer than 4continuous character times age.

This will cause a maximum character received to interrupt issued delay of 160ms at 300BAUD with a 12 bit character.

B. character times are calculated by using the RCLK input for a clock signal (This makes the delay proportional to the baudrate).

C. When a timeout interrupt has occurred it is cleared and the timer rest when the CPU reads one character from the RCVR FIFO.

D. When a timeout interrupt has not occurred the timeout timer is reset after a new character is received or after the CPU reads the RCVR FIFO.

When the XMIT FIFO and transmitter interrupts are enabled (FCR0=1, IER=1) XMIT interrupts will occur as follows:

A. The transmitter holding register interrupt (02) occurs when the XMIT FIFO is empty; it is cleared as soon as the transmitter holding register is written to (1 to 16 characters may be written to the XMIT FIFO while servicing this interrupt) or the IIR is read.

The transmitter FIFO empty indications will be delayed 1 character time minus the last stop bit time whenever the following occurs: THRE = 1 and there have not been at least two bytes at the same time in the transmit FIFO, since the last THRE = 1. The first transmitter interrupt affect changing FCR0 will be immediate, if it is enabled.

Character timeout and RCVR FIFO trigger level interrupts have the same priority as the current received data available interrupt; XMIT FIFO empty has the same priority as the current transmitter holding register empty interrupt.

FIFO POLLED MODE PRERATION

With FCRQ = 1 resetting IER0, IER1, IER2, IER3 or all to zero puts the RCVR and MITTER are controlled separately either one or both can be in the polled mode of operation.

In this mode the user's program will check RCVR and XMITTER status via the LSR. As stated previously:

LSR0 will be set as long as there is one byte in the RCR FIFO.

LSR1 to LSR4 will specify which error(s) has occurred. Character error status is handled the same way when in the interrupt mode, the IIR is not affected since IER2=0.

LSR5 will indicate when the XMIT FIFO is empty.

LSR6 will indicate that both the XMIT FIFO and shift register are empty.

LSR7 will indicate whether there are any errors in the RCVR FIFO.

There is no trigger level reached or timeout condition indicated in the FIFO polled Mode, however, the RCVR and XMIT FIFOs still fully capable of holding characters.

Application Circuit