Reed Solomon decoder IC — SAA7207H

FEATURES

- (204, 188 and 17) Digital Video Broadcasting (DVB) compliant Reed Solomon (RS) codes
- Automatic synchronization of bytes, blocks and frame
- Convolutional de-interleaving (I = 12)
- Energy dispersal de-randomizing
- Contained in a 44-pin quad flat package
- I²C-bus interface
- 6 quasi-bidirectional ports
- Boundary scan facility.

APPLICATIONS

- Forward Error Correction (FEC) for digital TV distribution according to the DVB standard.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	operational supply voltage	4.75	5.00	5.25	V
$I_{DD(tot)}$	total supply current	–	65	–	mA
T_{CLK}	input clock period	–	31.5	–	ns

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA7207H/C1	QFP44	plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 × 10 × 1.75 mm	SOT307-2

FOR MORE DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC02 OR DATA SHEET

BLOCK DIAGRAM

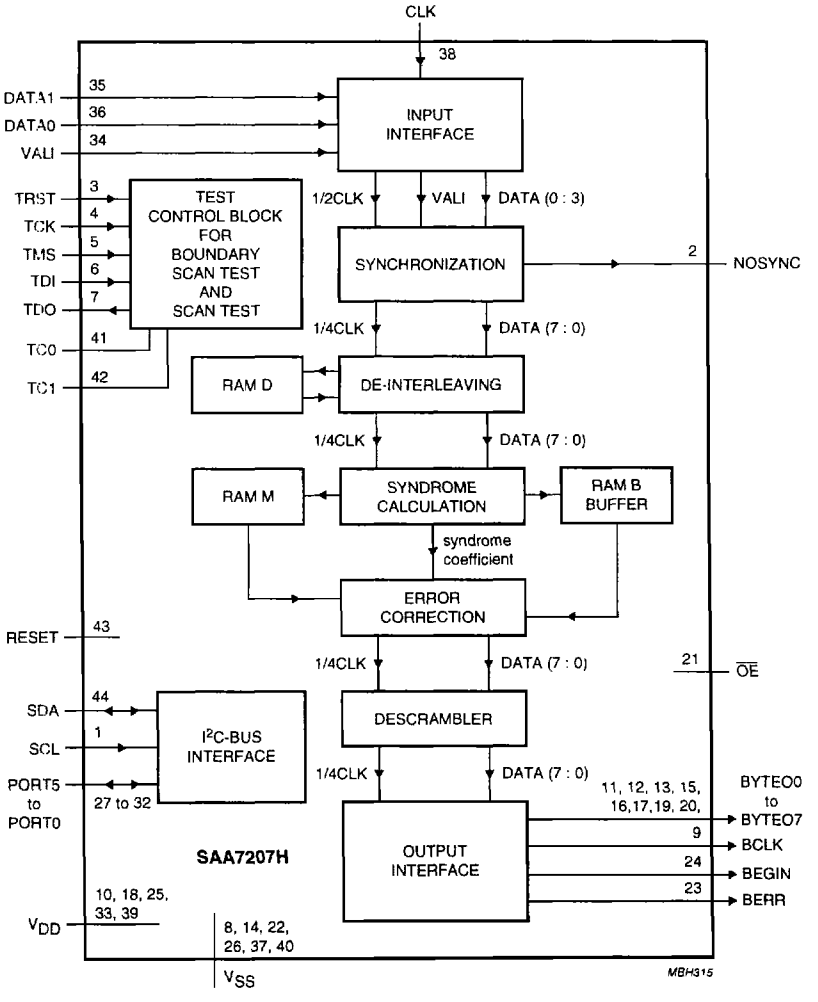

Fig.1 Block diagram.io

PINNING

SYMBOL	PIN	I/O	DESCRIPTION
SCL	1	I	serial clock input (I^2C-bus)
NOSYNC	2	O	not synchronized output (1 = not synchronized)
TRST	3	I	boundary scan test reset (0 = active)
TCK	4	I	boundary scan test clock
TMS	5	I	boundary scan test mode select (1 = BST select)
TDI	6	I	boundary scan test data input
TDO	7	O	boundary scan test data output
V_{SS}	8	–	ground
BCLK	9	O*(1)	byte clock output
V_{DD}	10	–	positive supply voltage
BYTEO0	11	O*(1)	output data byte 0 (LSB)
BYTEO1	12	O*(1)	output data byte 1
BYTEO2	13	O*(1)	output data byte 2
V_{SS}	14	–	ground
BYTEO3	15	O*(1)	output data byte 3
BYTEO4	16	O*(1)	output data byte 4
BYTEO5	17	O*(1)	output data byte 5
V_{DD}	18	–	positive supply voltage
BYTEO6	19	O*(1)	output data byte 6
BYTEO7	20	O*(1)	output data byte 7 (MSB)
$\overline{OE}$	21	I	output enable not (active LOW; 1 = O*(1) high impedance)
V_{SS}	22	–	ground
BERR	23	O*(1)	block error output (1 = uncorrectable block)
BEGIN	24	O*(1)	begin of block output (1st byte of block is output)
V_{DD}	25	–	positive supply voltage
V_{SS}	26	–	ground
PORT5	27	I/O	quasi-bidirectional port 5
PORT4	28	I/O	quasi-bidirectional port 4
PORT3	29	I/O	quasi-bidirectional port 3
PORT2	30	I/O	quasi-bidirectional port 2
PORT1	31	I/O	quasi-bidirectional port 1
PORT0	32	I/O	quasi-bidirectional port 0
V_{DD}	33	–	positive supply voltage
VALI	34	I	valid input (1 = data is valid)
DATA1	35	I	input data 1 (MSB)
DATA0	36	I	input data 0 (LSB)
V_{SS}	37	–	ground
CLK	38	I	master clock input (also acting as input data clock)
V_{DD}	39	–	positive supply voltage
V_{SS}	40	–	ground

SYMBOL	PIN	I/O	DESCRIPTION
TC0	41	I	test mode control input 0 (0 = application mode)
TC1	42	I	test mode control input 1 (0 = application mode)
RESET	43	I	master reset input (1 = active)
SDA	44	I/O	bidirectional serial data port (I^2C-bus)

Note

1. When $\overline{OE}$ is active (pin 21 = HIGH), all O* outputs become high impedance.

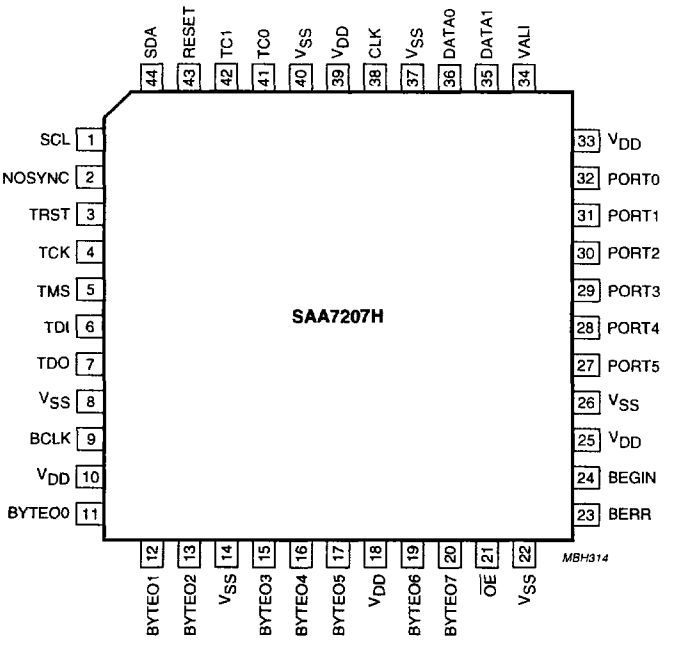

Fig.2 Pin configuration.