



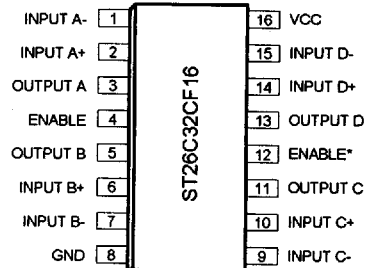
## QUAD RS-422, RS-423 CMOS DIFFERENTIAL LINE RECEIVER

### DESCRIPTION

The ST26C32 is a CMOS quad differential line receiver designed to meet the standard RS-422, RS-423 requirements. The ST26C32 has an input sensitivity of 200mv over the common mode input voltage range of  $\pm 7V$ . To improve noise margin and output stability for slow changing input signal, special hysteresis is built in the ST26C32 circuit.

The ST26C32 is a high speed line receiver designed to operate with MFM / RLL controllers and hard disk drives as well as RS-422, and RS-423 differential applications. ST26C32 provides TTL compatible outputs to interface with standard 74LS and CMOS design environments. ST26C32 is suitable for low power 5V operation.

### SOIC package

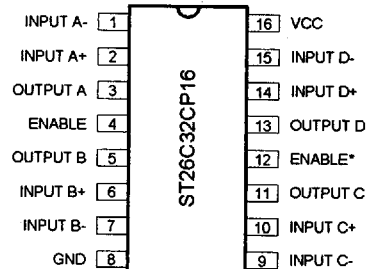


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### FEATURES

- Pin-to-pin compatible with National DS26C32C
- Low power CMOS design
- Three-state outputs with enable pin
- Meets the EIA RS-422 requirements
- Low propagation delays
- High speed

### Plastic-DIP package



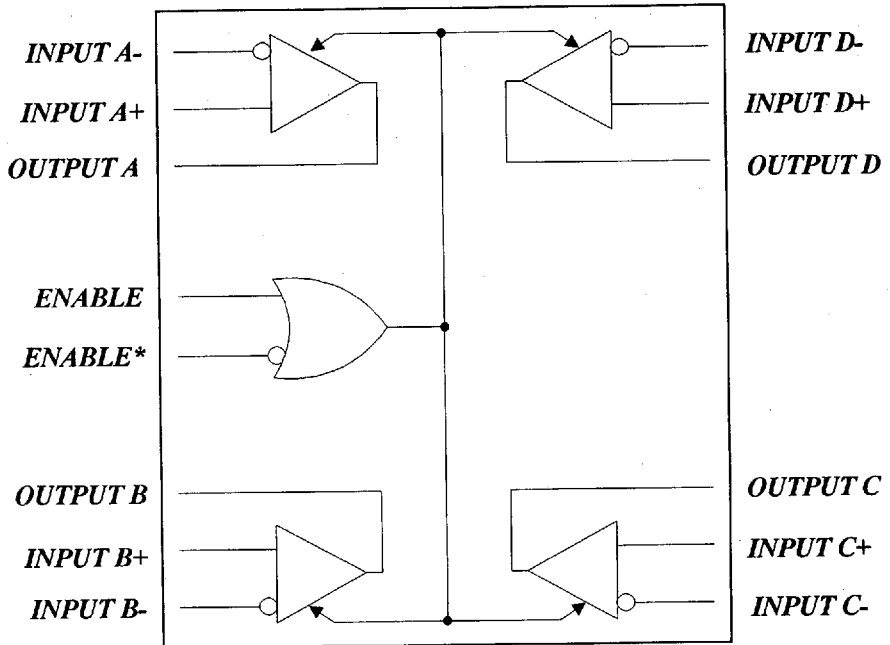
### ORDERING INFORMATION

Part number	Package	Operating temperature
ST26C32CP16	Plastic-DIP	0° C to + 70° C
ST26C32CF16	SOIC	0° C to + 70° C
ST26C32IP16	Plastic-DIP	-40° C to + 85° C
ST26C32IF16	SOIC	-40° C to + 85° C

# ST26C32

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## BLOCK DIAGRAM



## SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
INPUT A-	1	I	Receiver A differential inverting input pin.
INPUT A+	2	I	Receiver A differential non-inverting input pin.
OUTPUT A	3	O	Receiver A output pin.
ENABLE	4	I	Gate control (active high). This pin is one of the two control pins which enables or disables all four receivers.
OUTPUT B	5	O	Receiver B output pin.
INPUT B+	6	I	Receiver B differential non-inverting input pin.
INPUT B-	7	I	Receiver B differential inverting input pin.
GND	8	O	Signal and power ground.
INPUT C-	9	I	Receiver C differential inverting input pin.
INPUT C+	10	I	Receiver C differential non-inverting input pin.
OUTPUT C	11	O	Receiver C output pin.
ENABLE *	12	I	Gate control (active low). See ENABLE description
OUTPUT D	13	O	Receiver D output pin.
INPUT D+	14	I	Receiver D differential non-inverting input pin.
INPUT D-	15	I	Receiver D differential inverting input pin.
VCC	16	I	Power supply pin.

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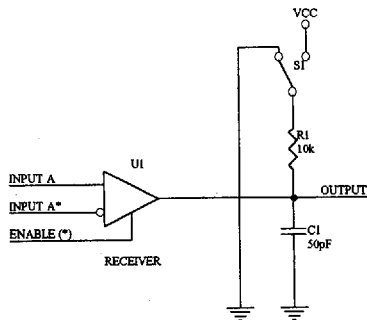
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Functional table

Enable	Enable*	Output	Differential Non-Inverting Input	Differential Inverting Input
L	H	Z	X	X
H	L	L	L	H
H	L	H	H	L

X=Don't care

Z=Three state (high impedance)



## AC ELECTRICAL CHARACTERISTICS

$T_A = 0^\circ - 70^\circ \text{ C}$ ,  $V_{CC} = 5.0 \text{ V} \pm 10\%$  unless otherwise specified.

Symbol	Parameter	Limits			Units	Conditions
		Min	Typ	Max		
T <sub>1</sub>	Propagation delay, input to output		8	10	ns	S1=VCC
T <sub>2</sub>	Propagation delay, input to putput		18	20	ns	S1=GND
T <sub>3</sub>	Output enable time		18	20	ns	V <sub>DIF</sub> =2.5V
T <sub>4</sub>	Output disable time		18	20	ns	V <sub>DIF</sub> =2.5V

## ABSOLUTE MAXIMUM RATINGS

Supply range	7 Volts
Voltage at any logic pin	GND-0.3 V to VCC+0.3 V
Operating temperature	0° C to +70° C
Storage temperature	-40° C to +150° C
Package dissipation	500 mW

## DC ELECTRICAL CHARACTERISTICS

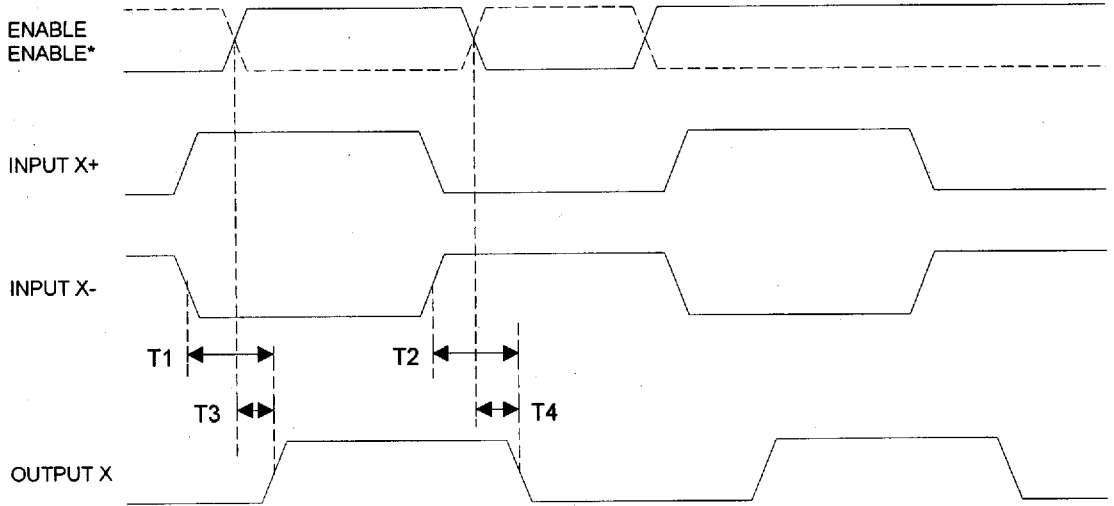
$T_A = 0^\circ - 70^\circ \text{C}$ ,  $V_{CC} = 5.0 \text{V} \pm 10\%$  unless otherwise specified.

Symbol	Parameter	Limits			Units	Conditions
		Min	Typ	Max		
$V_{IH}$	Enable high level	2.0			V	
$V_{IL}$	Enable low level			0.8	V	
$V_{OH}$	Output high level	3.8	4.2		V	$I_{OH} = -6\text{mA}$
$V_{OL}$	Output low level			0.4	V	$I_{OH} = 6\text{mA}$
$V_{ID}$	Differential input level	-0.2		+0.2	V	$-7\text{V} < V_{CM} < +7\text{V}$
$V_H$	Input hysteresis		50		mV	
$I_{IN}$	Input current			$\pm 1.0$	$\mu\text{A}$	
$I_{CC}$	Operating current		12		mA	$V_{DIF} = +1\text{V}$
$I_{OZ}$	Three state output leakage		$\pm 1.0$	$\pm 5.0$	$\mu\text{A}$	$V_{OUT} = V_{CC}$ or GND
$I_{EN}$	Enable input current		$\pm 1.0$		$\mu\text{A}$	$V_{IN} = V_{CC}$ or GND
$V_R$	Input resistance	5		15	k $\Omega$	$-7\text{V} < V_{CM} < +7\text{V}$

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## DIFFERENTIAL LINE RECEIVER TIMING



2632-CK-1