ABRIDGED VERSION

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# SSI 32P4782A
## 100 Mbit/s Read Channel Device

**Advance Information**

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## DESCRIPTION

The 32P4782A device is a high performance BiCMOS single chip read channel IC that, together with the 32D4680 time base generator, contains all the functions needed to implement a complete zoned recording read channel for hard disk drive systems. Functional blocks include the pulse detector, programmable filter, servo functions, data synchronizer, window shift, write precomp and 1,7 RLL ENDEC. Data rates from 33 to 100 Mbit/s can be programmed using an internal DAC whose reference current is set by a single external resistor.

The programmable functions of the 32P4782A device are controlled through a bi-directional serial port and banks of internal registers. This allows zoned recording applications to be supported without changing external component values from zone to zone.

The 32P4782A utilizes an advanced BiCMOS process technology along with advanced circuit design techniques which result in a high performance device with low power consumption.

## FEATURES

### GENERAL

- **Programmable data rate, internal DAC controlled: 33 to 100 Mbit/s**
- **Complete zoned recording application support**
- **Low power operation (850 mW typical @ 80 Mbit/s, 5V)**
- **Bi-directional serial port for register access**
- **Register programmable power management (sleep mode < 8 mW)**
- **Power supply range (4.5 to 5.5 volts)**
- **Small footprint 64-lead TQFP package**

### AGC

- **LowZ and fast decay timings independently set by two external resistors**
- **fast decay current set by an external resistor**
- **Low Drift AGC Hold circuitry**

(continued)

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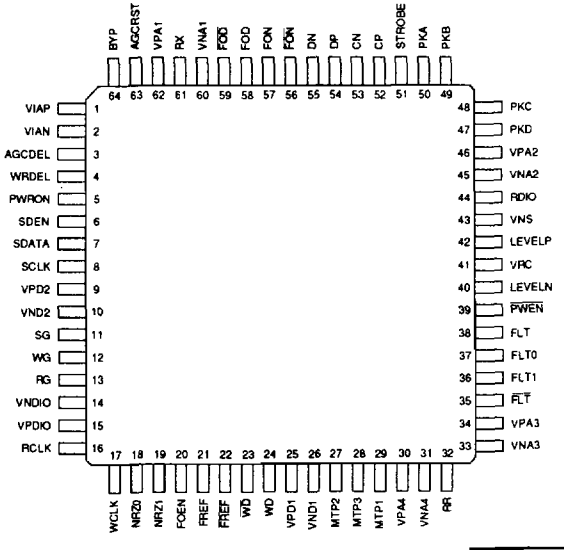
## PIN DIAGRAM




**64-Lead TQFP**

CAUTION: Use handling procedures necessary for a static sensitive component.

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## FEATURES (continued)

**AGC (continued)**

- Separate read and servo AGC levels (4-bit DAC)
- Temperature compensated, exponential control AGC
- Wide bandwidth, high precision full-wave rectifier
- Wide bandwidth, high precision multirate charge pump

**PULSE DETECTOR**

- DP, DN and CP, CN LowZ pin for rapid transient recovery
- Pulse qualification circuitry can be configured via serial port to support one of three modes of operation:
  - bit by bit qualification with polarity check
  - bit by bit qualification without polarity check
  - analog Viterbi detector
- Independent control of positive and negative thresholds levels in the data comparators
- CMOS RDIO signal output for servo timing support
- 500 ps max. pulse pairing with sine wave input
- Programmable fixed positive and negative threshold

**SERVO CAPTURE**

- 4-burst servo capture with A, B, C and D outputs.
- Separate full wave rectifier connected to filter differentiated output.
- Separate registers for filter cutoff, AGC level and qualification threshold during servo mode

**PROGRAMMABLE FILTER**

- External hold capacitors and reset line required
- Cutoff frequency programmable via serial port:
  - 9 to 27 MHz (4 - 9 MHz at degraded specs for filtering in servo mode)
- Advanced architecture minimizes filter settling characteristics when switching between servo mode and data mode
- Programmable boost/equalization range of 0 to 12 dB
- Separate boost for servo and read mode
- Programmable group delay equalization with asymmetric zeroes control
- Matched normal and differentiated outputs
- ±15% $fc$ accuracy over operating temperature and supply ranges
- ±2% maximum group delay variation (≤500 ps @ $fc$ = 27 MHz)
- Less than 1% total harmonic distortion
- No external filter components required

**DATA SEPARATOR**

- High performance dual-bit NRZ interface
- Integrated 1,7 RLL encoder decoder
- Fast acquisition phase lock loop with zero phase restart technique
- Fully integrated data separator
  - no external delay lines or active components are required
  - no external active PLL components are required
- Programmable decode window symmetry control via serial port
  - window shift control ±50% (4-bit)
  - delayed read data and VCO clock monitor points
- Programmable write precompensation (3-bit)
  - independent control of two precompensation levels

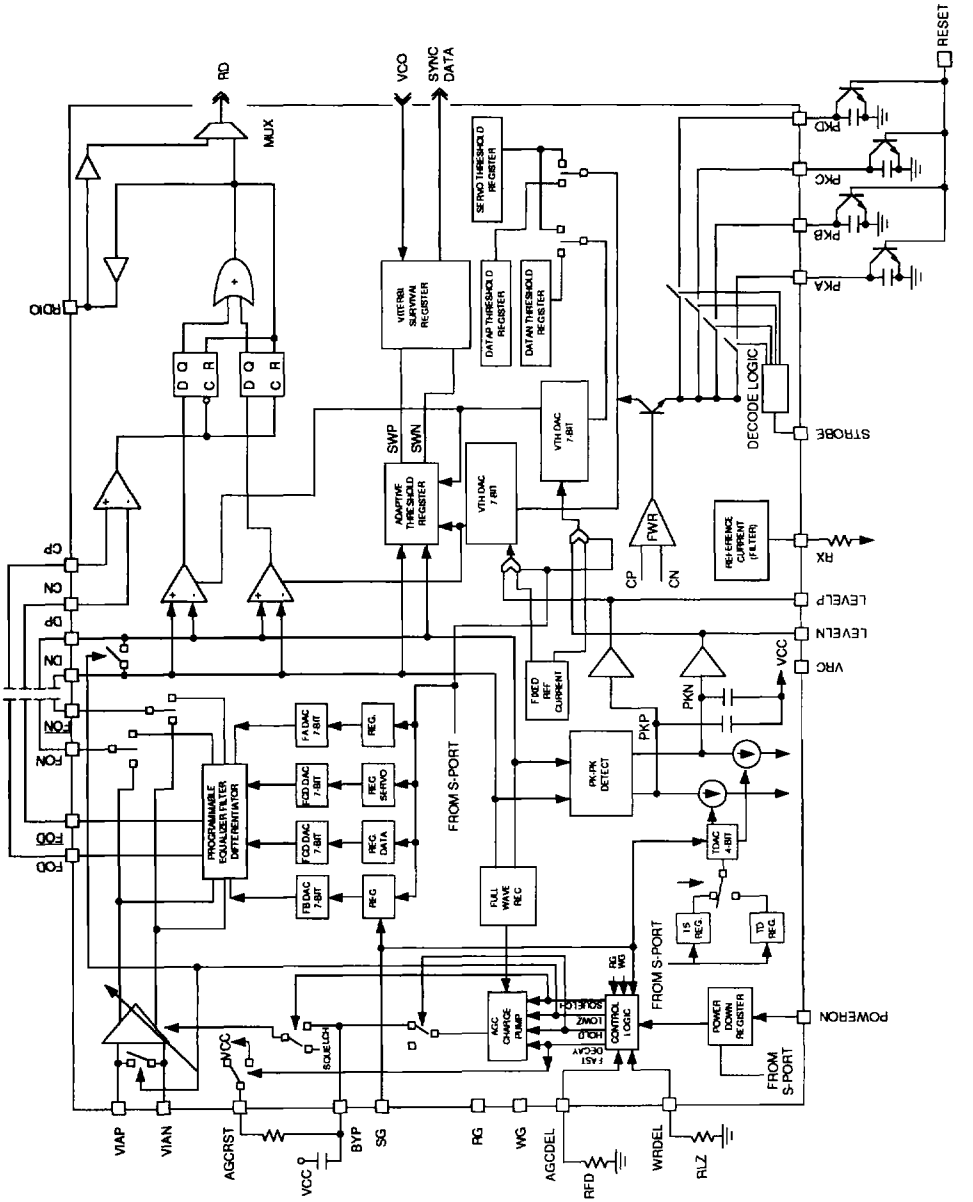


FIGURE 1: Block Diagram – Front End

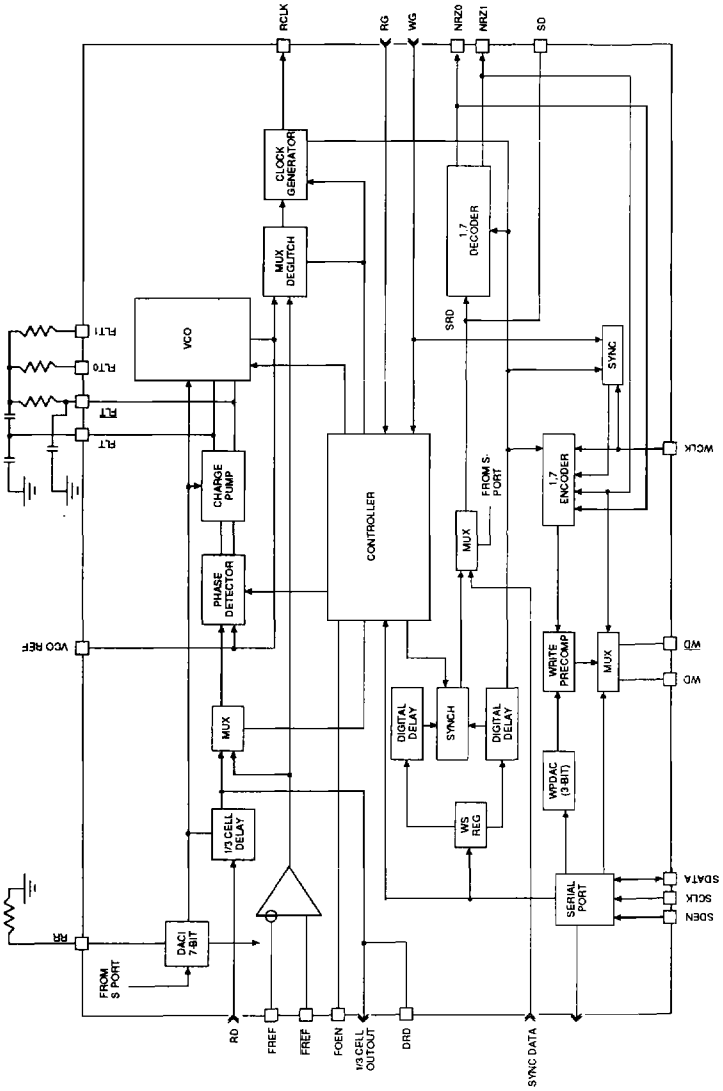


FIGURE 2: Block Diagram – Back End

**Advance Information:** Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.

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