

**TENTATIVE TOSHIBA HYBRID DIGITAL INTEGRATED CIRCUIT
8,388,608-WORD BY 72-BIT DYNAMIC RAM MODULE**

DESCRIPTION

The THM72V8015BTG is a 8,388,608-word by 72-bit dynamic RAM module consisting of nine TC5165805BFT DRAMs on a printed circuit board. This module is optimized for applications which require high density and high capacity, such as computer main memory and image memory, and also for applications which require compactness.

FEATURES

- 8,388,608-word by 72-bit organization
- Fast access and cycle times

	-4	-5
t _{RAC} RAS Access Time	40 ns	50 ns
t _{AA} Column Address Access Time	25 ns	30 ns
t _{CAC} CAS Access Time	16 ns	18 ns
t _{RC} Cycle Time	69 ns	84 ns
t _{HPC} Hyper Page Mode Cycle Time	16 ns	20 ns

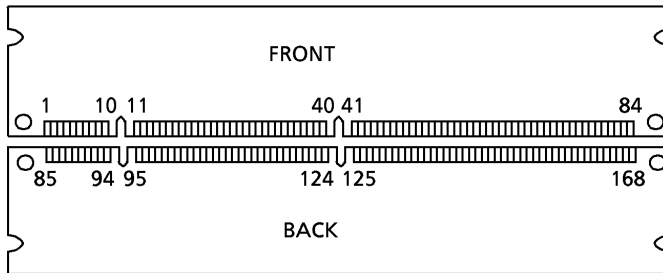
- Single power supply of 3.3 V ± 5%
- Low power dissipation (max)
 - Operating 3783 mW (40-ns type)
3158 mW (50-ns type)
 - Standby 50.4 mW (both devices)
- Read-Modify-Write, CAS-before-RAS refresh, RAS-Only refresh, Hidden refresh, EDO (Hyper Page mode) and Test mode capability
- All inputs and outputs LVTTTL-compatible
- 4096 refresh cycles per 64 ms
- Package: 168-pin Gold contacts

PIN NAMES

	-4	-5
B0,A0 to 10, A11R	Address Inputs	
DQ0 to 71	Data Inputs/Outputs	PD0 H H
/RAS0,2	Row Address Strobe	PD1 L L
/CAS0,4	Column Address Strobe	PD2 H H
/WE0,2	Read/Write Input	PD3 H H
/OE0,2	Output Enable	PD4 H H
V _{CC}	Power (+3.3 V)	PD5 H L
V _{SS}	Ground	PD6 L L
PD0 to 7	Presence Detect Pin	PD7 L L
ID0,1	ID bit	ID0 V _{SS} V _{SS}
NC	No Connection	ID1 V _{SS} V _{SS}

Note: H: High Level (buffered)
L: Low Level (buffered)

PIN ASSIGNMENT (TOP VIEW)

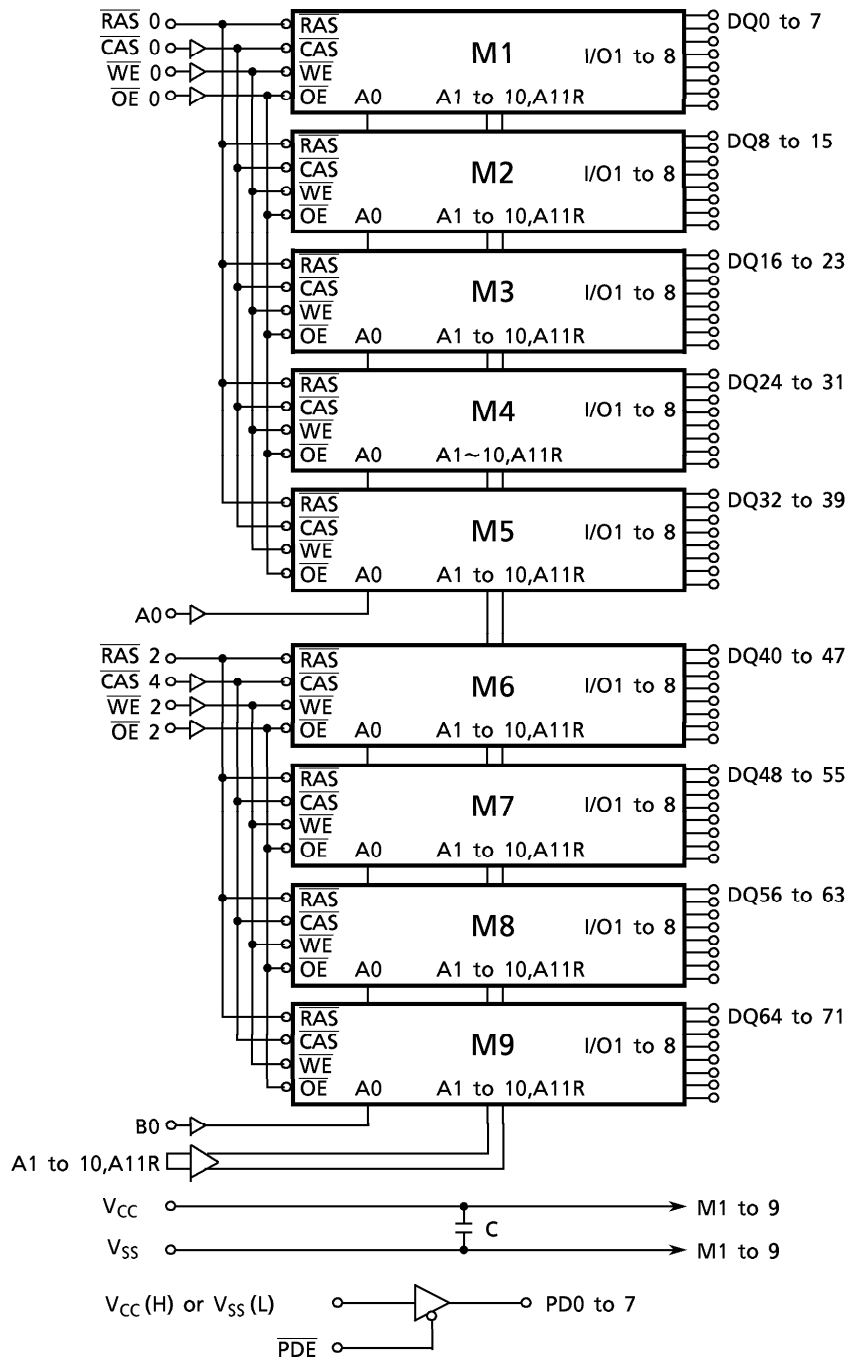


1	V _{SS}	85	V _{SS}	18	V _{CC}	102	V _{CC}	35	A4	119	A5	52	DQ18	136	DQ54	69	DQ28	153	DQ64
2	DQ0	86	DQ36	19	DQ14	103	DQ50	36	A6	120	A7	53	DQ19	137	DQ55	70	DQ29	154	DQ65
3	DQ1	87	DQ37	20	DQ15	104	DQ51	37	A8	121	A9	54	V _{SS}	138	V _{SS}	71	DQ30	155	DQ66
4	DQ2	88	DQ38	21	DQ16	105	DQ52	38	A10	122	A11R	55	DQ20	139	DQ56	72	DQ31	156	DQ67
5	DQ3	89	DQ39	22	DQ17	106	DQ53	39	NC	123	NC	56	DQ21	140	DQ57	73	V _{CC}	157	V _{CC}
6	V _{CC}	90	V _{CC}	23	V _{SS}	107	V _{SS}	40	V _{CC}	124	V _{CC}	57	DQ22	141	DQ58	74	DQ32	158	DQ68
7	DQ4	91	DQ40	24	NC	108	NC	41	NC	125	NC	58	DQ23	142	DQ59	75	DQ33	159	DQ69
8	DQ5	92	DQ41	25	NC	109	NC	42	NC	126	B0	59	V _{CC}	143	V _{CC}	76	DQ34	160	DQ70
9	DQ6	93	DQ42	26	V _{CC}	110	V _{CC}	43	V _{SS}	127	V _{SS}	60	DQ24	144	DQ60	77	DQ35	161	DQ71
10	DQ7	94	DQ43	27	WE0	111	NC	44	OE2	128	NC	61	NC	145	NC	78	V _{SS}	162	V _{SS}
11	DQ8	95	DQ44	28	CAS0	112	NC	45	RAS2	129	NC	62	NC	146	NC	79	PD0	163	PD1
12	V _{SS}	96	V _{SS}	29	NC	113	NC	46	CAS4	130	NC	63	NC	147	NC	80	PD2	164	PD3
13	DQ9	97	DQ45	30	RAS0	114	NC	47	NC	131	NC	64	NC	148	NC	81	PD4	165	PD5
14	DQ10	98	DQ46	31	OE0	115	NC	48	WE2	132	PDE	65	DQ25	149	DQ61	82	PD6	166	PD7
15	DQ11	99	DQ47	32	V _{SS}	116	V _{SS}	49	V _{CC}	133	V _{CC}	66	DQ26	150	DQ62	83	ID0	167	ID1
16	DQ12	100	DQ48	33	A0	117	A1	50	NC	134	NC	67	DQ27	151	DQ63	84	V _{CC}	168	V _{CC}
17	DQ13	101	DQ49	34	A2	118	A3	51	NC	135	NC	68	V _{SS}	152	V _{SS}				

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BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT	NOTES
V _{IN}	Input Voltage	- 0.3 to V _{CC} + 0.3	V	1
V _{OUT}	Output Voltage	- 0.3 to V _{CC} + 0.3	V	1
V _{CC}	Power Supply Voltage	- 0.3 to 4.6	V	1
T _{OPR}	Operating Temperature	0 to 70	°C	1
T _{STG}	Storage Temperature	- 55 to 125	°C	1
P _D	Power Dissipation	4.2	W	1
I _{OUT}	Short Circuit Output Current	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (Ta = 0° to 70°C)

SYMBOL	PARAMETER	MIN	TYP.	MAX	UNIT	NOTES
V _{CC}	Supply Voltage	3.13	3.3	3.47	V	2
V _{IH}	Input High Voltage	2.0	-	V _{CC} + 0.3*	V	2
V _{IL}	Input Low Voltage	- 0.3**	-	0.8	V	2

* V_{CC} + 1.2 V at pulse width ≤ 20 ns (pulse width is measured at V_{CC})

** - 1.2 V at pulse width ≤ 20 ns (pulse width is measured at V_{SS})

CAPACITANCE (V_{CC} = 3.3 V ± 5%, f = 1 MHz, Ta = 0° to 70°C)

SYMBOL	PARAMETER	MIN	MAX	UNIT
C _{I1}	Input Capacitance (B0, A0 to 10, A11R)	-	T.B.D.	pF
C _{I2}	Input Capacitance ($\overline{WE}0,2$)	-	T.B.D.	pF
C _{I3}	Input Capacitance ($\overline{RA}50,2$)	-	T.B.D.	pF
C _{I4}	Input Capacitance ($\overline{CA}50,4$)	-	T.B.D.	pF
C _{I5}	Input Capacitance ($\overline{OE}0,2$)	-	T.B.D.	pF
C _{I6}	Input Capacitance (\overline{PDE})	-	T.B.D.	pF
C _{DQ}	I/O Capacitance (DQ0 to 71)	-	T.B.D.	pF

DC CHARACTERISTICS ($V_{CC} = 3.3\text{ V} \pm 5\%$, $T_a = 0^\circ$ to 70°C)

SYMBOL	PARAMETER	MIN	MAX	UNIT	NOTES	
I _{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{\text{RAS}}$, $\overline{\text{CAS}}$, Address Cycling: $t_{RC} = t_{RC\text{ min}}$)	THMxxxxxx-4	-	1090	mA	3, 4, 5
		THMxxxxxx-5	-	910		
I _{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{\text{RAS}} = \overline{\text{CAS}} = V_{IH}$)	-	19	mA		
I _{CC3}	RAS-ONLY REFRESH CURRENT Average Power Supply Current, $\overline{\text{RAS}}$ -Only Mode ($\overline{\text{RAS}}$ Cycling, $\overline{\text{CAS}} = V_{IH}$; $t_{RC} = t_{RC\text{ min}}$)	THMxxxxxx-4	-	1090	mA	3, 5
		THMxxxxxx-5	-	910		
I _{CC4}	HYPER PAGE MODE CURRENT Average Power Supply Current, Hyper Page Mode ($\overline{\text{RAS}}$ $= \overline{\text{CAS}} = V_{IL}$, Address Cycling: $t_{HPC} = t_{HPC\text{ min}}$)	THMxxxxxx-4	-	820	mA	3, 4, 5
		THMxxxxxx-5	-	685		
I _{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{\text{RAS}} = \overline{\text{CAS}} = V_{CC} - 0.2\text{ V}$)	-	14.5	mA		
I _{CC6}	CAS-BEFORE-RAS REFRESH CURRENT Average Power Supply Current, $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ Mode ($\overline{\text{RAS}}$, $\overline{\text{CAS}}$ Cycling: $t_{RC} = t_{RC\text{ min}}$)	THMxxxxxx-4	-	1090	mA	3, 5
		THMxxxxxx-5	-	910		
I _{I(L)}	INPUT LEAKAGE CURRENT Input Leakage Current, Any Input ($0\text{ V} \leq V_{IN} \leq V_{CC}$, All Other Pins Not under Test = 0 V)	- 10	10	μA		
I _{O(L)}	OUTPUT LEAKAGE CURRENT (D_{OUT} Is Disabled, $0\text{ V} \leq V_{OUT} \leq V_{CC}$)	- 10	10	μA		
V _{OH}	OUTPUT LEVEL Output H Level Voltage ($I_{OUT} = -2\text{ mA}$)	2.4	-	V		
V _{OL}	OUTPUT LEVEL Output L Level Voltage ($I_{OUT} = 2\text{ mA}$)	-	0.4	V		

AC CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

($V_{CC} = 3.3\text{ V} \pm 5\%$, $T_a = 0^\circ$ to 70°C)

Please refer to DRAM MODULE AC CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS No. 45

DRAM MODULE AC CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS No.45

**TC5164405BJ/BFT/BJS/BFTS (BUFFER) USING MODULE
TC5165405BJ/BFT/BJS/BFTS (BUFFER) USING MODULE
TC5164805BJ/BFT/BJS/BFTS (BUFFER) USING MODULE
TC5165805BJ/BFT/BJS/BFTS (BUFFER) USING MODULE
TC5164165BFT/BFTS (BUFFER) USING MODULE
TC5165165BFT/BFTS (BUFFER) USING MODULE**

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AC CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

 ($V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$, $T_a = 0$ to 70°C) (Notes 6, 7, 8)

SYMBOL	PARAMETER					UNIT	NOTES
		-40		-50			
		MIN	MAX	MIN	MAX		
t_{RC}	Random Read or Write Cycle Time	69	-	84	-	ns	
t_{RMW}	Read-Modify-Write Cycle Time	102	-	121	-	ns	
t_{RAC}	Access Time from \overline{RAS}	-	40	-	50	ns	9, 14, 15
t_{CAC}	Access Time from \overline{CAS}	-	16	-	18	ns	9, 14
t_{AA}	Access Time from Column Address	-	25	-	30	ns	9, 15
t_{CPA}	Access Time from \overline{CAS} Precharge	-	27	-	33	ns	9
t_{CLZ}	\overline{CAS} to output in Low-Z	0	-	0	-	ns	
t_{OFF}	Output Buffer Turn-off Delay	0	16	0	18	ns	10, 16
t_T	Transition Time (Rise and Fall)	1	50	1	50	ns	8
t_{RP}	\overline{RAS} Precharge Time	25	-	30	-	ns	
t_{RAS}	\overline{RAS} Pulse Width	40	10,000	50	10,000	ns	
t_{RASP}	\overline{RAS} Pulse Width (Hyper Page Mode)	40	100,000	50	100,000	ns	
t_{RSH}	\overline{RAS} Hold Time	11	-	13	-	ns	
t_{RHCP}	\overline{RAS} Hold Time From \overline{CAS} Precharge (Hyper Page Mode)	27	-	33	-	ns	
t_{CSH}	\overline{CAS} Hold Time	30	-	35	-	ns	
t_{CAS}	\overline{CAS} Pulse Width	6	10,000	8	10,000	ns	
t_{RCD}	\overline{RAS} to \overline{CAS} Delay Time	10	24	12	32	ns	14
t_{RAD}	\overline{RAS} to Column Address Delay Time	8	15	10	20	ns	15
t_{CRP}	\overline{CAS} to \overline{RAS} Precharge Time	10	-	10	-	ns	
t_{CP}	\overline{CAS} Precharge Time	6	-	8	-	ns	
t_{ASR}	Row Address Set-Up Time	5	-	5	-	ns	
t_{RAH}	Row Address Hold Time	6	-	8	-	ns	
t_{ASC}	Column Address Set-Up Time	0	-	0	-	ns	
t_{CAH}	Column Address Hold Time	6	-	8	-	ns	
t_{RAL}	Column Address to \overline{RAS} Lead Time	25	-	30	-	ns	
t_{RCS}	Read Command Set-Up Time	0	-	0	-	ns	
t_{RCH}	Read Command Hold Time	0	-	0	-	ns	11
t_{RRH}	Read Command Hold Time referenced to \overline{RAS}	0	-	0	-	ns	11
t_{WCH}	Write Command Hold Time	6	-	8	-	ns	
t_{WP}	Write Command Pulse Width	6	-	8	-	ns	
t_{RWL}	Write Command to \overline{RAS} Lead Time	11	-	13	-	ns	
t_{CWL}	Write Command to \overline{CAS} Lead Time	6	-	8	-	ns	
t_{DS}	Data Set-Up Time	0	-	0	-	ns	12
t_{DH}	Data Hold Time	11	-	13	-	ns	12

AC CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS (Continued)

SYMBOL	PARAMETER					UNIT	NOTES
		-40		-50			
		MIN	MAX	MIN	MAX		
t _{REF}	Refresh Period	-	64	-	64	ms	
t _{REF}	Refresh Period (Self Refresh)	-	128	-	128	ms	
t _{WCS}	Write Command Set-Up Time	0	-	0	-	ns	13
t _{CWD}	CAS to WE Delay Time	36	-	40	-	ns	13
t _{RWD}	RAS to WE Delay Time	60	-	72	-	ns	13
t _{AWD}	Column Address to WE Delay Time	40	-	50	-	ns	13
t _{CPWD}	CAS Precharge to WE Delay Time	47	-	55	-	ns	13
t _{CSR}	CAS Set-Up Time (CAS before RAS Cycle)	10	-	10	-	ns	
t _{CHR}	CAS Hold Time (CAS before RAS Cycle)	6	-	8	-	ns	
t _{RPC}	RAS to CAS Precharge Time	5	-	5	-	ns	
t _{ROH}	RAS Hold Time referenced to OE	11	-	13	-	ns	
t _{OEa}	OE Access Time	-	16	-	18	ns	9
t _{OED}	OE to Data Delay	16	-	18	-	ns	
t _{OLZ}	OE to output in Low-Z	0	-	0	-	ns	
t _{OEZ}	Output buffer turn off Delay Time from OE	0	16	0	18	ns	10
t _{OEh}	OE Command Hold Time	6	-	8	-	ns	
t _{ODS}	Output Disable Set-Up Time	0	-	0	-	ns	
t _{WRP}	WE to RAS Precharge Time (CAS before RAS Cycle)	10	-	10	-	ns	
t _{WRH}	WE to RAS Hold Time (CAS before RAS Cycle)	6	-	8	-	ns	
t _{RNCD}	RAS to next CAS Delay Time (Hyper Page Mode)	40	-	50	-	ns	
t _{HPC}	Hyper Page Mode Cycle Time	16	-	20	-	ns	
t _{HPRWC}	Hyper Page Mode Read-Modify-Write Cycle Time	47	-	57	-	ns	
t _{COH}	Output Data Hold Time	5	-	5	-	ns	
t _{REZ}	Output Buffer Turn-off Delay from RAS	0	11	0	13	ns	10, 16
t _{WEZ}	Output Buffer Turn-off Delay from WE	0	16	0	18	ns	10
t _{WED}	WE to Data Delay	16	-	18	-	ns	
t _{OE}	OE Pulse Width	11	-	13	-	ns	
t _{OEP}	OE Precharge Time	6	-	8	-	ns	
t _{CPO}	CAS to OE Precharge Time	5	-	5	-	ns	
t _{OCH}	CAS Hold Time referenced to OE	6	-	8	-	ns	
t _{RASS}	RAS Pulse Width (CAS before RAS Self Refresh)	100	-	100	-	μs	
t _{RPS}	RAS Precharge Time (CAS before RAS Self refresh)	69	-	84	-	ns	
t _{CHS}	CAS Hold Time (CAS before RAS Self refresh)	-50	-	-50	-	ns	
t _{PD}	PDE to Presence Detect Data in Low-Z	-	10	-	10	ns	
t _{PDoff}	Presence Detect Data turn off Delay Time from PDE	1	-	1	-	ns	

NOTES:

1. Conditions outside the limits listed under “Absolute Maximum Ratings” may cause permanent damage to the device.
2. All voltages are referenced to V_{SS} .
3. I_{CC1} , I_{CC3} , I_{CC4} and I_{CC6} depend on the cycle rate.
4. I_{CC1} and I_{CC4} depend on output loading. Specified values are obtained with the output open.
5. The address can be changed once at most while $\overline{RAS}=V_{IL}$. In the case of I_{CC4} , it can be changed once at most during a Hyper Page Mode cycle (t_{HPC}).
6. An initial pause of $200\mu s$ is required after power-up followed by a minimum of eight \overline{RAS} -Only refresh cycles before proper device operation is achieved. When using the internal refresh counter, a minimum of eight \overline{CAS} -before- \overline{RAS} refresh cycles instead of eight \overline{RAS} -Only refresh cycles is required.
7. AC measurements assume $t_T=2ns$.
8. V_{IH} (min) and V_{IL} (max) are reference levels for measuring the timing of input signals. Also, transition times are measured between the V_{IH} and V_{IL} levels.
9. This is measured with a load equivalent to $100pF$ at $V_{OH} = 2.0V$ ($I_{OUT} = -2mA$), $V_{OL} = 0.8V$ ($I_{OUT} = 2mA$).
10. t_{OFF} (max), t_{OEZ} (max), t_{REZ} (max) and t_{WEZ} (max) define the time at which the output goes open circuit and are not referenced to output voltage levels.
11. Either t_{RCH} or t_{RRH} must be satisfied for a Read cycle.
12. These parameters are referenced to the leading edge of \overline{CAS} in Early Write cycles and to the leading edge of \overline{WE} in Read-Modify-Write cycles.
13. t_{WCS} , t_{RWD} , t_{CWD} , t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}(\min)$, the cycle is an Early Write cycle and the Data-out pin will remain open circuit (high impedance) throughout the entire cycle. If $t_{RWD} \geq t_{RWD}(\min)$, $t_{CWD} \geq t_{CWD}(\min)$, $t_{AWD} \geq t_{AWD}(\min)$ and $t_{CPWD} \geq t_{CPWD}(\min)$ (Hyper Page mode), the cycle is a Read-Modify-Write cycle and the data output will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the data output (at access time) is indeterminate.
14. Operation within the $t_{RCD}(\max)$ limit ensures that $t_{RAC}(\max)$ can be met.
 $t_{RCD}(\max)$ is specified as a reference point only; if t_{RCD} is greater than the specified $t_{RCD}(\max)$ limit, then the access time is determined by t_{CAC} .
15. Operation within the $t_{RAD}(\max)$ limit ensures that $t_{RAC}(\max)$ can be met.
 $t_{RAD}(\max)$ is specified as a reference point only; if t_{RAD} is greater than the specified $t_{RAD}(\max)$ limit, then the access time is determined by t_{AA} .
16. If \overline{RAS} goes high before \overline{CAS} goes high, the output goes open circuit when \overline{CAS} goes high (t_{OFF}).
If \overline{CAS} goes high before \overline{RAS} goes high, the output goes open circuit when \overline{RAS} goes high (t_{REZ}).

DATA-OUT HI-Z CONTROL LOGIC

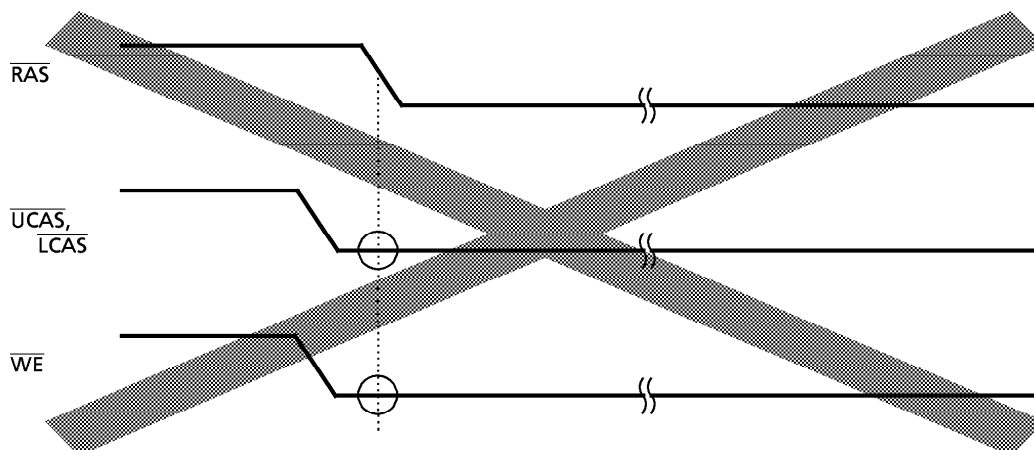
RAS	UCAS, LCAS	OE	WE	Timing Specification
H		L	H	t _{OFF}
	H	L	H	t _{REZ}
L	L		H	t _{OEZ}
L	H	L		t _{WEZ}

DATA-OUT LO-Z CONTROL LOGIC

RAS	UCAS, LCAS	OE	WE	Timing Specification
L		L	H	t _{CLZ}
L	L		H	t _{OLZ}
L	L		H	t _{OLZ}

CAUTION

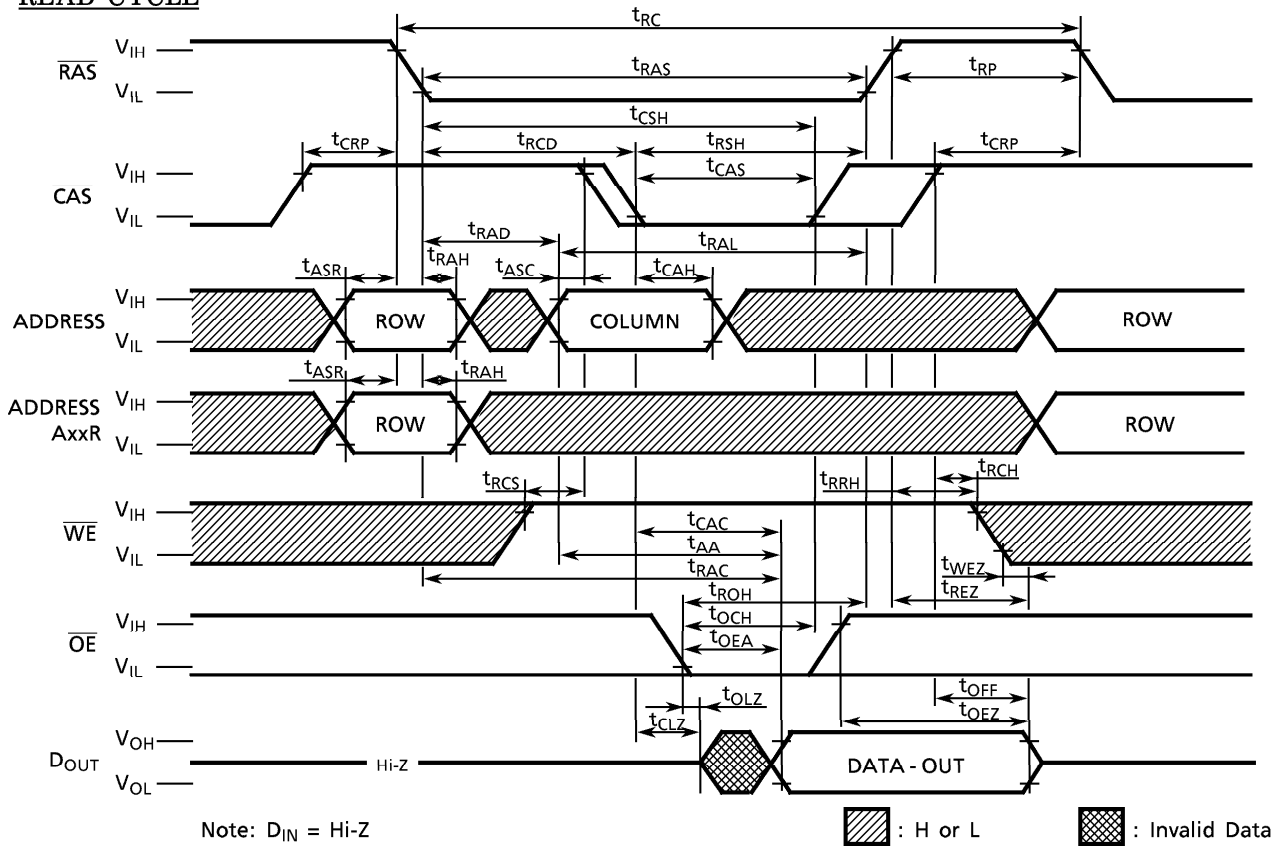
The WCBR (\overline{WE} , \overline{CAS} -before- \overline{RAS}) timing shown below is not allowed during normal operation, such as during Read, Write and Refresh operations. When WCBR is input, a malfunction may occur due to the change in internal circuit operation status.



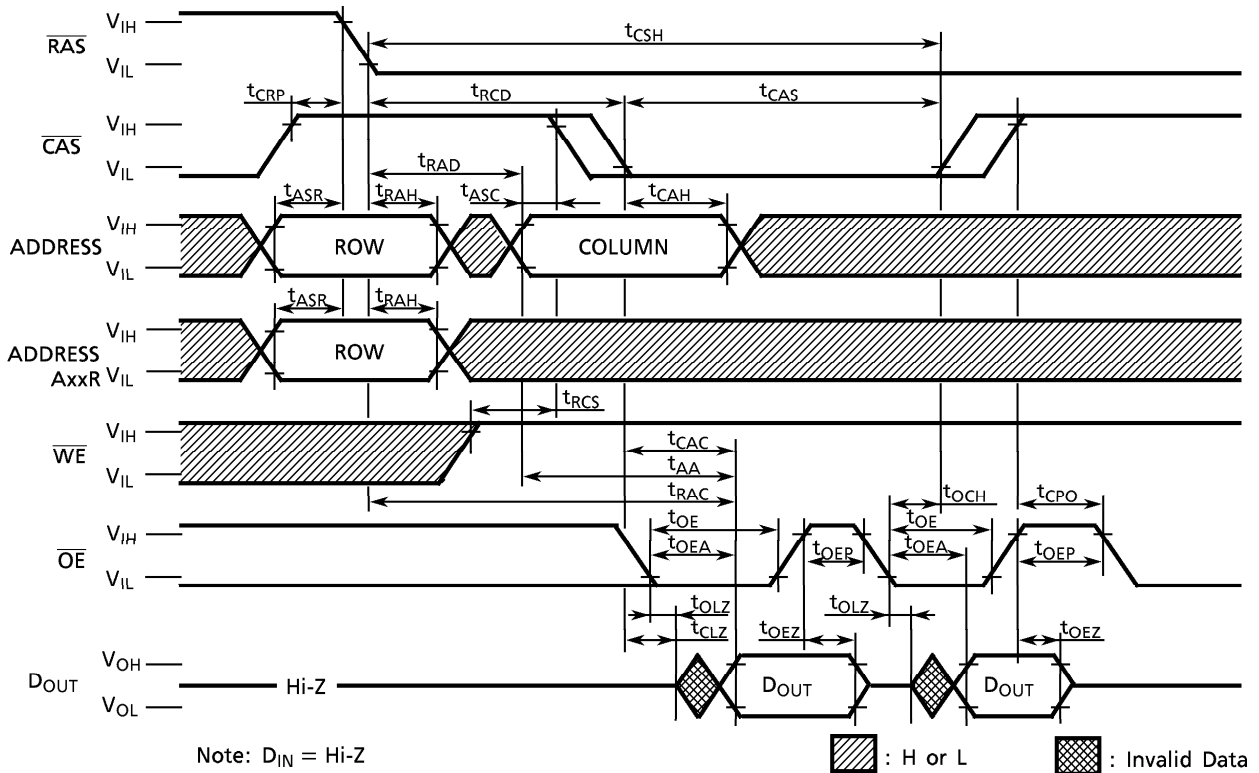
WCBR timing

TIMING DIAGRAMS

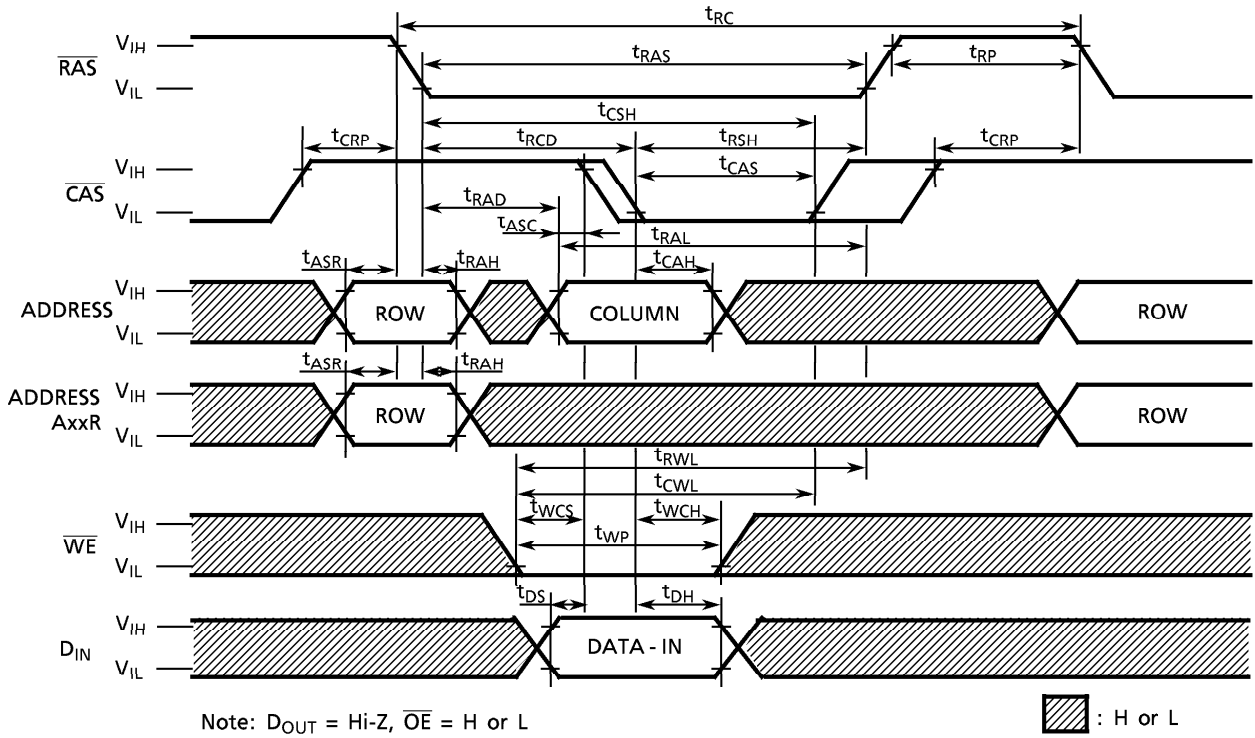
READ CYCLE



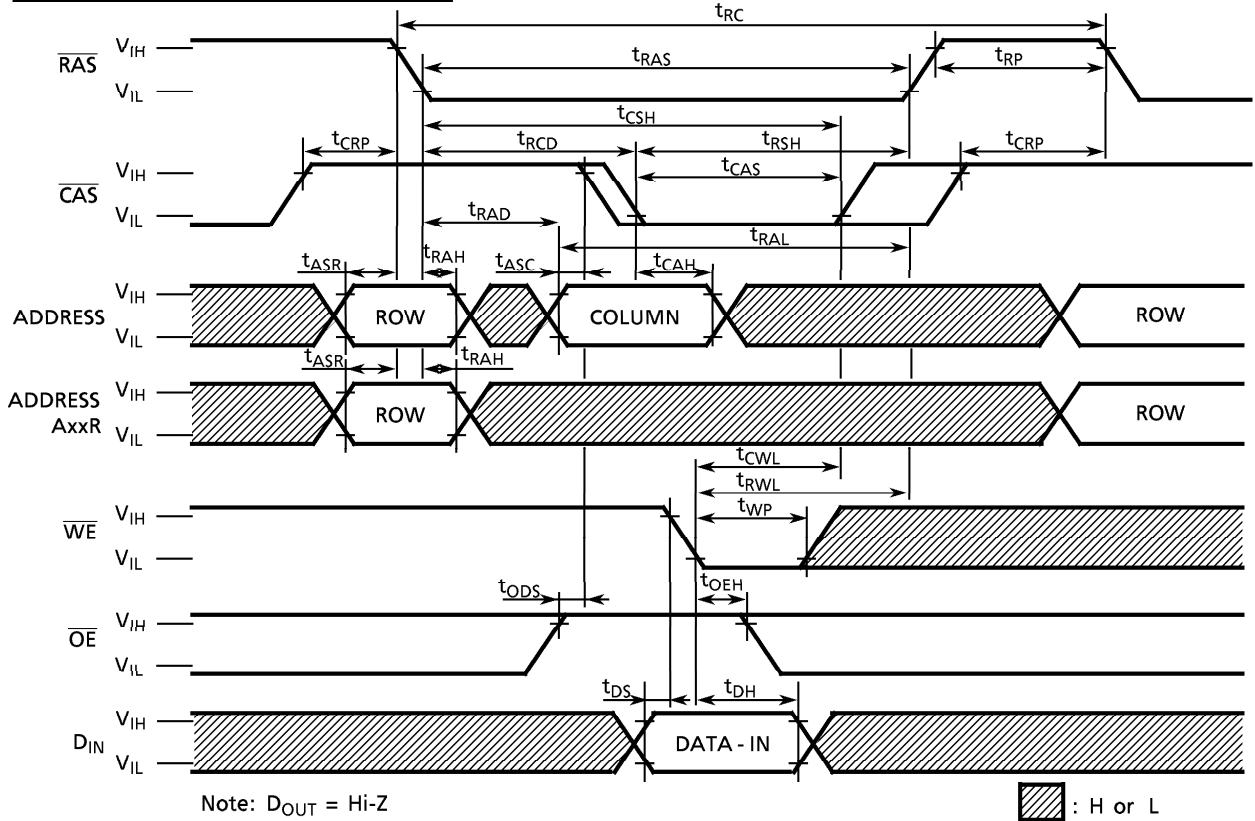
\overline{OE} -CONTROLLED READ CYCLE



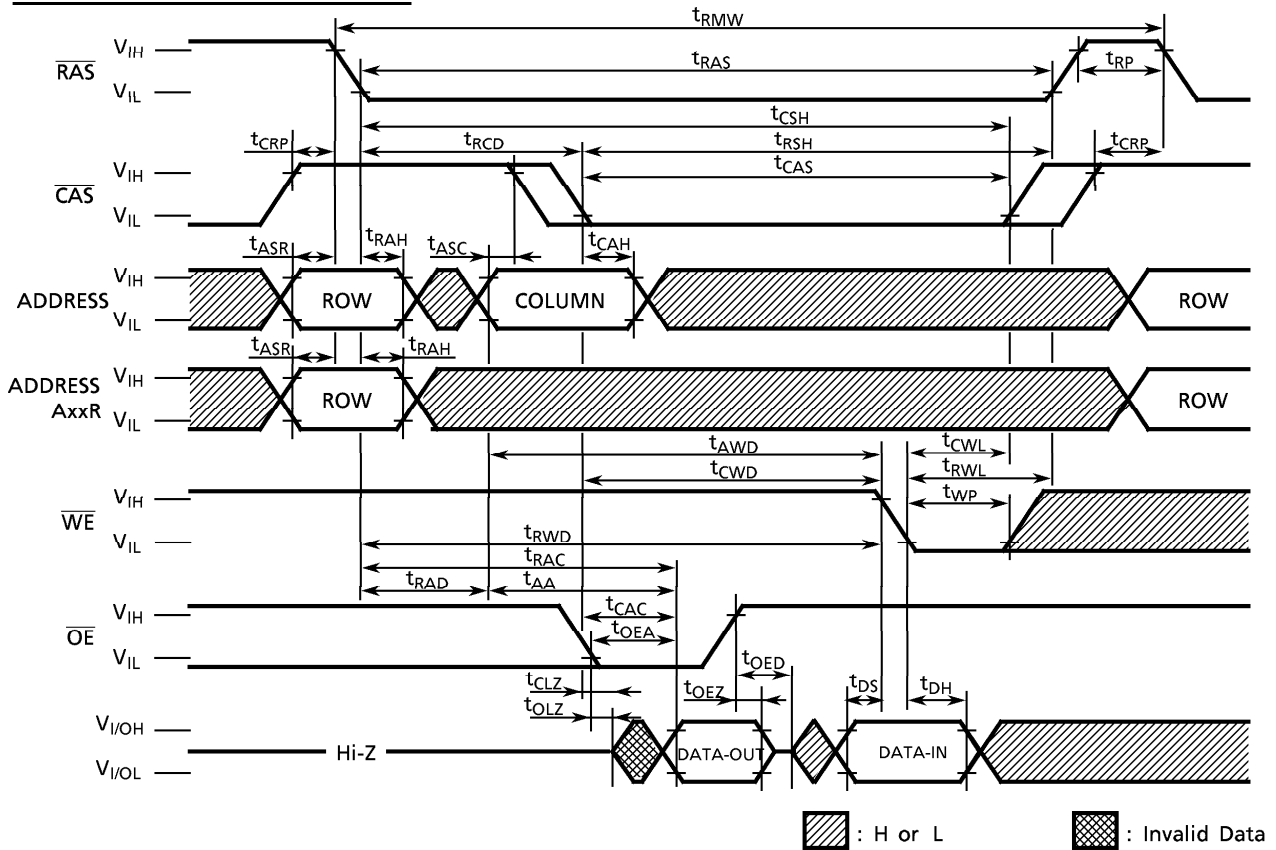
WRITE CYCLE (EARLY WRITE)



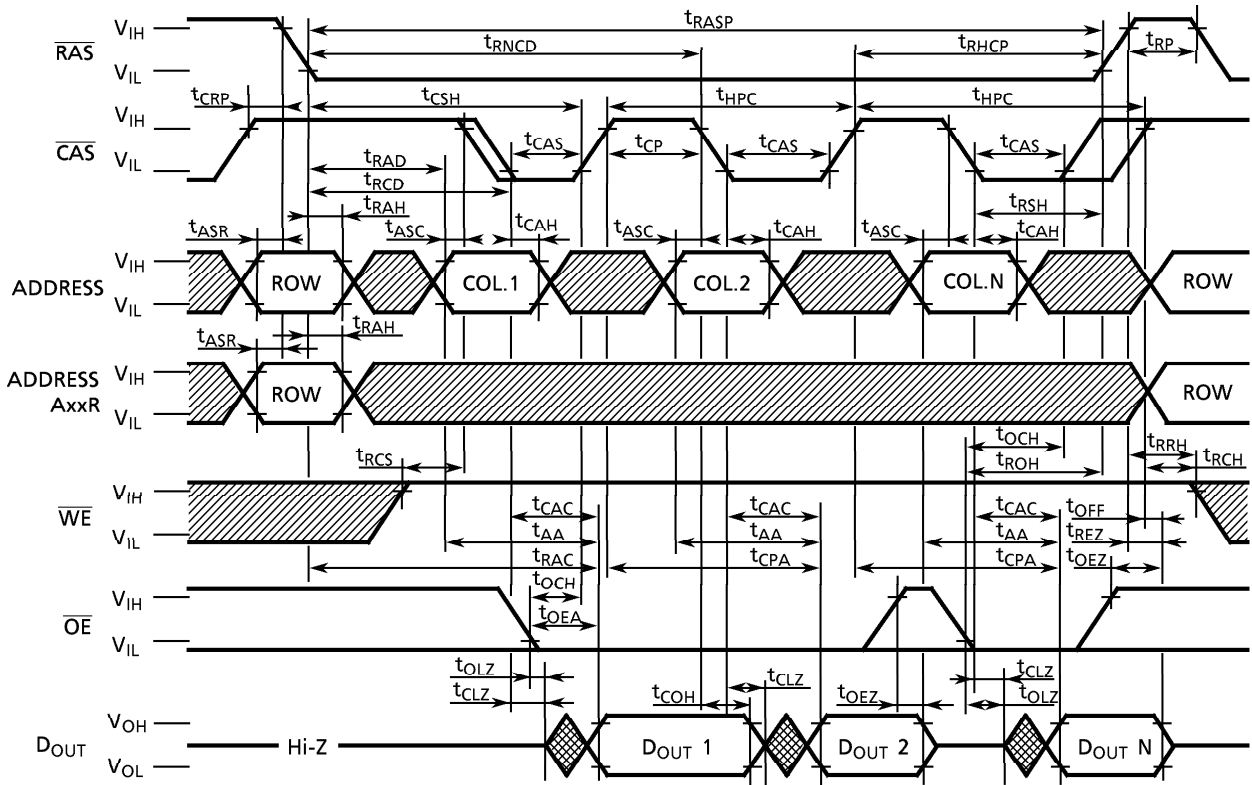
\overline{OE} -CONTROLLED WRITE CYCLE



READ-MODIFY-WRITE CYCLE



HYPER PAGE MODE READ CYCLE

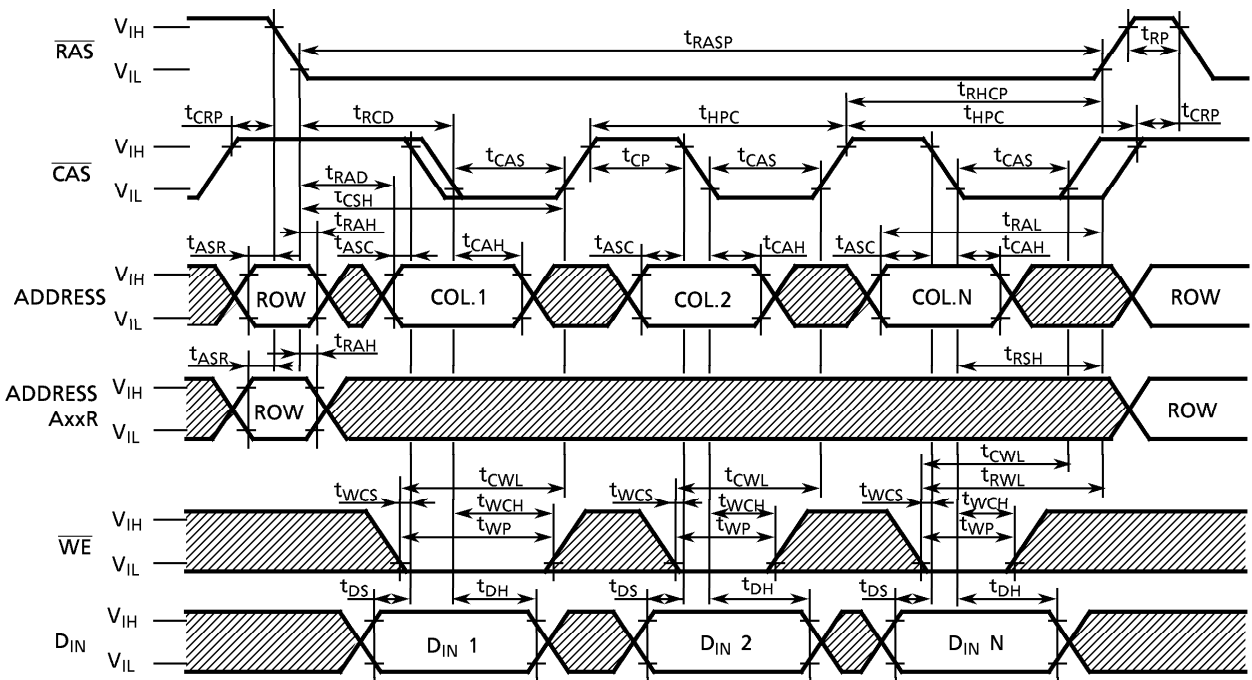


Note: $D_{\text{IN}} = \text{Hi-Z}$

▨ : H or L

▩ : Invalid Data

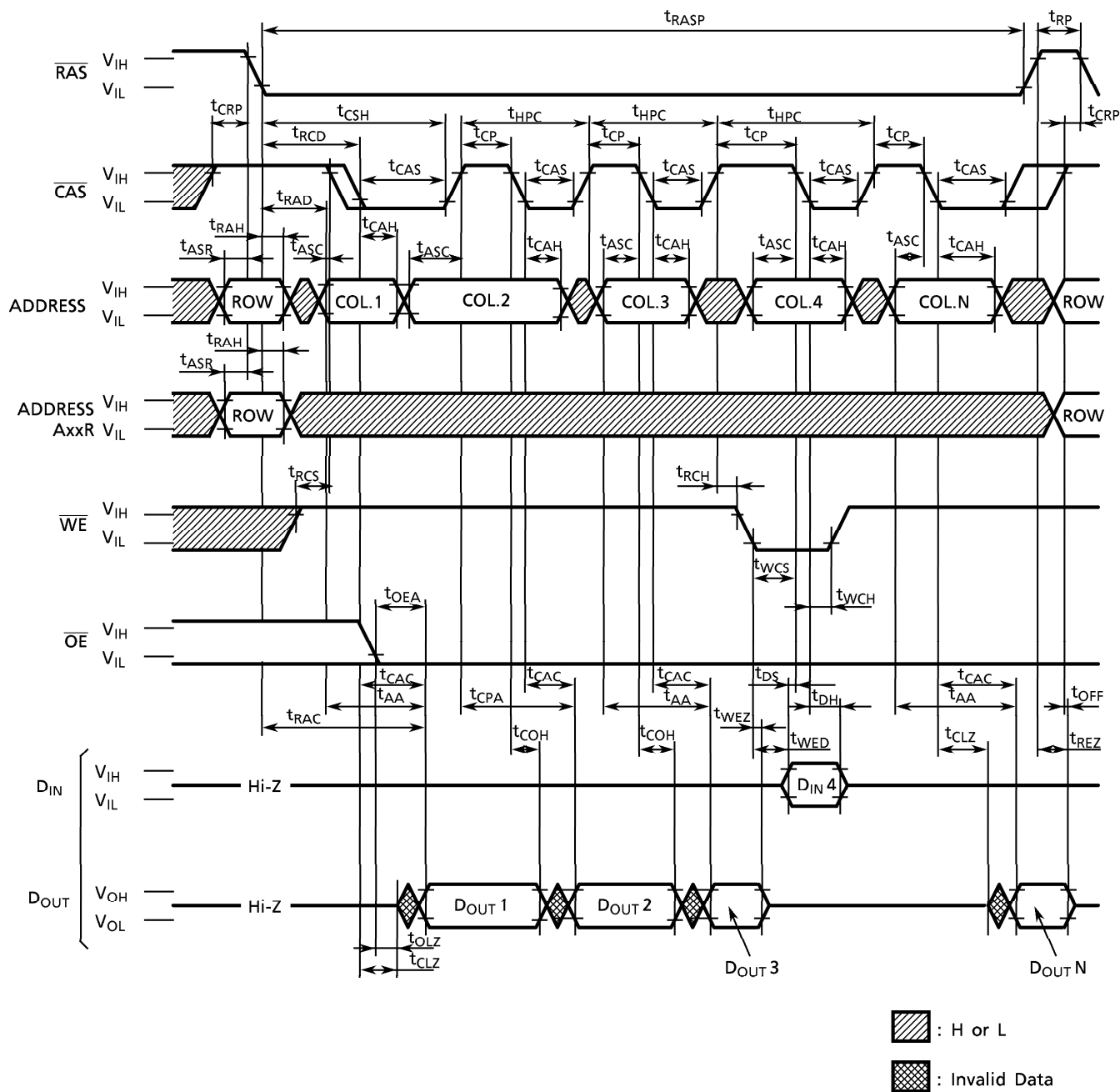
HYPER PAGE MODE WRITE CYCLE (EARLY WRITE)



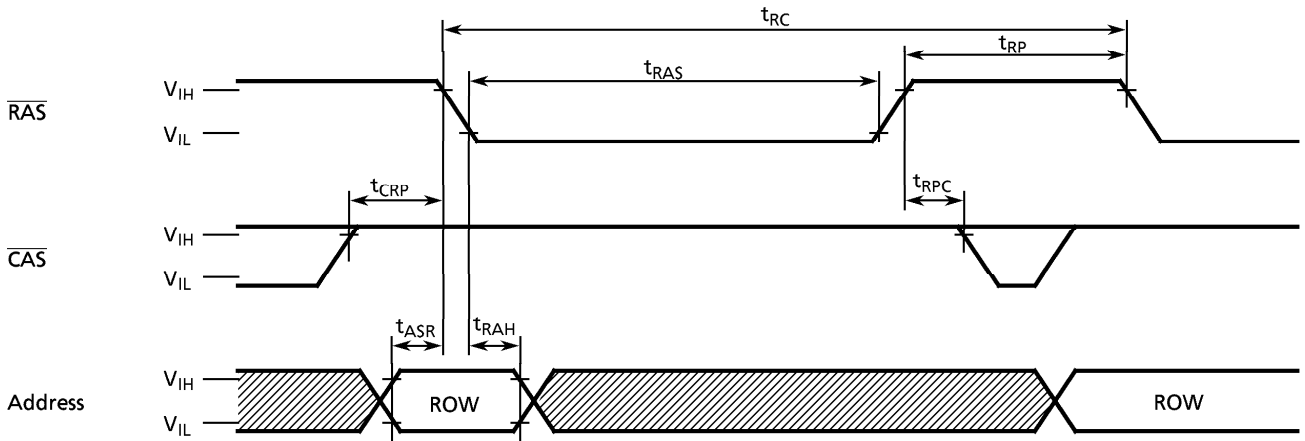
Note: $D_{\text{OUT}} = \text{Hi-Z}$, $\overline{\text{OE}} = \text{H or L}$

▨ : H or L

HYPER PAGE MODE READ WRITE MIXED CYCLE



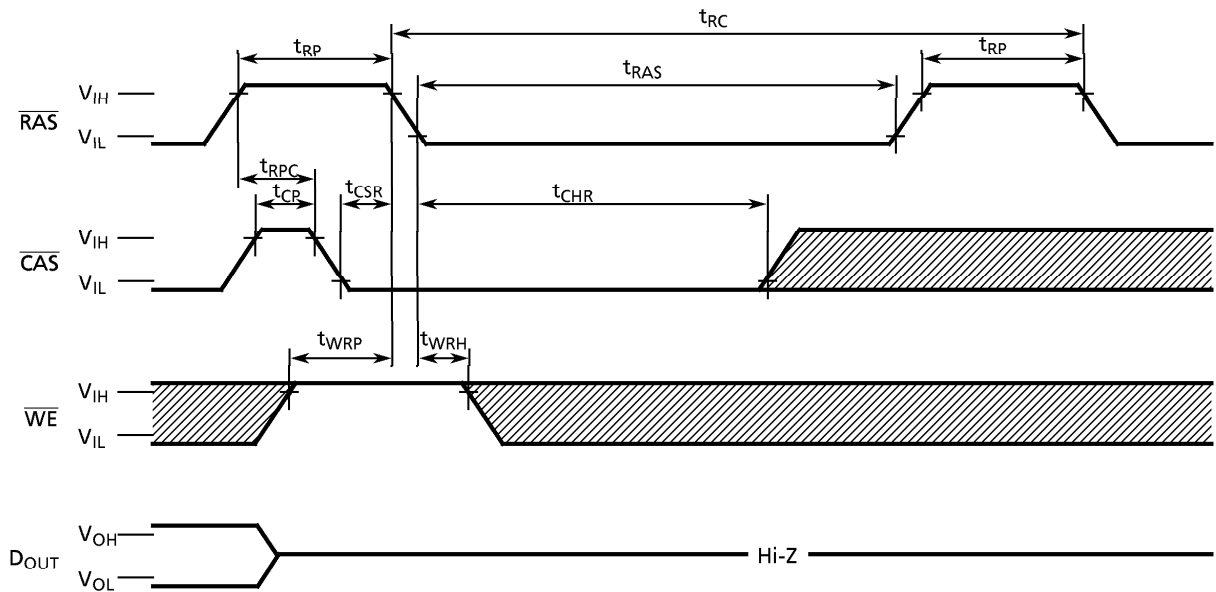
RAS-ONLY REFRESH CYCLE



Note: $\overline{\text{WE}}$, $\overline{\text{OE}}$ and $D_{IN} = \text{H or L}$

: H or L

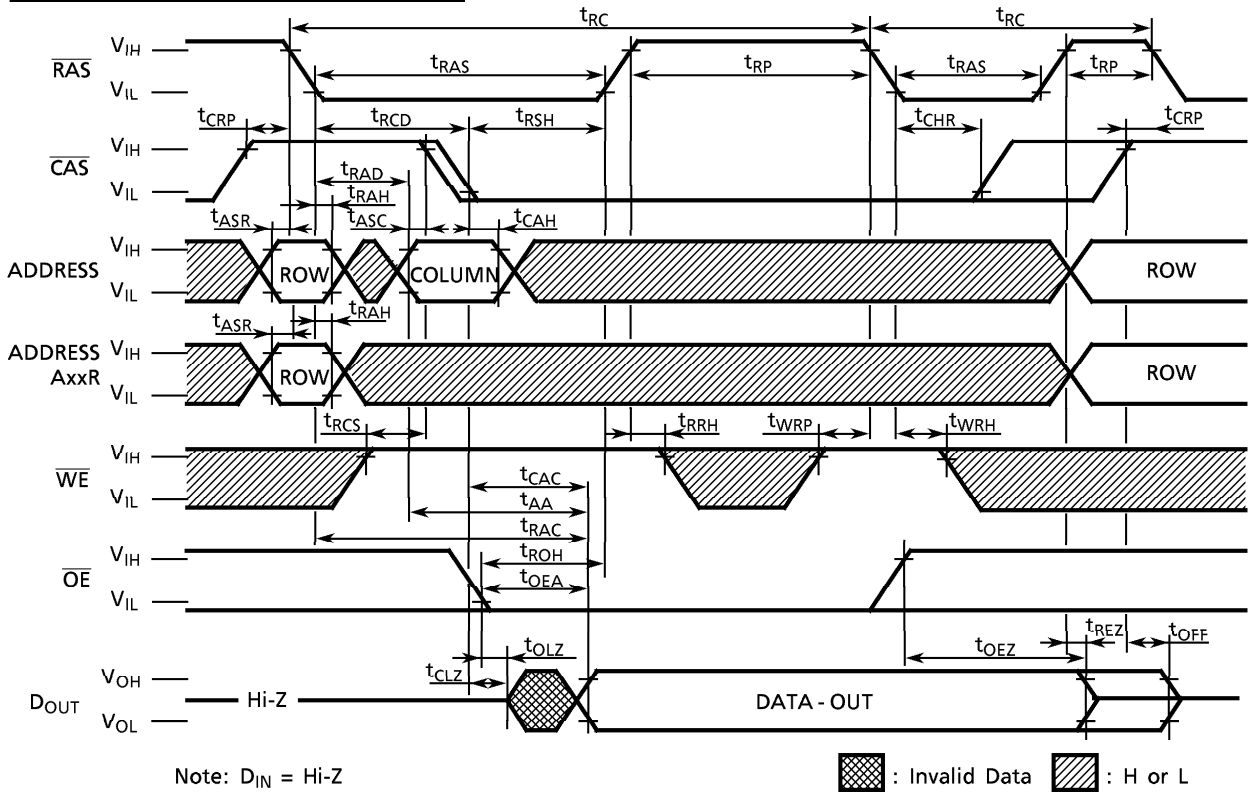
CAS-BEFORE-RAS REFRESH CYCLE



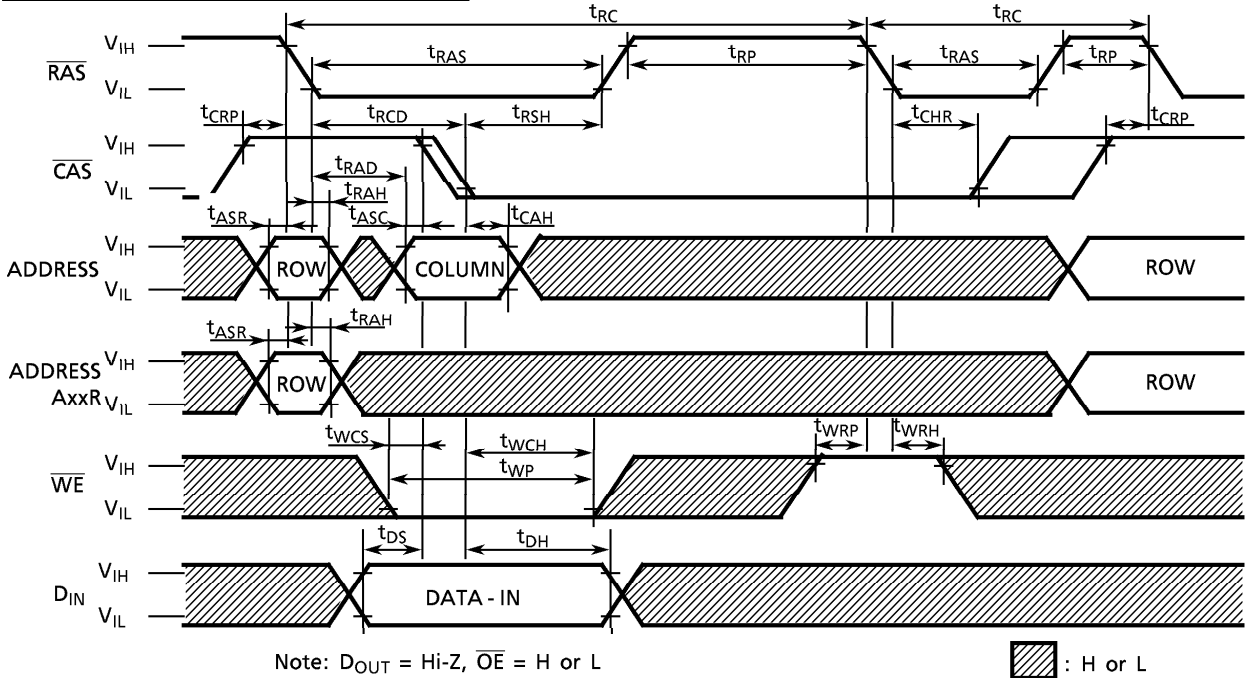
Note: D_{IN} , $\overline{\text{OE}}$, ADDRESS = H or L

: H or L

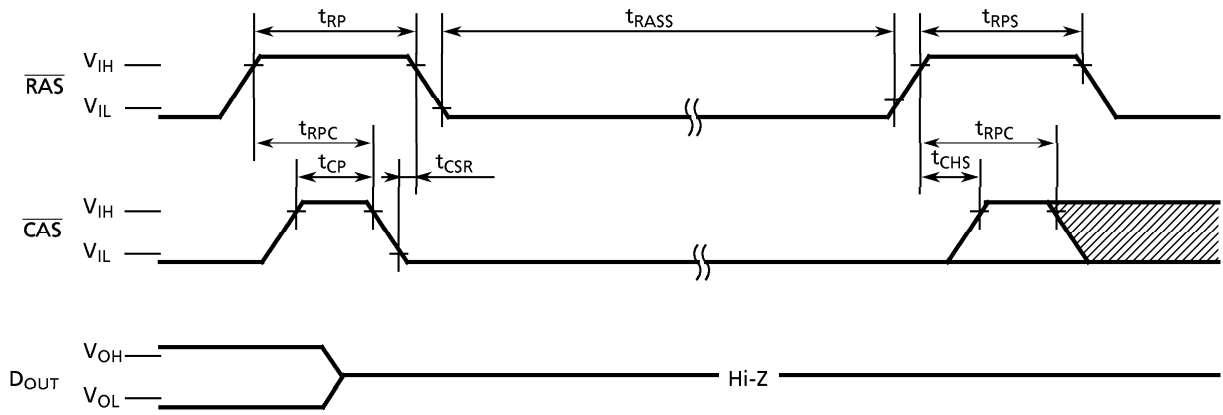
HIDDEN REFRESH CYCLE (READ)




HIDDEN REFRESH CYCLE (WRITE)



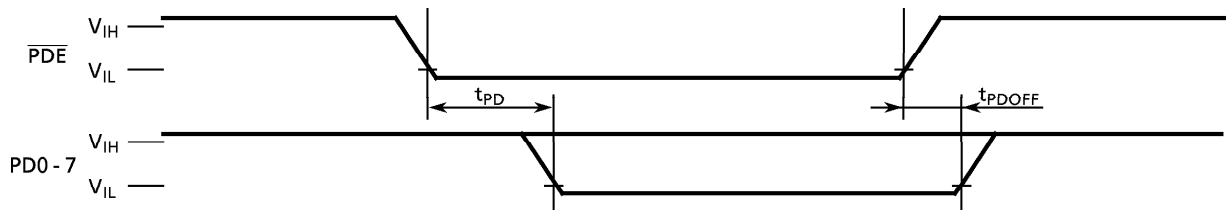
CAS-BEFORE-RAS SELF-REFRESH CYCLE (THL64VxxxxBTG-xS only)



Note: D_{IN} , \overline{WE} , \overline{OE} , ADDRESS = H or L

 : H or L

PRESENCE DETECT DATA READ CYCLE



Note: t_{PDOFF} is measured with PD pin pulled V_{CC} .