3-2 LCD Controllers/Interfaces

■ Video to LCD interfaces

Video to LCD interfaces convert separated CRT video signals into the data and control signals for dot-matrix LCD drivers.

SED1341F0C/0E

The SED1341F0C/0E supports PLL dot clock generation and generates an on/off display.

Features

- PLL dot clock generation
- Internal power-on clear function
- Display memory management (VRAM) of 16 to 40 Kbytes

SED1345F0A

The SED1345F0A uses an on-chip programmable palette to reproduce color in eight levels of gray.

Features

- CGA and EGA mode capability
- 8-level gray-scale display of IRGB video data
- Programmable internal color palette for optimum selection of gray scale levels
- Display memory management (VRAM) from 16 to 40 Kbytes
- 30 MHz maximum dot clock frequency

Part number	Display area (pixels)	Gray-scale level	Frame frequency	Package	Evaluation board
SED1341F0C	640X200/350/400/480	2 or 3	Adjusts automatically to the screen size.	QFP5-80pin	SDU1341B0C
SED1341F0E	640X200/350/400/480 720X350/400/480	2		QFP5-80pin	SDU1341B0E
SED1345F0A	640X200/350/400/480	8	Synchronizes to the video signal frequency.	QFP5-80pin	SDU1345B0A