FEATURES

- DUAL POSITIVE-LOGIC NAND TTL-TO-MOS DRIVER
- VERSATILE INTERFACE CIRCUIT FOR USE BETWEEN TTL AND HIGH-CURRENT, HIGH-VOLTAGE SYSTEMS
- CAPABLE OF DRIVING HIGH-CAPACITANCE LOADS
- COMPATIBLE WITH MANY POPULAR MOS RAMs
- V_{CC2} SUPPLY VOLTAGE VARIABLE OVER WIDE RANGE TO 24 VOLTS MAXIMUM
- TTL AND DTL COMPATIBLE DIODE-CLAMPED INPUTS
- OPERATES FROM STANDARD BIPOLAR AND MOS SUPPLY VOLTAGES
- HIGH-SPEED SWITCHING
- TRANSIENT OVERDRIVE MINIMIZES POWER DISSIPATION
- LOW STANDBY POWER DISSIPATION

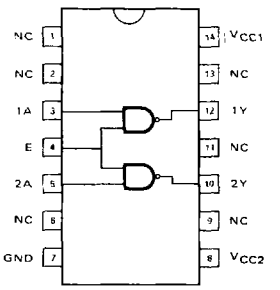
ABSOLUTE MAXIMUM RATINGS

Supply voltage range of V_{CC1} (Note 1)	−0.5V to 7V
Supply voltage range of V_{CC2}	−0.5V to 25V
Input voltage	5.5V
Inter-input voltage (Note 2)	5.5V
Continuous total dissipation at (or below) 25°C free-air temperature (Note 3):	
F package	1300mW
V package	1000mW
Operating free-air terperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds: F package	300°C
Lead temperature 1/16 inch from case for 10 seconds: V package	260°C

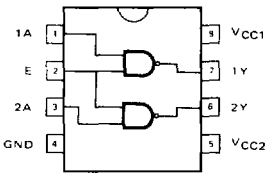
NOTES:
1. Voltage values are with respect to network ground terminal.
2. This rating applies between the A input of either driver and the common E input.
3. For operation above 25°C free-air temperature, refer to Dissipation Derating Curve, Figure 17.

PIN CONFIGURATION

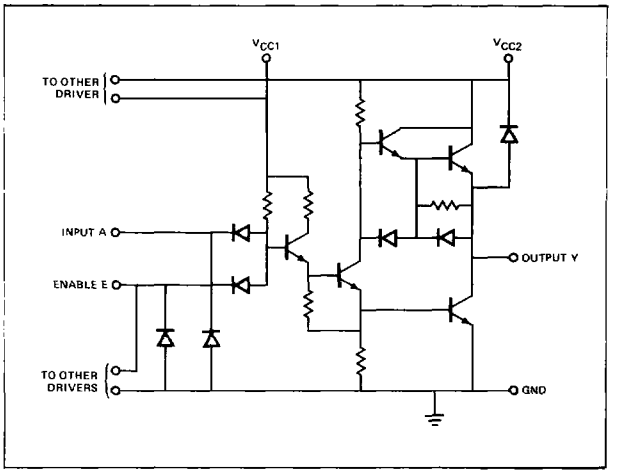
F PACKAGE



V PACKAGE



SCHEMATIC (EACH DRIVER)

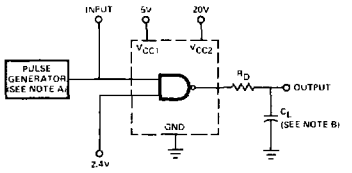


SWITCHING CHARACTERISTICS, V_{CC1} = 5V, V_{CC2} = 20V, TA = 25°C

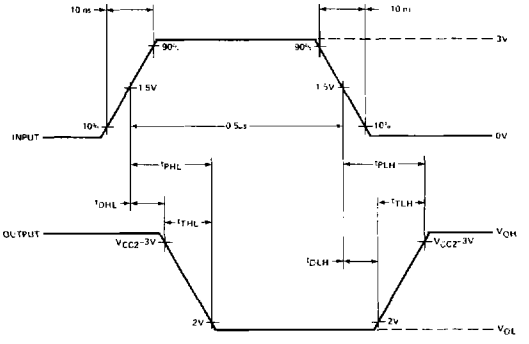
PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
t_{DLH}	Delay time, low-to-high-level output	C_L = 390pF, R_D = 10Ω See Figure 1, Unused gate input grounded		11	20	ns
t_{DHL}	Delay time, high-to-low-level output			10	18	ns
t_{TLH}	Transition time, low-to-high-level output			25	40	ns
t_{THL}	Transition time, high-to-low-level output			21	35	ns
t_{PLH}	Propagation delay time, low-to-high-level output		10	36	55	ns
t_{PHL}	Propagation delay time, high-to-low-level output		10	31	47	ns

PARAMETER MEASUREMENT INFORMATION

TEST CIRCUIT



VOLTAGE WAVEFORM



NOTES:
A. THE PULSE GENERATOR HAS THE FOLLOWING CHARACTERISTICS: PRR = 1MHz, Z_{OUT} = 50Ω
B. C_L INCLUDES PROBE AND JIG CAPACITANCE

FIGURE 1—SWITCHING TIMES, EACH DRIVER

DESIGN PRECAUTIONS

– USE OF DAMPING RESISTOR TO REDUCE OR ELIMINATE OUTPUT TRANSIENT OVERSHOOT IN CERTAIN 75361A APPLICATIONS

The fast switching speeds of this device may produce undesirable output transient overshoot because of load or wiring inductance. A small series damping resistor may be used to reduce or eliminate this output transient overshoot. The optimum value of the damping resistor to use depends on the specific load characteristics and switching speed. A typical value would be between 10Ω and 30Ω. See Figure 13.

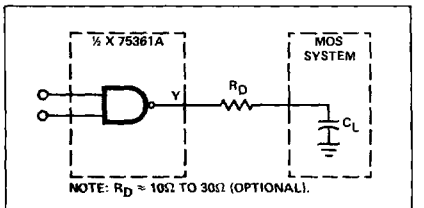


FIGURE 13

POWER DISSIPATION PRECAUTIONS

Significant power may be dissipated in the 75361A driver when charging and discharging high-capacitance loads over a wide voltage range at high frequencies. Figure 5 shows the power dissipated in a typical 75361A as a function of load capacitance and frequency. Average power dissipated by this driver can be broken into three components:

$$P_{T\,(AV)} = P_{DC(AV)} + P_{C(AV)} + P_{S(AV)}$$

where $P_{DC(AV)}$ is the steady-state power dissipation with the output high or low, $P_{C(AV)}$ is the power level during charging or discharging of the load capacitance, and $P_{S(AV)}$ is the power dissipation during switching between the low and high levels. None of these include energy transferred to the load and all are averaged over a full cycle.

The power components per driver channel are:

$$P_{DC(AV)} = \frac{PL\ t_L + PH\ t_H}{T}$$

$$P_{C(AV)} \approx C\ V_C^2\ f$$

$$P_{S(AV)} = \frac{PLH\ t_{LH} + PHL\ t_{HL}}{T}$$

where the times are as defined in Figure 14.

PL, PH, PLH, and PHL are the respective instantaneous levels of power dissipation and C is load capacitance.

The 75361A is so designed that P_S is a negligible portion of P_T in most applications. Except at very high frequencies, $t_L + t_H \gg t_{LH} + t_{HL}$ so that P_S can be neglected. Figure 5 for no load demonstrates this point. The power dissipation contributions from both channels are then added together to obtain total device power.

The following example illustrates this power calculation technique. Assume both channels are operating identically with C = 200pF, f = 2MHz, V_{CC1} = 5V, V_{CC2} = 20V, and duty cycle = 60% outputs high (t_H/T = 0.6). Also, assume V_{OH} = 19.3V, V_{OL} = 0.1V, PS is negligible, and that the current from V_{CC2} is negligible when the output is high.

On a per-channel basis using data sheet values:

$$P_{DC(AV)} = \left[(5V)\left(\frac{2mA}{2}\right) + (20V)\left(\frac{0mA}{2}\right)\right](0.6) + \left[(5V)\left(\frac{16mA}{2}\right) + (20V)\left(\frac{7mA}{2}\right)\right](0.4)$$

$P_{DC(AV)}$ = 47mW per channel

$P_{C(AV)} \approx$ (200pF) (19.2V)² (2MHz)

$P_{C(AV)} \approx$ 148mW per channel.

For the total device dissipation of the two channels:

$P_{T(AV)} \approx 2\ (47 + 148)$

$P_{T(AV)} \approx$ 390mW typical for total package.

VOLTAGE WAVEFORM

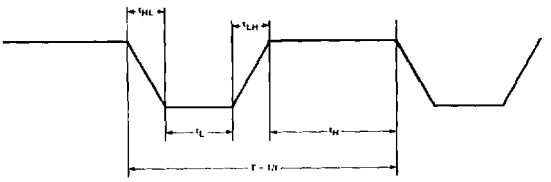


FIGURE 14—OUTPUT VOLTAGE WAVEFORM