

FEATURES

- Monolithic CMOS Construction
- Full Four-Quadrant Multiplication
- Excellent Stability Over Temperature and Time
- TTL/5 V CMOS Compatible
- Guaranteed Monotonic
- Low Sensitivity to Output Amplifier Vos
- Low Glitch Energy
- Buffered Version: MP7626
- 5 V Version: MP7616B

GENERAL DESCRIPTION

The MP7616 is a high density 16-bit CMOS multiplying Digital-to-Analog Converter. Silicon nitride passivation and untrimmed silicon chromium resistors have been combined to provide long term stability and reliability. Using the most significant bit (MSB) segmentation technique, the MP7616 features 13-bit (0.012%) differential and 12-bit (0.01%) integral linearity.

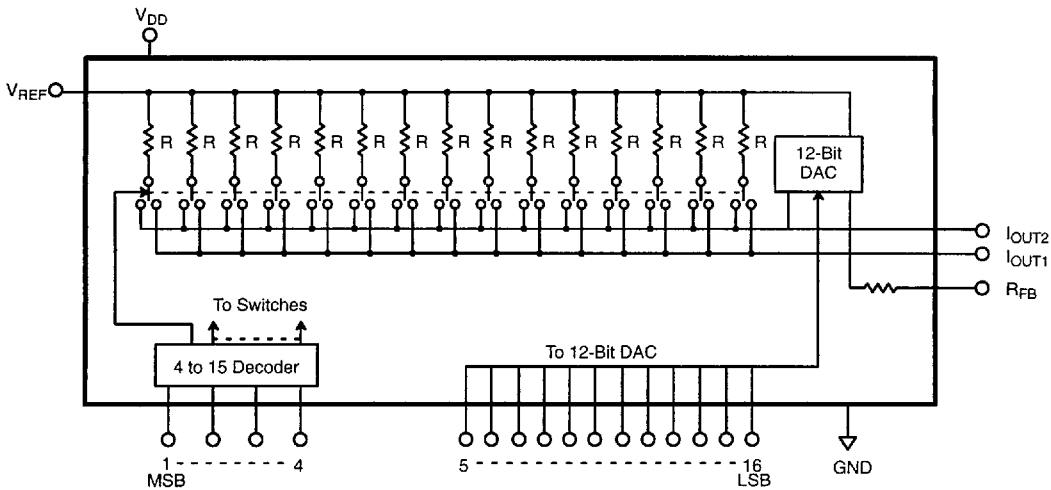
To achieve 13-bit linearity without laser trim, the MP7616 digitally decodes the four MSB's into 15 equal current sources,

rather than the standard binary-weighted sources. Each resistor contributes only 1/16 full scale output thus reducing the matching accuracy requirement of the resistor and CMOS switches from 0.0015% to 0.024%.

The decoding technique achieves an eightfold improvement in differential linearity stability over temperature, an eightfold improvement in relative accuracy due to aging effects (long term stability), a fourfold improvement in glitch amplitude, and a tenfold reduction in sensitivity to output amplifier offset voltage.

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SIMPLIFIED BLOCK DIAGRAM



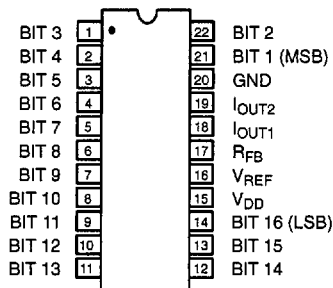
ORDERING INFORMATION

Package Type	Temperature Range	Part No.	INL (LSB)	DNL (LSB)	Gain Error (% FSR)
Plastic Dip	-40 to +85°C	MP7616JN	±14	±16	±0.8
Plastic Dip	-40 to +85°C	MP7616KN	±7	±8	±0.8
SOIC	-40 to +85°C	MP7616JS	±14	±16	±0.8
SOIC	-40 to +85°C	MP7616KS	±7	±8	±0.8
Ceramic Dip	-40 to +85°C	MP7616JD	±14	±16	±0.8
Ceramic Dip	-40 to +85°C	MP7616KD	±7	±8	±0.8
Ceramic Dip	-55 to +125°C	MP7616TD*	±7	±8	±0.8

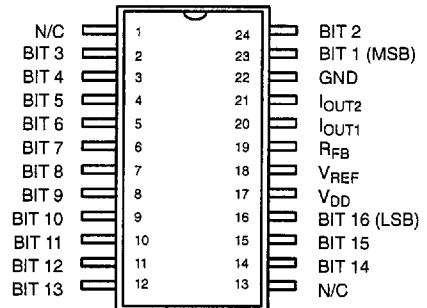
*Contact factory for non-compliant military processing

PIN CONFIGURATION

See Packaging Section for Package Dimensions



22 Pin CDIP, PDIP (0.400")
D22, N22



24 Pin SOIC (Jedec, 0.300")
S24

PIN OUT DEFINITIONS

DIP	SOIC	NAME	DESCRIPTION
	1	N/C	No Connection
1	2	BIT 3	Data Input Bit 3
2	3	BIT 4	Data Input Bit 4
3	4	BIT 5	Data Input Bit 5
4	5	BIT 6	Data Input Bit 6
5	6	BIT 7	Data Input Bit 7
6	7	BIT 8	Data Input Bit 8
7	8	BIT 9	Data Input Bit 9
8	9	BIT 10	Data Input Bit 10
9	10	BIT 11	Data Input Bit 11
10	11	BIT 12	Data Input Bit 12
11	12	BIT 13	Data Input Bit 13

DIP	SOIC	NAME	DESCRIPTION
	13	N/C	No Connection
12	14	BIT 14	Data Input Bit 14
13	15	BIT 15	Data Input Bit 15
14	16	BIT 16	Data Input Bit 16 (LSB)
15	17	V _{DD}	Positive Power Supply
16	18	V _{REF}	Reference Input Voltage
17	19	R _{FB}	Internal Feedback Resistor
18	20	I _{OUT1}	Current Output 1
19	21	I _{OUT2}	Current Output 2
20	22	GND	Ground
21	23	BIT 1	Data Input Bit 1 (MSB)
22	24	BIT 2	Data Input Bit 2

ELECTRICAL CHARACTERISTICS

($V_{DD} = +15\text{ V}$, $V_{REF} = +10\text{ V}$ unless otherwise noted)

Parameter	Symbol	25°C			Tmin to Tmax		Units	Test Conditions/Comments
		Min	Typ	Max	Min	Max		
STATIC PERFORMANCE¹								
Resolution (All Grades)	N	16			16		Bits	FSR = Full Scale Range
Integral Non-Linearity ⁵ (Relative Accuracy)	INL						LSB	Best Fit Straight Line Spec. (Max INL - Min INL) / 2
J				±14		±14		
K, T				±7		±7		
Differential Non-Linearity ⁵	DNL						LSB	
J				±16		±16		
K, T				±8		±8		
Gain Error	GE	±0.8					% FSR	Using Internal R _{FB}
Gain Temperature Coefficient ²	TC _{GE}					±2.0	ppm/°C	ΔGain/ΔTemperature
Non-Linearity Tempco ²						±0.5	ppm/°C	
Differential Linearity Tempco ²						±0.5	ppm/°C	
Power Supply Rejection Ratio	PSRR	±5	±50			±50	ppm/%	ΔGain/ΔV _{DD} ΔV _{DD} = ± 5%
Output Leakage Current ⁶	I _{OUT}	±1	±10			±200	nA	
DYNAMIC PERFORMANCE²								
Current Settling Time	t _S		2				μs	To 0.01% of FSR; all digital inputs low to high and high to low
Feedthrough at I _{OUT1}	F _T		1	2			mV p-p	V _{REF} = 10kHz, 20 Vp-p
REFERENCE INPUT								
Input Resistance	R _{IN}	1	3	10		1	10	kΩ
DIGITAL INPUTS³								
Logical "1" Voltage	V _{IH}	3.0	2.4		3.0			V
Logical "0" Voltage	V _{IL}			0.8		0.8		V
Input Leakage Current	I _{LKG}			±1.0		±1.0		μA
ANALOG OUTPUTS²								
Output Capacitance	C _{OUT1}		100					pF
	C _{OUT1}		50					pF
	C _{OUT2}		50					pF
	C _{OUT2}		100					pF
POWER SUPPLY⁴								
Functional Voltage Range ²	V _{DD}	4.5	15	16	4.5	16		V
Supply Current	I _{DD}		0.4	4		4		mA
								All digital inputs = 0 V or all = 5 V

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ELECTRICAL CHARACTERISTICS (CONT'D)

NOTES:

- 1 Full Scale Range (FSR) is 10V for unipolar mode.
- 2 Guaranteed but not production tested.
- 3 Digital input levels should not go below ground or exceed the positive supply voltage, otherwise damage may occur.
- 4 Specified values guarantee functionality. Refer to other parameters for accuracy.
- 5 Linearity error is degraded by $65\mu\text{V}$ for every mV of voltage offset at output amplifier.
- 6 Output leakage current refers to I_{OUT1} . One LSB of current constantly flows into I_{OUT2} (30nA at $5\text{k}\Omega$ input impedance, $V_{\text{REF}} = +10\text{V}$) due to ladder termination into I_{OUT2} .

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS ($T_A = +25^\circ\text{C}$ unless otherwise noted)^{1, 2}

V_{DD} to GND	0 to +17 V	Storage Temperature	-65°C to $+150^\circ\text{C}$
Digital Input Voltage to GND	GND -0.5 to $V_{\text{DD}} + 0.5\text{V}$	Lead Temperature (Soldering, 10 seconds)	$+300^\circ\text{C}$
$I_{\text{OUT1}}, I_{\text{OUT2}}$ to GND	GND -0.5 to $V_{\text{DD}} + 0.5\text{V}$	Package Power Dissipation Rating to 75°C	
V_{REF} to GND	$\pm 25\text{V}$	CDIP, PDIP, SOIC	1000mW
V_{RFB} to GND	$\pm 25\text{V}$	Derates above 75°C	13mW/ $^\circ\text{C}$

NOTES:

- 1 Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
- 2 Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies.

APPLICATION NOTES

Refer to Section 8 for Applications Information