

74LS168A, 74LS169A, S168A, S169A 4-Bit Bidirectional Counters

Logic Products

4-Bit Up/Down Synchronous Counter
Product Specification

FEATURES

- Synchronous counting and loading
- Up/down counting
- Modulo 16 binary counter — '169A
- BCD decade counter — '168A
- Two Count Enable inputs for n-bit cascading
- Positive edge-triggered clock

DESCRIPTION

The '168A is a synchronous, presettable BCD decade up/down counter featuring an internal carry look-ahead for applications in high-speed counting designs. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the Count Enable inputs and internal gating. This mode of operation eliminates the output spikes which are normally associated with asynchronous (ripple clock) counters. A buffered Clock input triggers the flip-flops on the LOW-to-HIGH transition of the clock.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74LS168A	32MHz	20mA
74S168A	70MHz	100mA
74LS169A	32MHz	20mA
74S169A	70MHz	100mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N74LS168AN, N74S168AN N74LS169AN, N74S169AN
Plastic SO	N74LS169AD, N74LS169AD, N74S169AD

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

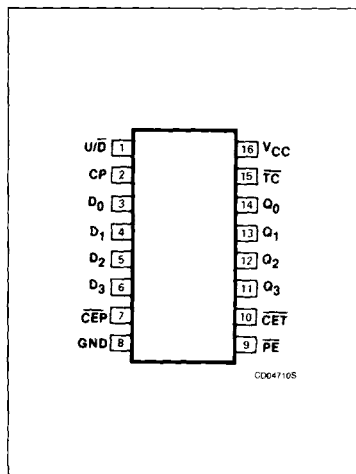
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74S	74LS
\overline{PE}	Input	1Sul	2LSul
\overline{CET}	Input	2Sul	1LSul
Other	Inputs	1Sul	1LSul
All	Outputs	10Sul	10LSul

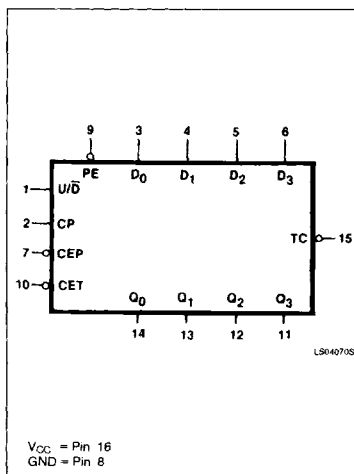
NOTE:

Where a 74S unit load (Sul) is understood to be $50\mu A$ I_{IH} and $-2.0mA$ I_{IL} and a 74LS unit load (LSul) is $20\mu A$ I_{IH} and $-0.4mA$ I_{IL} .

PIN CONFIGURATION

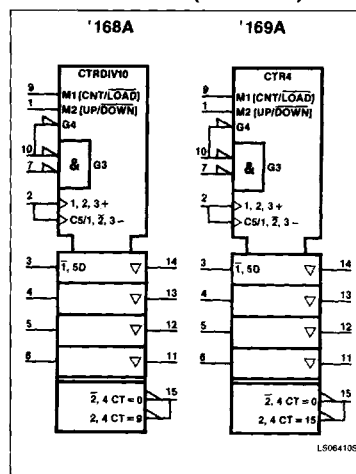


LOGIC SYMBOL



$V_{CC} = \text{Pin } 16$
 $GND = \text{Pin } 8$

LOGIC SYMBOL (IEEE/IEC)



4-Bit Bidirectional Counters

74LS168A, 74LS169A, S168A, S169A

The counter is fully programmable; that is, the outputs may be preset to either level. Presetting is synchronous with the clock and takes place regardless of the levels of the Count Enable inputs. A LOW level on the Parallel Enable (\overline{PE}) input disables the counter and causes the data at the D_n input to be loaded into the counter on the next LOW-to-HIGH transition of the clock.

The direction of counting is controlled by the Up/Down (U/\overline{D}) input; a HIGH will cause the

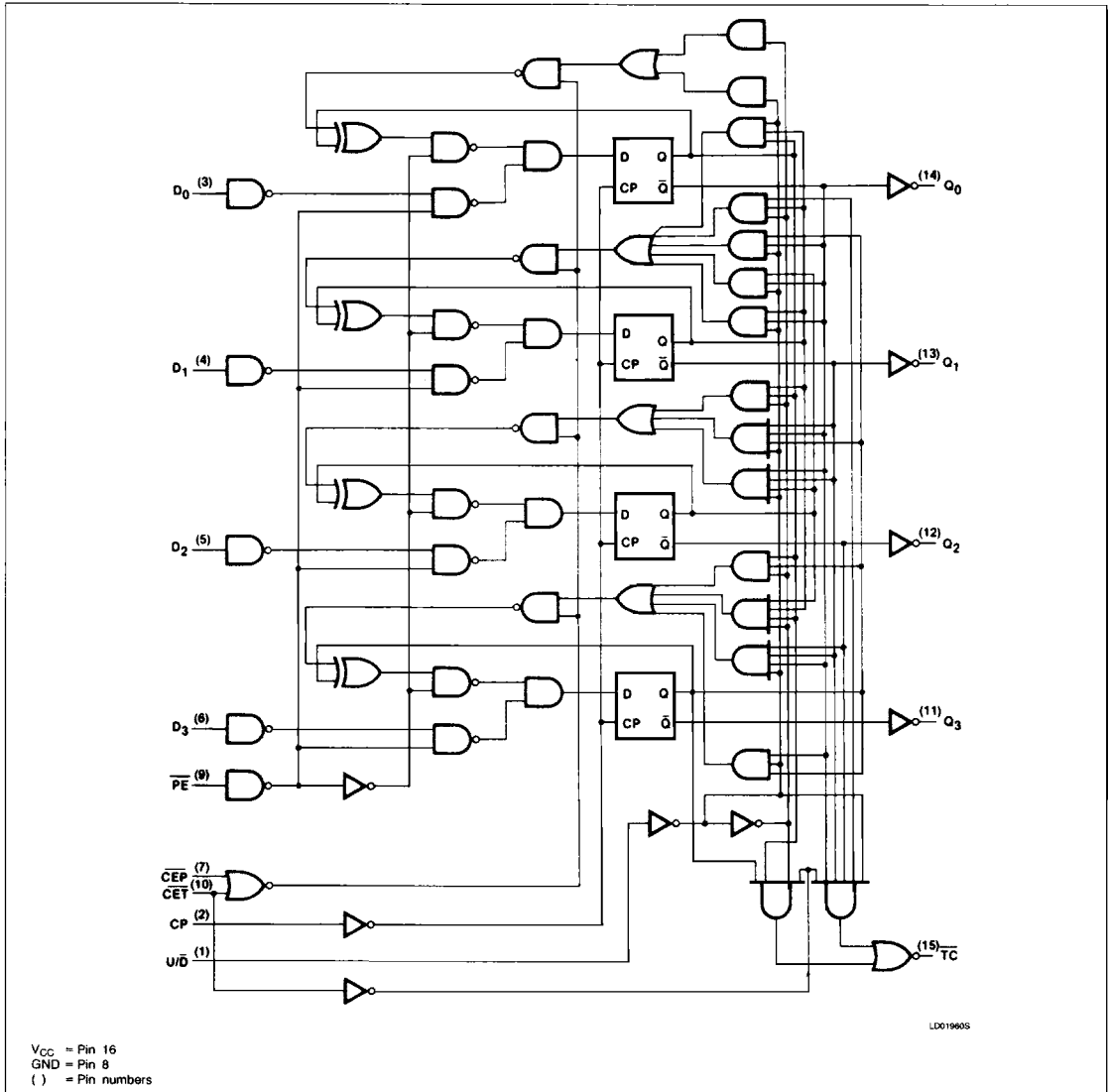
count to increase, a LOW will cause the count to decrease.

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two Count Enable inputs ($\overline{CET} \cdot \overline{CEP}$) and a Terminal Count (\overline{TC}) output. Both Count Enable inputs must be LOW to count. The \overline{CET} input is fed forward to enable the \overline{TC} output. The \overline{TC} output thus enabled will produce a LOW

output pulse with a duration approximately equal to the HIGH level portion of the Q_0 output. This LOW level \overline{TC} pulse is used to enable successive cascaded stages. See Figure A for the fast synchronous multistage counting connections.

The '169A is identical except that it is a Modulo 16 counter.

LOGIC DIAGRAM, '168A



4-Bit Bidirectional Counters

74LS168A, 74LS169A, S168A, S169A

LOGIC DIAGRAM, '169A

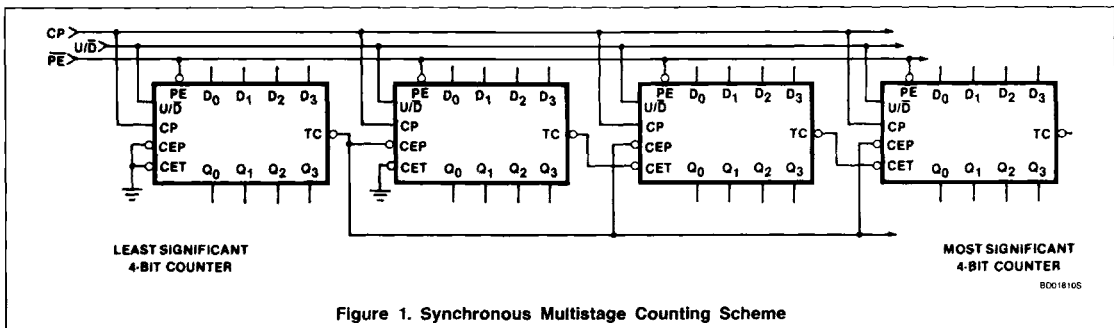
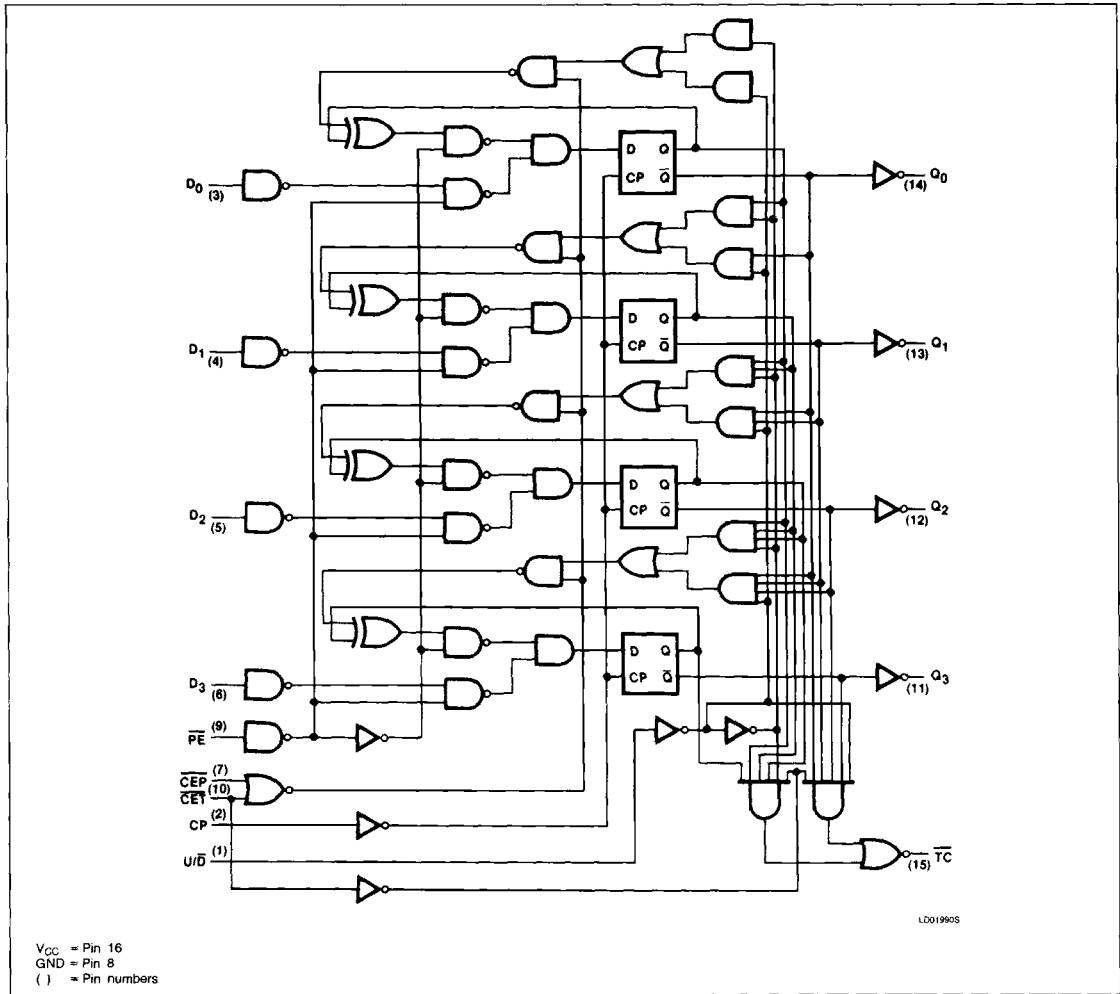


Figure 1. Synchronous Multistage Counting Scheme

4-Bit Bidirectional Counters

74LS168A, 74LS169A, S168A, S169A

MODE SELECT — FUNCTION TABLE

OPERATING MODE	INPUTS						OUTPUTS	
	CP	U/D	CEP	CE \bar{T}	PE	D _n	Q _n	$\bar{T}C$
Parallel Load	↑	X	X	X	l	i	L	(1)
	↑	X	X	X	i	h	H	(1)
Count Up	↑	h	i	l	h	X	Count Up	(1)
Count Down	↑	l	l	l	h	X	Count Down	(1)
Hold (do nothing)	↑	X	h	X	h	X	q _n	(1)
	↑	X	X	h	h	X	q _n	H

H = HIGH voltage level steady state
 h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition
 L = LOW voltage level steady state
 l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition
 X = Don't care
 q = Lower case letters indicate the state of the referenced output prior to the LOW-to-HIGH clock transition
 ↑ = LOW-to-HIGH clock transition

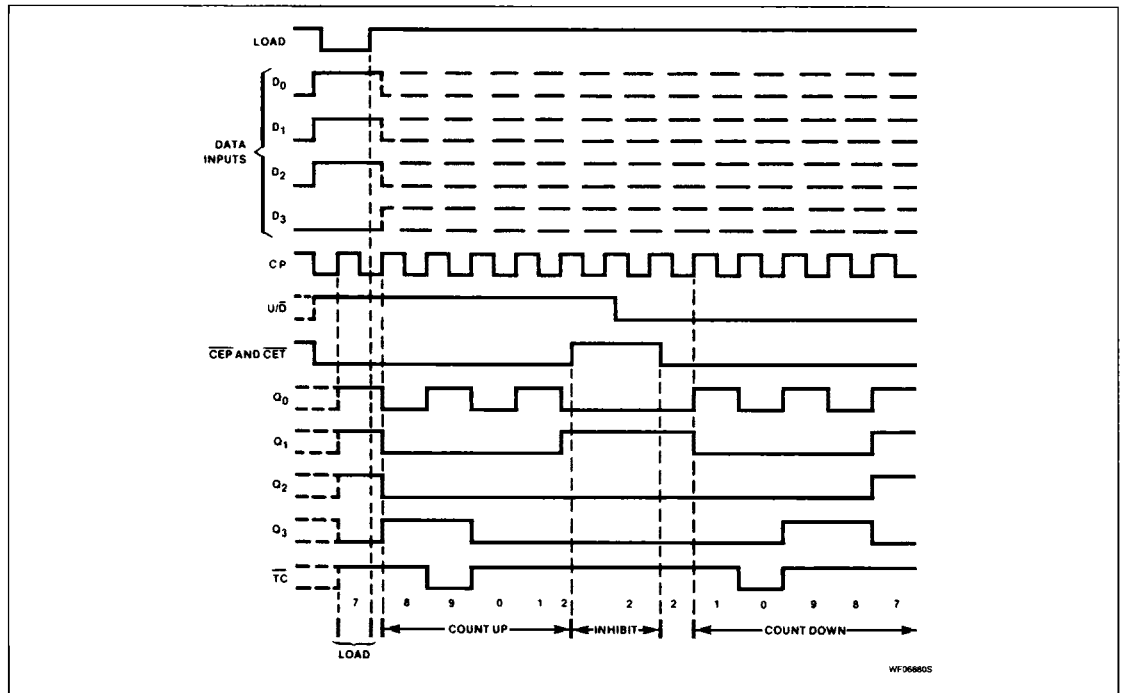
NOTE:

1. The $\bar{T}C$ is LOW when $\bar{C}E\bar{T}$ is LOW and the counter is at Terminal Count. Terminal Count Up is (HHHH) and Terminal Count Down is (LLLL) for '169A. The $\bar{T}C$ is LOW when $\bar{C}E\bar{T}$ is LOW and the counter is at Terminal Count. Terminal Count Up is (HLLH) and Terminal Count Down is (LLLL) for '168A.

WAVEFORM (Typical Load, Count, and Inhibit Sequences)

Illustrated below is the following sequence for the '168A. The operation of the '169A is similar.

1. Load (preset) to BCD seven.
2. Count up to eight, nine (maximum), zero, one, and two.
3. Inhibit.
4. Count down to one, zero (minimum), nine, eight, and seven.



4-Bit Bidirectional Counters

74LS168A, 74LS169A, S168A, S169A

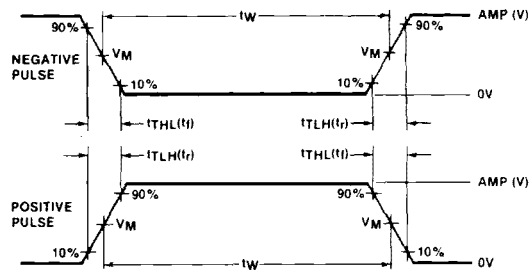
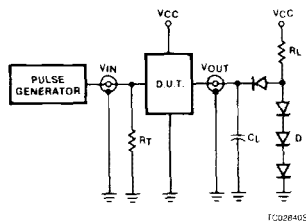
ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		74LS	74S	UNIT
V _{CC}	Supply voltage	7.0	7.0	V
V _{IN}	Input voltage	-0.5 to +7.0	-0.5 to +5.5	V
I _{IN}	Input current	-30 to +1	-30 to +5	mA
V _{OUT}	Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	-0.5 to +V _{CC}	V
T _A	Operating free-air temperature range	0 to 70		°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	74LS			74S			UNIT
	Min	Nom	Max	Min	Nom	Max	
V _{CC}	4.75	5.0	5.25	4.75	5.0	5.25	V
V _{IH}	2.0			2.0			V
V _{IL}			+0.8			+0.8	V
I _{IK}			-18			-18	mA
I _{OH}			-400			-1000	μA
I _{OL}			8			20	mA
T _A	0		70	0		70	°C

TEST CIRCUITS AND WAVEFORMS



V_M = 1.3V for 74LS; V_M = 1.5V for all other TTL families.

Test Circuit For 74 Totem-Pole Outputs

DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
 C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
 R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
 D = Diodes are 1N916, 1N3064, or equivalent.
 t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t _{TLH}	t _{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns

4-Bit Bidirectional Counters

74LS168A, 74LS169A, S168A, S169A

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	74LS168A, 169A			74S168A, 169A			UNIT
		Min	Typ ²	Max	Min	Typ ²	Max	
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX	2.7	3.4		2.7	3.4		V
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX	I _{OL} = MAX	0.35	0.5			0.5	V
		I _{OL} = 4mA (74LS)	0.25	0.4				V
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}			-1.5			-1.2	V
I _I Input current at maximum input voltage	V _{CC} = MAX	V _I = 5.5V					1.0	mA
		V _I = 7.0V	PE input		40			μA
			Other inputs		0.1			mA
I _{IH} HIGH-level input current	V _{CC} = MAX	V _I = 2.7V	PE input		0.2		100	mA
			CET input		20		100	μA
			Other inputs		20		50	μA
I _{IL} LOW-level input current	V _{CC} = MAX	V _I = 0.4V	PE input		-0.8			mA
			Other inputs		-0.4			mA
		V _I = 0.5V	CET input				-4.0	mA
							-2.0	mA
I _{OS} Short-circuit output current ³	V _{CC} = MAX	-20		-100	-40		-100	mA
I _{CC} Supply current ⁴ (total)	V _{CC} = MAX		20	34		55	80	mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- I_{CC} is measured after applying a momentary 4.5V, then ground to the Clock input with all other inputs grounded and outputs open.

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	74LS		74S				UNIT
		C _L = 15pF, R _L = 2kΩ		C _L = 15pF, R _L = 280Ω U/D = HIGH		C _L = 15pF, R _L = 280Ω U/D = LOW		
		Min	Max	Min	Max	Min	Max	
f _{MAX} Maximum clock frequency	Waveform 1	25		40		40		MHz
t _{PLH} Propagation delay	Waveform 1	20		12		12		ns
t _{PHL} Clock to Q output		23		15		15		
t _{PLH} Propagation delay	Waveform 1	35		17		15		ns
t _{PHL} Clock to TC		35		15		25		
t _{PLH} Propagation delay	Waveform 2	14		11		11		ns
t _{PHL} CET to TC		14		15		15		
t _{PLH} Propagation delay	Waveform 3	25		15		10		ns
t _{PHL} U/D control to TC ^(b)		29		15		20		

NOTE:

- b. Propagation delay time from up/down to terminal count must be measured with the counter at either a minimum or a maximum count. As the logic level of the Up/Down input is changed, the Terminal Count output will follow. If the count is minimum (0), the Terminal Count output transition will be in phase. If the count is maximum (9 for '168A or 15 for 169A, the Terminal Count output will be out of phase. Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

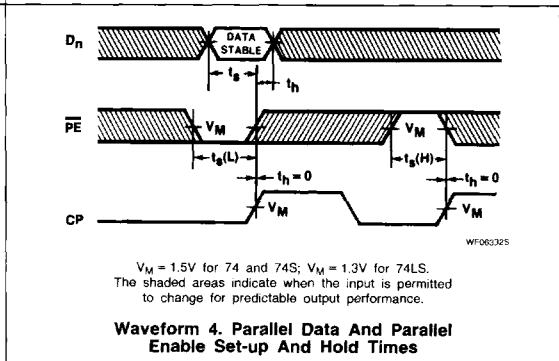
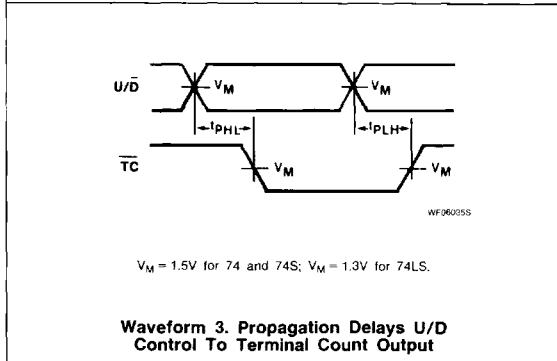
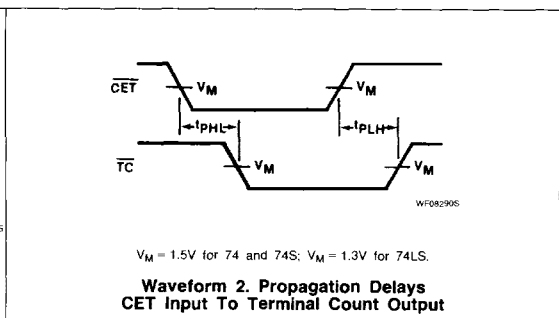
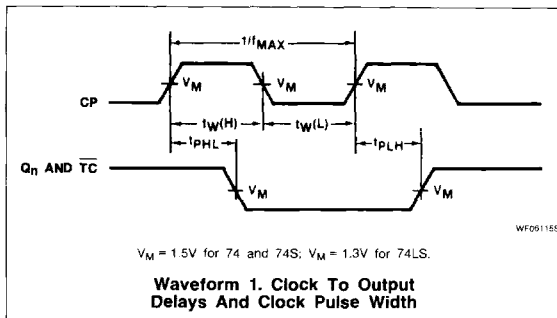
4-Bit Bidirectional Counters

74LS168A, 74LS169A, S168A, S169A

AC SET-UP REQUIREMENTS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	74LS		74S		UNIT
		Min	Max	Min	Max	
t_w	Clock pulse width	25		10		ns
t_s	Setup time, data to clock	20		6		ns
t_h	Hold time, data to clock	0		1		ns
t_s	Setup time, \overline{PE} to clock	25		9		ns
t_h	Hold time, \overline{PE} to clock	0		0		ns
t_s	Setup time, \overline{CEP} & \overline{CET} to clock	20		16		ns
t_h	Hold time, \overline{CEP} & \overline{CET} to clock	0		0		ns
t_s	Setup time, U/\overline{D} to clock	30		20		ns
t_h	Hold time, U/\overline{D} to clock	0		0		ns

AC WAVEFORMS



4-Bit Bidirectional Counters

74LS168A, 74LS169A, S168A, S169A

AC WAVEFORMS (Continued)

