

2GB – 2x128Mx72 DDR2 SDRAM REGISTERED, ECC, w/PLL

FEATURES

- 200-pin, small-outline dual in-line memory module (SO-DIMM)
- Fast data transfer rates: PC2-6400*, PC2-5300*, PC2-4200 and PC2-3200
- Utilizes 800*, 667*, 533 and 400 MT/s DDR2 SDRAM components
- $V_{cc} = V_{cc} = 1.8V (\pm 0.1V)$
- $V_{CCSPD} = 1.7V$ to 3.6V
- JEDEC standard 1.8V I/O (SSTL_18-compatible)
- Differential data strobe (DQS, DQS#) option
- Four-bit prefetch architecture
- Multiple internal device banks for concurrent operation
- Supports duplicate output strobe (RDQS/RDQS#)
- Programmable CAS# latency (CL): 3, 4, 5 and 6
- Adjustable data-output drive strength
- On-die termination (ODT)
- Posted CAS# latency: 0, 1, 2, 3 and 4
- Serial Presence Detect (SPD) with EEPROM
- 64ms: 8,192 cycle refresh
- Gold edge contacts
- Dual Rank
- RoHS compliant
- JEDEC Package
 - 200 Pin (SO-DIMM): 30.00mm (1.181") TYP.

DESCRIPTION

The W3HG2128M72EER is a 2x128Mx72 Double Data Rate DDR2 SDRAM high density SODIMM. This memory module consists of eighteen 128Mx8 (1Gb) bit with 4 banks DDR2 Synchronous DRAMs in FBGA packages, mounted on a 200-pin SO-DIMM FR4 substrate.

* This product is under development, is not qualified or characterized and is subject to change or cancellation without notice.

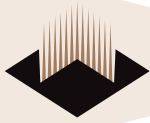
NOTE: Consult factory for availability of:

- Vendor source control options
- Industrial temperature option

OPERATING FREQUENCIES

	PC2-3200	PC2-4300	PC2-5300*	PC2-6400*
Clock Speed	200MHz	266MHz	333MHz	400MHz
CL-tRCD-tRP	3-3-3	4-4-4	5-5-5	6-6-6

* Consult factory for availability



PIN CONFIGURATION

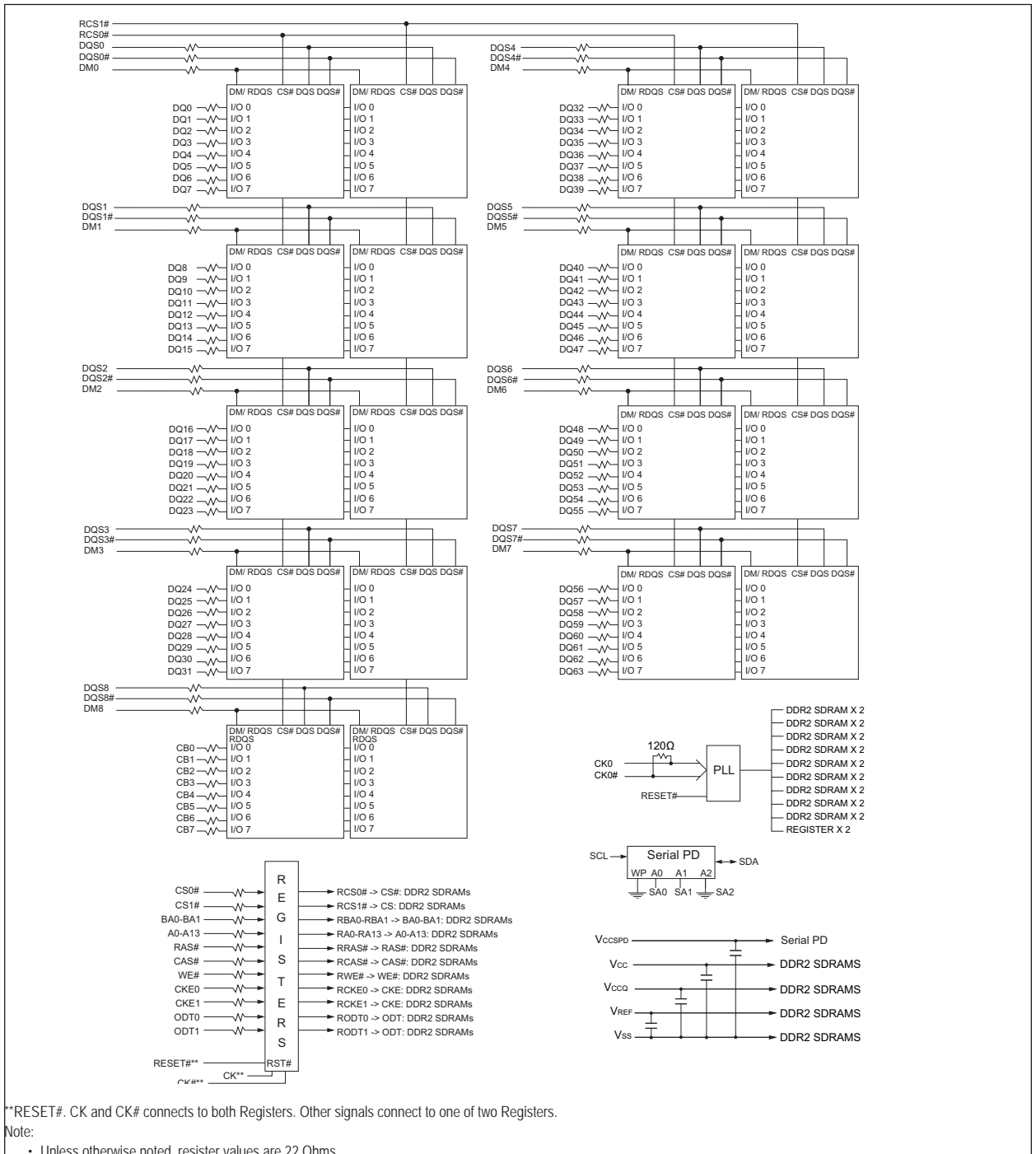
PIN#	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL
1	VREF	51	DQ18	101	Vcc	151	Vss
2	Vss	52	Vss	102	A6	152	Vss
3	DQ0	53	DQ19	103	A5	153	DQS5#
4	DQ4	54	DQ28	104	A4	154	DM5
5	Vss	55	Vss	105	A3	155	DQS5
6	DQ5	56	DQ29	106	Vcc	156	Vss
7	DQ1	57	DQ24	107	A2	157	Vss
8	Vss	58	Vss	108	A1	158	DQ46
9	DQS0#	59	DQ25	109	Vcc	159	DQ42
10	DM0	60	DM3	110	A0	160	DQ47
11	DQS0	61	Vss	111	A10/AP	161	DQ43
12	Vss	62	Vss	112	BA1	162	Vss
13	Vss	63	DQS3#	113	BA0	163	Vss
14	DQ6	64	DQ30	114	Vcc	164	DQ52
15	DQ2	65	DQS3	115	RAS#	165	DQ48
16	DQ7	66	DQ31	116	WE#	166	DQ53
17	DQ3	67	Vss	117	Vcc	167	DQ49
18	Vss	68	Vss	118	S0#	168	Vss
19	Vss	69	DQ26	119	CAS#	169	Vss
20	DQ12	70	CB4	120	ODT0	170	DM6
21	DQ8	71	DQ27	121	NC/S1#	171	DQS6#
22	DQ13	72	CB5	122	A13	172	Vss
23	DQ9	73	Vss	123	Vcc	173	DQS6
24	Vss	74	Vss	124	Vcc	174	DQ54
25	Vss	75	CB0	125	ODT1	175	Vss
26	DM1	76	DM8	126	CK	176	DQ55
27	DQS1#	77	CB1	127	NC/S3#	177	DQ50
28	Vss	78	Vss	128	CK#	178	Vss
29	DQS1	79	Vss	129	DQ32	179	DQ51
30	DQ14	80	CB6	130	Vss	180	DQ60
31	Vss	81	DQS8#	131	Vss	181	Vss
32	DQ15	82	CB7	132	DQ36	182	DQ61
33	DQ10	83	DQS8	133	DQ33	183	DQ56
34	Vss	84	Vss	134	DQ37	184	Vss
35	DQ11	85	Vss	135	DQS4#	185	DQ57
36	DQ20	86	CB2	136	Vss	186	DM7
37	Vss	87	CKE0	137	DQS4	187	Vss
38	DQ21	88	CB3	138	DM4	188	DQ62
39	DQ16	89	NC/CKE1	139	Vss	189	DQS7#
40	Vss	90	Vss	140	Vss	190	Vss
41	DQ17	91	NC/S2#	141	DQ34	191	DQS7
42	RESET#	92	NC/BA2	142	DQ38	192	DQ63
43	Vss	93	Vcc	143	DQ35	193	DQ58
44	DM2	94	NC	144	DQ39	194	SDA
45	DQS2#	95	A12	145	Vss	195	Vss
46	Vss	96	A11	146	Vss	196	SCL
47	DQS2	97	A9	147	DQ40	197	DQ59
48	DQ22	98	Vcc	148	DQ44	198	SA1
49	Vss	99	A7	149	DQ41	199	VCCSPD
50	DQ23	100	A8	150	DQ45	200	SA0

PIN NAMES

Pin Name	Function
A0 - A13	Address Inputs
BA0 - BA1	Bank Address Inputs
DQ0 - DQ63	Data Input/Output
CB0 - CB7	Check Bits
DQS0 - DQS8	Data Strobes
DQS0# - DQS8#	Data Strobes Complement
ODT0, ODT1	On-die Termination Control
CK, CK#	Clock Input
CKE0, CKE1	Clock Enables
CS0# - CS3#	Chip Selects
RAS#	Row Address Strobes
CAS#	Column Address Strobes
WE#	Write Enable
DM0 - DM8	Data Masks
Vcc	Voltage Supply 1.8V +/- 0.1V
A10/AP	Address input/Autoprecharge
VccSPD	SPD Voltage supply 1.7V to 3.6V
Vcca	I/O Power (1.8v)
Vss	Ground
SA0 - SA2	SPD Address
SDA	SPD Data Input/Output
SCL	SPD Clock Input
VREF	SSTL_18 Reference Voltage
NC	No Connect



FUNCTIONAL BLOCK DIAGRAM



**RESET#. CK and CK# connects to both Registers. Other signals connect to one of two Registers.

Note:

- Unless otherwise noted, resistor values are 22 Ohms.



DC OPERATING CONDITIONS

All voltages referenced to V_{SS}

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Supply Voltage	V _{CC}	1.7	1.8	1.9	V	1
I/O Supply Voltage	V _{CC0}	1.7	1.8	1.9	V	4
V _{CC} L Supply Voltage	V _{CC} L	1.7	1.8	1.9	V	4
I/O Reference Voltage	V _{REF}	0.49 x V _{CC0}	0.50 x V _{CC0}	0.51 x V _{CC0}	V	2
I/O Termination Voltage	V _{TT}	V _{REF} -0.04	V _{REF}	V _{REF} +0.04	V	3

Notes:

- V_{CC} & V_{CC0} must track each other. V_{CC0} must be less than or equal to V_{CC}.
- V_{REF} is expected to equal V_{CC0}/2 of the transmitting device and to track variations in the DC level of the same. Peak-to-peak noise on V_{REF} may not exceed +/-1 percent of the DC value. Peak-to-peak AC noise on V_{REF} may not exceed +/-2 percent of V_{REF}. This measurement is to be taken at the nearest V_{REF} bypass capacitor.
- V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors, is expected to be set equal.
- V_{CC0} tracks with V_{CC}; V_{CC}L tracks with V_{CC}.

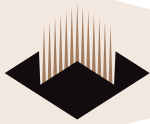
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Min	Max	Units	
V _{CC}	Voltage on V _{CC} pin relative to V _{SS}	-1.0	2.3	V	
V _{CC0}	Voltage on V _{CC0} pin relative to V _{SS}	-0.5	2.3	V	
V _{CC} L	Voltage on V _{CC} L pin relative to V _{SS}	-0.5	2.3	V	
V _{IN} , V _{OUT}	Voltage on any pin relative to V _{SS}	-0.5	2.3	V	
T _{STG}	Storage Temperature	-55	100	°C	
T _{CAS}	Device operating temperature	0	85	°C	
I _L	Input leakage current; Any input 0V < V _{IN} < V _{CC} ; V _{REF} input 0V, V _{IN} , 0.95V; Other pins not under test = 0V	Command/Address, RAS#, CAS#, WE#, CS#, CE, ODT	-5	5	μA
		CK, CK#	-10	10	μA
		DM	-10	10	μA
I _{OZ}	Output leakage current; 0V < V _{IN} < V _{CC} ; DQs and ODT are disable	-10	10	μA	
I _{VREF}	V _{REF} leakage current; V _{REF} = Valid V _{REF} level	-36	36	μA	

INPUT/OUTPUT CAPACITANCE

T_A = 25°C, f = 100MHz

Parameter	Symbol	Min	Max	Units
Input Capacitance (A0-A13, BA0-BA1, RAS#, CAS#, WE#)	C _{IN1}			pF
Input Capacitance (CKE0, CKE1), (ODT, ODT1)	C _{IN2}			pF
Input Capacitance (CS0#, CS1#)	C _{IN3}			pF
Input Capacitance (CK0, CK0#, CK1, CK1#)	C _{IN4}			pF
Input Capacitance (DM0 - DM7), (DQS0 - DQS7)	C _{IN5} (E6)			pF
	C _{IN5} (D5)			pF
Input Capacitance (DQ0 - DQ63)	C _{OUT1} (E6)			pF
	C _{OUT1} (D5)			pF

**OPERATING TEMPERATURE CONDITION**

Parameter	Symbol	Rating	Units	Notes
Operating temperature	TOPER	0°C to 85°C	°C	1, 2

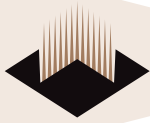
- Notes:
1. Operating temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JEDED JESD51.2
 2. At 0°C - 85°C, operation temperature range, all DRAM specification will be supported.

INPUT DC LOGIC LEVELAll voltages referenced to V_{SS}

Parameter	Symbol	Min	Max	Units
Input High (Logic 1) Voltage	V _{IH} (DC)	V _{REF} + 0.125	V _{CC} + 0.300	V
Input Low (Logic 0) Voltage	V _{IL} (DC)	-0.300	V _{REF} - 0.125	V

INPUT AC LOGIC LEVELAll voltages referenced to V_{SS}

Parameter	Symbol	Min	Max	Units
Input High (Logic 1) Voltage DDR2-400 & DDR2-533	V _{IH} (DC)	V _{REF} + 0.250	-	V
Input Low (Logic 1) Voltage DDR2-667	V _{IH} (DC)	V _{REF} + 0.200	-	V
Input Low (Logic 0) Voltage DDR2-400 & DDR2-533	V _{IL} (DC)	-	V _{REF} - 0.250	V
Input Low (Logic 0) Voltage DDR2-667, DDR2-800(TBD)	V _{IL} (DC)	-	V _{REF} - 0.200	V



Icc SPECIFICATION

Symbol	Proposed Conditions	806	665	534	403	Units
I _{CC0} *	Operating one bank active-precharge; t _{CK} = t _{CK} (I _{CC}), t _{RC} = t _{RC} (I _{CC}), t _{RAS} = t _{RAS} min(I _{CC}); CE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING					mA
I _{CC1} *	Operating one bank active-read-precharge; I _{OUT} = 0mA; BL = 4, CL = CL(I _{CC}), AL = 0; t _{CK} = t _{CK} (I _{CC}), t _{RC} = t _{RC} (I _{CC}), t _{RAS} = t _{RAS} min(I _{CC}); CE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as I _{CC4W}					mA
I _{CC2P} **	Precharge power-down current; All banks idle; t _{CK} = t _{CK} (I _{CC}); CE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING					mA
I _{CC2Q} **	Precharge quiet standby current; All banks idle; t _{CK} = t _{CK} (I _{CC}); CE is HIGH, CS# is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING					mA
I _{CC2N} **	Precharge standby current; All banks idle; t _{CK} = t _{CK} (I _{CC}); CE is HIGH, CS# is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are SWITCHING					mA
I _{CC3P} **	Active power-down current; All banks open; t _{CK} = t _{CK} (I _{CC}); CE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	Fast PDN Exit MRS(12) = 0				mA
		Slow PDN Exit MRS(12) = 1				mA
I _{CC3N} **	Active standby current; All banks open; t _{CK} = t _{CK} (I _{CC}), t _{RC} = t _{RC} (I _{CC}), t _{RAS} = t _{RAS} min(I _{CC}); CE is HIGH, CS# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING					mA
I _{CC4W} *	Operating burst write current; All banks open, Continuous burst writes; BL = 4, CL = CL(I _{CC}), AL = 0; t _{CK} = t _{CK} (I _{CC}), t _{RAS} = t _{RAS} max(I _{CC}), t _{RP} = t _{RP} (I _{CC}); CE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING					mA
I _{CC4R} *	Operating burst read current; All banks open, Continuous burst reads, I _{OUT} = 0mA; BL = 4, CL = CL(I _{CC}), AL = 0; t _{CK} = t _{CK} (I _{CC}), t _{RAS} = t _{RAS} max(I _{CC}), t _{RP} = t _{RP} (I _{CC}); CE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as I _{CC4W}					mA
I _{CC5} **	Burst auto refresh current; t _{CK} = t _{CK} (I _{CC}); Refresh command at every t _{RF} (I _{CC}) interval; CE is HIGH, CS# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING					mA
I _{CC6} **	Self refresh current; CK and CK# at 0V; CE 0.2V; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING					mA
I _{CC7} *	Operating bank interleave read current; All bank interleaving reads, I _{OUT} = 0mA; BL = 4, CL = CL(I _{CC}), AL = t _{RC} D(I _{CC})-1*t _{CK} (I _{CC}); t _{CK} = t _{CK} (I _{CC}), t _{RC} = t _{RC} (I _{CC}), t _{RRD} = t _{RRD} (I _{CC}), t _{RCD} = 1*t _{CK} (I _{CC}); CE is HIGH, CS# is HIGH between valid commands; Address bus inputs are STABLE during DESELECTS; Data bus inputs are SWITCHING.					mA

I_{CC} specification is based on xxx components. Other DRAM manufactures specification may be different.

Note:

* Value calculated as one module rank in this operating condition, and all other module ranks in I_{CC2P} (CE LOW) mode.

** Value calculated reflects all module ranks in this operating condition.



DDR2 SDRAM COMPONENT AC TIMING PARAMETERS & SPECIFICATIONS

AC CHARACTERISTICS			806		665		534		403		
PARAMETER			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
Clock	Clock cycle time	CL = 6	t _{CK} (6)								ps
		CL = 5	t _{CK} (5)								ps
		CL = 4	t _{CK} (4)								ps
		CL = 3	t _{CK} (3)								ps
	CK high-level width		t _{CH}								tck
	CK low-level width		t _{CL}								tck
	Half clock period		t _{HP}								ps
Clock jitter		t _{JIT}								ps	
Data	DQ output access time from CK/CK#		t _{AC}								ps
	Data-out high-impedance window from CK/CK#		t _{HZ}								ps
	Data-out low-impedance window from CK/CK#		t _{LZ}								ps
	DQ and DM input setup time relative to DQS		t _{DS}								ps
	DQ and DM input hold time relative to DQS		t _{DH}								ps
	DQ and DM input pulse width (for each input)		t _{DPW}								tck
	Data hold skew factor		t _{DHS}								ps
	DQ...DQS hold, DQS to first DQ to go nonvalid, per access		t _{DH}								ps
	Data valid output window (DVW)		t _{DVW}								ns
Data Strobe	DQS input high pulse width		t _{DOSH}								tck
	DQS input low pulse width		t _{DOSL}								tck
	DQS output access time from CK/CK#		t _{DOSCK}								ps
	DQS falling edge to CK rising ... setup time		t _{DSS}								tck
	DQS falling edge from CK rising ... hold time		t _{DSH}								tck
	DQS...DQ skew, DQS to last DQ valid, per group, per access		t _{DOSQ}								ps
	DQS read preamble		t _{RPRE}								tck
	DQS read postamble		t _{RPST}								tck
	DQS write preamble setup time		t _{WPRES}								ps
	DQS write preamble		t _{WPRE}								tck
	DQS write postamble		t _{WPST}								tck
	Write command to first DQS latching transition		t _{DOSS}								tck
	Address and control input pulse width for each input		t _{IPW}								tck
	Address and control input setup time		t _{IS}								ps
	Address and control input hold time		t _{IH}								ps
	Address and control input hold time		t _{CCD}								tck

AC specification is based on xxx components. Other DRAM manufactures specification may be different.

Continued on next page



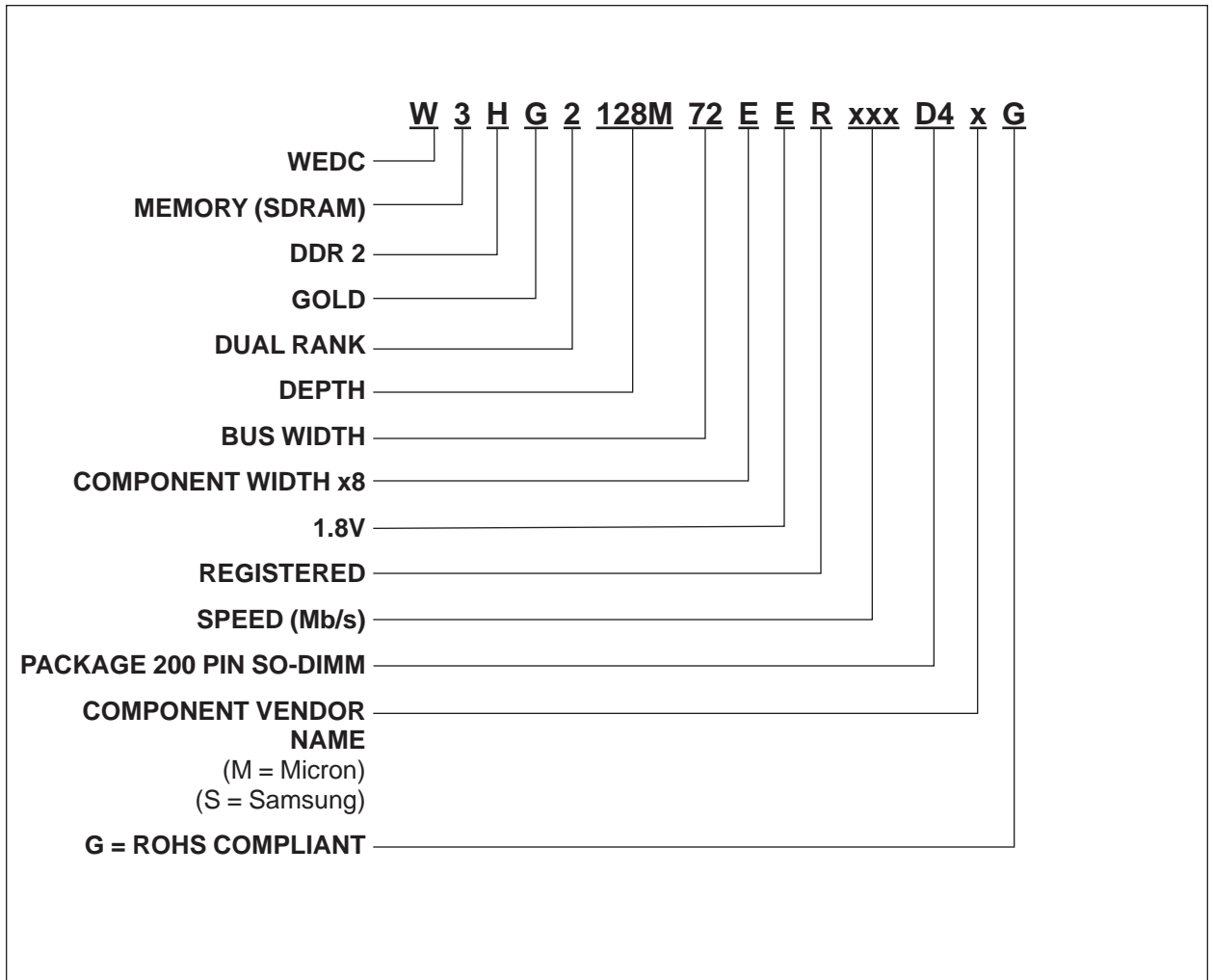
DDR2 SDRAM COMPONENT AC TIMING PARAMETERS & SPECIFICATIONS (cont'd)

AC CHARACTERISTICS			806		665		534		403		
PARAMETER		SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
Command and Address	ACTIVE to ACTIVE (same bank) command	t _{RC}									ns
	ACTIVE bank a to ACTIVE bank b command	t _{RRD}									ns
	ACTIVE to READ or WRITE delay	t _{RCD}									ns
	Four Bank Activate period	t _{FAW}									ns
	ACTIVE to PRECHARGE command	t _{RAS}									ns
	Internal READ to precharge command delay	t _{RTP}									ns
	Write recovery time	t _{WR}									ns
	Auto precharge write recovery + precharge time	t _{DAL}									ns
	Internal WRITE to READ command delay	t _{WTR}									ns
	PRECHARGE command period	t _{RP}									ns
	PRECHARGE ALL command period	t _{RPA}									ns
	LOAD MODE command cycle time	t _{MRD}									tck
CKE low to CK,CK# uncertainty	t _{DELAY}									ns	
Self Refresh	REFRESH to Active of Refresh to Refresh command interval	t _{RFC}									ns
	Average periodic refresh interval	t _{REFI}									μs
	Exit self refresh to non-READ command	t _{XSNR}									ns
	Exit self refresh to READ command	t _{XSRD}									tck
Exit self refresh timing reference	t _{LSXR}									ps	
ODT	ODT turn-on delay	t _{AOND}									tck
	ODT turn-on	t _{AON}									ps
	ODT turn-off delay	t _{AOFD}									tck
	ODT turn-off	t _{AOF}									ps
	ODT turn-on (power-down mode)	t _{AONPD}									ps
	ODT turn-off (power-down mode)	t _{AOFPD}									ps
	ODT to power-down entry latency	t _{ANPD}									tck
ODT power-down exit latency	t _{AXPD}									tck	
Power-Down	Exit active power-down to READ command, MR[bit12=0]	t _{XARD}									tck
	Exit active power-down to READ command, MR[bit12=1]	t _{XARDS}									tck
	A Exit precharge power-down to any non-READ command.	t _{XP}									tck
	CKE minimum high/low time	t _{CKE}									tck

AC specification is based on xxxx components. Other DRAM manufactures specification may be different.



PART NUMBERING GUIDE





Document Title

2GB – 2x128Mx72 DDR2 SDRAM REGISTERED,PLL, SO-DIMM

Revision History

Rev #	History	Release Date	Status
Rev 0	Created	January 2006	Concept
Rev 1	1.0 Updated AC title to indicate component AC spec only	October 2006	Advanced