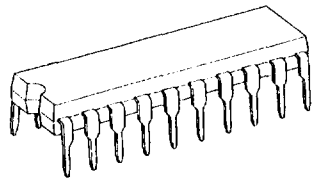
TC9802P, TC9802FW

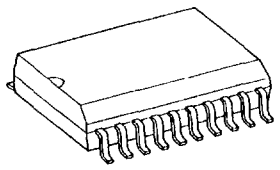
TC9802 is a CMOS programmable logic device (PLD) based on EEPROM cells. Designed using Toshiba's original technology, this device features low power dissipation and a wide operating voltage range (2V to 6V), and is applicable to a variety of electronic devices.
It has both AND and OR arrays which the user can program like a field programmable logic array (FPLA).
TC9802 is a high-speed version of TC9800. Its pin connections and functions are the same as those of TC9800.

TC9802P



DIP20-P-300A

TC9802FW



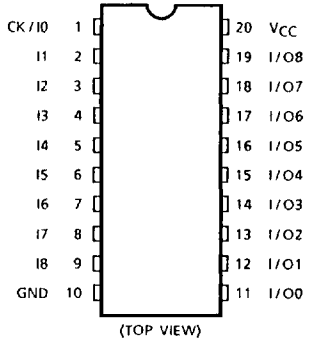
SOL20-P-300

Weight DIP20-P-300A : 1.30g (Typ.)
SOL20-P-300 : 0.46g (Typ.)

FEATURES

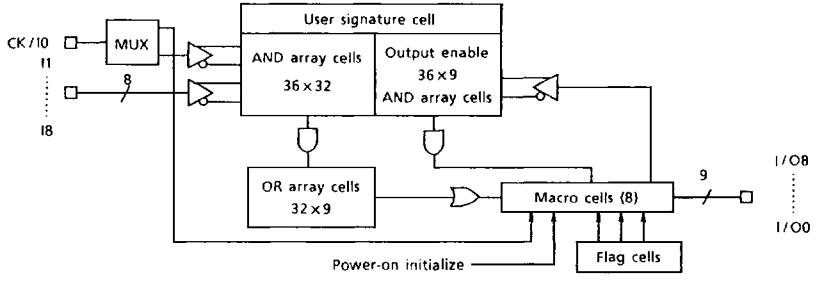
- Architecture ..... 41 AND terms
  9 OR terms
  8 macro cells with registers
- Security cell ..... Protection of proprietary information
- Signature word ..... 41 bits for user ID code or inventory control
- High speed operation ..... t_{pd} (input-output) = 23ns (Typ.)
  t_{co} (clock-output) = 10ns (Typ.)
- Low power dissipation ..... I_{CC} (standby) = 4μA (max. @25°C)
- Wide operating voltage range .. V_{CC} = 2~6V
- Package ..... 20-pin plastic DIP (TC9802P)
  20-pin plastic SOL (TC9802FW)

PIN NAMES & FUNCTIONS

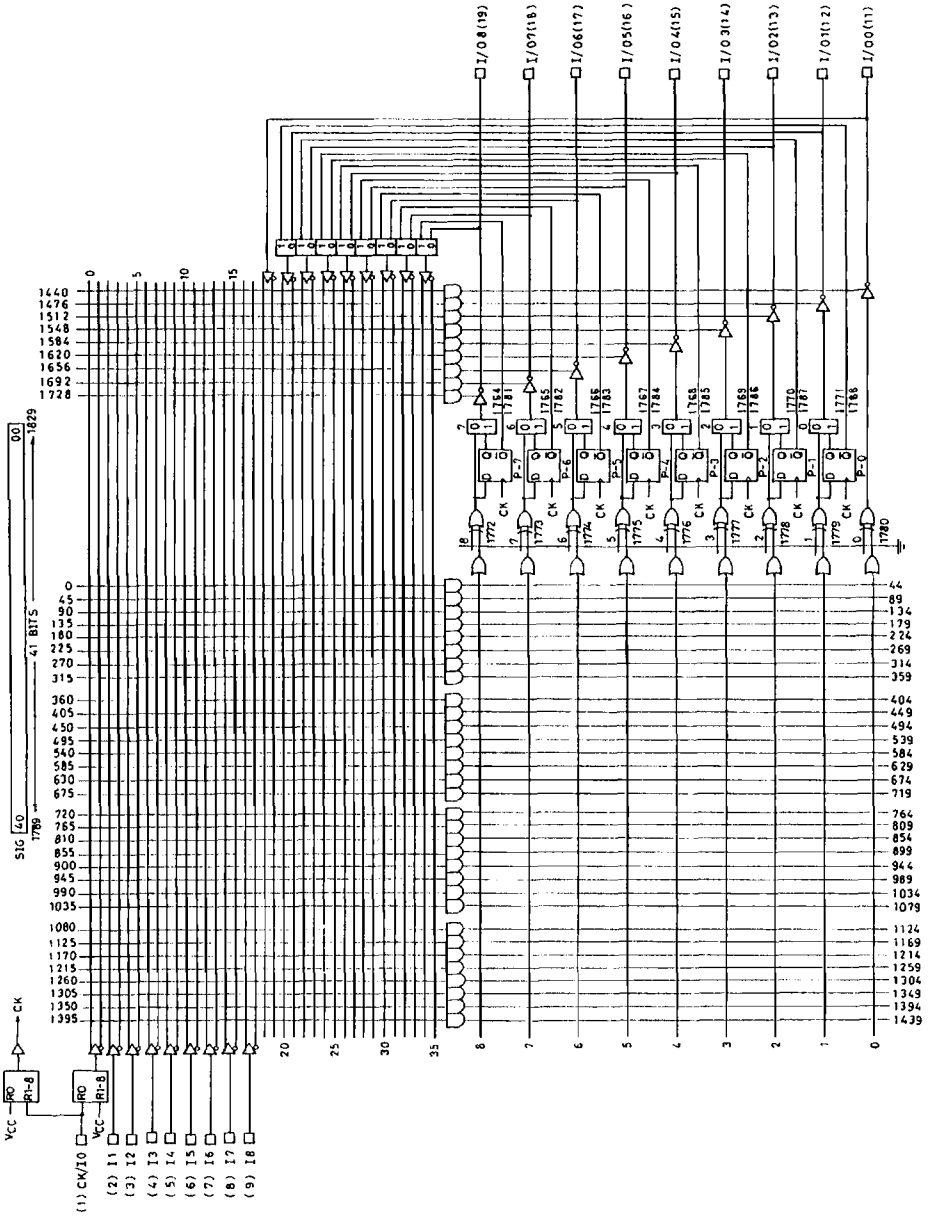


CK/I0	Clock input (when register is selected)
I1~I8	Dedicated to input
I/O0	Input/Output (without register output)
I/O1~I/O8 ...	Input/Output (with register output)

FUNCTION DIAGRAM



LOGIC DIAGRAM



ARCHITECTURE

1. MEMORY CELLS

Programmable memory cells are divided into the following five types : AND array, OR array, output control array, flag, and user signature.
Setting program data to 1 disconnects signals to an AND/OR array : setting to 0 connects.

(1) AND array (36 × 32)

Total of 41 product terms (32 AND terms and 9 output control terms)

(2) OR array (32 × 9)

32 AND terms input to 9 OR terms.

(3) Output control array (36 × 9)

Output from this array enables CMOS output (I/O0~I/O8).

(4) Flag cell

A. Output polarity selection cell .... 9 bits

B. Register selection cell ..... 8 bits

C. Initial register setting cell ..... 8 bits

D. Security cell ..... 1 bit

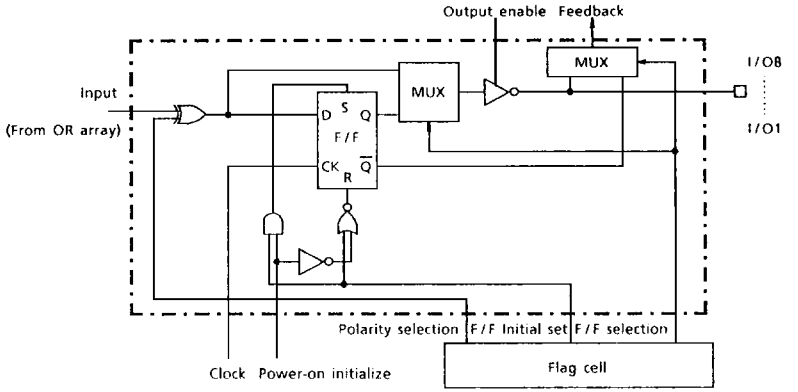
(5) User signature cell

User can program a 41-bit memory array for a variety of uses including ID codes, inventory control, and revision number.
Programming the security bit (security cell) disables access of cells other than the signature cell.

2. Macro cells

TC9802 has 8 macro cells containing D-type flip/flops (register).

Macro Cell



1) Output polarity of OR array

Nine exclusive OR gates control the output polarity of the OR array. These gates are user programmable : setting program data to 1 inputs the output signal from the OR array as inverted ; setting program data to 0, as non-inverted.

2) Register selection

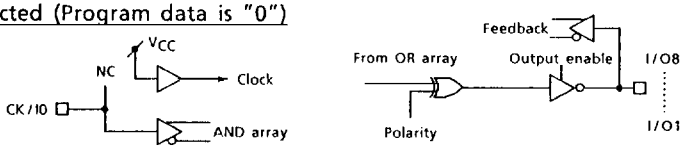
The eight output registers can be independently selected. Setting the program data to 1 selects an output register ; setting to 0 does not select an output register. When an output register is selected, the CK/I0 pin (pin 1) is automatically set to clock input. If an output register is not selected, pin 1 (like I1~I8) is set to dedicated data input. The register operates when the clock pulse goes positive.

3) Initial state of registers at power-up

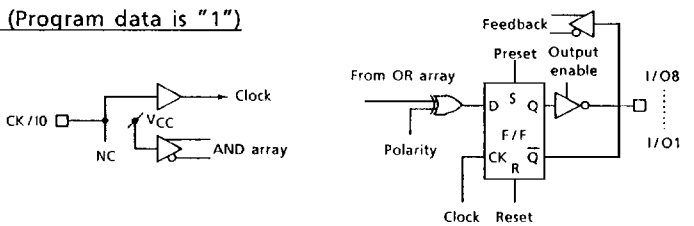
The user can program reset or preset of register outputs at power-up. Setting program data to 1 presets register output ; setting to 0 resets register output. This function can only be used when registers are selected.

Selected / Not selected

A) Not selected (Program data is "0")



B) Selected (Program data is "1")



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5~7	V
DC Input Voltage	V_{IN}	−0.5~V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	−0.5~V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±35	mA
DC V_{CC}/Ground Current	I_{CC}	±70	mA
Power Dissipation	P_D	500 (DIP) * / 180 (SOL)	mW
Storage Temperature	T_{stg}	−65~150	°C
Lead Temperature (10s)	T_L	300	°C

* 500mW in the range of Ta = −40~65°C. From Ta = 65°C to 85°C a derating factor of −10mW/°C should be applied up to 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2~6	V
Input Voltage	V_{IN}	0~V_{CC}	V
Output Voltage	V_{OUT}	0~V_{CC}	V
Operating Temperature	T_{opr}	−40~85	°C
Input Rise and Fall Time	t_r, t_f	0~ 1000 (V_{CC} = 2.0V) 0~ 500 (V_{CC} = 4.5V) 0~ 400 (V_{CC} = 6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

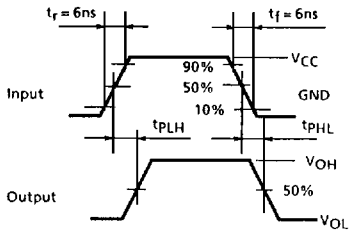
PARAMETER	SYMBOL	TEST CIRCUIT	TEST CONDITION		V_{CC}	Ta = 25°C MIN.	Ta = 25°C TYP.	Ta = 25°C MAX.	Ta = −40 ~85°C MIN.	Ta = −40 ~85°C MAX.	UNIT
High-level input voltage	V_{IH}	—			2.0	1.5	—	—	1.5	—	V
					4.5	3.15	—	—	3.15	—	
					6.0	4.2	—	—	4.2	—	
Low-level input voltage	V_{IL}	—			2.0	—	—	0.5	—	0.5	V
					4.5	—	—	1.35	—	1.35	
					6.0	—	—	1.8	—	1.8	
High-level output voltage	V_{OH}	—	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −20μA	2.0	1.9	2.0	—	1.9	—	V
					4.5	4.4	4.5	—	4.4	—	
					6.0	5.9	6.0	—	5.9	—	
				I_{OH} = −6mA	4.5	4.18	4.31	—	4.13	—	
				I_{OH} = −7.8mA	6.0	5.68	5.80	—	5.63	—	
Low-level output voltage	V_{OL}	—	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 20μA	2.0	—	0.0	0.1	—	0.1	V
					4.5	—	0.0	0.1	—	0.1	
					6.0	—	0.0	0.1	—	0.1	
				I_{OL} = 6mA	4.5	—	0.17	0.26	—	0.33	
				I_{OL} = 7.8mA	6.0	—	0.18	0.26	—	0.33	
3-State output off-state current	I_{OZ}	—	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND		6.0	—	—	±0.5	—	±5.0	μA
Input leakage current	I_{IN}	—	V_{IN} = V_{CC} or GND		6.0	—	—	±0.1	—	±1.0	
Quiescent current	I_{CCSB}	—	V_{IN} = V_{CC} or GND Standby		6.0	—	—	4.0	—	40.0	μA
Operating current	I_{CCOP}	—	f_{IN} = 1MHz Operating		5.0	—	—	—	—	25.0	mA

AC ELECTRICAL CHARACTERISTICS (C_L = 50pF, Input $t_r = t_f$ = 6ns)

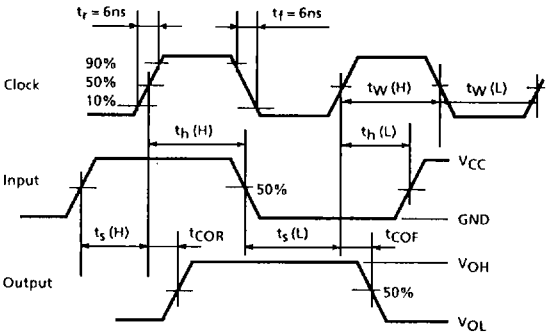
PARAMETER	SYMBOL	TEST CIRCUIT	TEST CONDITION		Ta = 25°C			Ta = −40 ~85°C		UNIT
				V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time (Input, I/O-Output)	t_{PLH} t_{PHL}	—		2.0	—	120	200	—	250	ns
				4.5	—	23	35	—	40	
				6.0	—	19	28	—	32	
Propagation Delay Time (Clock-Output)	t_{COR} t_{COF}	—		2.0	—	34	56	—	65	ns
				4.5	—	10	17	—	19	
				6.0	—	8	15	—	17	
Output Enable Time	t_{PZL} t_{PZH}	—		2.0	—	59	90	—	104	ns
				4.5	—	19	30	—	34	
				6.0	—	15	21	—	24	
Output Disable Time	t_{PLZ} t_{PHZ}	—		2.0	—	51	74	—	77	ns
				4.5	—	23	33	—	38	
				6.0	—	18	27	—	31	
Minimum Pulse Width	t_W (L) t_W (H)	—		2.0	—	35	54	—	62	ns
				4.5	—	7	11	—	13	
				6.0	—	6	10	—	12	
Minimum Set-up Time	t_S	—		2.0	—	—	210	—	240	ns
				4.5	—	—	30	—	34	
				6.0	—	—	21	—	24	
Minimum Hold Time	t_H	—		2.0	—	—	0	—	0	ns
				4.5	—	—	0	—	0	
				6.0	—	—	0	—	0	
Maximum Clock Frequency	f_{MAX}	—		2.0	4.1	—	—	2.3	—	MHz
				4.5	16	—	—	14	—	
				6.0	23	—	—	20	—	

Switching Characteristic Test Waveform

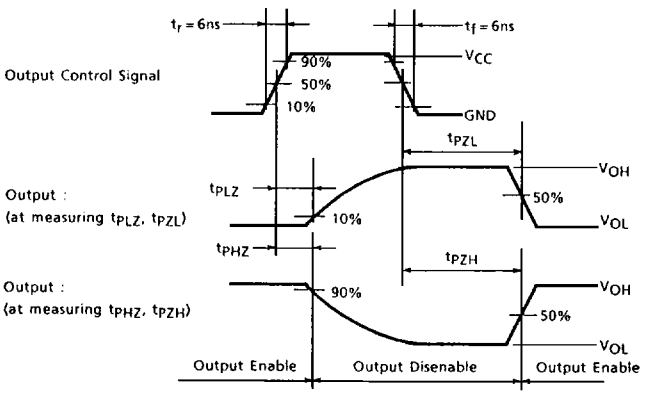
1) t_{PD} (t_{PLH}, t_{PHL})



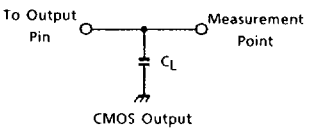
2) t_{CO} (t_{COR}, t_{COF}, t_s, t_h, t_w)

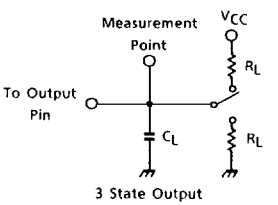


3) t_{PLZ}, t_{PHZ}, t_{PZL}, t_{PZH}



4) Output Test Connection Diagram





Note) C_L includes the capacitance of probe.