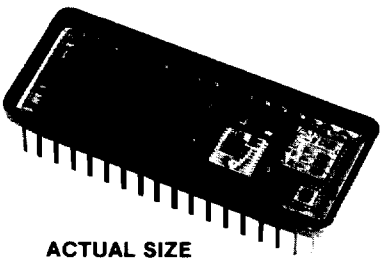
NATEL
HSCT/HRCT3006

Solid State Control Transformer Microprocessor Compatible 16-bit Hybrid

Features

- **Single 36-pin hybrid DDIP package**
- **1 arc-minute accuracy**
- **Single main power supply** (15 V-dc nominal)
- **8- and 16-bit microprocessor compatible**
- **Double buffered inputs**
- **TTL and CMOS compatible** (without external pull-up resistors)
- **True differential analog inputs**
- **MIL-STD-883 Processing is Available**



ACTUAL SIZE

Applications

Synchro-to-Digital converters
Closed loop servo systems
Testing of synchro/resolver converters

Description

Offering both 8 and 16-bit microprocessor compatibility, the HSCT3006 (HRCT3006) is a solid-state synchro (resolver) control transformer. The converter accepts an analog synchro (resolver) signal containing angle "θ" and a 16-bit digital word containing angle "ϕ" as inputs and provides an output signal "e" proportional to sin (θ-ϕ). Packaged in a 36-pin DDIP hybrid the converter offers an excellent null accuracy of 1 arc-minute. The double-buffered latch input and high accuracy have been made possible by incorporating Natel designed monolithic integrated circuits in the converter.

The model 3006 uses a high accuracy differential signal conditioner for the Resolver input and resistive scott-tee for the Synchro input. The common mode rejection is in excess of 70 dB, thereby eliminating the need for external transformers for most applications. The digital inputs are double buffered, and the converter is TTL, standard CMOS and high-level CMOS compatible. The two input registers (buffers) permit the converter to interface with a microprocessor data bus. The digital inputs are compatible with a logic supply voltage (V_L) of 4.5 V-dc to the main power supply voltage, without requiring external pull-up resistors.

Model 3006 control transformers are available with null accuracies of 1, 2 or 4 arc-minutes. These accuracies are guaranteed over the specified operating temperature range. The exceptionally high accuracy of these converters is achieved by a unique design approach that uses buffer amplifier circuits to eliminate the effects of analog switch resistance instead of requiring compensating circuits.

Although designed to interface with a microprocessor, and offering higher resolution and accuracy, the model 3006 control transformer may be used in existing 14-bit designs without any changes in circuit connections and/or components. Data-bits B15 and B16 have internal active pull-down to ground thus permitting these pins to be left unconnected. Control signals for the latching registers and load converter (LBE, HBE and LDC) have internal active pull-up to logic supply voltage, thus allowing these pins to be left open when not required. The digital data bits do not require any pull-up resistors, but if your present design already has these resistors, the performance of the 3006 is not affected. In addition, the Model 3006 uses established reliability (ER) components and is built in accordance with the requirements of MIL-STD-883B, including 168 hours of active burn-in.

Essentially, the model 3006 allows you to use Natel converters in existing designs, at the same time offering the option of performance and cost improvements for future.

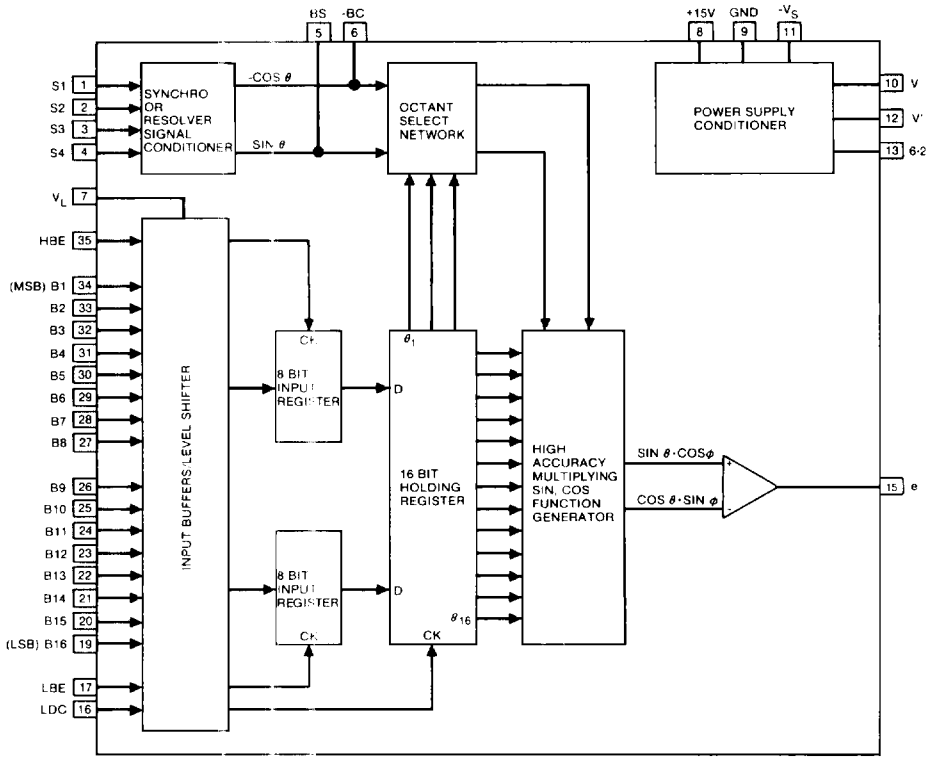


FIGURE 1 3006 BLOCK DIAGRAM

Theory of Operation

The operation of the Model 3006 is illustrated in the functional block diagram of figure 1. The analog signal conditioner accepts either a Synchro or Resolver input and converts it into the low level signals, sin θ and cos θ. The digital word representing the input angle is applied to input buffers and level shifters. Two input registers accept 16-bits from the microprocessor. In conjunction with an 8-bit data bus, each input register can be independently enabled to accept the 16-bit word in two 8-bit bytes. When interfacing with the 16-bit data bus, both input registers are enabled simultaneously to accept a 16-bit parallel input word. The 16-bit data word is then parallel-loaded into a holding register and processed through a solid state control transformer.

The solid state control transformer is made up of two function generators (sin ϕ and cos ϕ) and an octant select network. The digital input code is natural binary angle. The three most significant bits (Bit 1 = 180°, Bit 2 = 90°, Bit 3 = 45°) determine the octant information. Bits 4 through 16, containing angular information, together with the sin θ and cos θ analog voltages, are applied to two function generators to obtain sin $\theta \cdot \cos\phi$ and cos $\theta \cdot \sin\phi$. These are then differenced in a summing amplifier to obtain error voltage "e":

$$\text{"e"} = \sin\theta\cos\phi - \cos\theta \cdot \sin\phi = \sin(\theta-\phi)$$

The operation of the function generators is very similar to a 4-quadrant multiplying DAC. Like a conventional DAC, the function generators use resistive ladder networks and solid state switching to control the attenuation of the sin θ and cosθ analog signals. The ladder networks, however, are designed to attenuate the analog signal proportional to cosine and sine of the digital input angle ϕ.

Microprocessor Compatibility and Logic Inputs

Two input registers accept 16-bits from the microprocessor. Used in conjunction with an 8-bit data bus, each input register can be separately enabled to accept the 16-bit word in two 8-bit bytes. This is accomplished by setting HBE to Logic "High" (High Byte enable), to load 8 MSBs (most significant bits). And . . . setting LBE (Low Bytes enable) to Logic "High" to load 8 LSBs (least significant bits). The 16-bit data word is then parallel loaded into a holding register and processed through a solid-state control transformer. Without the holding register, output transients would occur due to the two-byte loading scheme. The holding register is enabled by setting LDC (Load Converter) to Logic "High." When interfacing with a 16-bit data bus, both input registers are enabled simultaneously to accept a 16-bit parallel input word.

For other applications: LDC, HBE and LBE can be controlled by system timing or left open to allow continuous updating. Internal active pullups allow HBE, LBE and LDC to be left open when the converter is being used in the continuous updating mode.

All digital inputs are TTL and CMOS compatible. For a +5 V-dc logic supply, the low threshold is 0.8 V-dc and the high threshold is 2.4 V-dc. For logic voltages between +5 V-dc and +15 V-dc, the logic "0" threshold is $0.2V_L$, and the logic "1" threshold is $0.8V_L$.

Data bits B15 and B16 are actively pulled-down to ground. If your application requires only a 14-bit digital input, the unused data bits (pins 19 and 20) may be left open. Control signals LBE, HBE and LDC are actively pulled-up to the V_L supply voltage. When not required by your application, these pins may also be left open.

Synchro/Resolver Connections and Phasing

The connections for synchro and resolver inputs are shown in figure 2. The input signal conditioner of the Model 3006 converter is designed to accept either synchro or resolver inputs. In addition it uses differential amplifiers and matched precision resistors to provide a high common-mode rejection ratio. This eliminates the need for external transformers for most applications. The input signal conditioner performs two functions. For both synchro and resolver format inputs it serves as a precision attenuator reducing the amplitude of high level ac input signals to levels which can be processed by the converter. For a synchro input, this network transforms three wire synchro information into resolver format ($\sin\theta$ and $\cos\theta$)

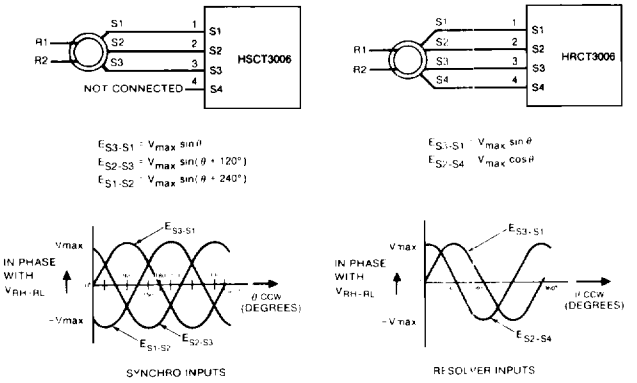


FIGURE 2 Synchro/Resolver Inputs

DC Voltages and Analog Outputs

6.2, V' and V are internally generated dc voltages.

6.2 (pin 13) is an internally generated dc voltage of 6.2 V-dc, with a drive capability of 1 mA. Although not needed for model 3006, this voltage is brought out to make 3006 pin compatible for existing designs.

V' (pin 12) is an unbuffered dc voltage. For unipolar output this pin is left unconnected. For bipolar analog outputs pin 12 is connected to ground (figure 4), and a negative power supply of -3.5 V-dc to -7 V-dc is applied to -Vs (pin 11)

V (pin 10) is buffered dc bias voltage. It serves as a reference ground for analog outputs. If V' is left unconnected this reference voltage is 3.9 V-dc. If V' is connected to ground the reference bias voltage is 0 V-dc.

The outputs of the signal conditioner . . . resistive scott-tee for synchro-input and the differential attenuator for resolver input . . . are the sine and cosine of the input shaft angle "θ." In the converter the sine and cosine outputs of the signal conditioner are processed to obtain an error output. These outputs are also brought out on pin 5 (BS) and pin 6 (-BC) as buffered sine and cosine outputs. Nominal voltage for sine maximum and cosine maximum is 1 V-rms referred to bias voltage V (pin 10) . . . the internal analog ground. The ratio accuracy of the sine and cosine outputs is better than 1 arc-minute.

The error voltage "e" (pin 15) as well as BS and -BC are referenced to the bias voltage V. Depending upon the application and availability of a negative power supply, the Model 3006 may be connected for unipolar or bipolar analog outputs. Figure 3 shows connections for unipolar output. Figure 4 shows a convenient way to obtain bipolar analog outputs from 3006 without using external operational amplifier.

The analog output "e" is mathematically represented as:

$$e = K \cdot \sin(\theta - \phi) \cdot \cos \omega t.$$

where "θ" is the shaft angle contained in Synchro or Resolver input signals and ϕ is the digital angle represented by data bits B1-B16. ω contains the carrier frequency of analog input signals. K is gain of the converter.

For nominal voltages of analog input signals K = 1 ±0.02. The 2 percent scaling error includes absolute gain error as well as variations with digital angle ϕ. The analog input varies directly proportional to, and has the same waveform as, the analog signals (synchro or resolver inputs). For example, if input levels are 10% higher than model being used, the "e" output will be 10% high. If a different scaling factor is required for your application contact one of our Application Engineers.

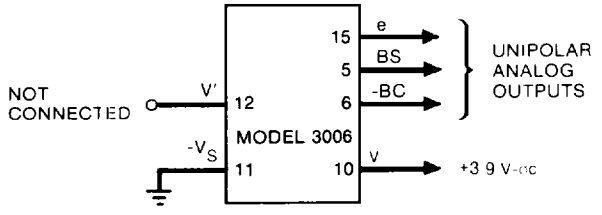


FIGURE 3 CONNECTIONS FOR UNIPOLAR ANALOG OUTPUTS

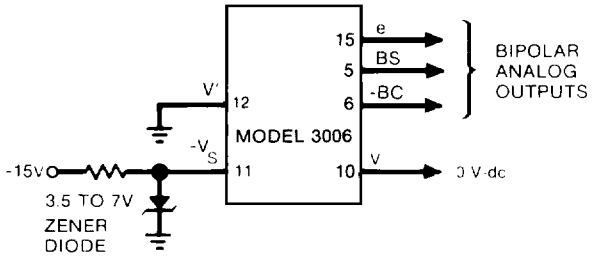


FIGURE 4 CONNECTIONS FOR BIPOLAR ANALOG OUTPUTS

Specifications

PARAMETER	VALUE		REMARKS
Digital Angular Resolution	16 bits (0.33 arc-minutes)		MSB = 180° LSB = 0.0055°
Accuracy	±4 arc-minutes (option S) ±2 arc-minutes (option H) ±1 arc-minute (option V)		Accuracy applies over operating temp. range
Synchro/Resolver Inputs			
Input Voltages (Line-to-Line)	11.8 V-rms 26 V-rms 90 V-rms		Output is directly proportional to variations in input voltages.
Input Impedance	Differential	Line-to-GND	
	60 kΩ 150 kΩ 500 kΩ	30 kΩ 75 kΩ 250 kΩ	11.8 V-rms L-L models 26 V-rms L-L models 90 V-rms L-L models
Impedance Unbalance	0.1% maximum		For all models
Common Mode Range	± 30 V peak ± 60 V peak ±180 V peak		11.8 V-rms models 26 V-rms models 90 V-rms models
Common Mode Rejection Ratio	70 dB minimum		dc to 1000 Hz
Digital Inputs Logic Voltage Levels			CMOS transient protected
Logic "0" Logic "1"	-0.3 V-dc to 0.8 V-dc +2.4 V-dc to +V		For V_L = 5 V-dc.
Logic "0" Logic "1"	-0.3 V-dc to 0.3 V_L 0.7 V_L to V_L		For V_L = 15 V-dc
Input Currents			
Data Bits B1-B14	±1 μA maximum		
Data Bits B15, B16	15 μA typical, "active" pull-down to Ground (GND)		For 14 bits digital inputs B15 (pin 20) and B16 (pin 19) may be left unconnected
HBE, LBE, LDC	-15 μA typical, "active" pull up to Logic Supply (V_L)		When not used pins can be left unconnected
Register Controls			
HBE	Logic "1" Logic "0"		8 MSBs enter high byte input register High byte register remains unaffected
LBE	Logic "1" Logic "0"		8 LSBs enter low byte input register Low byte register remains unaffected
LDC	Logic "1" Logic "0"		Data from input registers transferred to holding register Data in holding register remains unaffected
Pulse Width	600 nsec minimum		For guaranteed data transfer
Data Set-up time	200 nsec minimum		Before data transfer
Data Hold time	200 nsec minimum		Before input data changes
Analog Outputs			
Error Output (e)	$K \cdot \sin(\theta-\phi) \cos \omega t$		ac voltage referenced to V
Scale Factor (K) (for nominal input voltages)	1 ± 0.02		± 2% error includes absolute gain error as well as variation with digital angle ϕ.
Output Voltage	1 V-rms for $(\theta-\phi)$ = 90 degrees		For nominal input voltages
Output current	2 mA-rms		Short circuit proof
Output impedance	< 1 ohm		Operational amplifier output
Zero offset (dc)	±10 mV typical, ±25 mV maximum		
Offset drift	25 μV/°C		

PARAMETER	VALUE	REMARKS
Dynamic Characteristics		
Output settling time	10μsec maximum to accuracy of the converter	For any analog or digital step change
For normal tracking rate	No lag error	
Maximum Conversion Rate	Limited only by digital input changes	
Other Analog Voltages		
Internally Regulated 6.2 voltage	6.2 V-dc ± 10%	
current capability	1 mA maximum	
Unbuffered Bias Voltage (V_F)	3.9 V-dc nominal 0.0 V-dc	When left unconnected When connected to ground
Bias Voltage (V)	3.9 V-dc nominal 0.0 V-dc nominal	V_F (pin 12) unconnected V_F connected to ground
Current Capability	1 mA maximum	Operational amplifier output
BS (Buffered Sin θ) - BC (Buffered-Cos θ)	1 V-rms maximum Angular accuracy 1 arc-minute	ac voltage referenced to V (θ is input shaft angle)
Power Supplies		
Main Power Supply (+15V)		
Voltage Current	11 V-dc to 16.5 V-dc 25 mA maximum	
Negative Supply (-Vs)		Optional
Voltage	0 to -8.8 V-dc (V_L + |-V_S|) must not exceed +15 V supply	Used for obtaining bipolar analog outputs (see text for details)
Current	25 mA maximum	
Logic Voltage (V_L)		
Voltage	4.5 V-dc to +15 V power supply	
Current	1 mA maximum 3 mA maximum	For V_L = 5 V-dc. For V_L = 15 V-dc
Physical Characteristics		
Type	36 PIN Double DIP	3 standoffs are added to the package to insulate it from printed circuit board traces (standoffs included in 2.1 inch height dimension)
Size	0.78 x 1.9 x 0.21 inch (20 x 48 x 5.3 mm)	
Weight	0.6 oz (17 g) max	

Absolute Maximum Ratings

Analog Signal Inputs ..... Twice Normal Voltage
Power Supply (+ 15V) ..... + 18 V-dc
Logic Voltage (V_L) ..... + 4.5 V-dc to + 18 V-dc
Digital Input ..... - 0.3 V-dc to V_L
Negative Supply (- V_S) ..... 0.0 V-dc to (V_L - 15 V)
Storage Temperature ..... - 65°C to + 135°C

Although Digital inputs are CMOS protected, storage in conductive foam is recommended.

When installing on or removing the converter from printed circuit boards or sockets it is recommended that the power supplies and input signals be turned off. Decoupling capacitors are recommended on the main power supply (+ 15 V) as well as logic supply (V_L). A 1μF tantalum capacitor in parallel with 0.01μ ceramic capacitor should be mounted as close to the supply pins (8 and 7) as possible. Also if used in your application decoupling capacitors are recommended for the negative supply (-V_S).

Pin Designations

V_L — Logic Supply Voltage - 4.5 V-dc to +15 V-dc supply

+15 V — Supply Voltage - 11 V-dc to 16.5 V-dc.

GND — Power Supply Ground Digital Ground

S1, S2, S3, S4 — Input Analog Signals - Leave S4 unconnected for synchro-input

BS, -BC — Buffered Sinθ and -Cosθ outputs

B1 - B16 — Parallel Data Input Bits B1 is MSB = 180 degrees B16 is LSB = 0.0055 degree

HBE — High Byte Enable - Data inputs B1 through B8 enter the input buffer register when HBE is set to a Logic "High." When HBE is set to Logic "Low" the input register is in the hold mode and is not affected by digital activity at the input data bits B1-B8 pins

LBE — Low Byte Enable - Data inputs B9 through B16 enter the input buffer register when LBE is set to Logic "High." When LBE is set to Logic "Low" the input register is in the hold mode and is not affected by digital activity at the input data bits B9-B16 pins.

LDC — Load Converter - When LDC is set to a Logic "High," the converter will transfer the contents of the input buffer registers to the 16-bit holding register. When LDC is set to Logic "Low," the converter is in the hold mode and is not affected by the digital activity in the input registers.

Note: For continuous updating HBE, LBE and LDC may be left open. Internal active pull-up will force these functions to a Logic "High"

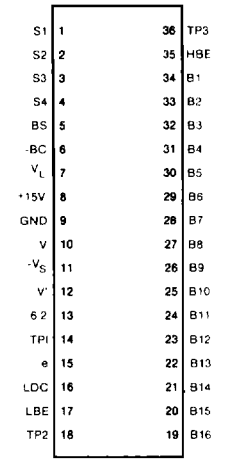


FIGURE 5 HSCT3006/HRCT3006 PIN ASSIGNMENTS

6.2 — 6.2 V-dc ---- Internally generated dc voltage

$-V_S$ — Negative Supply Voltage ---- Optional (normally connected to ground) Used for obtaining bipolar output (see text for details)

V' — Unbuffered Bias Voltage ---- Normally left unconnected Used for obtaining bipolar output (see text for details)

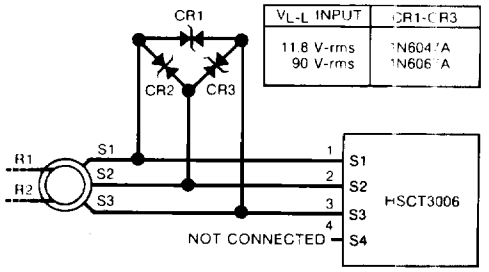
V — Bias voltage ---- Internally generated reference voltage serves as reference ground for all analog outputs

TP1 - TP3 — Test Points ---- Do not connect (For factory use only)

e — The AC Analog Output ---- Output is referenced to bias voltage (V)

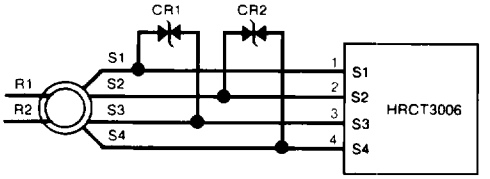
Input Protection

The analog signal inputs are true diffential inputs and use precision thin-film resistors for signal attenuation. If input voltages exceed the absolute maximum ratings, the thin-film resistors may be destroyed. To prevent this from happening, it is recommended that transient voltage suppressors be installed on signal lines. Synchros and resolvers are highly inductive and can generate or couple transients many times greater than their normal signal voltages and can easily exceed the absolute maximum ratings. This situation is particularly likely to occur in cases where the excitation or source voltage for the synchro (resolver) is switched on or off. Transients can also occur by other equipment being turned on or off. Figures 6 and 7 show recommended methods of connecting synchro and resolver inputs. Transient voltage suppressor given in the tables (or equivalent) must be used to assure input protection.



V_{L-L} INPUT	CR1-CR3
11.8 V-rms	1N6047A
90 V-rms	1N6067A

FIGURE 6 HSCT3006 Input Protection



V_{L-L} INPUT	CR1, CR2
11.8 V-rms	1N6047A
26 V-rms	1N6054A
90 V-rms	1N6067A

FIGURE 7 HRCT3006 Input Protection

Digital Interface

The double buffered input registers of the HSCT3006 offer the user an easily implemented interface with 8 or 16 bit microprocessor data buses. For applications not involving a microprocessor, independently controlled 8-bit latching registers give the user the flexibility of designing his own interface system. Provision has also been made for asynchronous data inputs through the use of the LDC control function. Memory Mapped I/O with an 8080 microprocessor is described in our data sheets HDSC2016 and HDSR2006.

Continuous Operation

Asynchronous converter operation, without timing controls, is shown in figure 8. Inputs LBE, HBE and LDC have internal pull-up circuitry, permitting these pins to be left open. The parallel information at the data inputs B1-B16 is continuously converted to error voltage (e) at the analog output. For applications requiring 14-bit resolution, unused pins can be left open. Internal pull-down circuitry applies a logic "0" to unconnected data inputs B15 and B16 (pins 20 and 19).

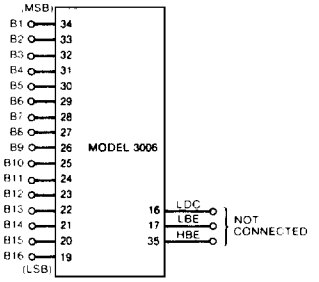


FIGURE 8 Digital Connection for Continuous Operation

Two-Byte Loading

The circuit configuration for two-byte loading of angular data from a data bus is shown in figure 9 As shown in figure 10 timing diagram, the 8 LSBs (B9-B16) are transferred to the low-byte input register when LBE is a logic "1". LBE can be "High" when data bits are changing, but must remain "High" for a minimum of 600 nsec after the data is stable. Data should be held for 200 nsec (data hold time) after LBE goes "Low." Bits B1-B8 are transferred to the high-byte input register when HBE is a logic "1." The timing requirements are the same as those for LBE Data are transferred from the two input registers to the holding register when LDC (load converter) is at logic "1." If LDC is at logic "0", the contents of the holding register are latched and remain at their prev ous values unaffected by changes at the data inputs or input registers.

Note that LBE, HBE and LDC are level-actuated functions.

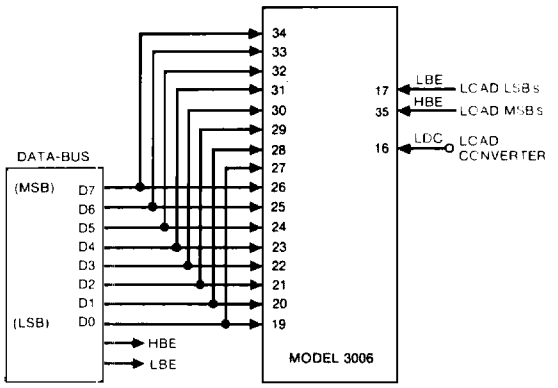


FIGURE 9 Digital Connections for Two-Byte Loading

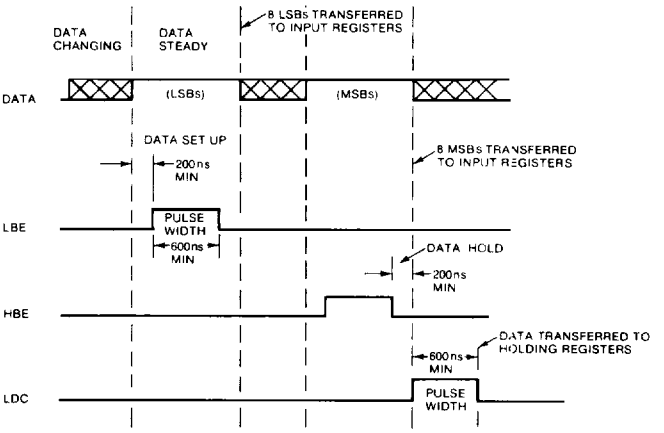


FIGURE 10 Two-Byte Loading

Single Byte Loading

Single 16-bit byte loading is illustrated in figure 11. As shown in the timing diagram (figure 12), 200 nsec after the data is stable, the input angular information is transferred to the holding register when LDC is at a logic "1". LDC is a level-actuated function and must remain high for the times specified in the timing diagram.

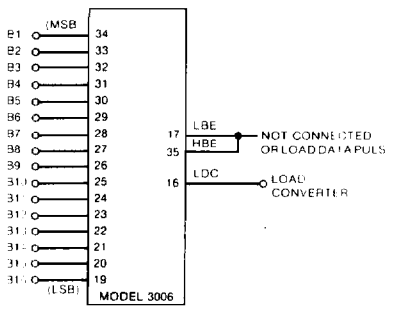


FIGURE 11 Digital Connections for One Byte (16 bits) Loading

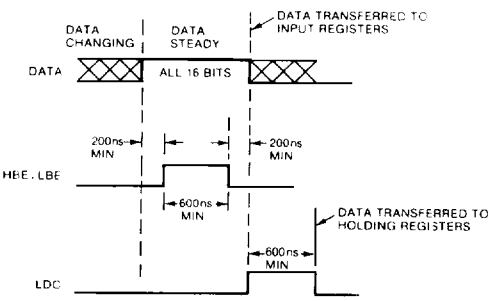
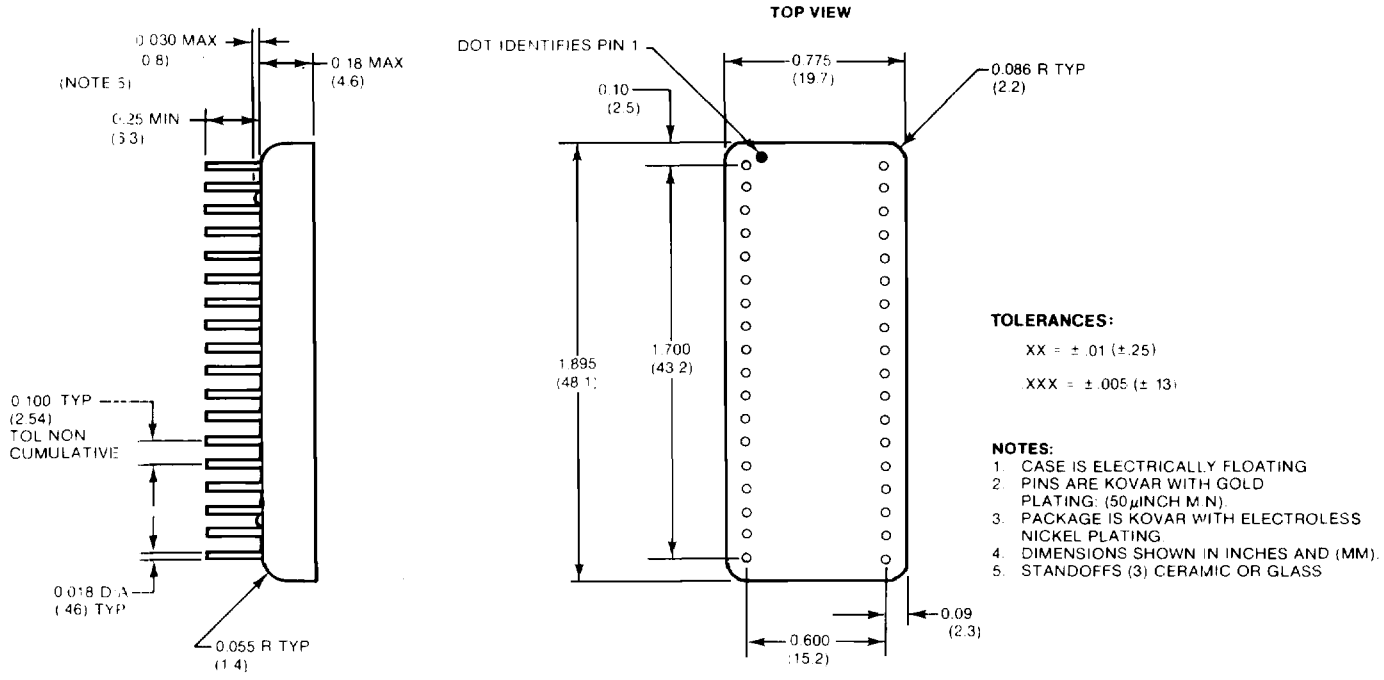


FIGURE 12 Single-Byte Loading



MECHANICAL OUTLINE (36 PIN DOUBLE DIP)

Ordering Information

HSCT3006 - T | A

Temperature Range
1 = 0°C to + 70°C
2 = -25°C to + 85°C
3 = -55°C to +125°C

Accuracy
S = ±4 arc-minutes
H = ±2 arc-minutes
V = ±1 arc-minute

Input Signal
1 = 11.8 V-rms
2 = 26 V-rms
9 = 90 V-rms
0 = Ext. Signal XFMRS

SPECIFTY HRCT3006 FOR RESOLVER INPUT

MIL-STD-883 COMPLIANT HYBRIDS AVAILABLE
Contact Natel Engineering for Delivery

Other Hybrid products in 36 pin DDIP size:

- 16-bit microprocessor-compatible synchro/resolver-to-digital converter, with 3 state output, operating from a single +5-V power supply (HSRD1006)
- 16-bit microprocessor-compatible digital to synchro/resolver converter with double buffered inputs and 1 arc-minute accuracy (HDSR2006).
- 14-bit synchro (resolver)-to-digital converters pin-compatible with existing designs, but with superior performance (HSD/HRD1014)
- 14-bit digital-to-synchro/resolver converter that is pin-compatible with existing designs with transformation and angular accuracy improvement of a factor of 2 to 4 (HDSR2504)
- 10-bit synchro (resolver)-to-digital converters that are pin compatible with existing designs (HSD/HRD1510)

A wide range of applications assistance is available from Natel. Application Notes can be requested when available . . . and Natel's applications engineers are at your disposal for specific problems.

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