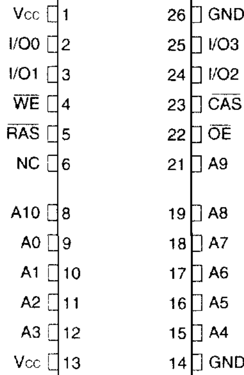
4Mx4 CMOS FPM Dynamic RAM

*PRELIMINARY**

PIN CONFIGURATION

300 MIL TSOP II
TOP VIEW



PIN DESCRIPTION

A0-10	Address Inputs
I/O0-3	Data Input/Outputs
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
Vcc	+5.0V Power
GND	Ground
NC	Not Connected

PLASTIC PLUS™ FEATURES

- Fast Access Time (t_{RAC}): 70ns (Max)
- Power Supply: 5V ±0.5V
- Packaging
  - 300 Mil Thin-Small-Outline Package (TS)
- Industrial and Military Temperature Ranges
- Three-State Data Output
- Fast Page Mode
- TTL-Compatible Inputs and Outputs
- $\overline{RAS}$-Only Refresh
- $\overline{CAS}$ Before $\overline{RAS}$ Refresh
- Hidden Refresh
- 2K Cycle Refresh = 32ms
- Low Active Power Dissipation
- Low Standby Power Dissipation

* *This data sheet describes a product under development, not fully characterized, and is subject to change without notice.*

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T_A	-55	+125	°C
Storage Temperature	T_{STG}	-65	+150	°C
Short Circuit Output Current	I_{OS}		50	mA
Power Dissipation	P_D		900	mW
Supply Voltage Range	V_{CC}	-0.5	7.0	V
Voltage Range on any Pin*	V_T	-0.5	7.0	V

Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

* All voltage values are with respect to GND.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	4.5	5.5	V
Input High Voltage	V_{IH}	2.4		V
Input Low Voltage	V_{IL}		+0.8	V
Operating Temp. (Mil.)	T_A	-55	+125	°C
Operating Temp. (Ind.)	T_A	-40	+85	°C

CAPACITANCE

(T_A = 25°C)

Parameter	Symbol	Max	Unit
A0-10 Input Capacitance	$C_{I(A)}$	5	pF
$\overline{RAS}$ and $\overline{CAS}$ Input Capacitance	$C_{I(RC)}$	7	pF
$\overline{OE}$ Input Capacitance	$C_{I(OE)}$	7	pF
$\overline{WE}$ Input Capacitance	$C_{I(WE)}$	7	pF
I/O Capacitance ($\overline{CAS}$ = V_{IH} to Disable Output)	$C_{I/O}$	7	pF

This parameter is guaranteed by design but not tested.

DC CHARACTERISTICS

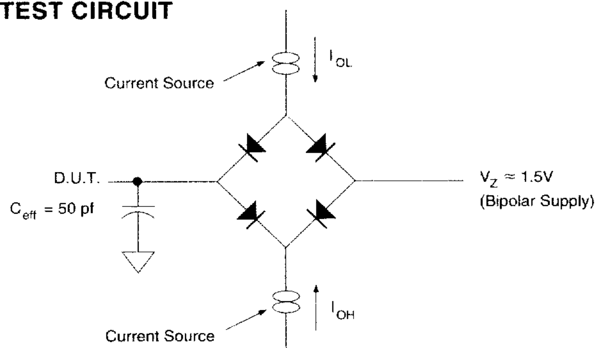
(V_{CC} = 5.0V, T_A = -55°C to +125°C)

Parameter	Test Condition	Symbol	Min	Max	Units
High Level Output Voltage	I_{OH} = -5mA	V_{OH}	2.4		V
Low Level Output Voltage	I_{OL} = 4.2mA	V_{OL}		0.4	V
Input Current (Leakage)	V_I = 0V to +6.0V All others = 0V	I_I		10	µA
Output current (Leakage)	VO = 0V to Vcc, data floating	I_O		10	µA
Read or Write Cycle Current (1,2)	Vcc = 5.5V, minimum cycle	I_{CC1}		130	mA
Standby Current	$\overline{RAS}$ and $\overline{CAS}$ = V_{IH}, output open	I_{CC2}		2	mA
Average Page Current (1,2)	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling	I_{CC4}		100	mA

NOTES:

1. I_{CC1} and I_{CC4} depend on cycle rate.
2. I_{CC1} and I_{CC4} depend on output loading, specified values are obtained with the output open.

AC TEST CIRCUIT



AC TEST CONDITIONS

Parameter	Typ	Unit
Input Pulse Levels	V_{IL} = 0, V_{IH} = 3.0	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

NOTES:

V_Z is programmable from -2V to +7V.
I_{OL} & I_{OH} programmable from 0 to 16mA.
Tester Impedance Z_0 = 75 Ω.
V_Z is typically the midpoint of V_{OH} and V_{OL}.
I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit.
ATE tester includes jig capacitance.

AC OPERATING CONDITIONS AND CHARACTERISTICS

(T_A = -55°C to +125°C, V_{CC} = 5.0V ± 10%)

Read, Write, and Read-Write Cycles (1,2)

Parameter	Symbol		Min	Max	Units
Random Read or Write Cycle Time	t_{RELREL}	t_{RC}	130	–	ns
Read-Write Cycle Time	t_{RELREL}	t_{RWC}	180	–	ns
Access Time from $\overline{RAS}$ (7,8)	t_{RELQV}	t_{RAC}	–	70	ns
Access Time from $\overline{CAS}$ (7)	t_{CELQV}	t_{CAC}	–	20	ns
Access Time from Column Address (8)	t_{AVQV}	t_{AA}	–	35	ns
Access Time from Precharge $\overline{CAS}$	t_{CEHQV}	t_{CPA}	–	40	ns
$\overline{CAS}$ to Output in Low-Z	t_{CELQX}	t_{CLZ}	0	–	ns
Output Buffer and Turn-Off Delay (2)	t_{CEHQZ}	t_{OFF}	0	15	ns
Transition Time (Rise and Fall)	t_T	t_T	3	50	ns
$\overline{RAS}$ Precharge Time	t_{REHREL}	t_{RP}	50	–	ns
$\overline{RAS}$ Pulse Width	t_{RELREH}	t_{RAS}	70	10,000	ns
$\overline{RAS}$ Hold Time	t_{CELREH}	t_{RSH}	20	–	ns
$\overline{CAS}$ Hold Time	t_{RELCEH}	t_{CSH}	70	–	ns
$\overline{CAS}$ Precharge to $\overline{RAS}$ Hold Time	t_{CEHREH}	t_{RHCP}	40	–	ns
$\overline{CAS}$ Pulse Width	t_{CELCEH}	t_{CAS}	20	10,000	ns
$\overline{RAS}$ to $\overline{CAS}$ Delay Time (7)	t_{RELCEL}	t_{RCD}	20	50	ns
$\overline{RAS}$ to Column Address Delay Time (8)	t_{RELAV}	t_{RAD}	15	35	ns
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CEHREL}	t_{CRP}	5	–	ns
$\overline{CAS}$ Precharge Time	t_{CEHCEL}	t_{CP}	10	–	ns
Row Address Setup Time	t_{AVREL}	t_{ASR}	0	–	ns
Row Address Hold Time	t_{RELAX}	t_{RAH}	10	–	ns
Column Address Setup Time	t_{AVCEL}	t_{ASC}	0	–	ns
Column Address Hold Time	t_{CELAX}	t_{CAH}	15	–	ns
Column Address to $\overline{RAS}$ Lead Time	t_{AVREH}	t_{RAL}	35	–	ns
Read Command Setup Time	t_{WHCEL}	t_{RCS}	0	–	ns
Read Command Hold Time Referenced to $\overline{CAS}$ (4)	t_{CEHWX}	t_{RCH}	0	–	ns
Read Command Hold Time Referenced to $\overline{RAS}$ (4)	t_{REHWX}	t_{RRH}	0	–	ns
Write Command Hold Time Referenced to $\overline{CAS}$	t_{CELWH}	t_{WCH}	15	–	ns
Write Command Pulse Width	t_{WLWH}	t_{WP}	15	–	ns
Write Command to $\overline{RAS}$ Lead Time	t_{WLREH}	t_{RWL}	20	–	ns
Write Command to $\overline{CAS}$ Lead Time	t_{WLCEH}	t_{CWL}	20	–	ns
Data In Setup Time (5)	t_{DVCEL}	t_{DS}	0	–	ns
Data In Hold Time (5)	t_{CELDX}	t_{DH}	15	–	ns
Write Command Setup Time (6)	t_{WLCEL}	t_{WCS}	0	–	ns
$\overline{CAS}$ to Write Delay (6)	t_{CELWL}	t_{CWD}	45	–	ns
$\overline{RAS}$ to Write Delay (6)	t_{RELWL}	t_{RWD}	95	–	ns
Column Address to Write Delay (6)	t_{AVWL}	t_{AWD}	60	–	ns

(continued)

AC OPERATING CONDITIONS AND CHARACTERISTICS

(T_A = -55°C to +125°C, V_{CC} = 5.0V ±10%)

Read, Write, and Read-Write Cycles (Continued)

Parameter	Symbol		Min	Max	Units
Refresh Period	t_{RVRV}	t_{RFSH}	–	32	ms
$\overline{CAS}$ Setup Time for $\overline{CAS}$ Before $\overline{RAS}$ Refresh	t_{RELCEL}	t_{CSR}	5	–	ns
$\overline{CAS}$ Hold Time for $\overline{CAS}$ Before $\overline{RAS}$ Refresh	t_{RELCEH}	t_{CHR}	10	–	ns
$\overline{RAS}$ Precharge to $\overline{CAS}$ Active Time	t_{REHCEL}	t_{RPC}	5	–	ns
$\overline{CAS}$ Precharge Time for $\overline{CAS}$ Before $\overline{RAS}$ Counter Time	t_{CEHCEL}	t_{CPT}	20	–	ns
Write Command Setup Time (Test Mode)	t_{WLREL}	t_{WTS}	10	–	ns
Write Command Hold Time (Test Mode)	t_{RELWH}	t_{WTH}	10	–	ns
Write to $\overline{RAS}$ Precharge Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh)	t_{WHREL}	t_{WRP}	10	–	ns
Write to $\overline{RAS}$ Hold Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh)	t_{RELWL}	t_{WRH}	10	–	ns

NOTES:

1. Address can be changed once or less while $\overline{RAS}$ = V_{IL}. In case of I_{CC4}, it can be changed once or less during a fast page mode cycle (t_{PC}).
2. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper operation is achieved. When using internal refresh counter, a minimum of 8 CAS before RAS refresh cycles instead of 8 RAS only refresh cycles are required.
3. t_{OFF} (max) and t_{OEZ} (max) define the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.
4. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
5. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in Ready-Modify-Write cycles.
6. t_{WCS}, t_{CWD}, t_{RWD}, t_{AWD} and t_{CPWD} are specified as reference points only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the I/O pins remain high impedance throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), $t_{AWD} \geq t_{AWD}$ (min), and $t_{CPWD} \geq t_{CPWD}$ (min) (for fast page mode cycle only), the cycle is read-modify-write cycle and the I/O pins will contain the data read from the selected address. If neither of these conditions are met, I/O is indeterminate until $\overline{CAS}$ or $\overline{OE}$ goes back to V_{IH}.
7. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
8. Operation within t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (max), then access time is controlled exclusively by t_{AA}.

SPECIFIC AC OPERATING CONDITIONS AND CHARACTERISTICS

(T_A = -55°C to +125°C, V_{CC} = 5.0V ± 10%)

Specific Read, Write, and Read-Write Cycles (1)

Parameter	Symbol		Min	Max	Units
$\overline{RAS}$ Hold Time Reference to $\overline{OE}$	t_{OELREH}	t_{ROH}	10	–	ns
$\overline{OE}$ Access Time	t_{OELQV}	t_{OEA}	–	15	ns
$\overline{OE}$ to Data Delay	t_{OELHDX}	t_{OED}	15	–	ns
Output Buffer Turn-Off Delay Time from $\overline{OE}$	t_{OEHQZ}	t_{OEZ}	0	15	ns
$\overline{OE}$ Command Hold Time	t_{WLOEL}	t_{OEH}	15	–	ns
Output Disable Setup Time	t_{OEHCEL}	t_{OEDS}	0	–	ns

NOTES:

1. An initial pause of 200µs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper operation is guaranteed.
2. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD}, and t_{CPWD} are not restrictive parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), $t_{AWD} \geq t_{AWD}$ (min), and $t_{CPWD} \geq t_{CPWD}$ (min) (page mode), the cycle is read-write cycle and the data out will contain data read from the selected cell. If neither of these sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

Fast Page Mode Read, Write, and Read-Write Cycles (1)

Parameter	Symbol		Min	Max	Units
Fast Page Mode Cycle Time	t_{CELCEL}	t_{PC}	45	–	ns
$\overline{CAS}$ Precharge to $\overline{RAS}$ Hold Time (Fast Page Mode)	t_{CEHREH}	t_{RHCP}	40	–	ns
Fast Page Mode Read-Writre Cycle Time	t_{CELCEL}	t_{PRWC}	95	–	ns
$\overline{RAS}$ Pulse Width (Fast Page Mode)	t_{RELREH}	t_{RASP}	70	200 k	ns
$\overline{CAS}$ Precharge to Write Delay (2)	t_{CEHWL}	t_{CPWD}	65	–	ns

NOTES:

1. An initial pause of 200µs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper operation is guaranteed.
2. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD}, and t_{CPWD} are not restrictive parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), $t_{AWD} \geq t_{AWD}$ (min), and $t_{CPWD} \geq t_{CPWD}$ (min) (page mode), the cycle is read-write cycle and the data out will contain data read from the selected cell. If neither of these sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

OPERATIONS

On power-up, an initial pause of 200 microseconds is required for the internal substrate generator to establish the correct bias voltage. This must be followed by a minimum of eight active cycles of the row address strobe (clock) to initialize all dynamic nodes within the RAM. During an extended inactive state (greater than 32 milliseconds), a wakeup sequence of eight active cycles is necessary to ensure proper operation.

ADDRESSING THE RAM

The eleven address pins on the device are time multiplexed at the begining of a memory cycle by two clocks, row address strobe ($\overline{RAS}$) and column address strobe ($\overline{CAS}$), into two separate 11-bit address fields. A total of twenty two address bits, eleven rows and eleven columns, will decode one of the 4,194,304 four bit word locations in the device. $\overline{RAS}$ active transition is followed by $\overline{CAS}$ active transition (active = V_{IL} , t_{RCD} minimum) for all read or write cycles. The delay between $\overline{RAS}$ and $\overline{CAS}$ active transitions, referred to as the multiplex window, gives a system designer flexibility in setting up the external addresses into the RAM.

The external $\overline{CAS}$ signal is ignored until an internal $\overline{RAS}$ signal is available. This "gate" feature on the external $\overline{CAS}$ clock enables the internal $\overline{CAS}$ line as soon as the row address hold time (t_{RAH}) specification is met (and defines t_{RCD} minimum). The multiplex window can be used to absorb skew delays in switching the address bus from row to column addresses and in generating the $\overline{CAS}$ clock.

There are three other variations in addressing the 16M DRAM: $\overline{RAS}$-only refresh cycle, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle, and page mode. All are discussed in separate sections that follow.

READ CYCLE

The DRAM may be read with four different cycles: "normal" random read cycle, fast page mode read cycle, read-write cycle, and fast page mode read-write cycle. The normal read cycle is outlined here, while the other cycles are discussed in separate sections.

The normal read cycle begins as described in ADDRESSING THE RAM, with $\overline{RAS}$ and $\overline{CAS}$ active transitions latching the desired bit location. The write ($\overline{WE}$) input level must be high (V_{IH}), t_{RCS} (minimum) before the $\overline{CAS}$ or active transition, to enable read mode.

Both the $\overline{RAS}$ and $\overline{CAS}$ clocks trigger a sequence of events that are controlled by several delayed internal clocks. The internal clocks are linked in such a manner that the read access time of the device is independent of the address multiplex window.

Both $\overline{CAS}$ and output enable ($\overline{OE}$) control read access time: $\overline{CAS}$ must be active before or at t_{RCD} maximum and $\overline{OE}$ must be active t_{RAC} - t_{GA} (both minimum) after $\overline{RAS}$ active transition to guarantee valid data out at t_{RAC}. If the t_{RCD} maximum is exceeded and/or $\overline{OE}$ active transition does not occur in time, read access time is determined by either the $\overline{CAS}$ or $\overline{OE}$ clock active transition (t_{CAC} or t_{GA}).

WRITE CYCLE

The user can write to the DRAM with any of four cycles: early write, late write, fast page mode early write, and fast page mode read-write. Early and late write modes are discussed here, while fast page mode write operation is covered in a separate section.

A write cycle begins as described in ADDRESSING THE RAM. Write mode is enabled by the transition of $\overline{WE}$ to active (V_{IL}). Early and late write modes are distinguished by the active transition of $\overline{WE}$, with respect to $\overline{CAS}$. Minimum active time t_{RAS} and t_{CAS}, and precharge time t_{RP}, apply to write mode, as in the read mode.

An early write cycle is characterized by $\overline{WE}$ active transition at minimum time t_{WCS} before $\overline{CAS}$ active transition. Column address setup and hold times (t_{ASC}, t_{CAH}) and data in setup and hold times (t_{DS}, t_{DH}) are referenced to $\overline{CAS}$ in an early write cycle. $\overline{RAS}$ and $\overline{CAS}$ clocks must stay active for t_{RWL} and t_{CWL}, respectively, after the start of the early write operation to complete the cycle.

A late-write cycle (refferred to as $\overline{OE}$ - controlled write) occurs when $\overline{WE}$ active transition is made after $\overline{CAS}$ active transition. $\overline{WE}$ active transition could be delayed for almost 10 microseconds after $\overline{CAS}$ active tarnsition, ($t_{RCD} + t_{CWD} + t_{RWL} + 2t_T) \leq t_{RAS}$, if other timing minimums (t_{RCD}, t_{RWL}, and t_T) are maintained. Data timing parameters are referred to $\overline{WE}$ active transition in a late write cycle. Output buffers are enabled by $\overline{CAS}$ active transition. 4M x 4 outputs are switched off by $\overline{OE}$ inactive transition, which is required to write to the device. Output data may be indeterminate. $\overline{RAS}$ and $\overline{CAS}$ must remain active for t_{RWL} and t_{CWL}, respectively, after $\overline{WE}$ active transition to complete the write cycle. $\overline{OE}$ must remain inactive for t_{GH} after $\overline{WE}$ active transition to complete the write cycle.

READ-WRITE CYCLE

A read-write cycle performs a read and then a write at the same address, during the same cycle. This cycle is basically a late write cycle, as discussed in the WRITE CYCLE section, except $\overline{WE}$ must remain high for t_{CWD} and/or t_{AWD} minimum, to guarantee valid data output before writing the bit.

PAGE MODE CYCLES

Page mode allows fast successive data operations at all column locations on a selected row of the 16M DRAM. Read access time in page mode (t_{CAC}) is typically half the regular RAS clock access time, t_{RAC}. Page mode operation consists of keeping RAS active while toggling CAS between V_{IH} and V_{IL}. The row is latched by RAS active transition, while each CAS active transition allows selection of a new column location on the row.

A page mode cycle is initiated by a nominal read, write, or read-write cycle, as described in prior sections. Once the timing requirements for the first cycle are met, CAS transitions to inactive for minimum t_{CP}, while RAS remains low (V_{IL}). The second CAS active transition while RAS is low initiates the first page mode cycle (t_{PC} or t_{PRWC}). Either a read, write, or read-write operation can be performed in a page mode cycle, subject to the same conditions as in normal operation (previously described). These operations can be intermixed in consecutive page mode cycles and performed in any order. The maximum number of consecutive page mode cycles is limited by t_{RASP}. Page mode operation is ended when RAS transitions to inactive, coincident with or following CAS inactive transition.

REFRESH CYCLES

The dynamic RAM design is based on capacitor charge storage for each bit in the array. This charge will tend to degrade with time and temperature. Each bit must be periodically **refreshed** (recharged) to maintain the correct bit state. Bits in the device require refresh every 32 milliseconds.

This is accomplished by cycling through the 2048 row addresses in sequence within the specified refresh time. All the bits on a row are refreshed simultaneously when the row is addressed. Distributed refresh implies a row refresh every 15.6 microseconds for the 16M DRAM. Burst refresh, a refresh of all rows consecutively, must be performed every 32 milliseconds.

A normal read, write, or read-write operation to the RAM will refresh all the bits (2048) associated with the particular row decodes. Three other methods of refresh, **RAS-only refresh, CAS before RAS refresh,** and **hidden refresh** are available on this device for greater system flexibility.

RAS-ONLY REFRESH

RAS-only refresh consists of RAS transition to active, latching the row address to be refreshed, while CAS remains high (V_{IH}) throughout the cycle. An external counter should be employed to ensure that all rows are refreshed within the specified limit.

CAS BEFORE RAS REFRESH

CAS before RAS refresh is enabled by bringing CAS active before RAS. This clock order activates an internal refresh counter that generates the row address to be refreshed. External address lines are ignored during the automatic refresh cycle. The output buffer remains at the same state it was in during the previous cycle (hidden refresh). WE must be inactive for time t_{WRP} before and time t_{WRH} after RAS active transition to prevent switching the device into a **test mode cycle**.

HIDDEN REFRESH

Hidden refresh allows refresh cycles to occur while maintaining valid data at the output pin. Holding CAS active at the end of a read or write cycle while RAS cycles inactive for t_{RP} and back to active starts the hidden refresh. This is essentially the execution of a CAS before RAS refresh from a cycle in progress. WE is subject to the same conditions with respect to RAS active transition (to prevent test mode entry) as in CAS before RAS refresh.

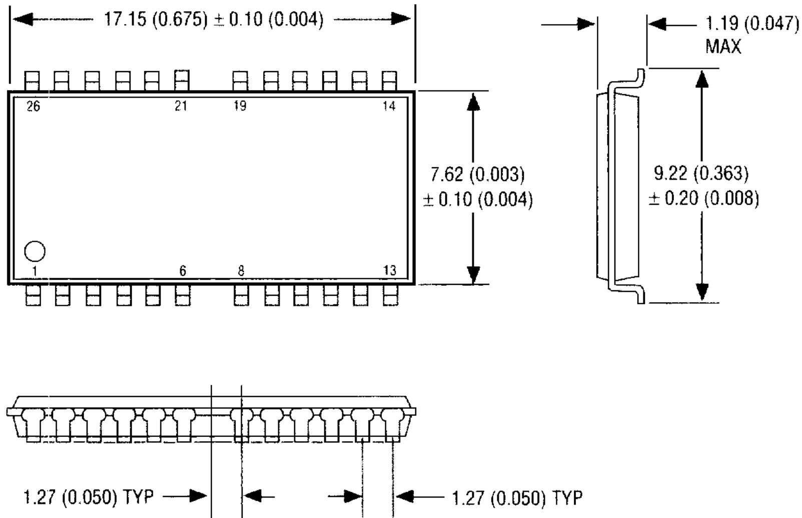
CAS BEFORE RAS REFRESH COUNTER TEST

The internal refresh counter of this device can be tested with a CAS before RAS refresh counter test. This test is performed with a read-write operation. During the test, the internal refresh counter generates the row address, while the external address supplies the column address. The entire array is refreshed after 2048 cycles, as indicated by the check data written in each row.

The test can be performed after a minimum of eight **CAS before RAS** initialization cycles. Test procedure:

1. Write 0s into all memory cells with normal write mode.
2. Select a column address, read 0 out and write 1 into the cell by performing the **CAS before RAS refresh counter test, read-write cycle**. Repeat this operation 2048 times.
3. Read the 1s that were written in step two in normal read mode.
4. Using the same starting column address as in step two, read 1 out and write 0 into the cell by performing the **CAS before RAS refresh counter test, read-write cycle**. Repeat this operation 2048 times.
5. Read 0s which were written in step four in normal read mode.
6. Repeat steps one through five using complement data.

PACKAGE DIMENSION: 24/26 PIN, TSOP II



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

15 PLASTIC PLUS DRAM

ORDERING INFORMATION

W P D 4M 4 X - 70 TS X

DEVICE GRADE:
- M = Military Temperature -55°C to +125°C
- I = Industrial Temperature -40°C to +85°C

PACKAGE:
TS = 300 MIL TSOP II

ACCESS TIME (ns)

IMPROVEMENT MARK
- B = Burn-in
- T = Temperature Cycle
- C = Burn-in and Temp Cycle

ORGANIZATION, 4M x 4

DRAM

PLASTIC PLUS™

WHITE MICROELECTRONICS